AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH (AIUB)

FACULTY OF SCIENCE & TECHNOLOGY DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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DIGITAL LOGIC AND CIRCUITS LABORATORY

Section: D Group: 03

LAB REPORT NAME:

Deriving logic equations and truth table from a given statement or expression and construction of combinational circuits

Supervised By:
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Title: Deriving logic equations and truth table from a given statement or expression and construction of combinational circuits

Abstract:

This experiment is designed to-

1. Help students implement the logic circuits derived from a given statement in the breadboard using gate ICs and observe whether the output verifies the truth table of the given logic statement or not.

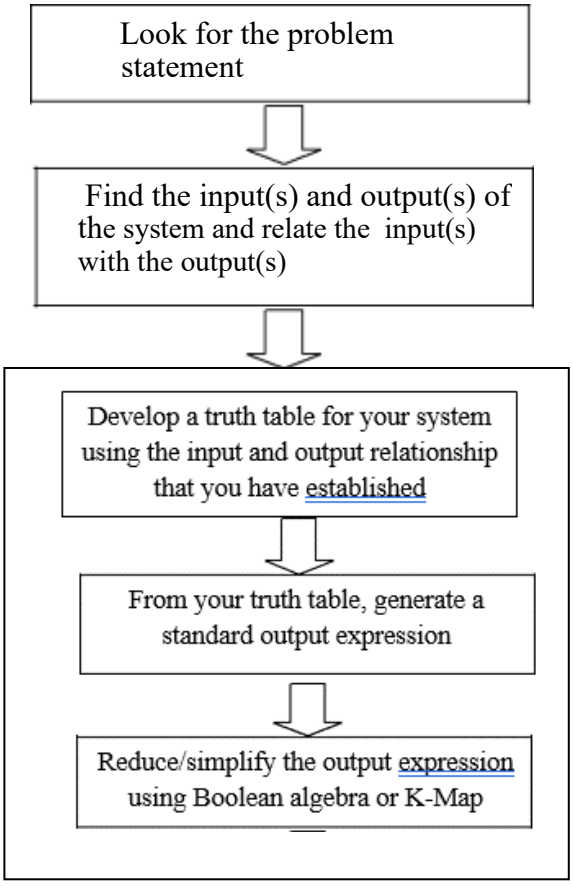
2. Perform relevant theoretical work by deriving the logic circuit and truth table from the given logic equation/statement and get familiarized with Boolean algebra and De Morgan's law.

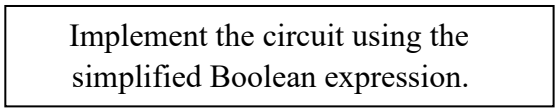
3. Simplify the logic expressions with K-Map and verify accuracy by breadboard implementation.

Theory and Methodology:

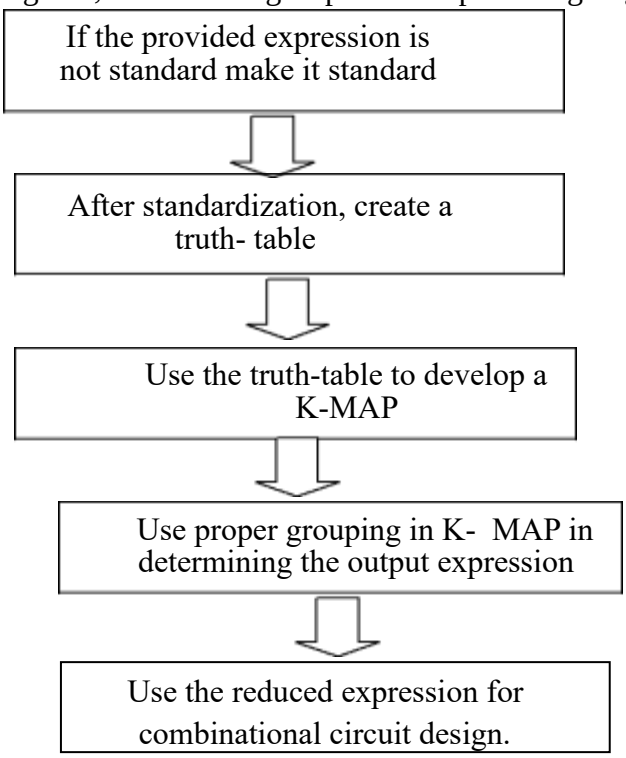
Combinational circuits are built with logic gates and other components. It does not include any values to be taken from a previous state of the circuit. Designing such a combinational digital system requires use of one of the following methods:

1. If a problem statement is given, the following steps will help designing the system





1. Or if an expression is given, the following steps will help in designing the system



Some useful definitions related to these procedures are given below:

Boolean algebra: In Boolean algebra, a variable is a symbol used to represent an action, a condition, or data. A single variable can only have a value of 1 or 0.

1. **Variable:** A symbol used to represent a logical quantity that can have a value of 1 or 0, usually designated by an italic letter.
2. **Complement:** The inverse or opposite of a number. In Boolean algebra, the inverse function, expressed with a bar over the variable.
3. **Sum term:** The Boolean sum of two or more literals equivalent to an OR operation
4. **Product term:** The Boolean product of two or more literals equivalent to an AND operation.
5. **Sum of Products (SOP):**

When two or more product terms are summed by boolean addition, the resulting expression is a sum of product. Ex.

Implementing an SOP expression simply requires ORing the outputs of two or more AND gates. A product term is produced by an AND operation, and the sum (addition) of two or more product terms is produced by an OR operation. Therefore, an SOP expression can be

implemented by AND-OR logic in which the outputs of a number (equal to the number of product terms in the expression) of AND gates connect to the inputs of an OR gate.

A standard SOP expression is one in which all the variables in the domain appear in each product term. Ex.

Standard SOP expressions are important in constructing truth-tables and in Karnaugh map simplification method.

The SOP expression is equal to 1 only if one or more of the product terms in the expression is equal to 1.

6. Product of Sums (POS):

When two or more sum terms are multiplied, the resulting expression is a product of sums (POS). Ex.

Implementing a POS expression simply requires ANDing the outputs of two or more OR gates. A sum term is produced by an OR operation, and the product of two or more sum terms is produced by an AND operation. Therefore, a POS expression can be implemented by logic in which the outputs of a number (equal to the number of sum terms in the expression) of OR gates connect to the inputs of an AND gate.

A standard POS expression is one in which all the variables in the domain appear in each sum term in the expression. Ex.

A POS expression is equal to 0 only if one or more of the sum terms in the expression is equal to 0.

7. Karnaugh Map:

A Karnaugh map provides a systematic method for simplifying Boolean expressions and, if properly used, will produce the simplest SOP or POS expression possible le, known as the minimum expression.

A Karnaugh map is similar to a truth table because it presents all of the possible values of input variables and the resulting output of each valued. Instead of being organized into columns and rows like truth table, the Karnaugh map is an array of cells in which each cell presents binary value of the input variables. The cells are arranged in a way so that the simplification of a given expression is simply a matter of properly grouping the cells. Karnaugh maps can be used for expressions with two, three, four and five variables. The number of cells in a Karnaugh map is

equal to the total number of possible input variable combinations as is the number of rows in a truth table

Introduction:

From any given logic statement, it is possible to construct a digital logic circuit. The first step in this process is to construct a truth table and then determine a standard SOP (sum of products) or POS (product of sums). At the same time, it is also possible to derive a logic expression from a given combinational circuit diagram by observing the individual logic operations performed in the circuit and matching them with their corresponding logic gates. Expressions are simplified using Boolean algebra and De Morgan's law or K-Map to reduce the number of gates used. Then the circuit is implemented in the breadboard using gate ICs and observed whether the output verifies the truth table of the given statement.

This experiment shows the students a practical verification of deriving logic equations and truth table from combinational circuits. Knowing how to derive logic equations and truth table from combinational circuits helps a person with detecting the output logic expressions from any unknown logic circuit.

Apparatus:

1. Digital trainer board
2. IC 7432:1 pcs
3. IC 7408:1 pcs
4. IC 7402:1 pcs
5. IC 7400:1 pcs
6. IC 7486:1 pcs
7. Connecting wires

Experimental Procedure:

a) **Problem1.** A Building has 4 floors which share the same water tank for water supply. In order to start the motor, each floor has a designated switch- Ground Floor with switch A, 1st Floor with switch B, 2nd Floor with switch C and 3rd Floor with switch D. The motor starts if someone presses the switch from the 3rd floor or from both ground and 2nd floor or from 1st and 2nd floor. Your job is to design the system.

Solution: Experimental Procedure:

Truth Table for problem 1

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

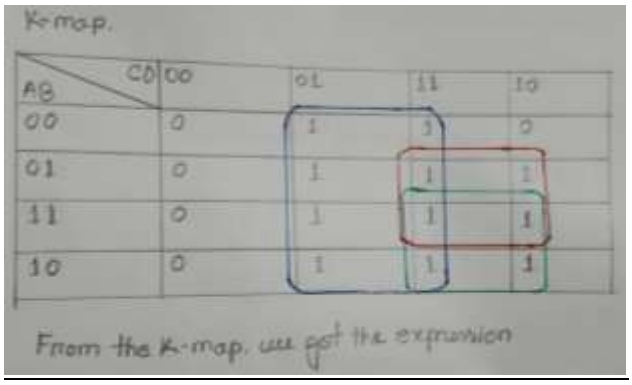
The SOP expression:

Y=A′B′C′D+A′B′CD+A′BC′D+A′BCD′+A′BCD+AB′C′D+AB′CD′+AB′CD+ABC′D+AB CD′+ ABCD

The POS expression:

Y=(A+B+C+D) (A+B+C′+D) (A+B′+C+D) (A′+B+C+D) (A′+B′+C+D)

Reducing using K-map:



From the K-map, we get the expression,

Y=D+BC+AC Using this equation, the circuit was designed.

Problem2. For the expression ***(AB+AC)'+ A'B'C,*** find the truth-table and the logic gate diagram, reduced expression using K-MAP.

Solution: Experimental Procedure:

a)

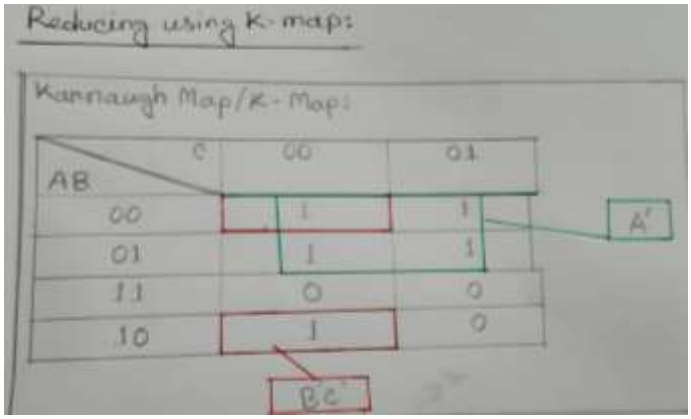
Truth Table for problem 2

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

SOP Expression:

Y=A'B'C'+A'B'C+A'BC'+A'BC+AB'C'

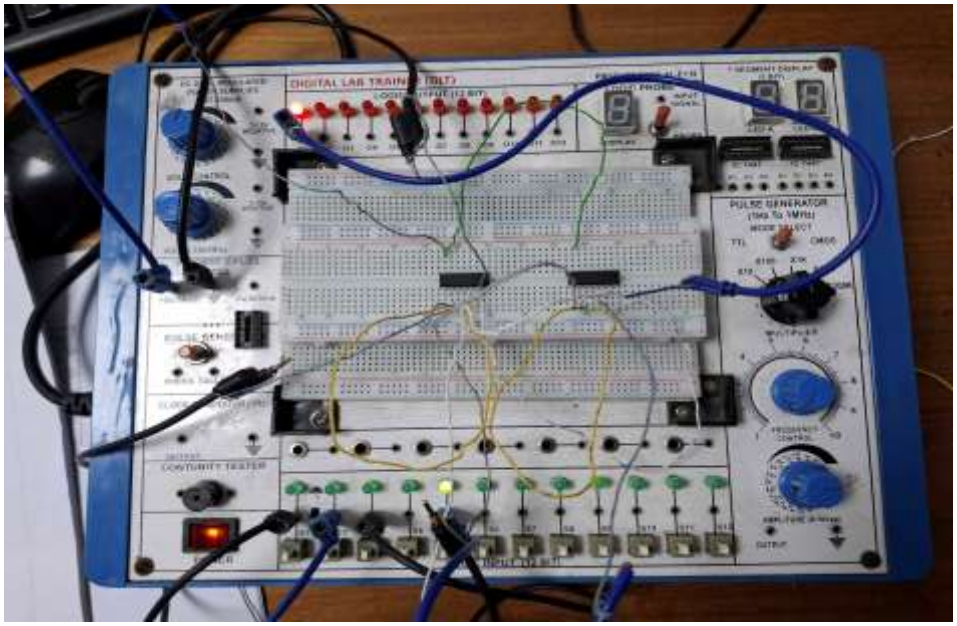
Reducing using K-map:

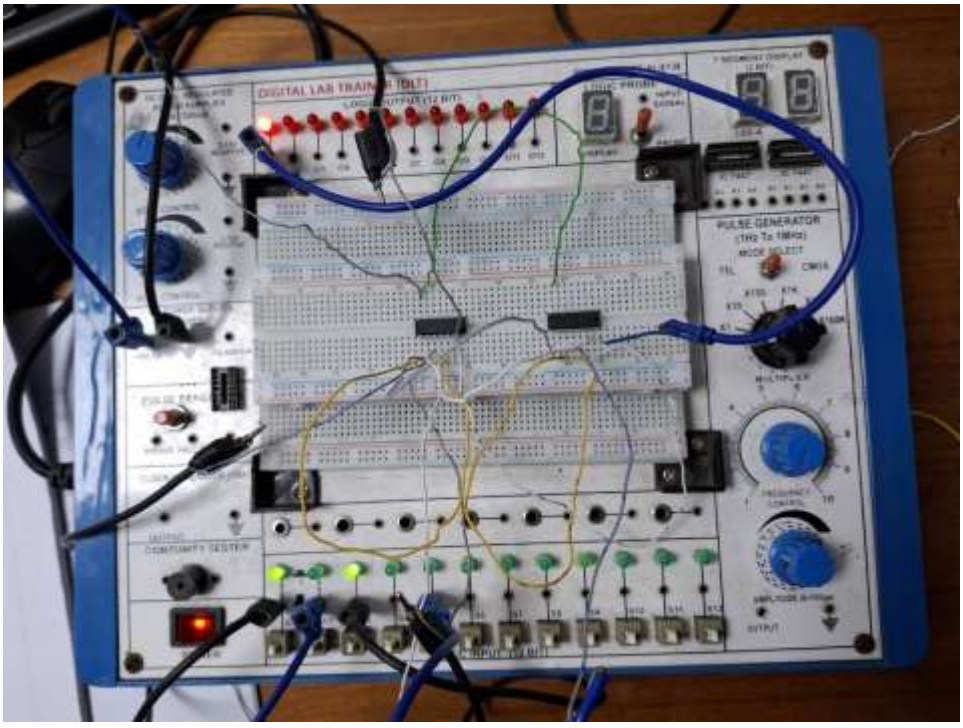


From the K-map, we get the expression,

$$F=A'+B'.C'$$

Hardware setup





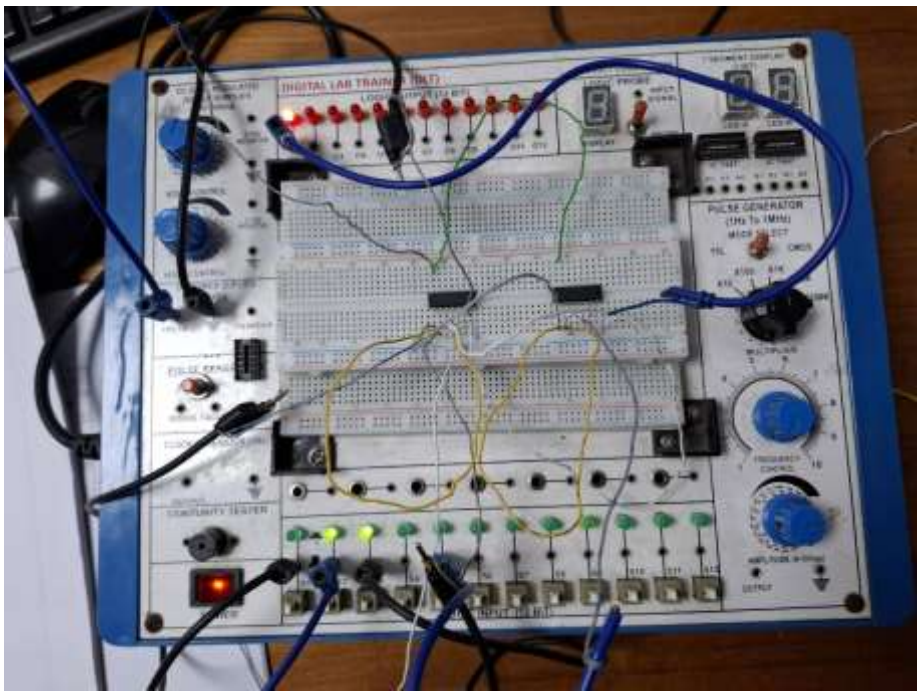
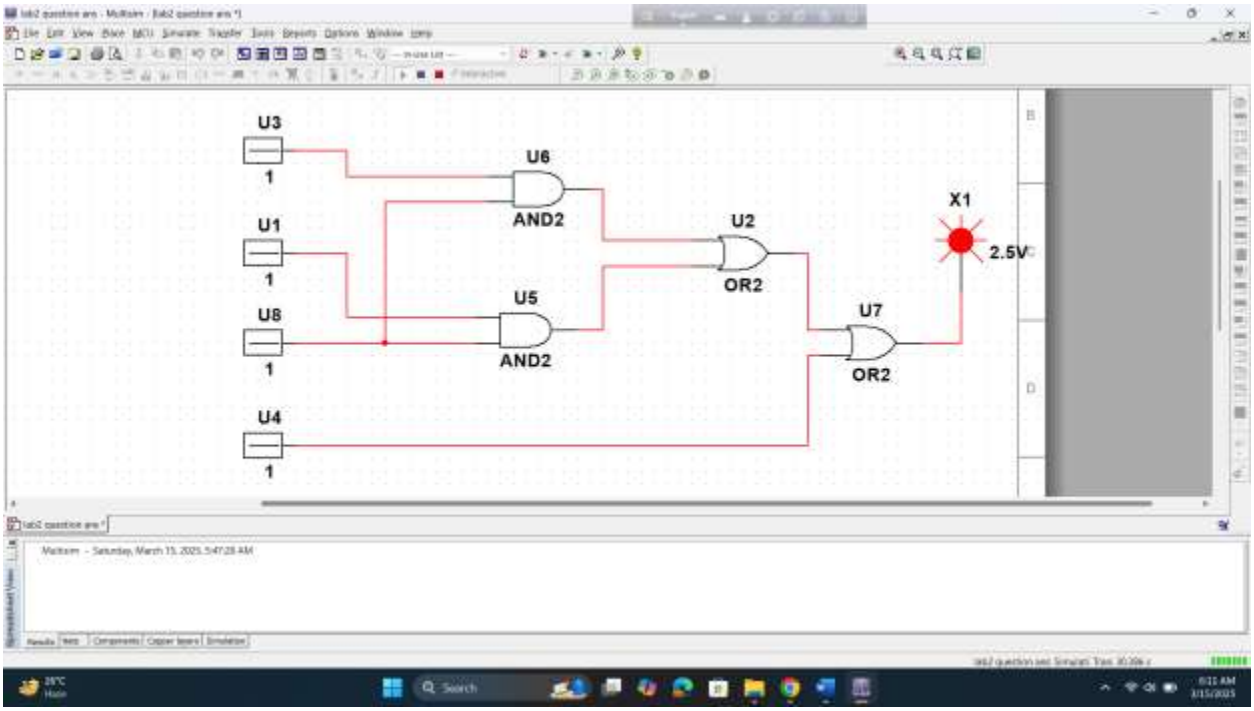
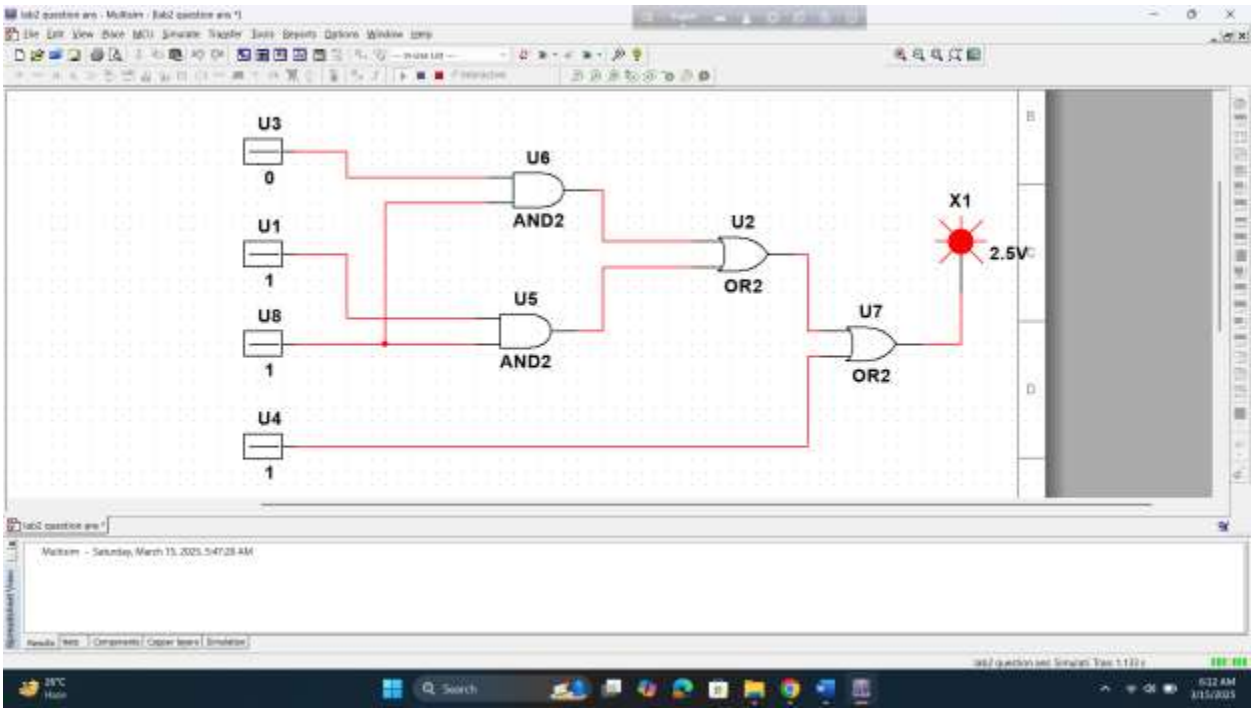


Fig: Problem 1

Simulation and Measurement:

Problem 1




U3
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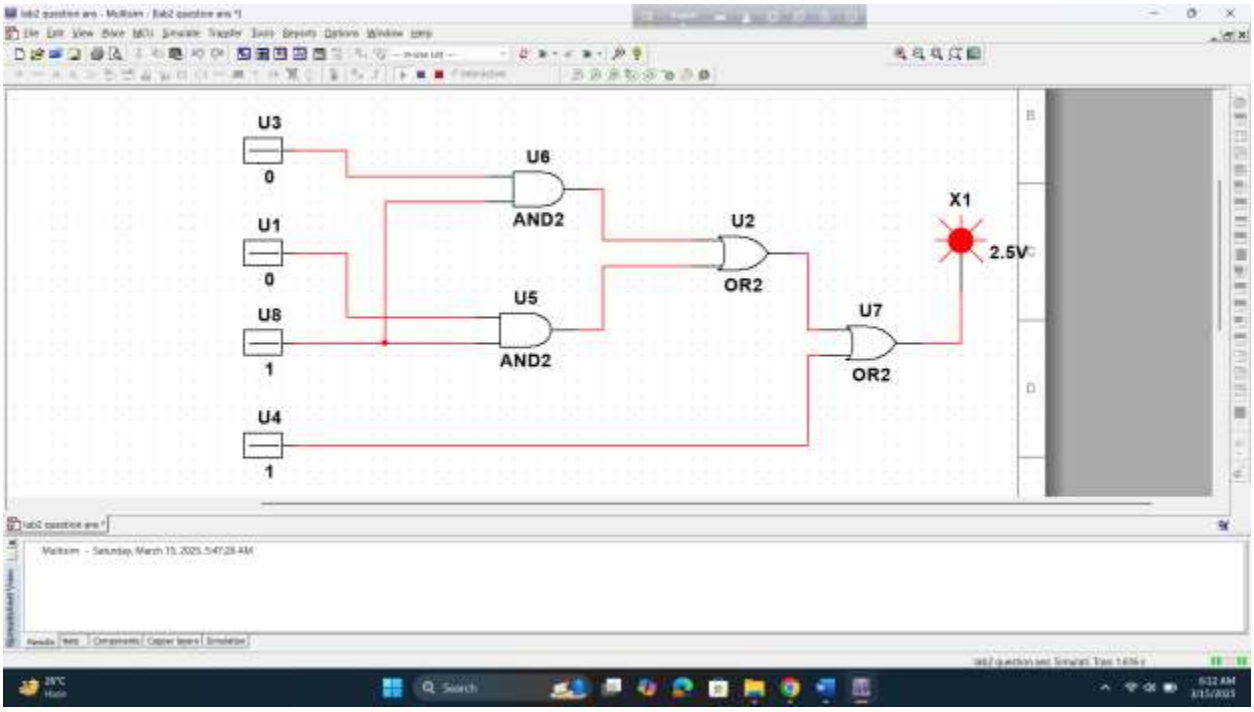
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U8
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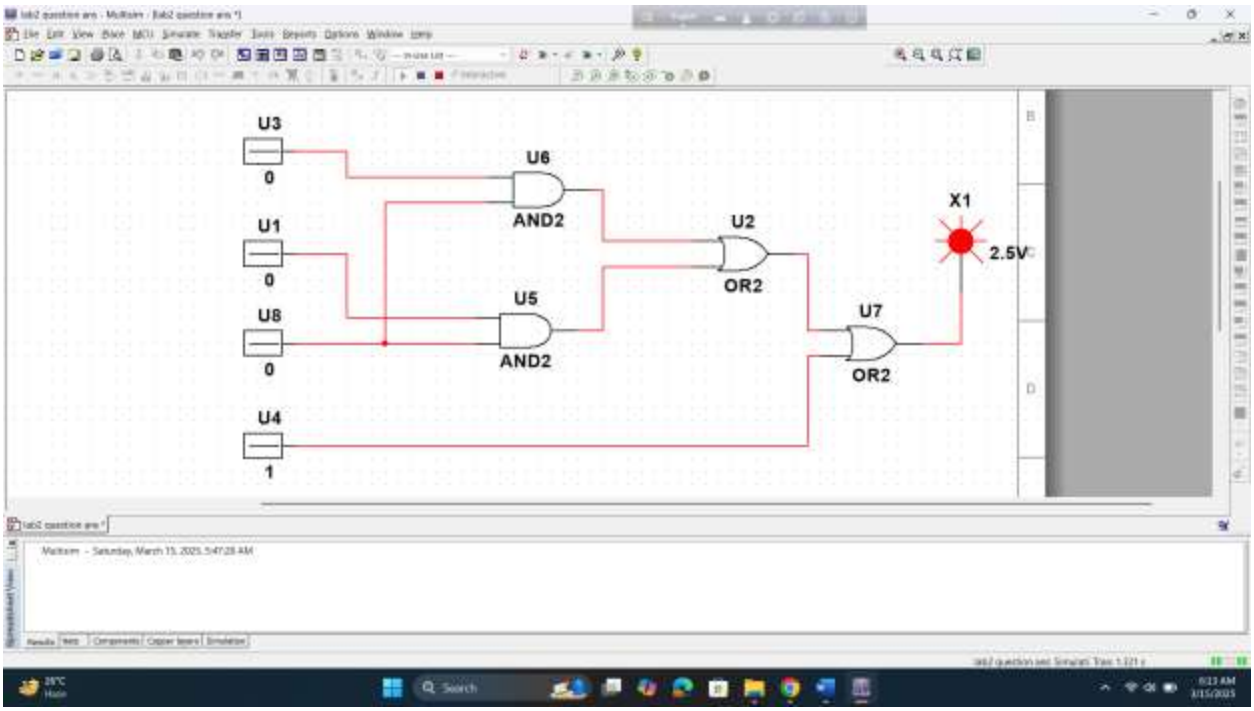
U3
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U1
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AND2
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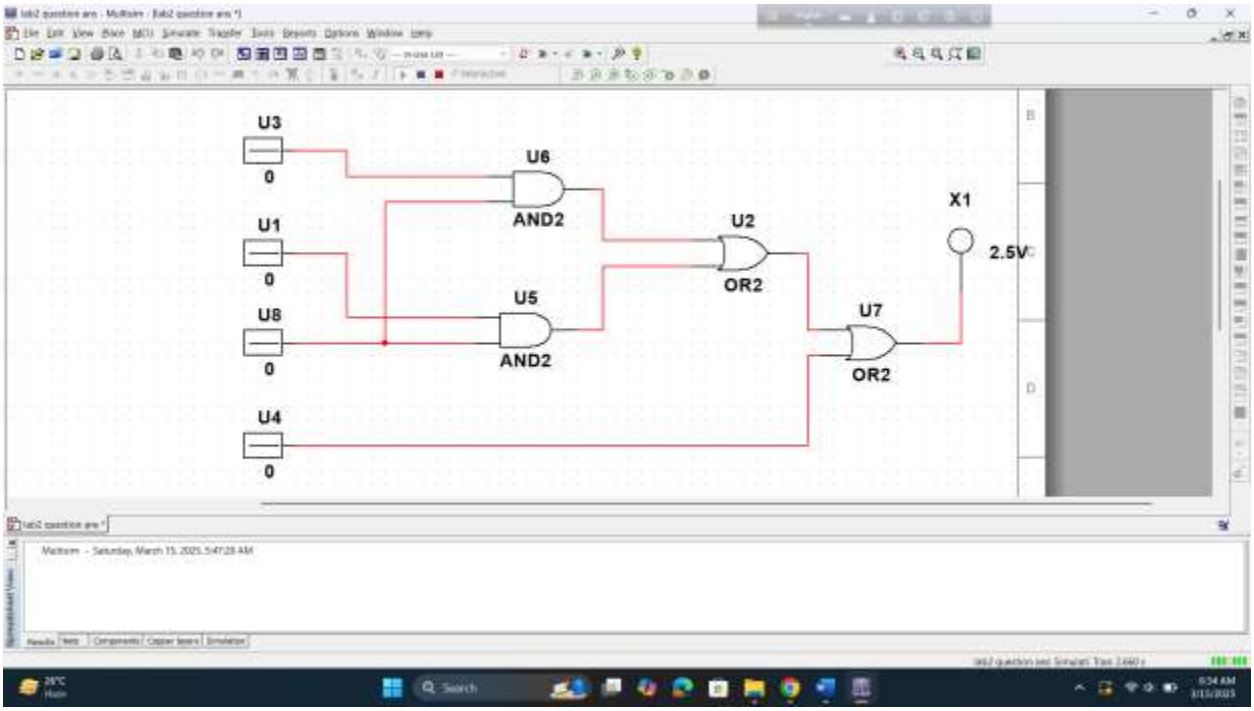
U3
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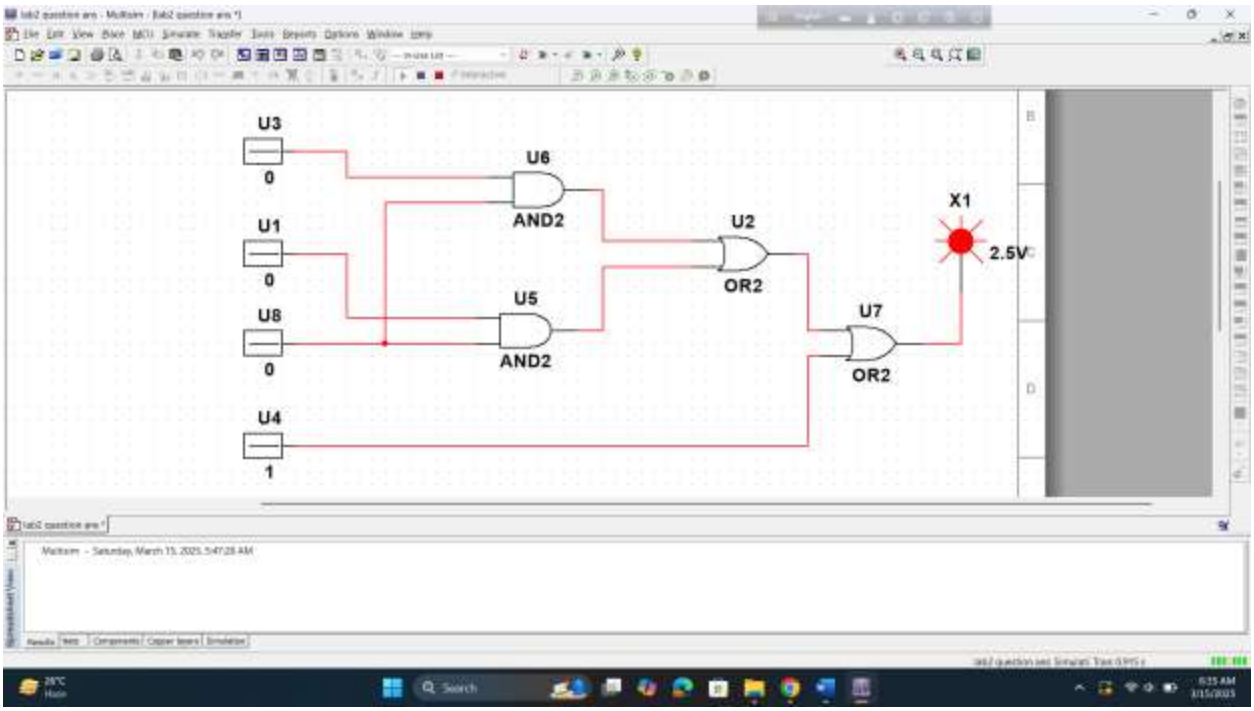
U3
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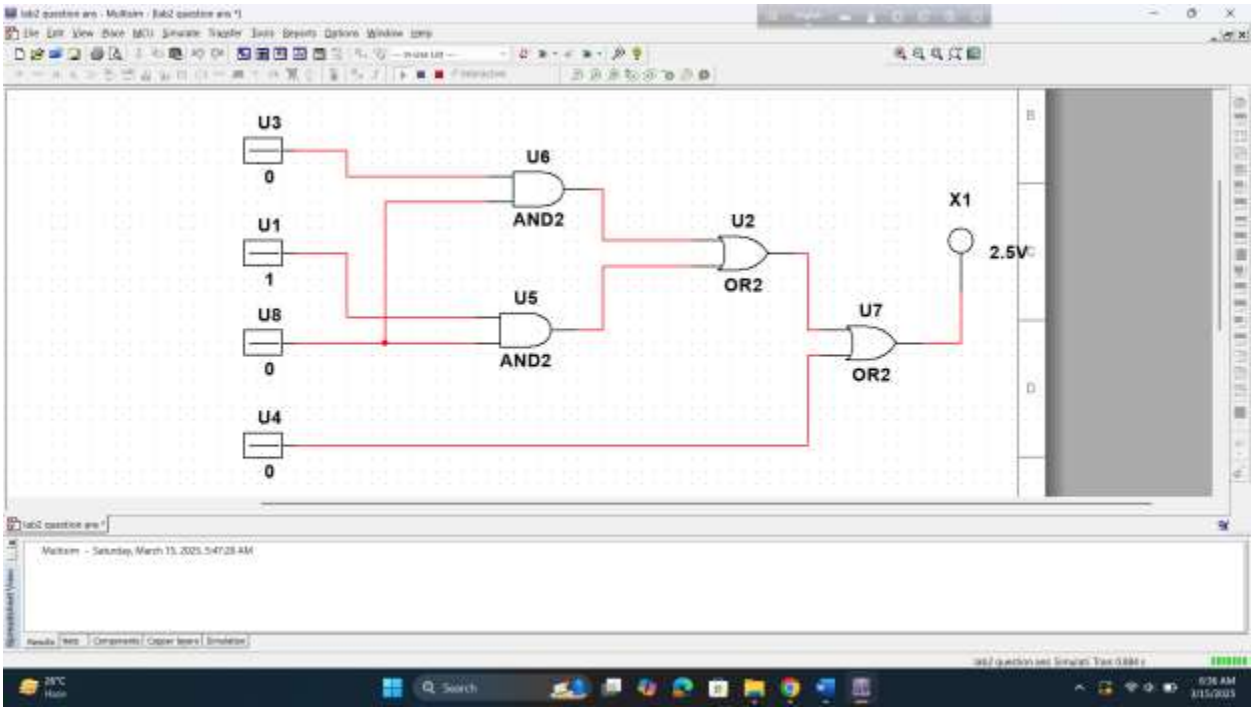
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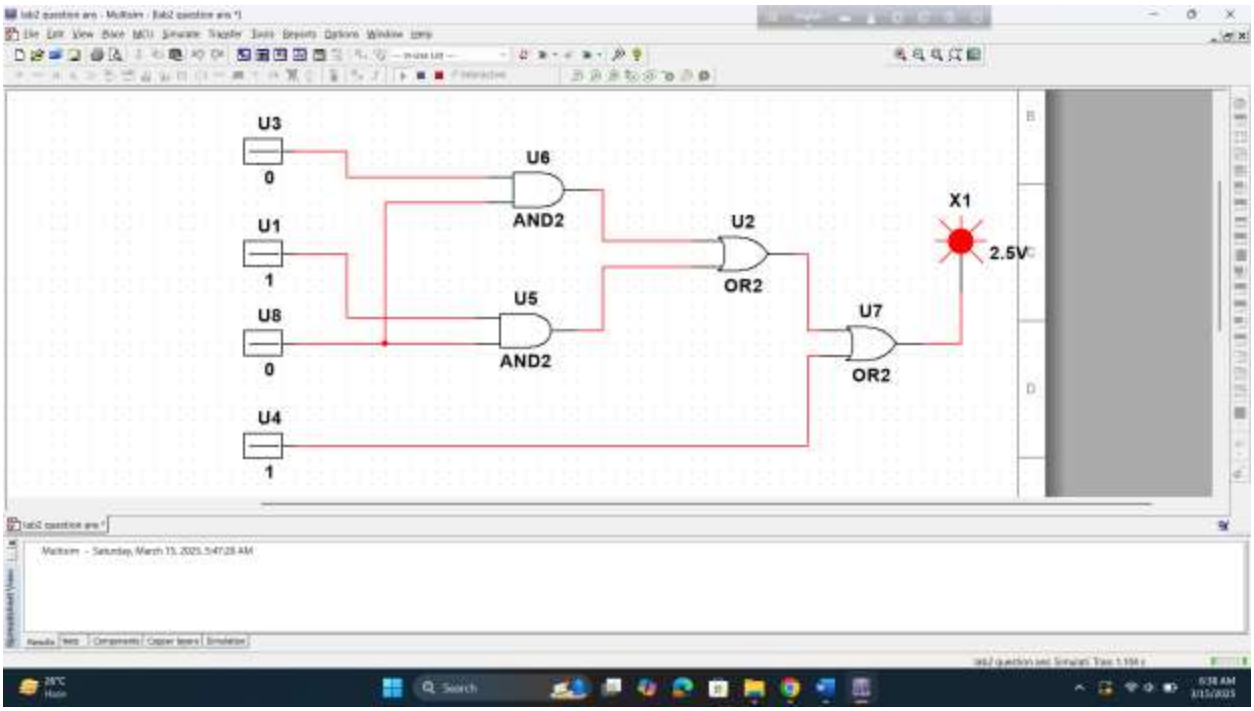
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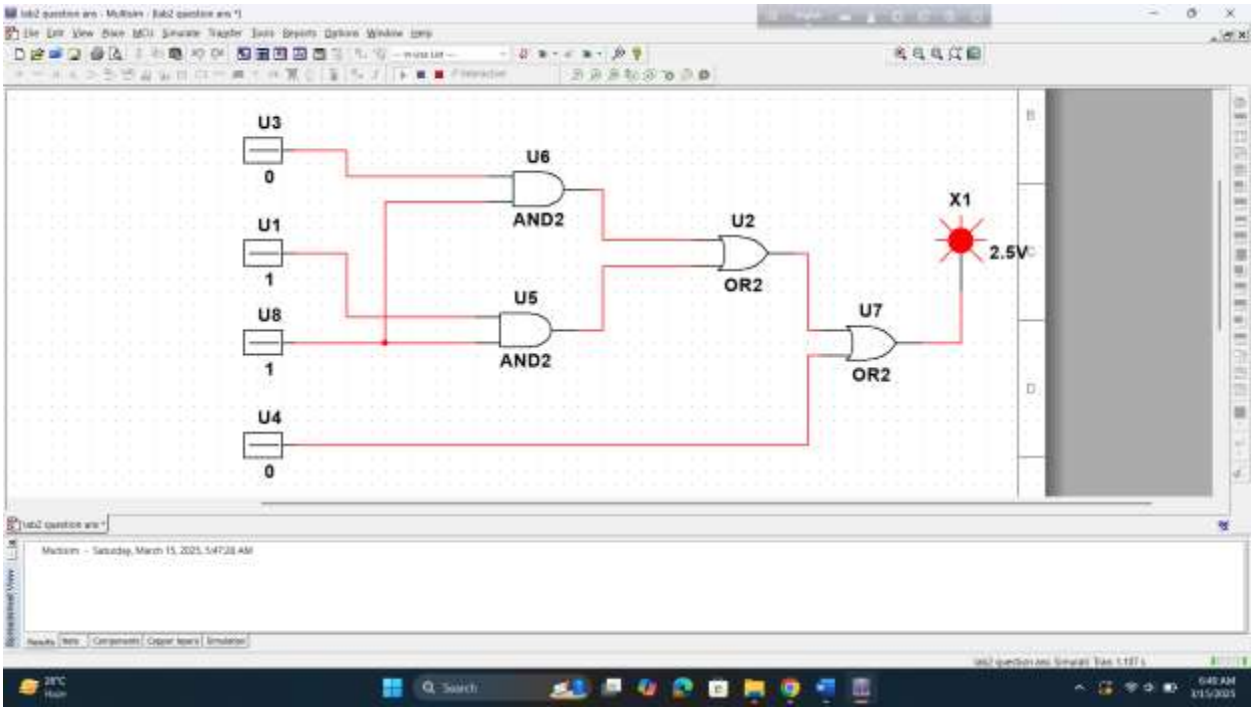
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U1
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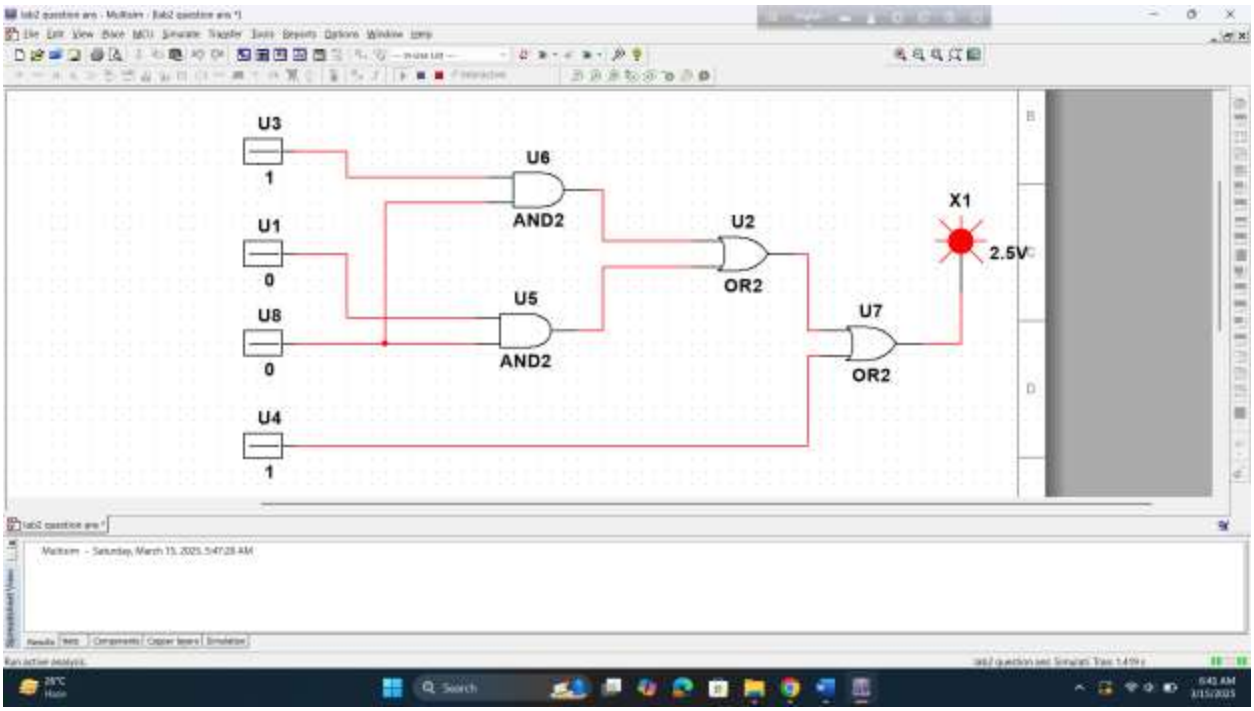
U3
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U1
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U8
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U4
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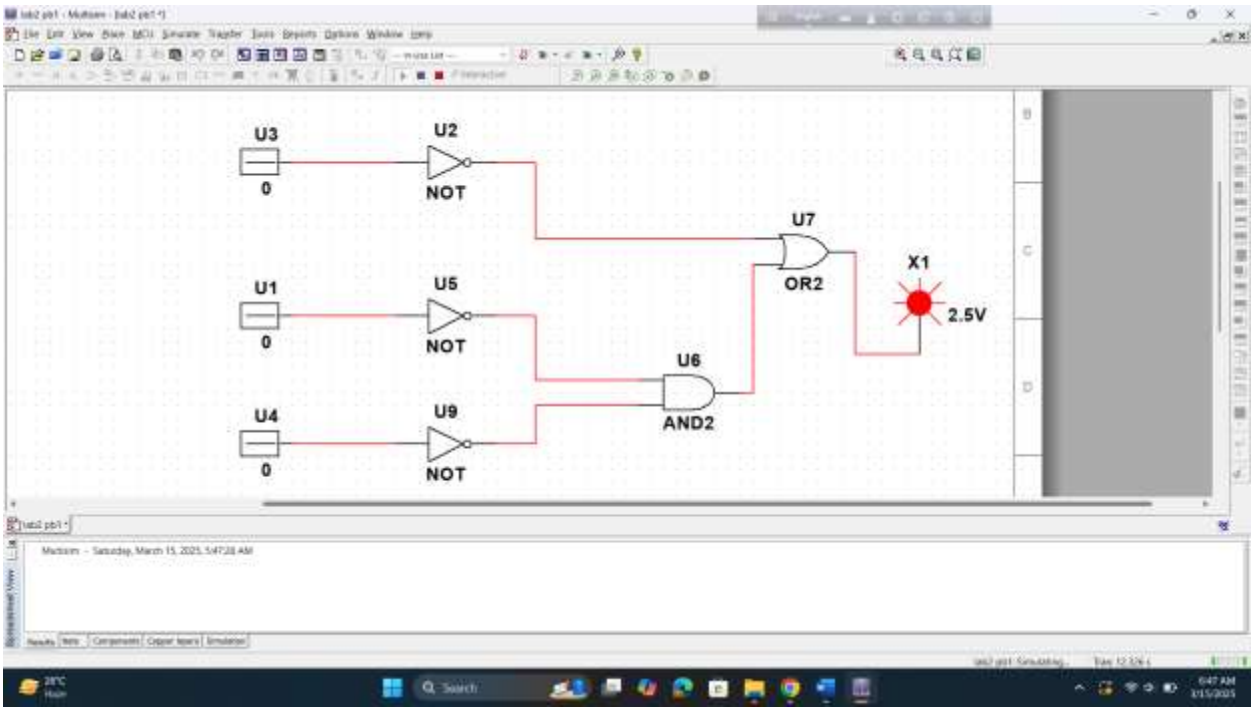
problem 2:


U3
0
U1
0
U4
0
U2
NOT
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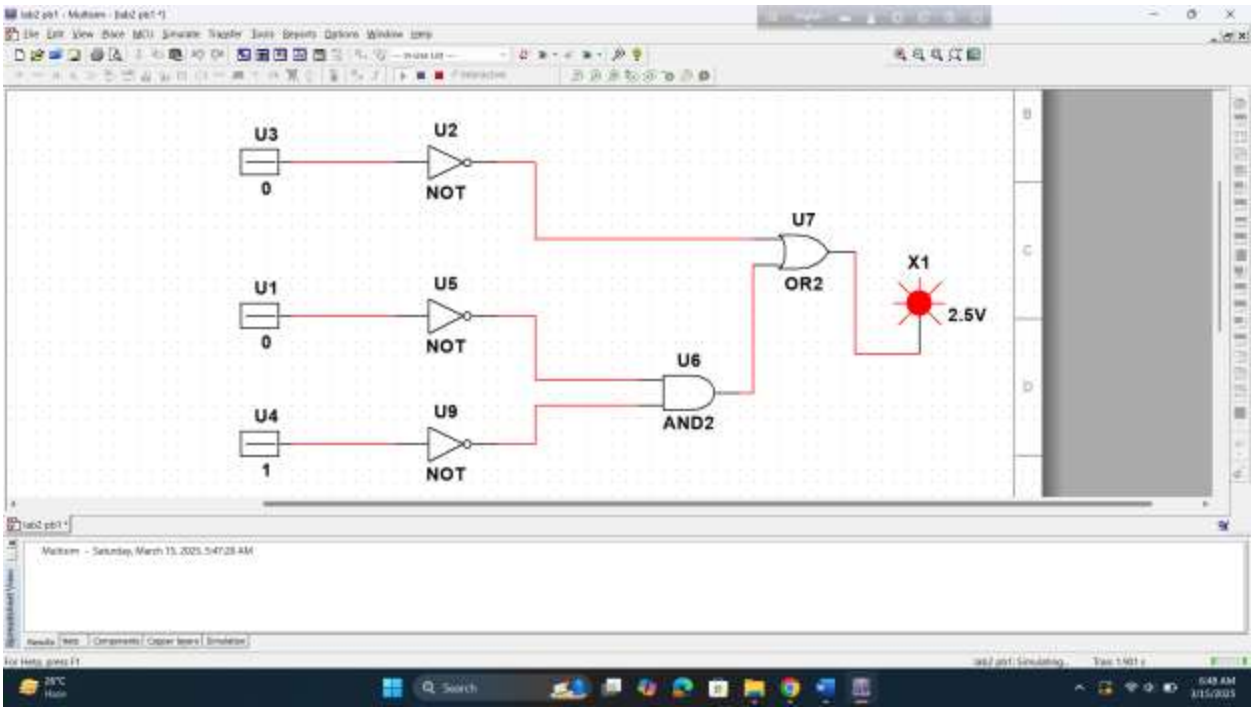
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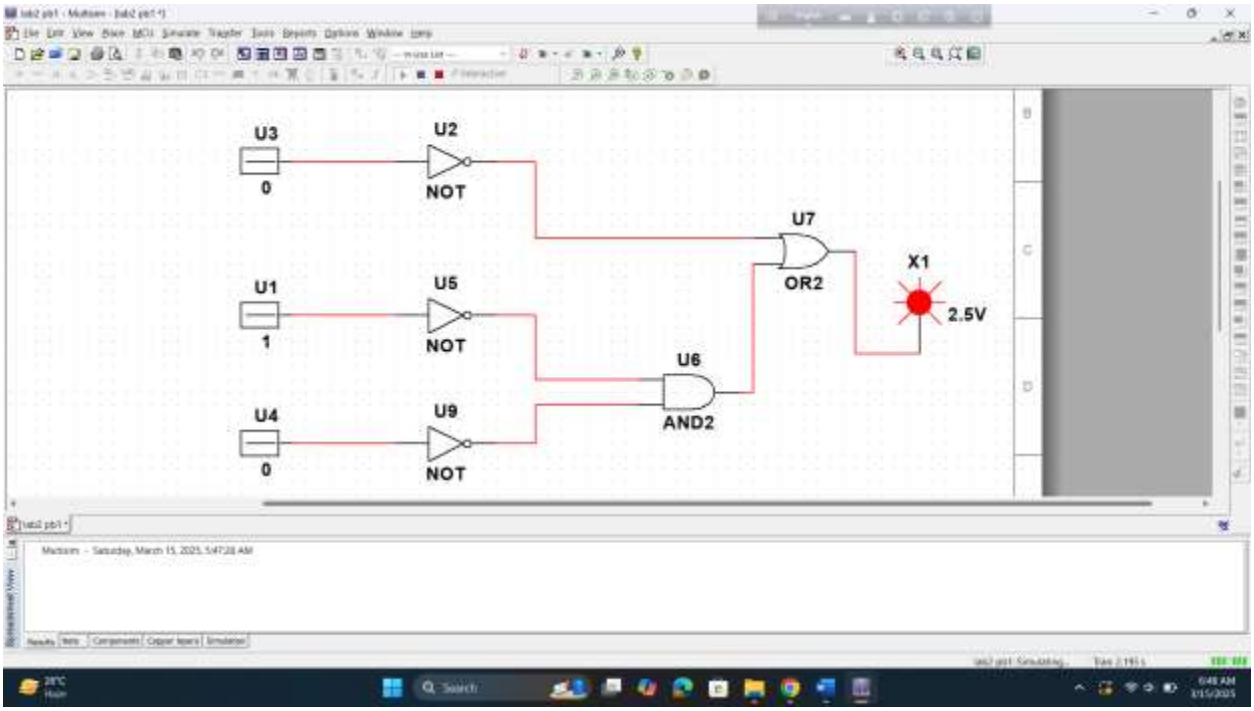
U3
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U7
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U5
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U6
AND2
U4
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U9
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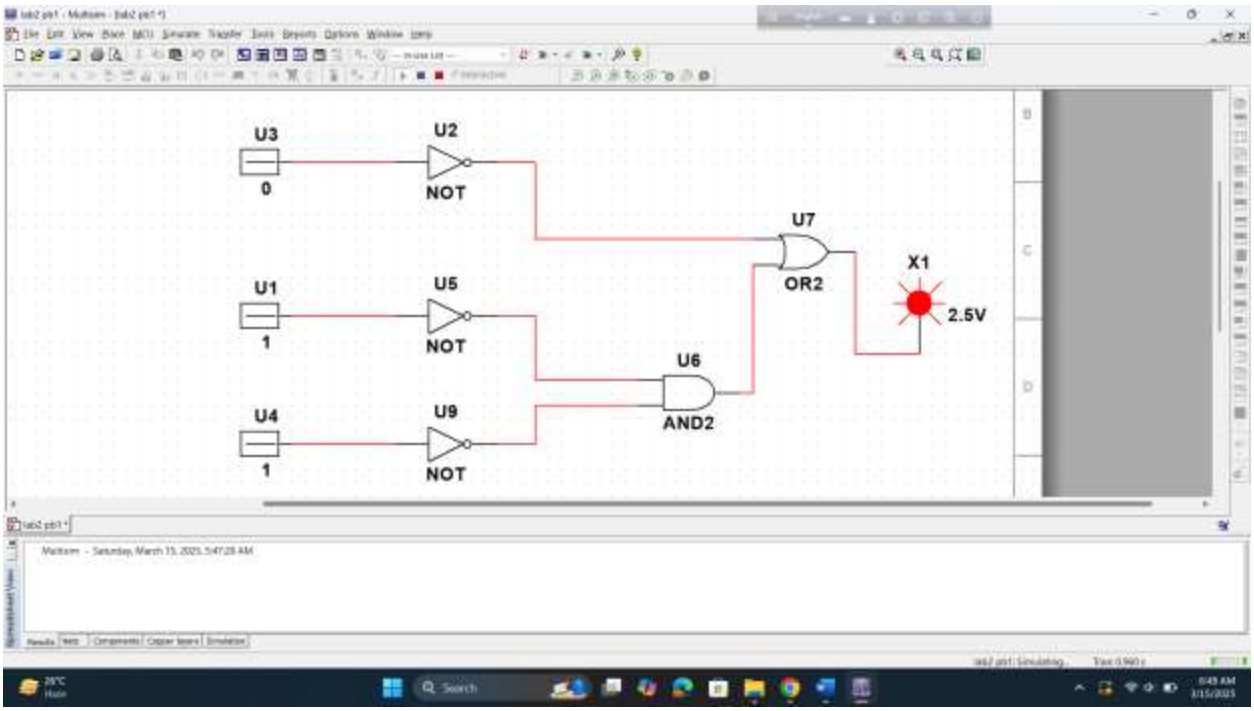
U3
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U2
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U7
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2.5V
U1
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U5
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U6
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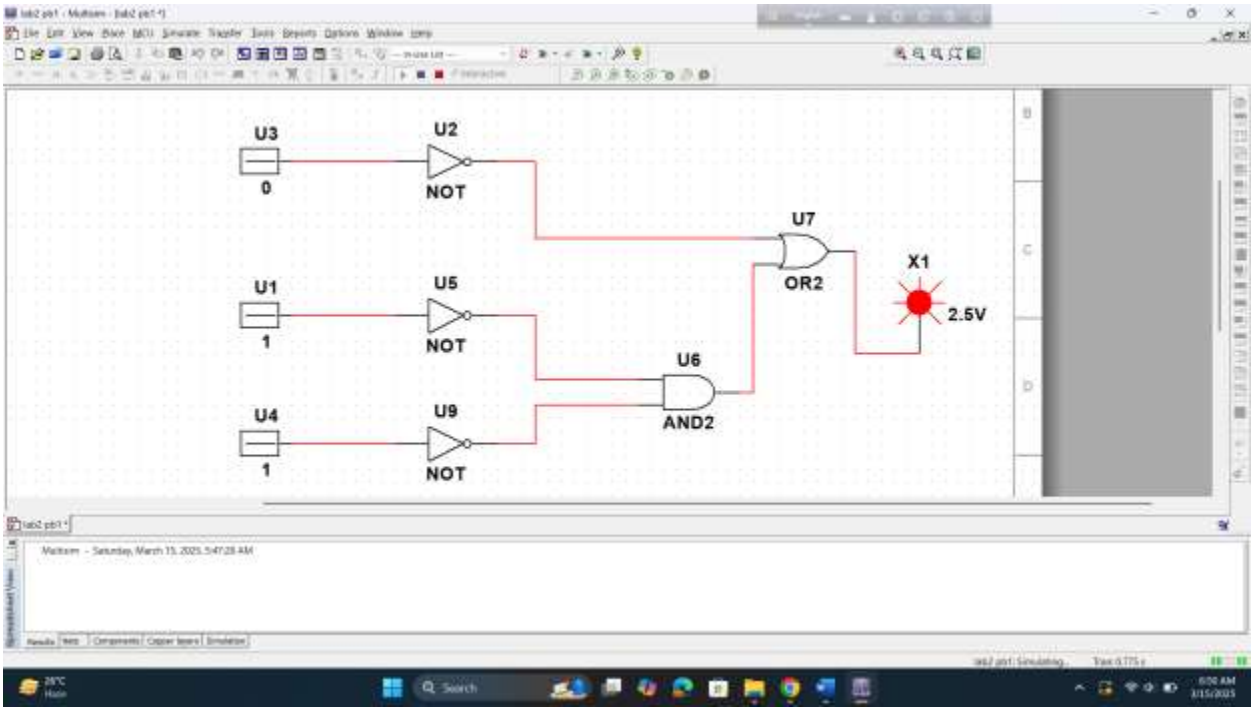
U3
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U2
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U7
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2.5V
U1
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U5
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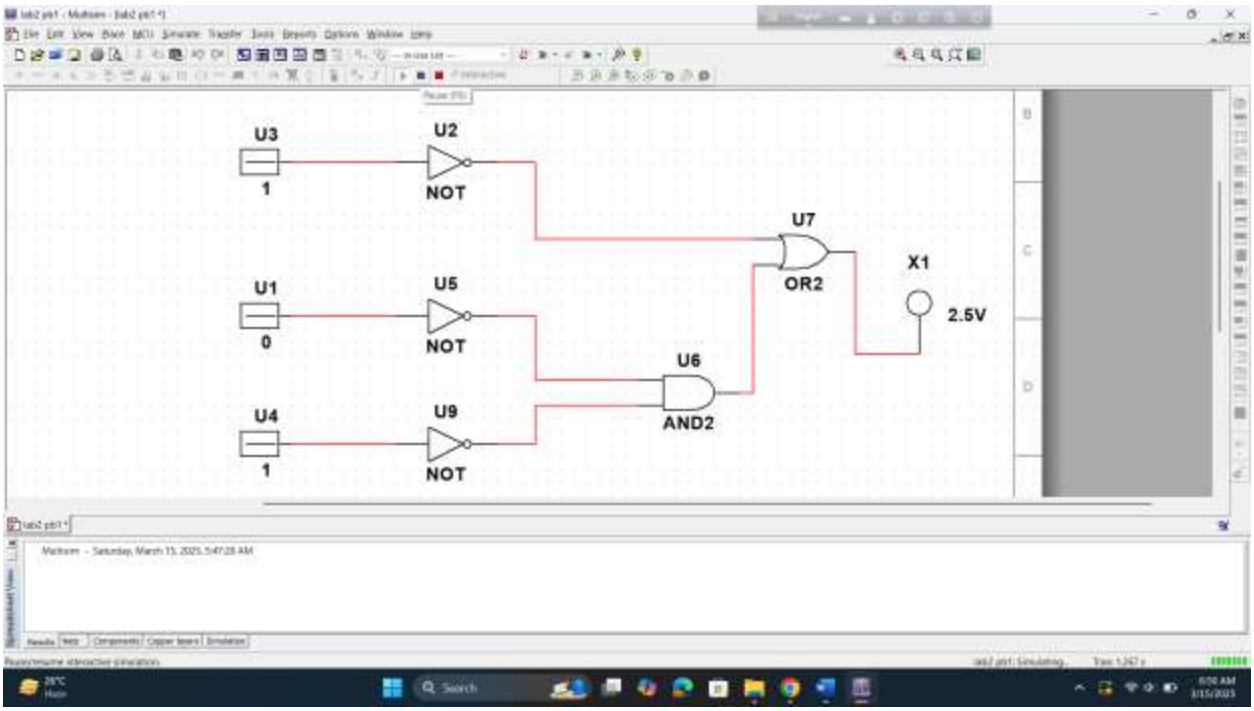
U3
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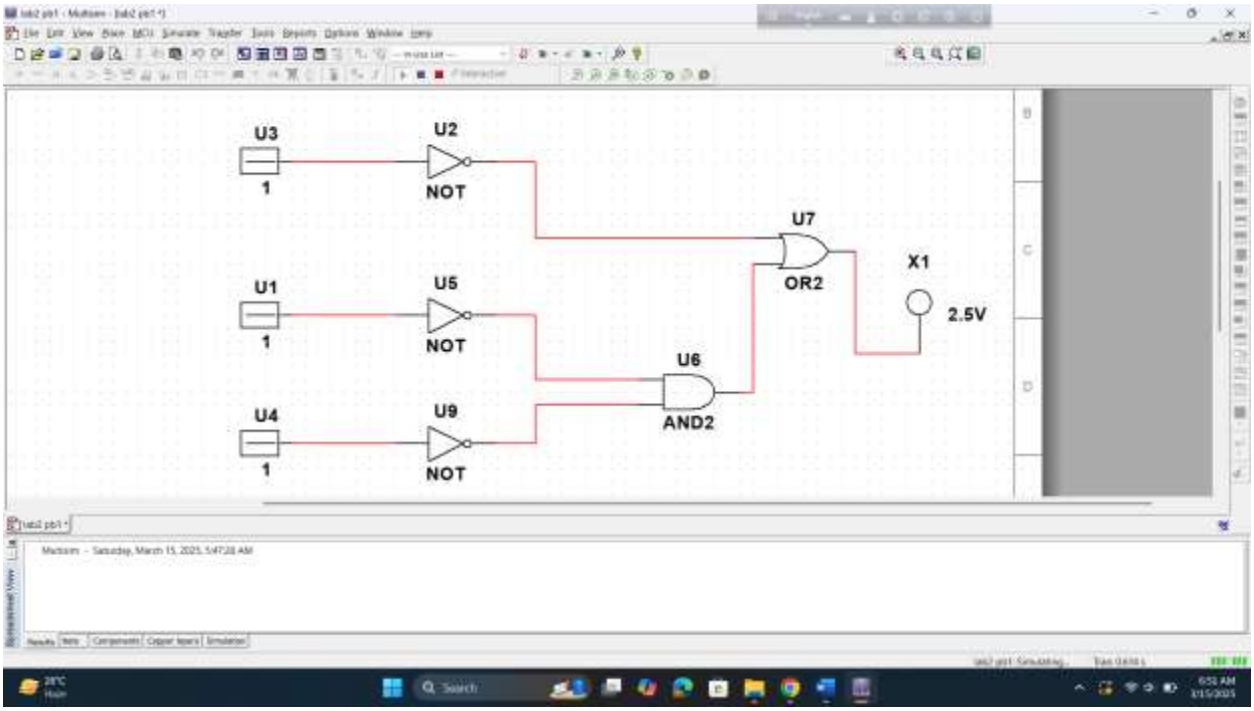
U3
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U2
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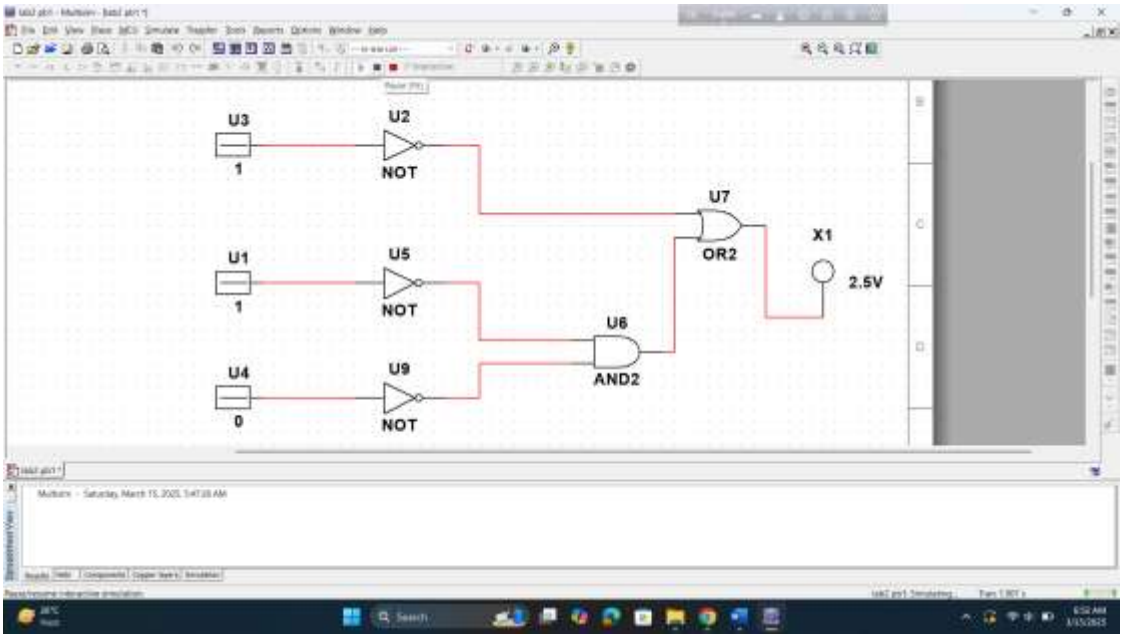
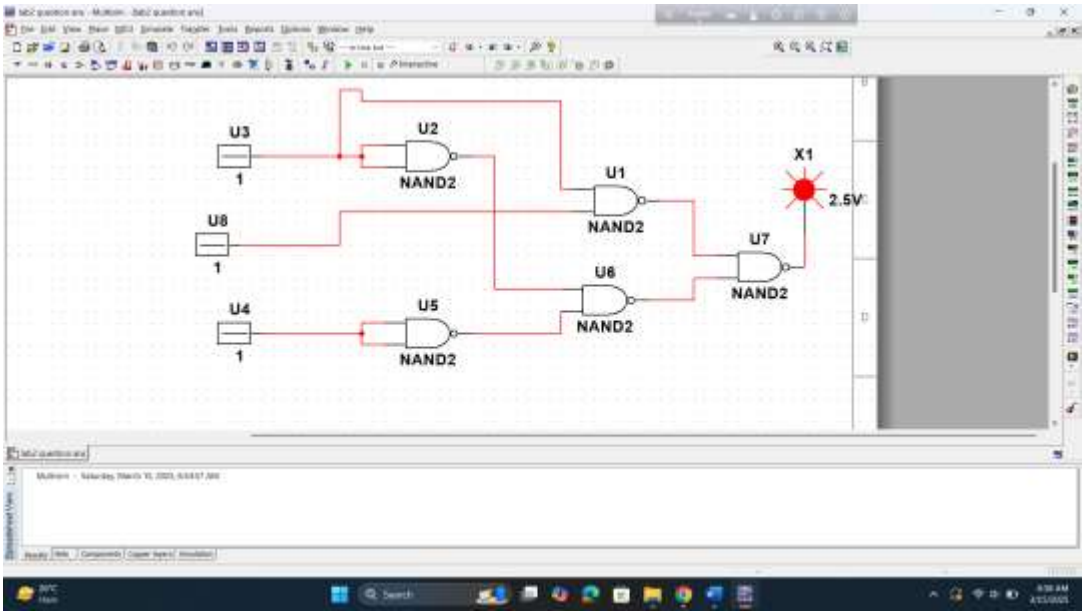


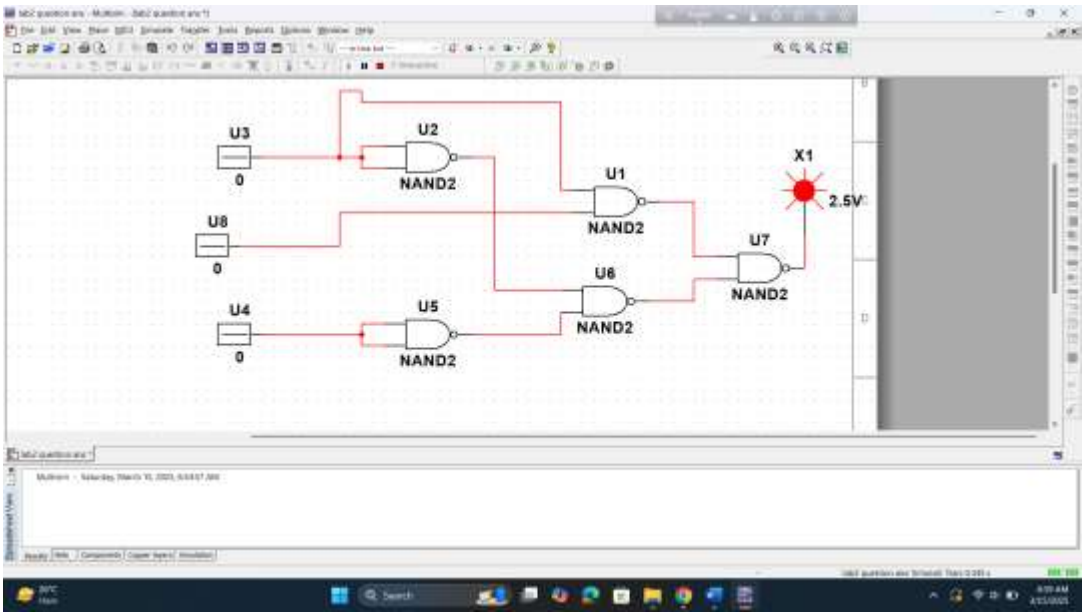
Answer to Questions:

1. **Construct the derived equations (i) and (ii), using Universal gates (both NAND and NOR).**

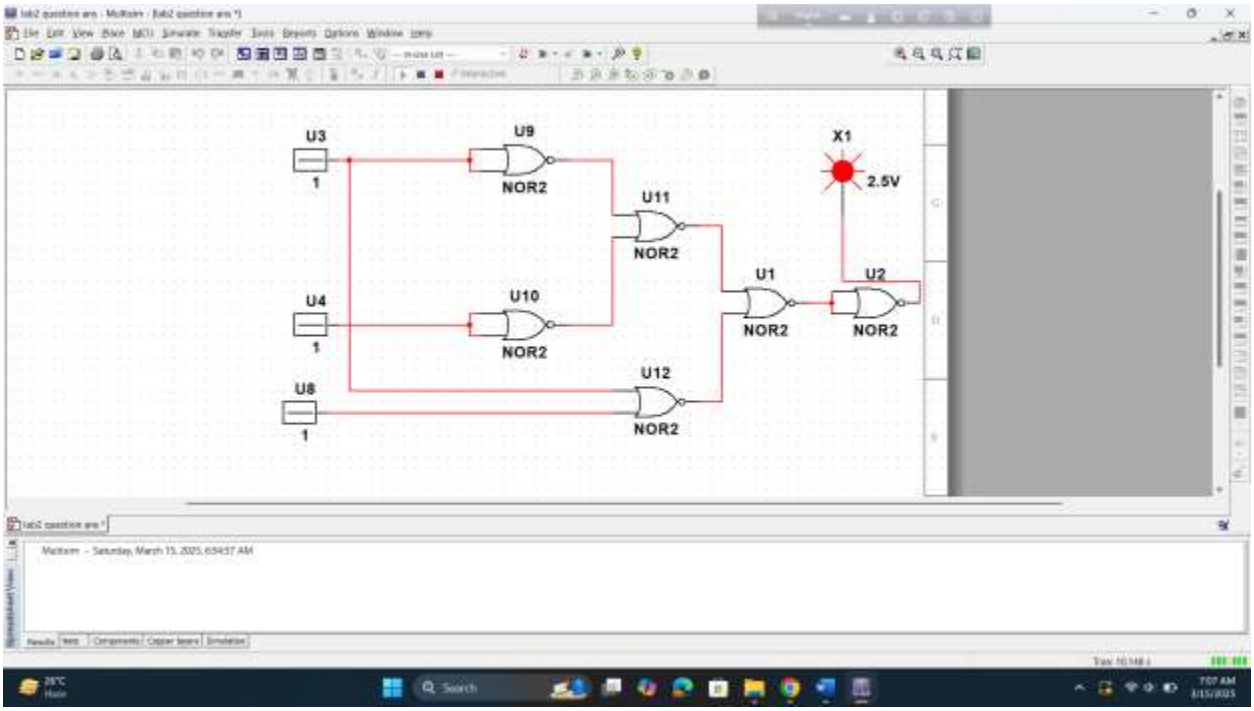
Answer:

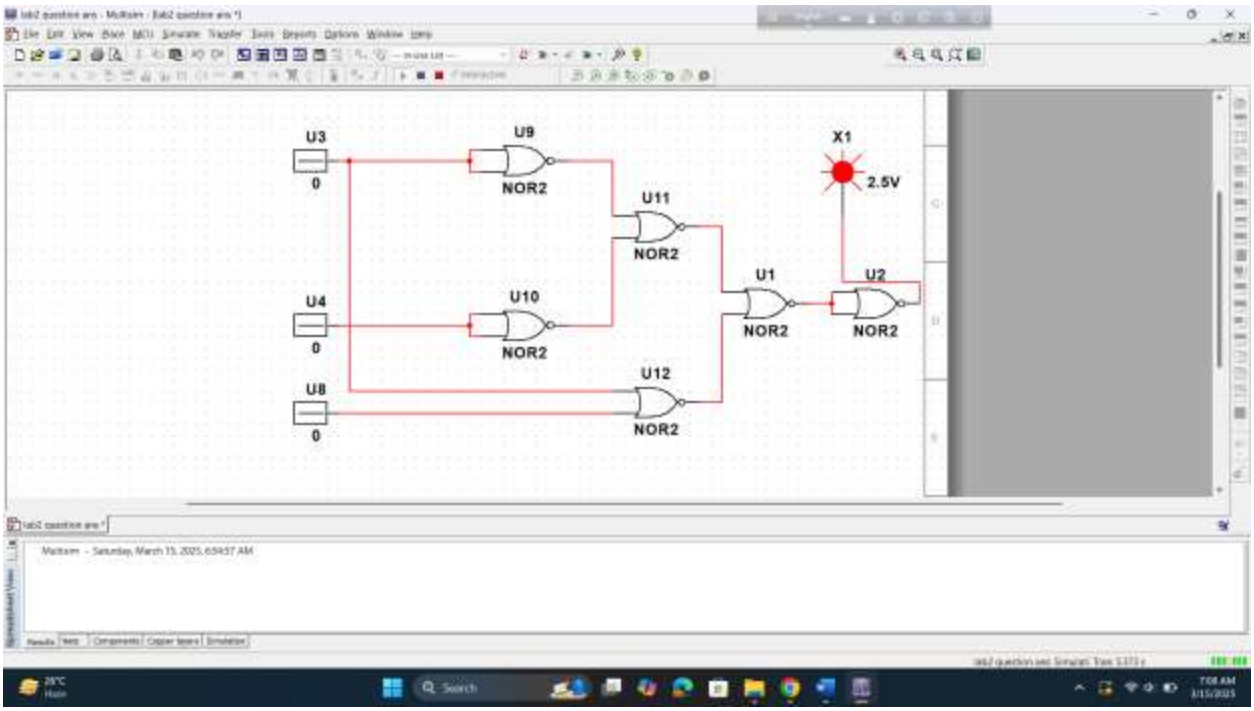
Using NAND Gate





Using NOR Gate



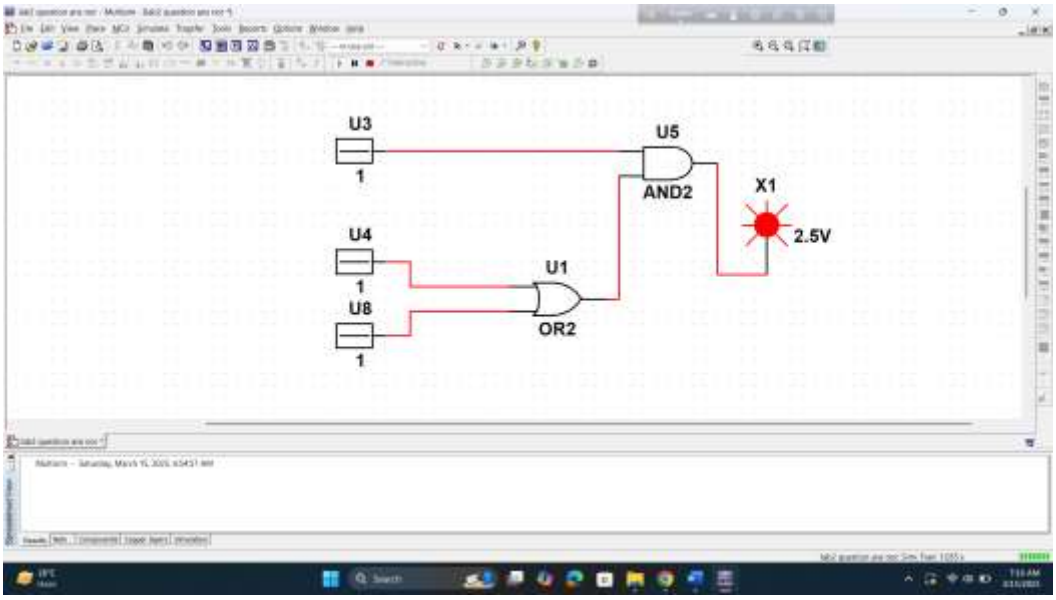


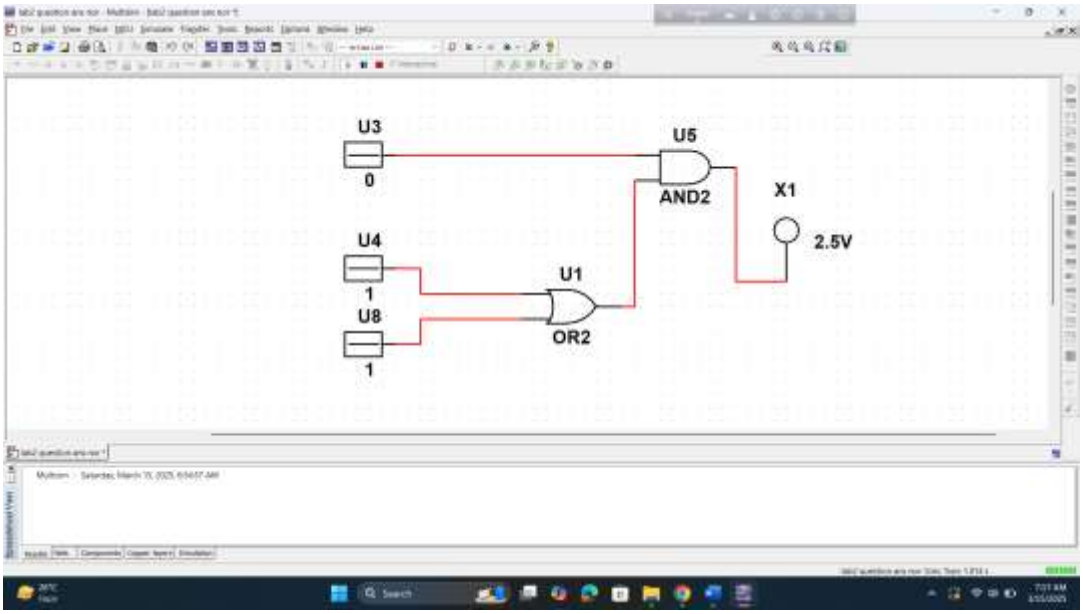
2.Develop the truth table for a certain three-input logic circuit with the output expression Y=ABC+(AB)'C+A'BC+AB'C+A(B'+C).

A	B	C	A'	B'	(AB'	B'+ C	ABC	(AB) 'C	A'B C	AB' C	A(B' +C)	Y
0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	1	1	1	1	1	0	1	0	0	0	1
0	1	0	1	1	1	0	0	0	0	0	0	0
0	1	1	1	1	1	1	0	1	1	0	0	1
1	0	0	0	0	1	1	0	0	0	0	1	1
1	0	1	0	0	1	1	0	1	0	1	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	1	1	0	0	0	1	1

3.Implement the following logic expressions with logic gates Y=ABC+AB+AC

Y=ABC+AB+AC
Y = AB + AC
Y= A (B+C)





Discussion:

We studied combinational circuits and created a truth table in the lab to see whether the circuit was in Sum of Products (SOP) or Product of Sums (POS) form. Logic gates and some other components were used to create the circuits. Using the truth table, we constructed it to generate a Karnaugh map (K-map), where appropriate grouping was achieved to get the output expression.

Input (Vin) and output (Vout) voltages were maintained between GND to VCC for correct operation. It was ensured that ICs were properly connected according to their individual pin configurations. The problem arose when constructing circuit number 2 that prevented us from completing the experiment. Thus, experiment number 2 was left incomplete.

Conclusion:

In this lab, we performed combinational circuits beginning with designing truth tables to achieve the SOP (Sum of Products) and POS (Product of Sums) expressions. We then employed logic gates and other elements to design these circuits. We also employed Karnaugh maps (K-maps) to reduce Boolean expressions by finding the best groupings on the map. This practical exercise helped solidify our understanding in the design of logic circuits and optimization.

References:

1. Thomas L. Floyd, “Digital Fundamentals”, available Edition, Prentice Hall International Inc.