

**AMERICAN INTERNATIONAL**

**UNIVERSITY BANGLADESH (AIUB)**

**FACULTY OF SCIENCE & TECHNOLOGY DEPARTMENT OF**

**ELECTRICAL AND ELECTRONICS ENGINEERING**

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**DIGITAL LOGIC AND CIRCUITS LABORATORY**

**Section: D Group: 03**

**LAB REPORT NAME:**

# Design of adder and comparator circuits.

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# Title:

# Design of adder and comparator circuits.

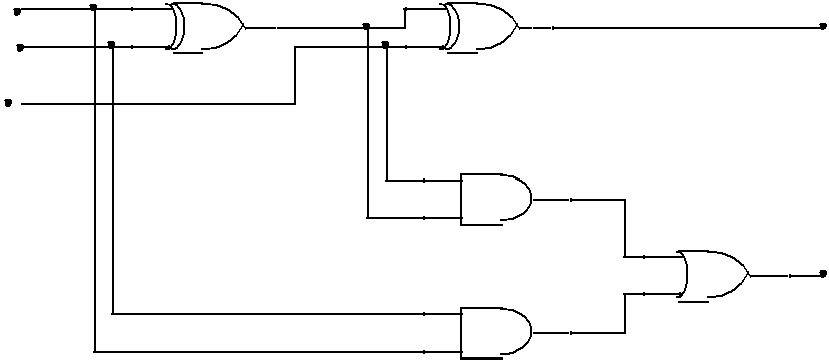
**Abstract:**

The purpose of this experiment is to learn the design and behaviour of adder, subtractor and comparator logic circuits. Adders and subtractors are the most basic and most important part of digital electronics.

**Theory and Methodology:**

An adder or summer is a combinational circuit that adds binary numbers. There are mainly two kinds of adders, half adder and full adder. The half adder can add only two single bits of binary digit and outputs the sum of the bits and a carry which is the overflow of the sum. A full adder can add two single bit digits and one carry bit which is the overflow of the sum of the previous stage of addition and outputs the sum and the carry.

S



A B

in

Cin

C

Full Adder

**Fig.1.1**: Schematics of Full Adder

The Boolean expression for half and full adder is given below –

Half Adder:

S = A ⊕ B

Cout = AB

Full Adder:

S = A ⊕ B ⊕ Cin

Cout = Cin (A ⊕ B) + AB

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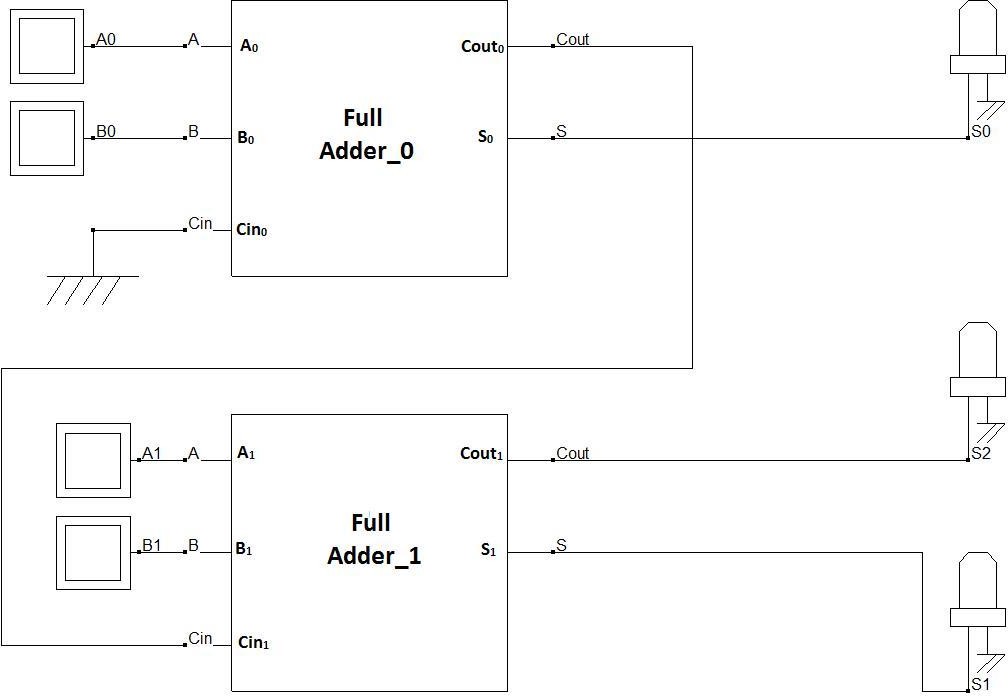
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Truth table for full adder –

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Cin | S | C |
| 0 | 0 | 0 |  |  |
| 0 | 0 | 1 |  |  |
| 0 | 1 | 0 |  |  |
| 0 | 1 | 1 |  |  |
| 1 | 0 | 0 |  |  |
| 1 | 0 | 1 |  |  |
| 1 | 1 | 0 |  |  |
| 1 | 1 | 1 |  |  |

## **Using Full Adder blocks for addition of n- bit systems:**

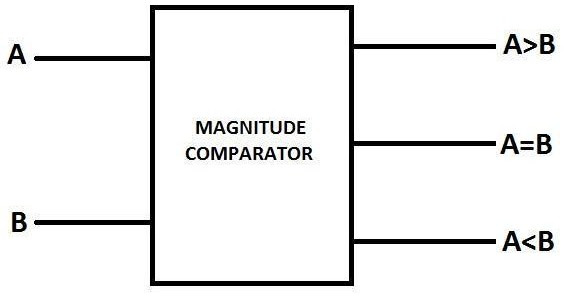
Full adder blocks can be connected for summation of n-bit systems. To design a 2 bit full adder, two 1 bit full adders are connected in parallel connection as shown in the figure below. The same process can be used for designing n-bit Full Adder for addition of words having a length of n-bits.



**Fig. 1.3:** 2-bit Full adder design using 1 bit full adder blocks

Here, the LSB of both word A and B (A0 and B0) are connected in the first stage full adder block and Cin of this block (Cin0) is connected to ground (as there is no carry in available at the initial stage). The MSB of both word A and B (A1 and B1) are connected in the first stage full adder block and Cin of this block (Cin1) is connected to the previous stage Cout (Cout0). Summation output for the LSB is available from the first stage Sum (S0). The next stage block outputs Sum (S1) and Carry out (Cout1) provide the MSBs for the next stage output (S1 and and S2).

**Theory and Methodology:** Magnitude Comparators are combinational logic circuits that take 2 sets of data as its inputs and tests whether the value represented by one binary word is greater than, less than, or equal to the value represented by another binary word.



**Fig.2.1**: Block Diagram of 1 Bit Magnitude Comparator

Depending on the input combination for a 1-bit magnitude comparator, following behavior table can be developed using the logic expressions.

# A=B if, A=B=0 or A=B=1;

**A>B if A=1 and B=0; A<B if A=0 and B=1;**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** |  | **B** |  |  | **A=B** |  |  | **A>B** |  |  | **A<B** |  |
| **0** | | **0** | | **1** | | | **0** | | | **0** | | |
| **0** | | **1** | | **0** | | | **0** | | | **1** | | |
| **1** | | **0** | | **0** | | | **1** | | | **0** | | |
| **1** | | **1** | | **1** | | | **0** | | | **0** | | |

The SOP expressions for the output lines can be written as

# (A=B)= A’B’+AB;

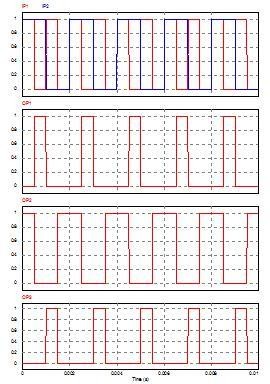
**(A<B)= AB’;**

**(A>B)=A’B;**

A diagram of a circuit

Description automatically generated

**Fig.2.2:** 1-Bit Comparator



**Fig.2.3**: Timing Diagram for 1 - Bit

## **Apparatus:**

1. Digital trainer board 2. IC 7408:2 pcs

3. IC 7404:2 pcs

4. IC 7486:2 pcs

5. IC 7431:2 pcs

6. IC 7483:1 pcs

7. Connecting wires

## **Precautions:**

1. It should be ensured that all the LEDs and toggle switches on the trainer board are functioning properly.
2. Short circuits must be avoided, as excessive current flow can generate heat, which may damage the components.

## **Experimental Procedure:**

1. The output and the truth tables of the logic circuits for the full adder, as described in the theory and methodology section, should be determined.

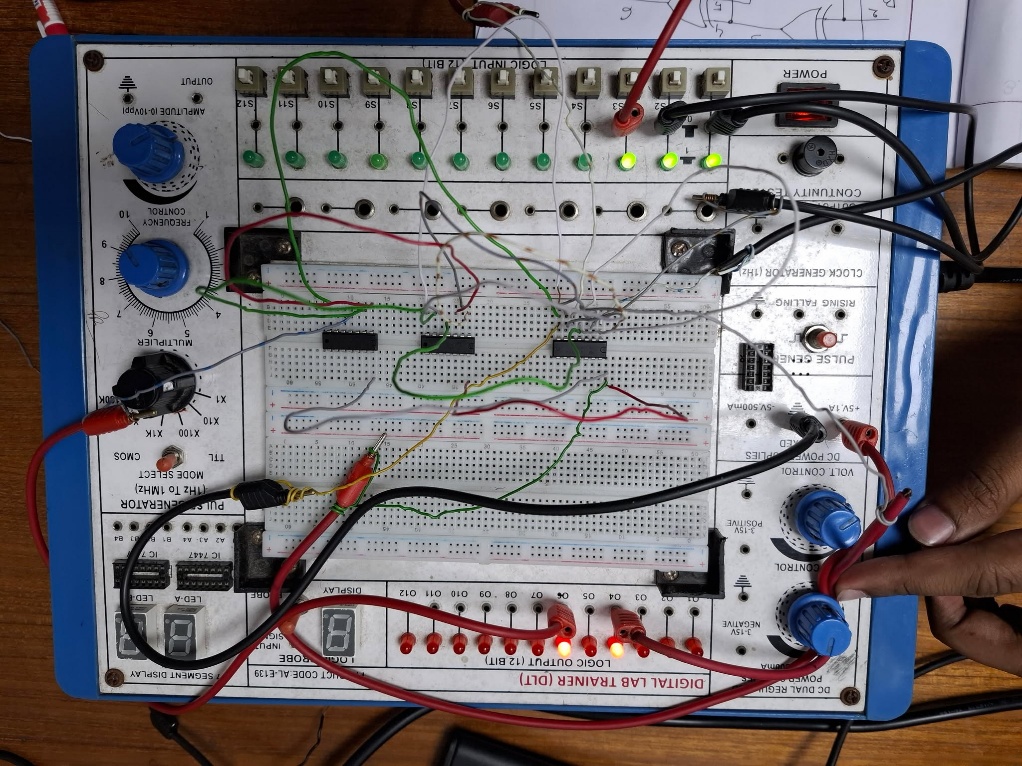
2. The required logic gates and their quantities should be identified, and all relevant IC numbers must be checked and recorded.

3. The ICs should be carefully placed on the Trainer Board and biased by connecting them to the +5V DC supply and ground.

4. The connections should be made using wires according to the logic diagram, and the outputs should be connected to the LEDs.

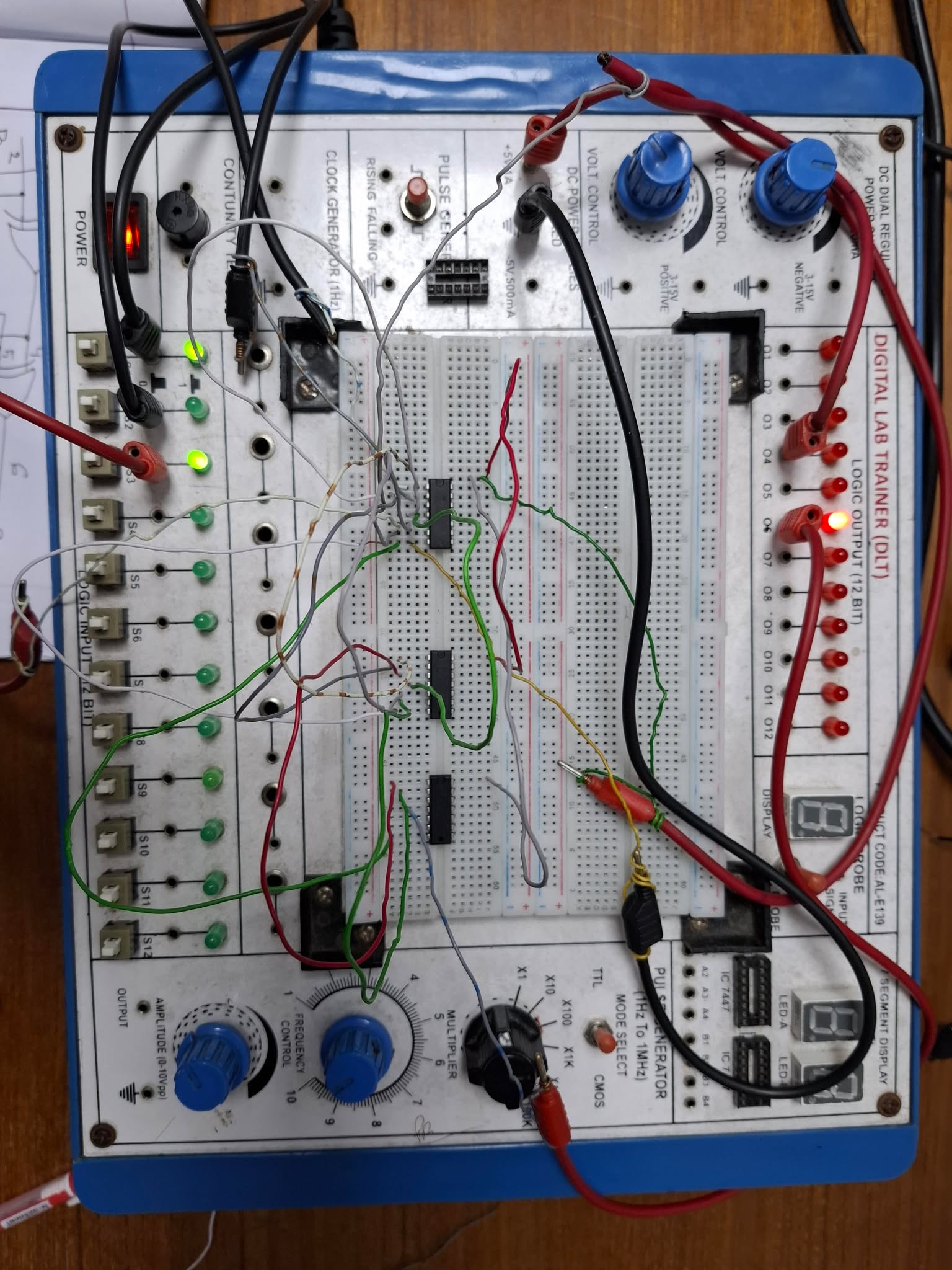
5. Different input combinations, as per the derived truth table, should be applied, and the resulting outputs should be observed and recorded.

**Measurement :**



A close-up of a circuit board

Description automatically generated

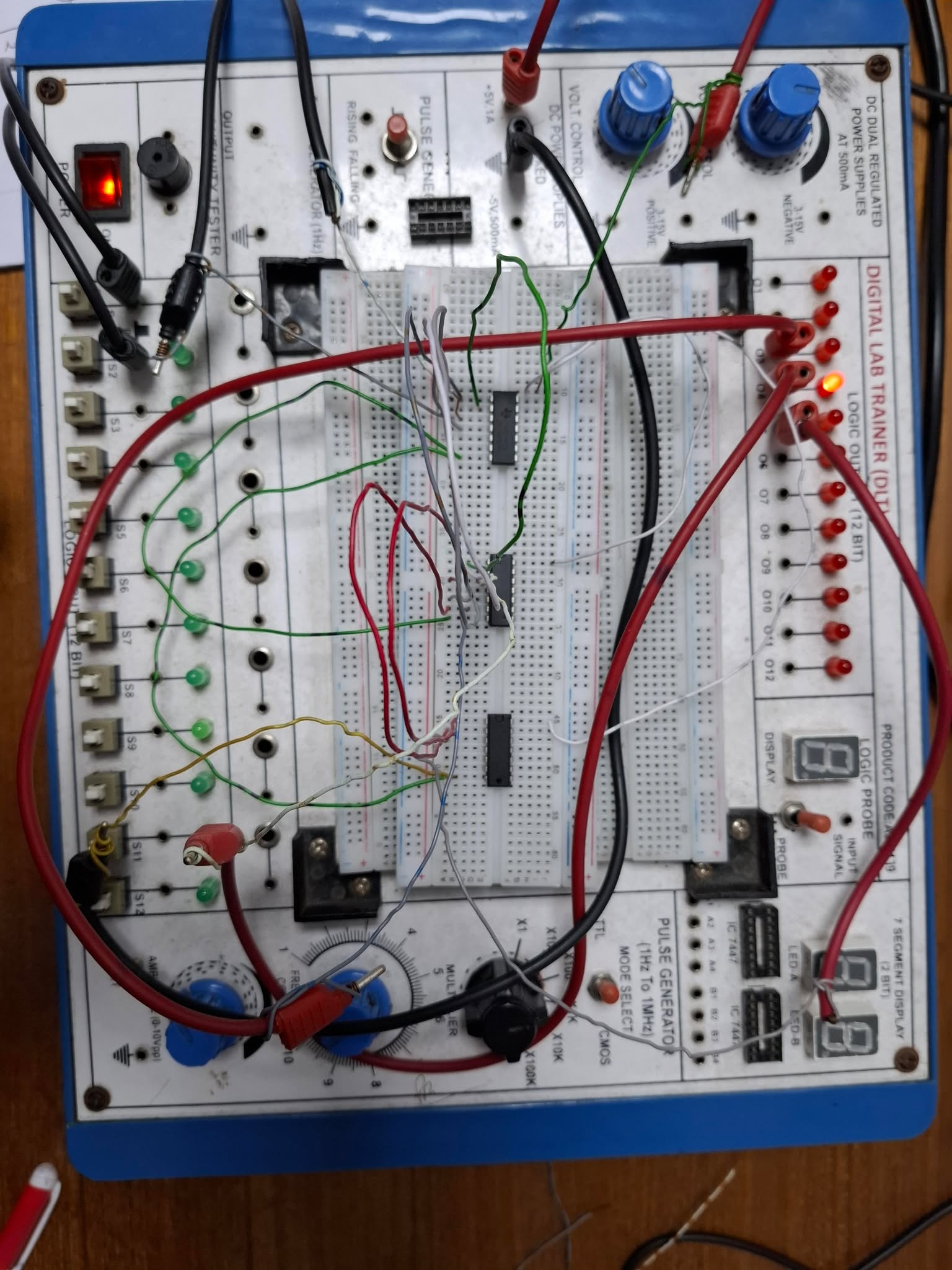


A circuit board with wires and switches

Description automatically generated

A white electronic device with wires and switches

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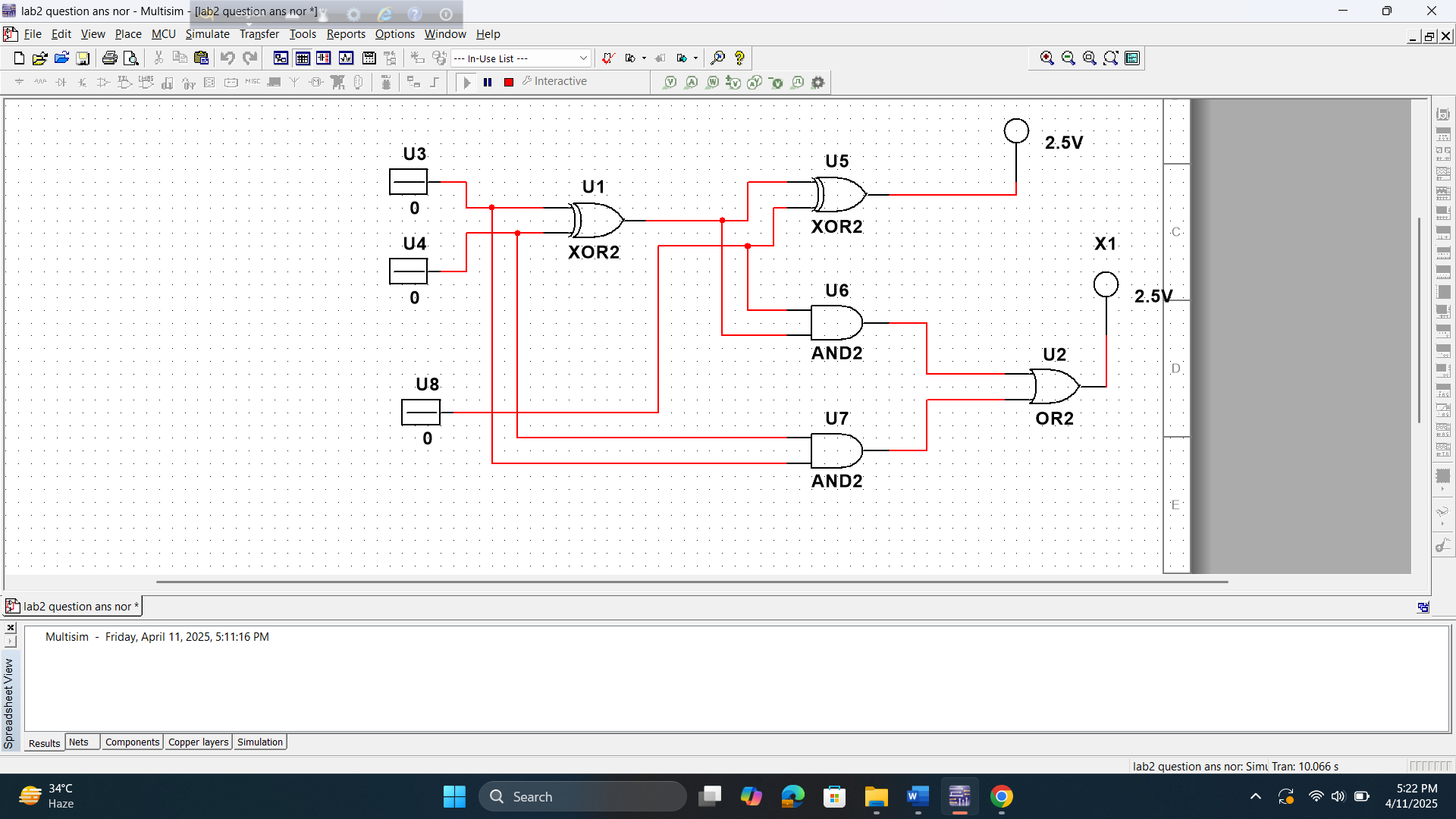


A close-up of a circuit board

Description automatically generated

**Simulation and Measurement:**

**Full adder :**



A computer screen shot of a computer screen

Description automatically generated

A computer screen shot of a computer screen

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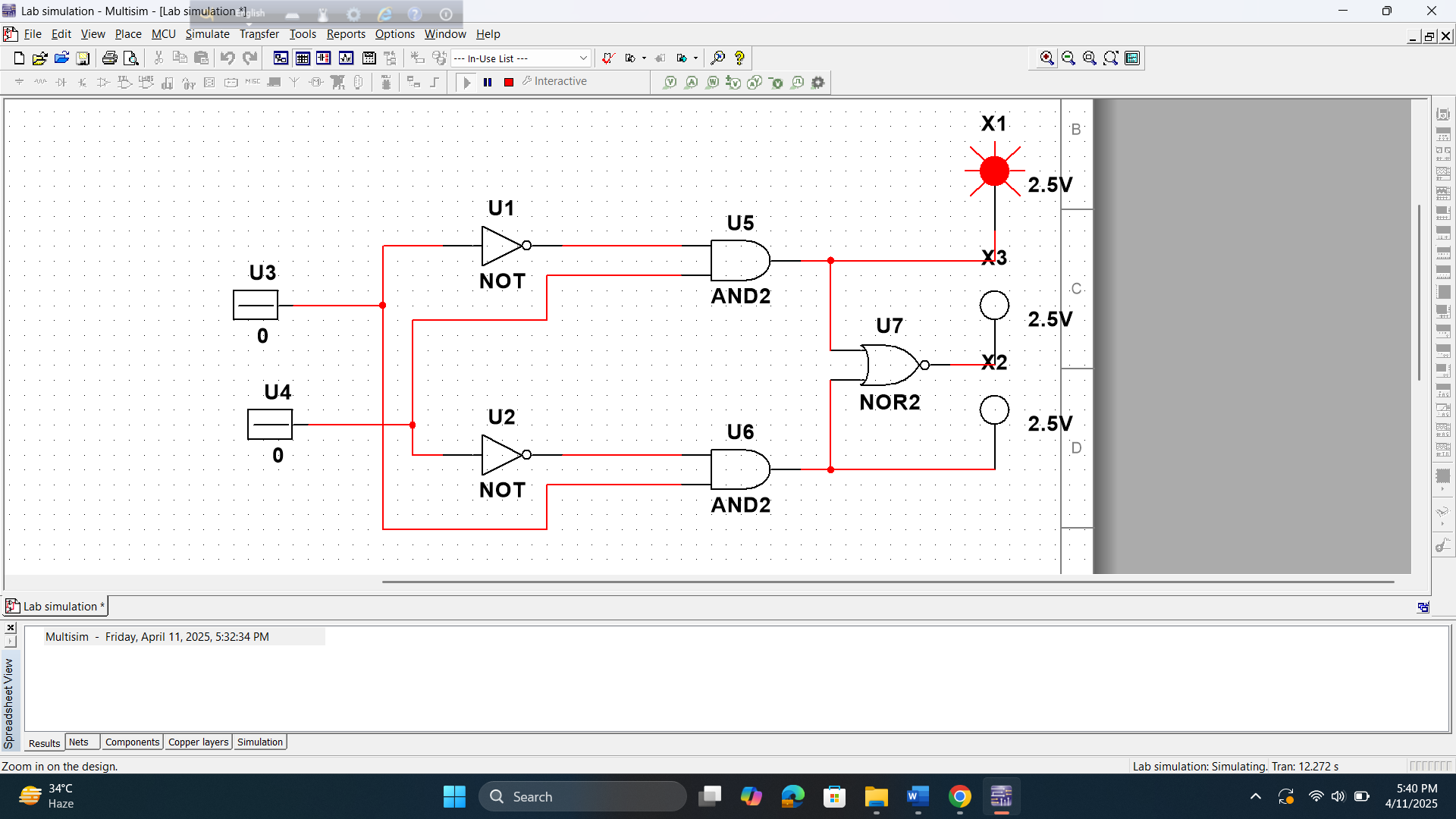
A computer screen shot of a computer screen

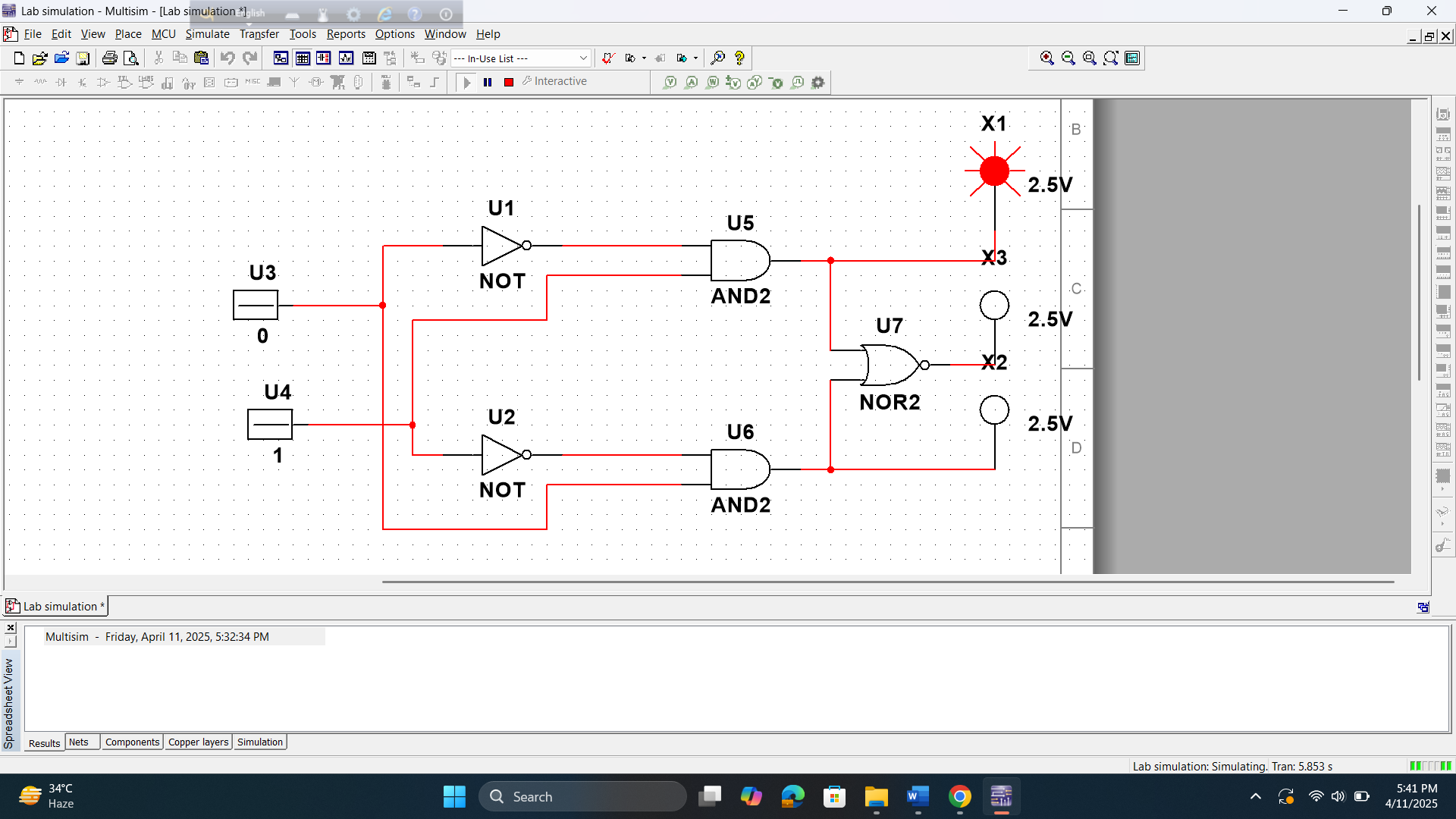
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**1-Bit Comparator :**

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**A computer screen shot of a diagram

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**A computer screen shot of a diagram

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**Discussion and Conclusion:**

The data and findings suggest the extent to which the experiment successfully met its initial objectives. By analyzing the results, it is evident that the experiment achieved several of its intended outcomes, though some deviations from the expected results were observed. These discrepancies may be attributed to certain procedural errors or limitations in the experimental setup.

One notable mistake involved [insert a specific error if known, e.g., inaccurate measurements, inconsistent conditions, or human error], which may have impacted the reliability of the data. To improve the study, future investigations could implement stricter control of variables, enhance measurement precision, and ensure a more rigorous adherence to the experimental procedure. Additionally, increasing the sample size or conducting repeated trials could help in obtaining more reliable and generalizable results.

**Reference:**

<http://www.circuitstoday.com/half-adder-and-full-adder>