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**FACULTY OF SCIENCE & TECHNOLOGY DEPARTMENT OF**

**ELECTRICAL AND ELECTRONICS ENGINEERING**

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**DIGITAL LOGIC AND CIRCUITS LABORATORY**

**Section: D Group: 03**

**LAB REPORT NAME:**

Construction of Diode and Transistor Logic Gates

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**Title:** Construction Logic Gates using various MOS transistors

**Part I: Construction of MOSFET Logic Gates**

# Theory and Methodology:

#### CMOS Logic:

CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors. Thus they became the obvious choice of replacing NMOS transistors at the integrating circuit level design in all applications.

CMOS consists of one p-channel MOSFET or PMOS and one NMOS. The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. When OFF, their resistance is effectively infinite; when ON, their channel resistance is quite low (around 200 Ω). Since the gate is essentially an open circuit it draws no current and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

#### CMOS Inverter:

When the input is grounded (logic 0), the N-channel MOSFET is unbiased, and therefore has no channel enhanced within itself. It is an open circuit, and therefore leaves the output line disconnected from ground. At the same time, the P-channel MOSFET is forward biased, so it has a channel enhanced within itself. This channel has a resistance of about 200 Ω, connecting the output line to the +V supply. This pulls the output up to +V (logic 1).

When input A is at +V (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

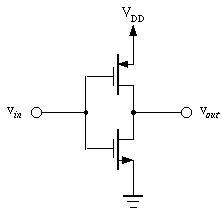


Fig.5 CMOS Inverter

**Part I: Construction of MOSFET Logic Gates**

# Introduction:

### MOSFET:

Pronounced MAWS-feht. Acronym for metal-oxide semiconductor field-effect transistor. These are used in many scenarios where you want to convert voltages. On your motherboard for example to generate CPU Voltage, Memory Voltage, AGP Voltage etc. Mosfets are usually used in pairs. If you see six mosfets around your CPU socket you have three-phase power.

### Technical Info

MOSFETs come in four different types. They may be enhancement or depletion mode, and they may be n-channel or p-channel. For this application we are only interested in n-channel enhancement mode MOSFETs, and these will be the only ones talked about from now on. There are also logic-level MOSFETs and normal MOSFETs. The only difference between these is the voltage level required on the gate.

A diagram of a circuit

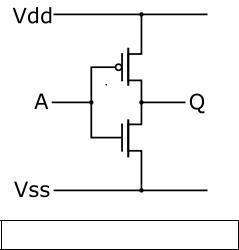
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Unlike bipolar transistors that are basically current-driven devices, MOSFETs are voltage-controlled power devices. If no positive voltage is applied between gate and source the MOSFET is always non- conducting. If we apply a positive voltage UGS to the gate we'll set up an electrostatic field between it and the rest of the transistor. The positive gate voltage will push away the 'holes' inside the p-type substrate and attracts the moveable electrons in the n-type regions under the source and drain electrodes. This produces a layer just under the gate's insulator through which electrons can get into and move along from source to drain. The positive gate voltage therefore 'creates' a channel in the top layer of material between oxide and p-Si. Increasing the value of the positive gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel. As a result we find that the size of the channel we've made increases with the size of the gate voltage and enhances or increases the amount of current which can go from source to drain- this is why this kind of transistor is called an enhancement mode device. Hence the operation of a p-channel MOSFET is just the opposite of an n-channel MOSFET.

### **CMOS:**

**Complementary metal–oxide–semiconductor** (**CMOS**) is a technology for constructing [integrated](http://en.wikipedia.org/wiki/Integrated_circuit) [circuits.](http://en.wikipedia.org/wiki/Integrated_circuit) CMOS technology is used in [microprocessors,](http://en.wikipedia.org/wiki/Microprocessor) [microcontrollers,](http://en.wikipedia.org/wiki/Microprocessor) [static RAM,](http://en.wikipedia.org/wiki/Static_Random_Access_Memory) and other [digital](http://en.wikipedia.org/wiki/Digital_logic) [logic](http://en.wikipedia.org/wiki/Digital_logic) circuits. CMOS technology is also used for several analog circuits such as [image sensors (CMOS](http://en.wikipedia.org/wiki/Image_sensor) [sensor),](http://en.wikipedia.org/wiki/CMOS_sensor) [data converters,](http://en.wikipedia.org/wiki/CMOS_sensor) and highly integrated [transceivers](http://en.wikipedia.org/wiki/Transceiver) for many types of communication. [Frank](http://en.wikipedia.org/wiki/Frank_Wanlass) [Wanlass](http://en.wikipedia.org/wiki/Frank_Wanlass) patented CMOS in 1963 [(US patent 3,356,858).](http://en.wikisource.org/wiki/United_States_patent_3356858)

CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of [p-type](http://en.wikipedia.org/wiki/P-type_semiconductor) and [n-type metal oxide semiconductor](http://en.wikipedia.org/wiki/N-type_semiconductor) [field effect transistors](http://en.wikipedia.org/wiki/Metal_oxide_semiconductor_field_effect_transistor) (MOSFETs) for logic functions.



CMOS inverter ([NOT logic gate](http://en.wikipedia.org/wiki/Inverter_%28logic_gate%29))

Two important characteristics of CMOS devices are high [noise immunity](http://en.wikipedia.org/wiki/Electronic_noise) and low static [power](http://en.wikipedia.org/wiki/Power_consumption) [consumption.](http://en.wikipedia.org/wiki/Power_consumption) Since one [transistor](http://en.wikipedia.org/wiki/Transistor) of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much [waste heat](http://en.wikipedia.org/wiki/Waste_heat) as other forms of logic, for example [transistor–transistor logic](http://en.wikipedia.org/wiki/Transistor%E2%80%93transistor_logic) (TTL) or [NMOS logic,](http://en.wikipedia.org/wiki/NMOS_logic) which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in [VLSI](http://en.wikipedia.org/wiki/VLSI) chips.

Some advantages of CMOS over TTL are:

* CMOS gate inputs draw far less current than TTL inputs, because MOSFETs are voltage- controlled, not current-controlled, devices.
* CMOS gates are able to operate on a much wider range of power supply voltages than TTL: typically 3 to 15 volts versus 4.75 to 5.25 volts for TTL
* CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors.

In this experiment, we will first look at some logic circuit designs using NMOS. Then we will implement the same logic circuits using CMOS and try to identify the potential design advantages of CMOS over NMOS.

# Designing a Half Adder using CMOS

# Theory and Methodology:

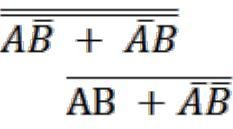
To design any logic circuit first the truth table is needed to be established using different combinations of logic ‘0’ and ‘1’ to get the desired output. After that the gate level design is found from which transistor level design is done using desired transistors. Here CMOS is used for the transistor level design of the Half Adder. The whole process is given step wise below:

# Half Adder:

## **A diagram of a circuit AI-generated content may be incorrect.Gate Level Design:**

Fig-2 Logic diagram of a Half Adder.

Equation of Sum = A (XOR) B



=  +

This equation can be rewritten as =

=

Equation of Carry= AB

**Introduction:**

**ADDER:**

In electronics, an **adder** or **summer** is a [digital circuit](http://en.wikipedia.org/wiki/Digital_circuit) that performs [addition](http://en.wikipedia.org/wiki/Addition) of numbers. In many [computers](http://en.wikipedia.org/wiki/Computer) and other kinds of processors, adders are used not only in the [arithmetic logic unit](http://en.wikipedia.org/wiki/Arithmetic_logic_unit)(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.

Although adders can be constructed for many numerical representations, such as [binary-coded decimal](http://en.wikipedia.org/wiki/Binary-coded_decimal) or [excess-3,](http://en.wikipedia.org/wiki/Excess-3) the most common adders operate on [binary](http://en.wikipedia.org/wiki/Binary_numeral_system) numbers. In cases where [two's complement](http://en.wikipedia.org/wiki/Two%27s_complement) or [ones' complement](http://en.wikipedia.org/wiki/Ones%27_complement) is being used to represent negative numbers, it is trivial to modify an adder into an [adder– subtractor.](http://en.wikipedia.org/wiki/Adder%E2%80%93subtractor) Other [signed number representations](http://en.wikipedia.org/wiki/Signed_number_representations) require a more complex adder.

A black and white diagram

AI-generated content may be incorrect.

## Fig-1 Half adder logic diagram

The **half adder** adds two single binary digits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2*C*

*S*. The simplest half-adder design, pictured above, incorporates an [XOR gate](http://en.wikipedia.org/wiki/XOR_gate) for S and an [AND gate](http://en.wikipedia.org/wiki/AND_gate) for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.

The half-adder adds two input bits and generate carry and sum which are the two outputs of half-adder. The input variables of a Half adder are called the Augend and addend bits. The output variables are the Sum and Carry. The

Truth table and equations for the Half adder are :



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **A+B** | **S** | **C** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 2 | 0 | 1 |

This experiment is to help the student in understanding the design at the transistor level.

# Apparatus:

1. PMOS,
2. NMOS,
3. IC 7404(Inverter).
4. Connecting wires.
5. Trainer Board

# Precautions:

All connections should be checked by the instructor after the circuit has been set up. Only the required voltage, within the VDD range, should be applied to ensure that the transistors and/or chip are turned on properly. Excess voltage must be avoided, as it may lead to damage of the components.

**Experimental Procedure:**

The Half Adder circuit using CMOS should be constructed on the breadboard based on the provided expression and truth table. The schematic circuit diagrams for the SUM and CARRY outputs should be drawn and presented to the instructor for verification. Once approved, the circuit should be implemented, and the corresponding values should be recorded in the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| Input A | Input B | Carry Out | Sum |
| 0 V | 0 V |  |  |
| 0 V | 5 V |  |  |
| 5 V | 0 V |  |  |
| 5 V | 5 V |  |  |

**MOSFET pin configuration:**

A diagram of a transistor

Description automatically generated

### **Apparatus:**

1. 10KΩ resistor (brown-black-orange).
2. 1N914 diodes or equivalent.

Connecting wires. (4)Trainer Board

**Precautions:**

After the circuit has been set up, all connections should be checked by the instructor. Only sufficient voltage within the VDD range should be applied to ensure proper operation of the transistors and/or chip. Application of excessive voltage must be avoided, as damage to the components may occur.

# Experimental Procedure:

1. The circuit for the NMOS inverter should be set up as shown in Fig. 1.

2. For each input combination, the output should be determined and recorded in a Truth Table. Two sets of outputs should be included in the table—one representing the ideal values and the other representing the experimental results.

3. Steps 1 and 2 should be repeated for each circuit configuration shown from Fig. 2 to Fig. 7.

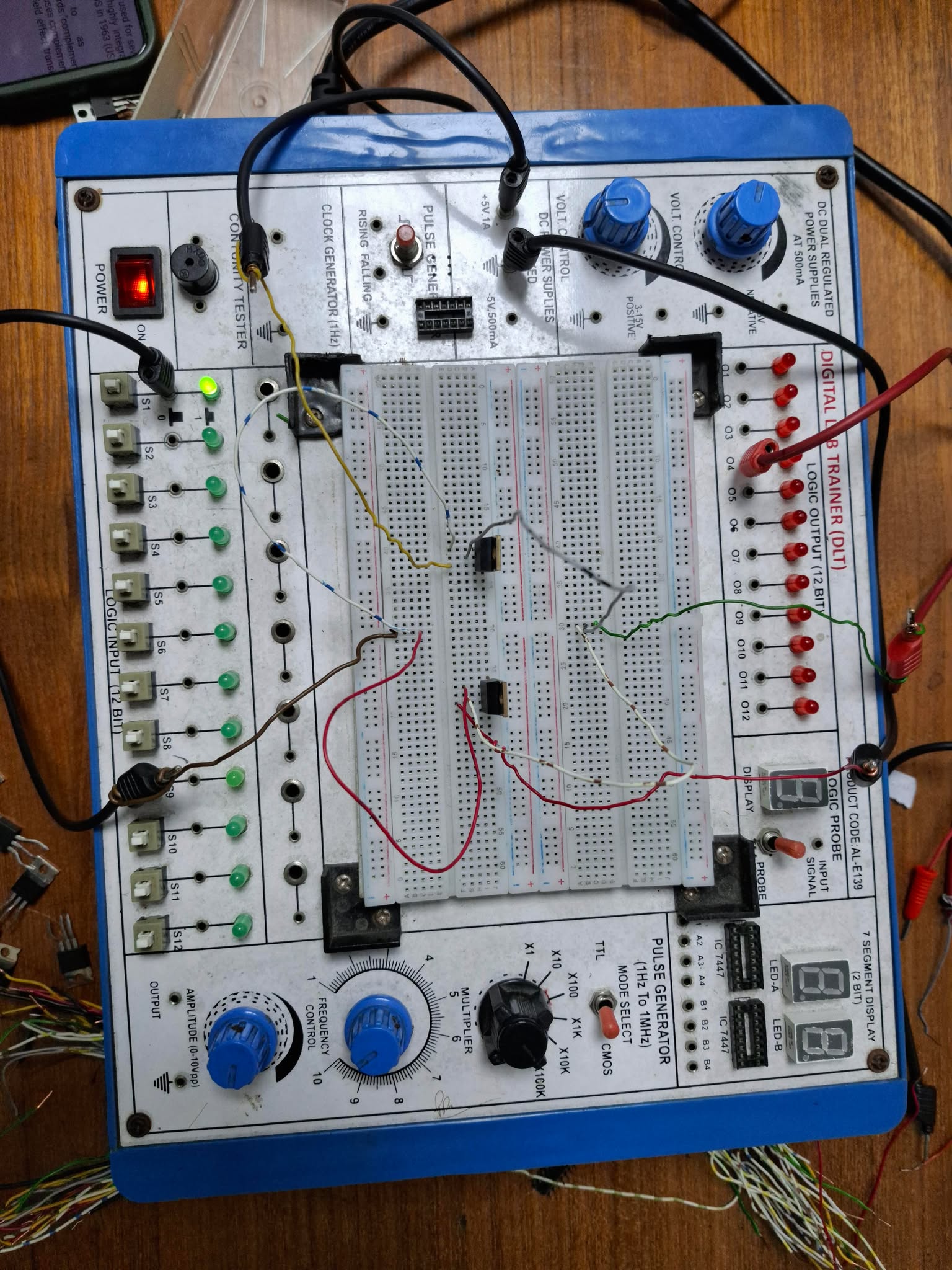
**Results and Discussion:**

In this experiment:  
• CMOS transistors were used to construct an inverter and a half adder.  
• Simulations were performed to verify the theoretical behavior of the circuits.

Tests were then conducted on the constructed CMOS inverter and half adder. The output from the gates aligned well with both the ideal and simulated results. The performance of the implemented circuits was accurate and consistent, confirming the validity of the design through both experimental and simulated analysis.

**Circuit Build Up Lab Measurement:**

**Inverter:**

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**A electronic device with wires and switches

Description automatically generated**

**Sum:**

A electronic device with wires and switches

Description automatically generated

A white electronic device with blue knobs and wires

Description automatically generated

A electronic device with wires and switches

Description automatically generated

A electronic device with wires and switches

Description automatically generated

A electronic device with wires and switches

Description automatically generated

**Carry:**

A electronic device with wires and switches

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A close-up of a circuit board

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A circuit board with wires and switches

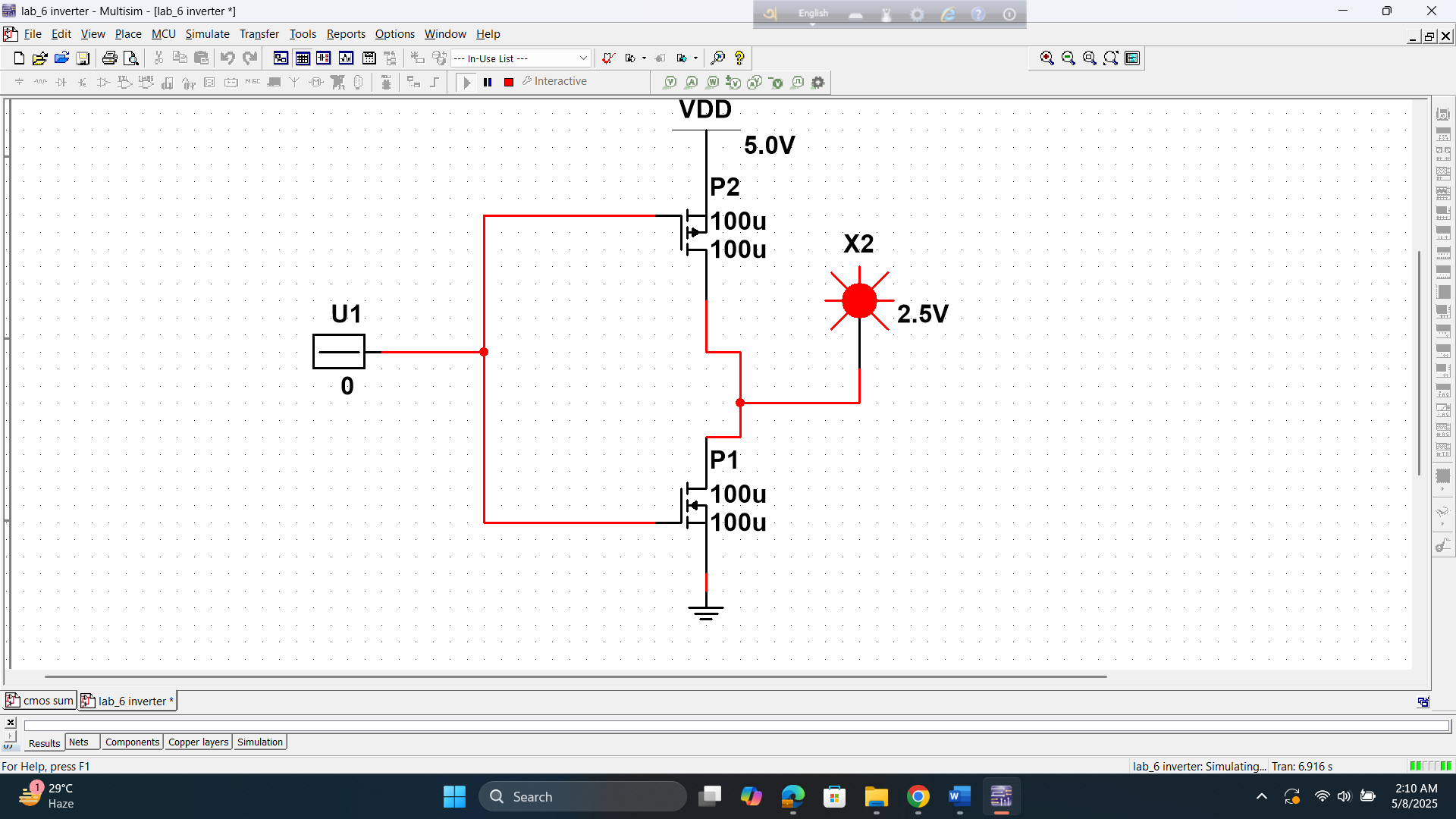
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A blue electronic device with wires and switches

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**Simulation :**

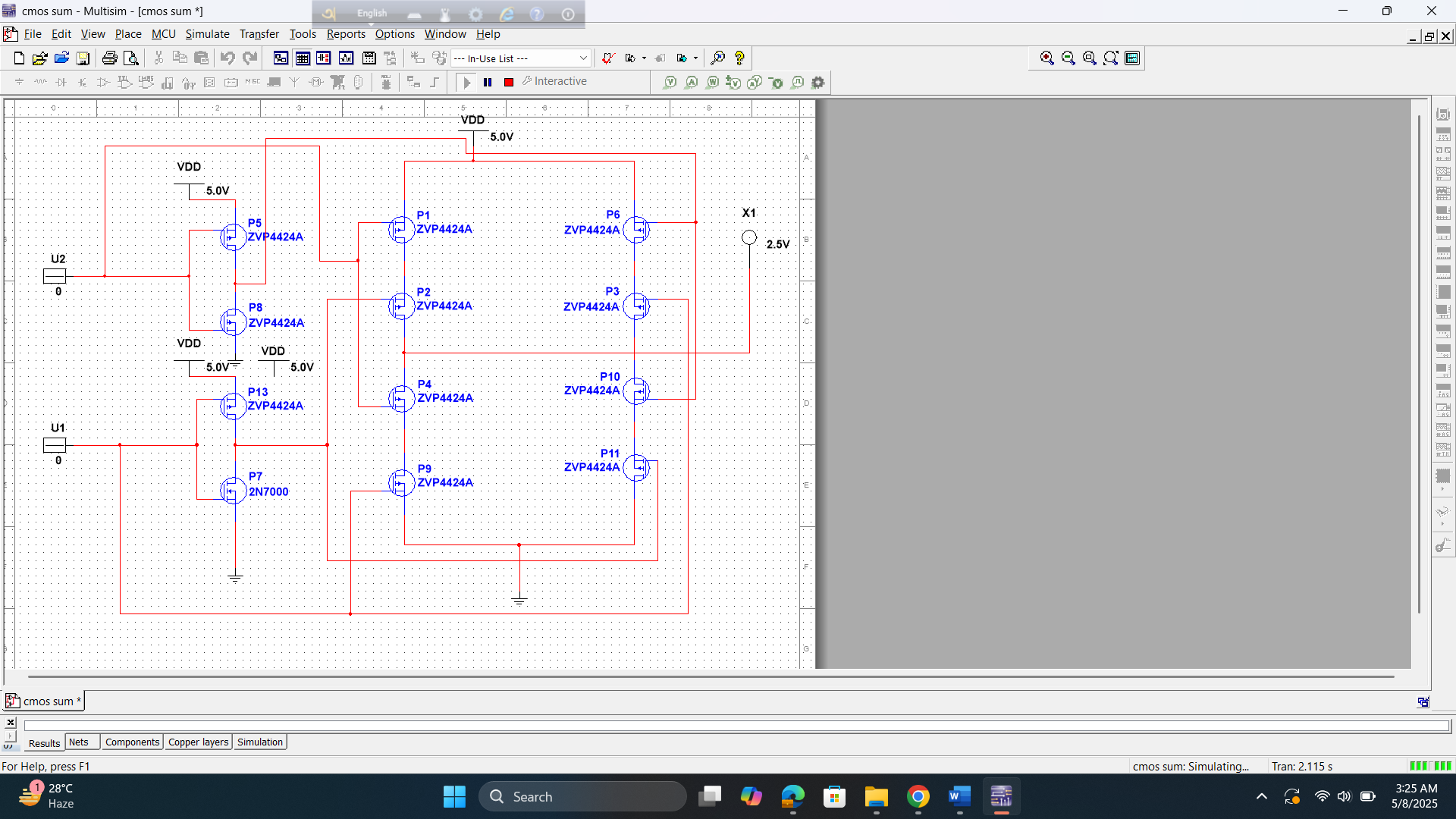
CMOS inverter



A screenshot of a computer

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**Half Adder (Sum) using CMOS**



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A screenshot of a computer

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Description automatically generated

**Reference(s):**

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.
2. Link: <http://www.techpowerup.com/articles/overclocking/voltmods/21>