Name and Number :

COMP 3315 Quiz 2

1. Convert the given Pseudo code to MIPS code and write it to table. (You are only allowed to use instructions in control table.)

```
1-reg1 = 7
2-reg2 = 5
3-reg3 = reg1 OR reg2
4-reg4 = reg2 - reg1
5-store( reg3,0x00000004)#store reg3 to memaddr=0x00000004
7-load( reg5,0x00000004)#load value in memaddr =0x00000004 to reg5
```

1	addi $1,$0,7
2	addi $2,$0,5
3	or $3,$1,$2
4	sub $4,$2,$1
5	sw $3,4($0)
6	lw $5,4($0)

(Use registers as $0,$1 etc. Register 0($0) is always 0)

2. Fill the instruction tables with respect to your written MIPS code below:

1-

31–26	25–21	20–16	15–0
001000	00000	00001	0000000000000111 (Hex 7)
6 bits	5 bits	5 bits	16 bits

2-

31–26	25–21	20–16	15–0
001000	00000	00010	0000000000000101 (Hex 5)
6 bits	5 bits	5 bits	16 bits

3-

31–26	25–21	20–16	15–11	10–6	5–0
000000	00001	00010	00011	00000	001
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

4-

31–26	25–21	20–16	15–11	10–6	5–0
000000	00010	00001	00100	00000	011
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

5-

31–26	25–21	20–16	15–0
101011	00000	00011	0000000000000100 (Hex 4)
6 bits	5 bits	5 bits	16 bits

6-

31–26	25–21	20–16	15–0
100011	00000	00101	0000000000000100 (Hex 4)
6 bits	5 bits	5 bits	16 bits

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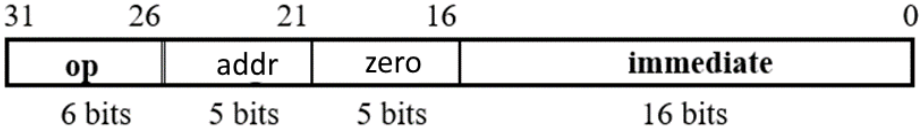
3. For single cycle MIPS processor, you will create an instruction named **swi** (Store Word Immediate) that stores immediate data to a memory location.
The instruction format is as below:

swi addr, immediate



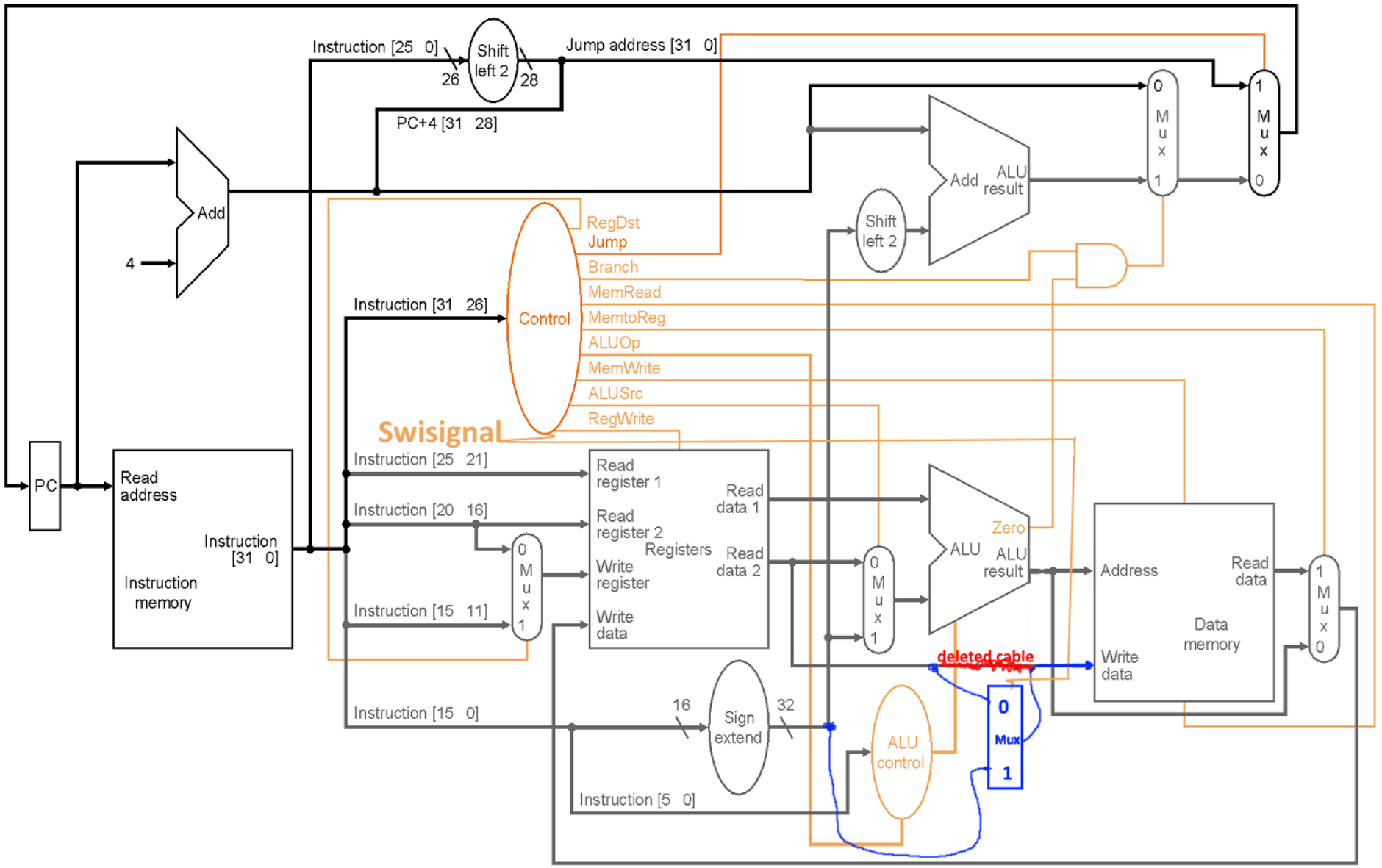
For example: Lets assume Register 1 ($1) has value of 0x10010000. Instruction **swi $1, 0x1000** will store immediate value 0x1000 to memory address 0x10010000 which is in register $1.

Explain whether MIPS Single cycle datapath is enough for this instruction, If it is not add necessary new components to Single cycle MIPS datapath on page 3 and determine the values of newly added control signals and alu control signals in the tables on page 4**.**

MIPS Single cycle datapath is not enough for this instruction. New connection should be implemented to write immediate value to RAM. Without breaking the datapath, both read data 2 part and immediate part must be connected to RAM. A 2 to 1 MUX is enough for this operation. Also new control signal must be added to control this newly added MUX.

It's control signals are similar to sw instruction, only ALUSrc signal is different. ReadregB must be selected in order to send the register's value to ALU. Also Op code must be different than the other Opcodes.

Added MUX's location and control signal values are below.



MIPS Datapath

Instruction opcode	Instruction operation	ALUop	Funct field	Desired ALU action	ALU Control
lw	Load word	00	xxx	add	010
sw	Store word	00	xxx	add	010
swi	Store wordi	00	xxx	add	010
addi	Add Imm.	00	xxx	add	010
R-type	Add	10	010	add	010
R-type	Subtract	10	011	subtract	011
R-type	AND	10	000	and	000
R-type	OR	10	001	or	001

Alu Control Table

	Op Code				Outputs											
INST	Op3	Op2	Op1	Op0	RegDst	ALUSrc	Jump	MemtoReg	RegWrite	MemRead	MemWrite	Branch	ALUOp1	ALIOp0	Swisign	
R-format	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	
lw	0	0	1	1	0	1	0	1	1	1	0	0	0	0	0	
sw	1	0	1	1	x	1	0	x	0	0	1	0	0	0	0	
beq	0	1	0	0	x	0	0	x	0	0	0	1	0	1	0	
addi	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	
swi	1	1	1	1	x	0	0	x	0	0	1	0	0	0	1	

Controller Table