ECE 554: Group2 - Sega Master System

SMS System I/O Protocol and Definition

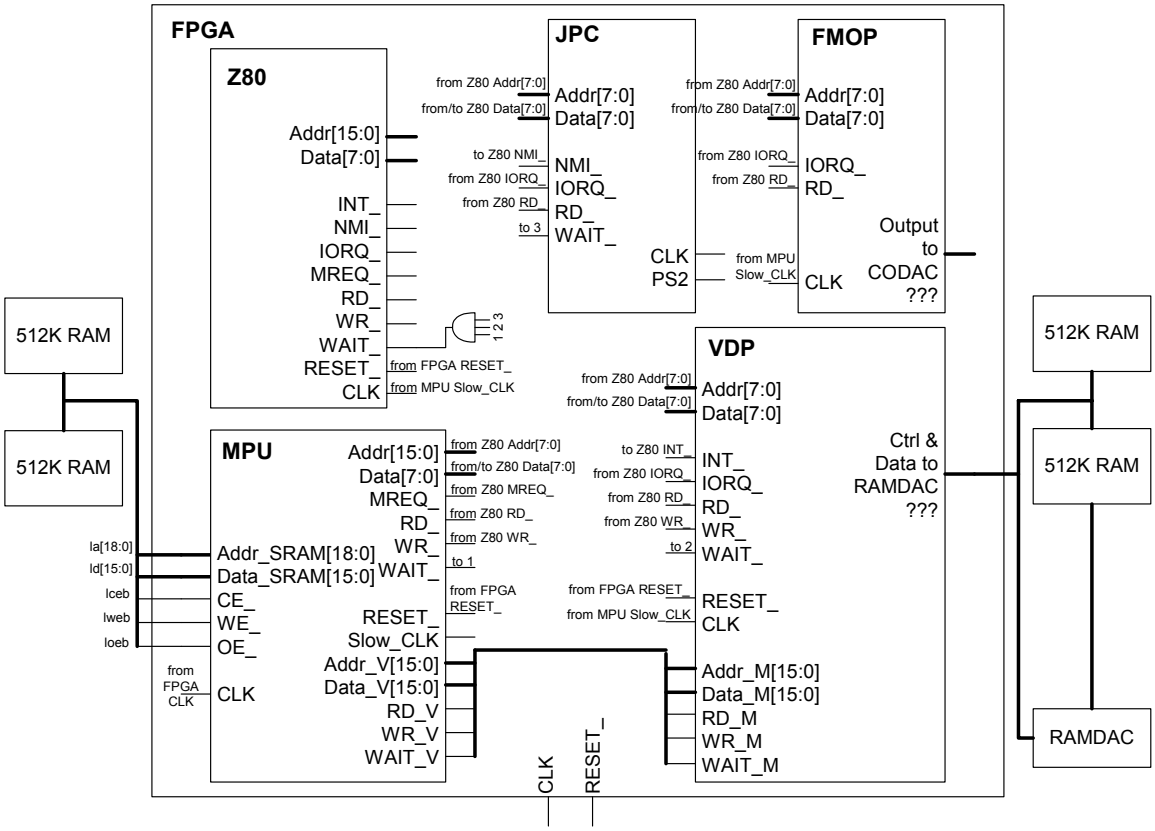

Figure 1. Overview of the SMS system I/O

Z80 Microprocessor

1. **Addr[15:0]** Address Bus (Output, active High). This is a 16-bit address bus that provides the address for memory paging chip and all other I/O device.
2. **Data[7:0]** Data Bus (Input/Output, active High, 3-state). This is an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.
3. **INT_** Interrupt Request (Input, active Low). It takes the IRQ interrupt signal generated by VDP unit. When activated, the PC jumps to address 0x0038.
4. **NMA_** Non-Maskable Interrupt (Input, active Low). It takes the NMA interrupt signal generated by JPC unit. It is activated when pulse key is pressed, and the PC jumps to address 0x0066.
5. **IORQ_** Input/Output Request (Output, active Low). This signal indicates that the lower 8-bit of the address bus holds a valid I/O address for an I/O read or write operation.
6. **MREQ_** Memory Request (Output, active Low). This signal indicates that the address bus holds a valid address for a memory read or a write operation.

7. **RD_** Read (Output, active Low). This signal indicates that the CPU wants to read data from memory or an I/O device.
8. **WR_** Write (Output, active Low). This signal indicates that the data bus holds a valid data to be written into memory or an I/O device.
9. **WAIT_** Wait (Input, active Low). This signal indicates to CPU that the addressed memory or I/O devices are not ready for a data transfer. CPU should stall until this signal is inactivated.
10. **RESET_** Reset (Input, active Low). When activated, CPU should do the follows: reset the interrupt enable flip-flop, and clear the PC and Register I and R. During reset time, Data[7:0] goes to z, all control output signals go to the inactive state.
11. **CLK** Clock (Input, Positive edge trigger). This clock comes from the Slow_CLK signal of MPU, which is twice slower than the system clock.

VDP Video Display Processor

1. **Addr[7:0]** Address Bus (Input, active High). This is an 8-bit address bus that comes from the Z80 CPU indicated the I/O port address.
2. **Data[7:0]** Data Bus (Input/Output, active High, 3-state). This is an 8-bit bidirectional data bus, used for data exchanges with Z80 CPU.
3. **INT_** Interrupt Request (Output, active Low). It generates the IRQ interrupt signal.
4. **IORQ_** Input/Output Request (Input, active Low). This signal indicates that the address bus holds a valid I/O address from Z80 CPU.
5. **RD_** Read (Input, active Low). This signal indicates that the CPU wants to read data from memory or an I/O device.
6. **WR_** Write (Input, active Low). This signal indicates that the data bus holds a valid data to be written into memory or an I/O device.
7. **WAIT_** Wait (Output, active Low). This signal indicates to CPU that VDP is not ready for a data transfer. CPU should stall until this signal is inactivated.
8. **RESET_** Reset (Input, active Low).
9. **CLK** Clock (Input, Positive edge trigger). This clock comes from the Slow_CLK signal of MPU, which is twice slower than the system clock.
10. **Addr_M[15:0]** Address Bus to Memory (Output, active High). This is a 16-bit address bus that provides the address for memory paging chip.
11. **Data_M[15:0]** Data Bus to Memory (Input/Output, active High, 3-state). This is a 16-bit bidirectional data bus, used for data exchanges with memory.
12. **RD_M** Read from Memory (Output, active Low). This signal indicates that the VDP wants to read data from memory.
13. **WR_M** Write to Memory (Output, active Low). This signal indicates that Data_M[15:0] and Addr_M[13:0] hold a valid data and a valid address to be written into memory.
14. **WAIT_M** Wait from Memory (Input, active Low). This signal indicates to VPD that the addressed memory is not ready for a data transfer. VDP should stall until this signal is inactivated.

MPU Memory Paging Unit

1. **Addr[15:0]** Address Bus (Input, active High). This is an 16-bit address bus that comes from the Z80 CPU indicated the address for memory access.
2. **Data[7:0]** Data Bus (Input/Output, active High, 3-state). This is an 8-bit bidirectional data bus, used for data exchanges with Z80 CPU.
3. **MREQ_** Memory Request (Input, active Low). This signal indicates that the address bus holds a valid address for a memory read or a write operation from Z80 CPU.
4. **RD_** Read (Input, active Low). This signal indicates that the CPU wants to read data from memory or an I/O device.
5. **WR_** Write (Input, active Low). This signal indicates that the data bus holds a valid data to be written into memory or an I/O device.
6. **WAIT_** Wait (Output, active Low). This signal indicates to CPU that the addressed memory is not ready for a data transfer. CPU should stall until this signal is inactivated.
7. **RESET_** Reset (Input, active Low).
8. **Slow_CLK** Slow Clock (Input, Positive edge trigger). This clock divides the original clock by half and sends to other units in the system.
9. **Addr_V[15:0]** Address Bus from VDP (Input, active High). This is a 16-bit address bus that provides the address of memory that the VDP needs.
10. **Data_V[15:0]** Data Bus from VDP (Input/Output, active High, 3-state). This is a 16-bit bidirectional data bus, used for data exchanges with the VDP.
11. **RD_V** Read by VDP (Input, active Low). This signal indicates that the VDP wants to read data from memory.
12. **WR_V** Write from VDP (Input, active Low). This signal indicates that Data_V[15:0] and Addr_V[13:0] hold a valid data and a valid address to be written into memory.
13. **WAIT_V** Wait (Output, active Low). This signal indicates to VDP that the addressed memory is not ready for a data transfer. VDP should stall until this signal is inactivated.
14. **CLK** Clock (Input, Positive edge trigger). This clock is the original clock signal coming from the external clock generator.
15. **Addr_SRAM[18:0]** Address Bus to SRAM (Output, active High).
16. **Data_SRAM[15:0]** Data Bus to SRAM (Input/Output, active High, 3-state).
17. **CE_** Chip Enable (Output, active Low). This signal controls the left bank of the SRAM.
18. **WE_** Write Enable (Output, active Low). This signal controls the left bank of the SRAM.
19. **OE_** Output Enable (Output, active Low). This signal controls the left bank of the SRAM.

JPC Joypad Controller

1. **Addr[7:0]** Address Bus (Input, active High). This is an 8-bit address bus that comes from the Z80 CPU indicated the I/O port address.
2. **Data[7:0]** Data Bus (Input/Output, active High, 3-state). This is an 8-bit bidirectional data bus, used for data exchanges with Z80 CPU.
3. **NMI_** Non-Maskable Interrupt (Output, active Low). It generates the NMI interrupt signal when the pause button is pushed.
4. **IORQ_** Input/Output Request (Input, active Low). This signal indicates that the address bus holds a valid I/O address from Z80 CPU.
5. **RD_** Read (Input, active Low). This signal indicates that the CPU wants to read data from memory or an I/O device.
6. **CLK** Clock (Input, Positive edge trigger). This clock comes from the PS/2 Keyboard, which is not synchronized with the system clock.
7. **PS2** PS/2 Signal (Input, active Low). This is a sequential signal coming from the PS/2 keyboard.

FMOP FM Operator

1. **Addr[7:0]** Address Bus (Input, active High). This is an 8-bit address bus that comes from the Z80 CPU indicated the I/O port address.
2. **Data[7:0]** Data Bus (Input/Output, active High, 3-state). This is an 8-bit bidirectional data bus, used for data exchanges with Z80 CPU.
3. **IORQ_** Input/Output Request (Input, active Low). This signal indicates that the address bus holds a valid I/O address from Z80 CPU.
4. **RD_** Read (Input, active Low). This signal indicates that the CPU wants to read data from memory or an I/O device.
5. **CLK** Clock (Input, Positive edge trigger). This clock comes from the Slow_CLK signal of MPU, which is twice slower than the system clock.

Timing Information

1. **Use of WAIT_ signal** - Since there is always only one device using the I/O bus, when any one (and the only one) of them asserts WAIT_, the CPU should stall until the device cancels the WAIT_ signal.
2. **Read and Input timing** - As soon as a device gets an I/O request from CPU, decodes it, and figures out this request is for him, he should send out the data immediately. If he cannot, he should activate (low) the WAIT_ signal, and latter on sends out the data and deactivates the wait signal at the same time. Until the CPU cancels this request, the device should release the bus (makes it z state).
3. **Write and Output timing -** When the CPU wants to write or outputs some data to some device, the data and the write request should be sent out at the same time. The device should be able to have this data recorded done in one cycle. No handshaking for these types of I/O.

Memory Paging Unit

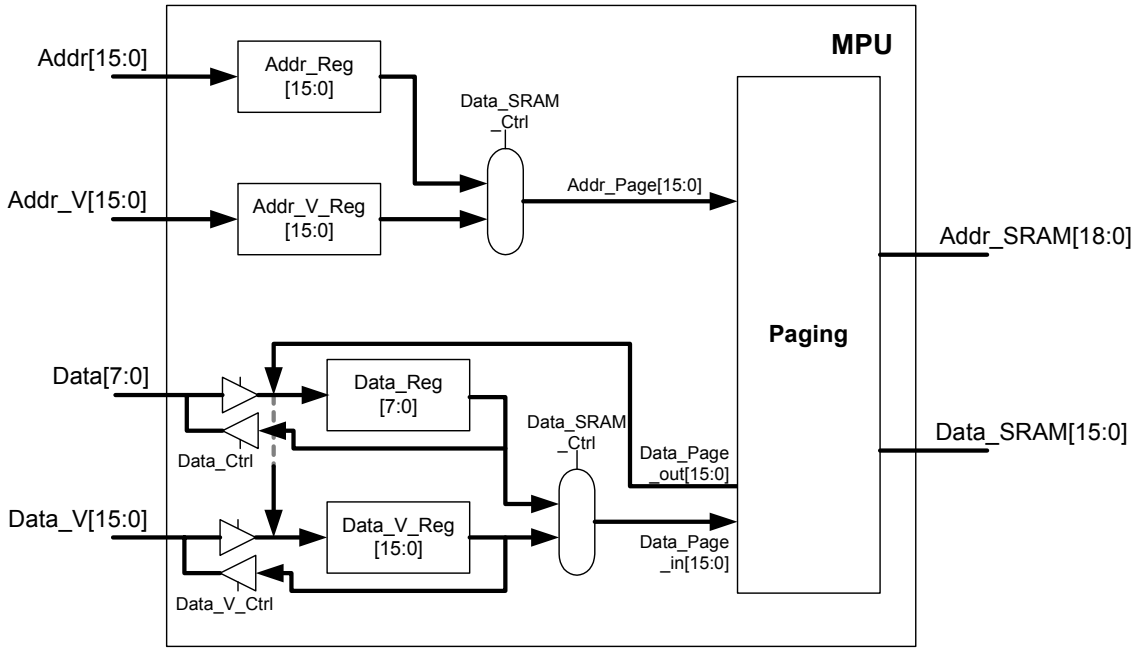

Figure 2. Block diagram of the MPU

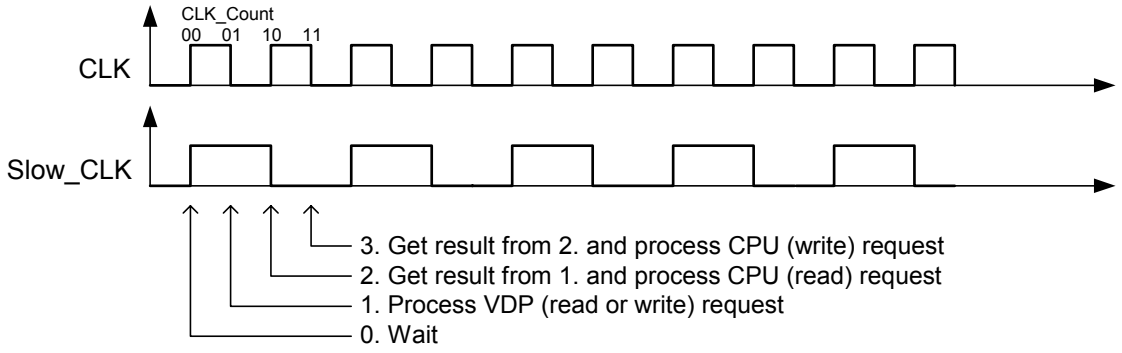

Figure 3. Timing of the MPU

Figure 2 shows the block diagram of the memory-paging unit. Since both the CPU and VDP use the right bank of memory as their memory, the MPU serves both requests from the CPU and the VDP, runs at double the clock speed as the system clock, and arbitrates the traffic flows.

Figure 3. shows the timing information of the MPU. At 00, which is the positive edge of the system clock, it waits for the CPU and the VDP sending out request for half clock cycle. At 01, the MPU scans in the request from the VDP and performs read or write to the memory. At 10, it gets the result from memory if the previous action is read, and process the CPU read request. Similarly, the MPU gets the reading result and process the

CPU write request if there is one. The CPU write request is separated from the VDP requests to avoid both the memory and the MPU driving the bus at the same time. The CPU doesn't care the timing how the MPU write to memory, but only cares when the read is available. Therefore, this memory arbitration scheme can have the read data available to both CPU and VDP at the next positive clock edge after they send out the request.