

BLM1033 - Circuit Theory and Electronics

The Instructors:

Doç. Dr. Hamza Osman İlhan
hoilhan@yildiz.edu.tr

Prof. Dr. Gökhan Bilgin
gbilgin@yildiz.edu.tr

Lab Assistants:

Arş. Gör. Burak Ahmet Özden

Arş. Gör. Emre Parlak

Arş. Gör. Elif Aşıcı

Arş. Gör. Ömer Mutlu Türk Kaya

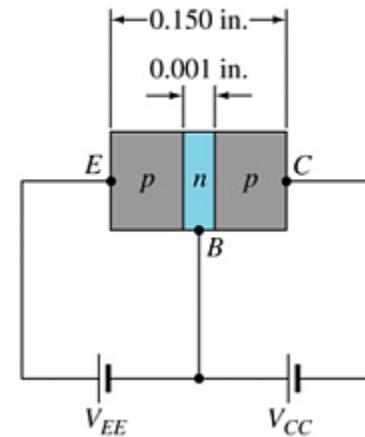
Arş. Gör. Yunus Karatepe

Transistor Construction

There are two types of transistors:

- *pnp*
- *npn*

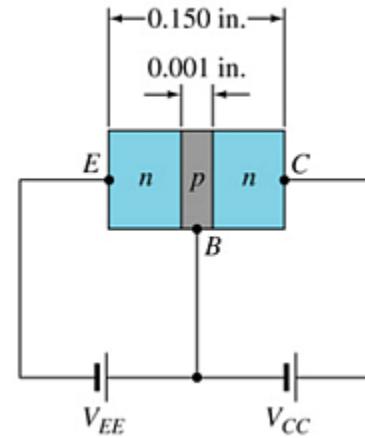
pnp



The terminals are labeled:

- **E - Emitter**
- **B - Base**
- **C - Collector**

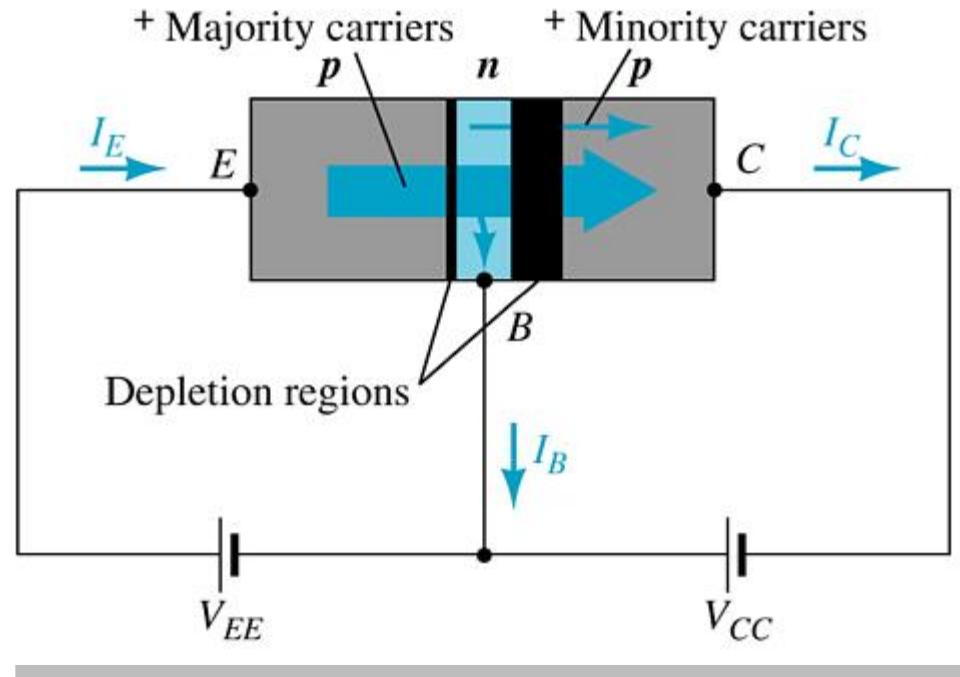
npn



Transistor Operation

With the external sources, V_{EE} and V_{CC} , connected as shown:

- The emitter-base junction is forward biased
- The base-collector junction is reverse biased



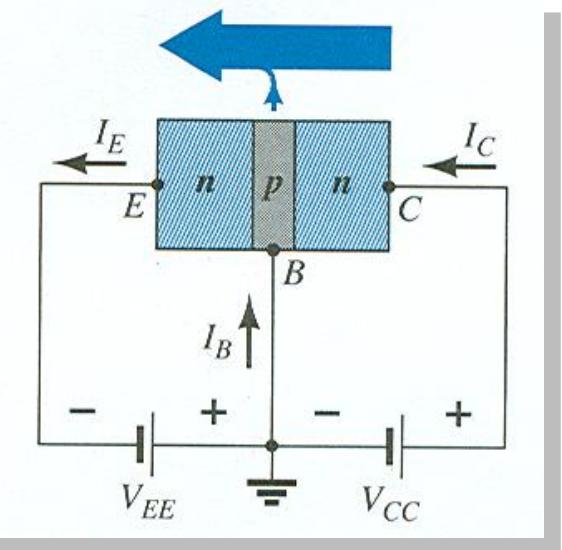
Currents in a Transistor

Emitter current is the sum of the collector and base currents:

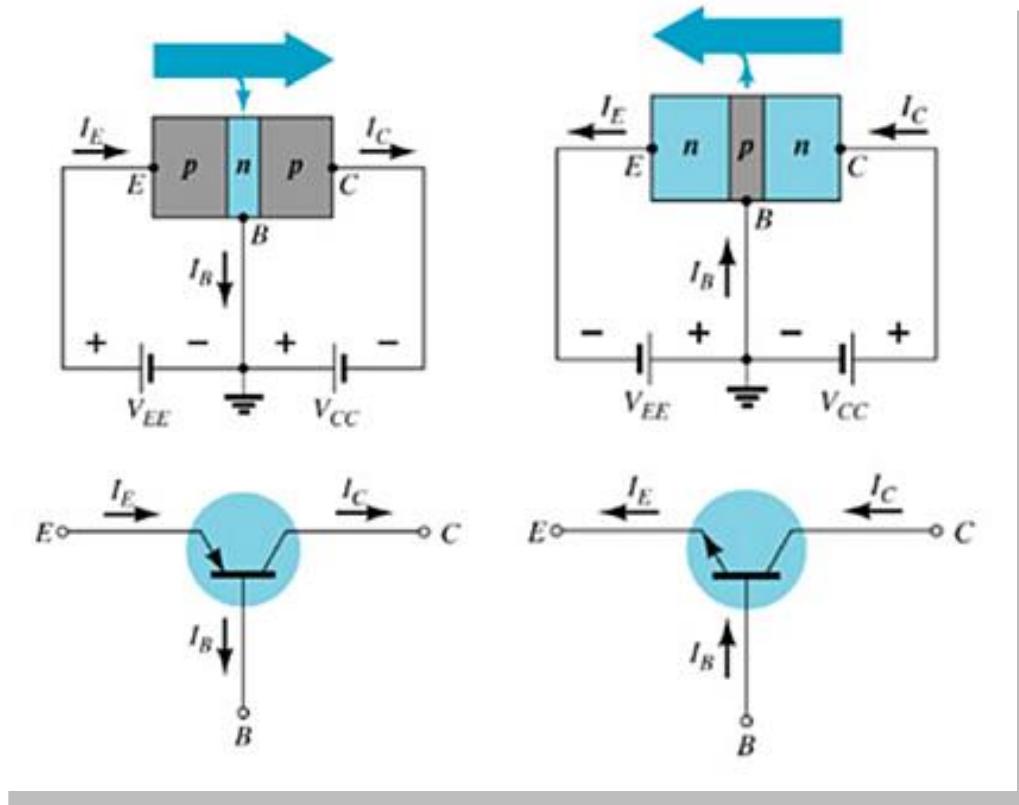
$$I_E = I_C + I_B$$

The collector current is comprised of two currents:

$$I_C = I_{C \text{ majority}} + I_{C \text{ minority}}$$



Common-Base Configuration

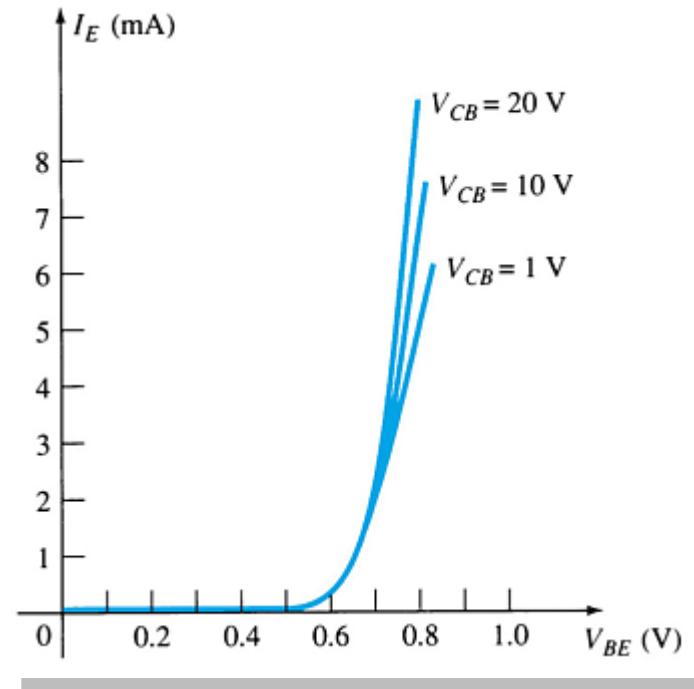


The base is common to both input (emitter–base) and output (collector–base) of the transistor.

Common-Base Amplifier

Input Characteristics

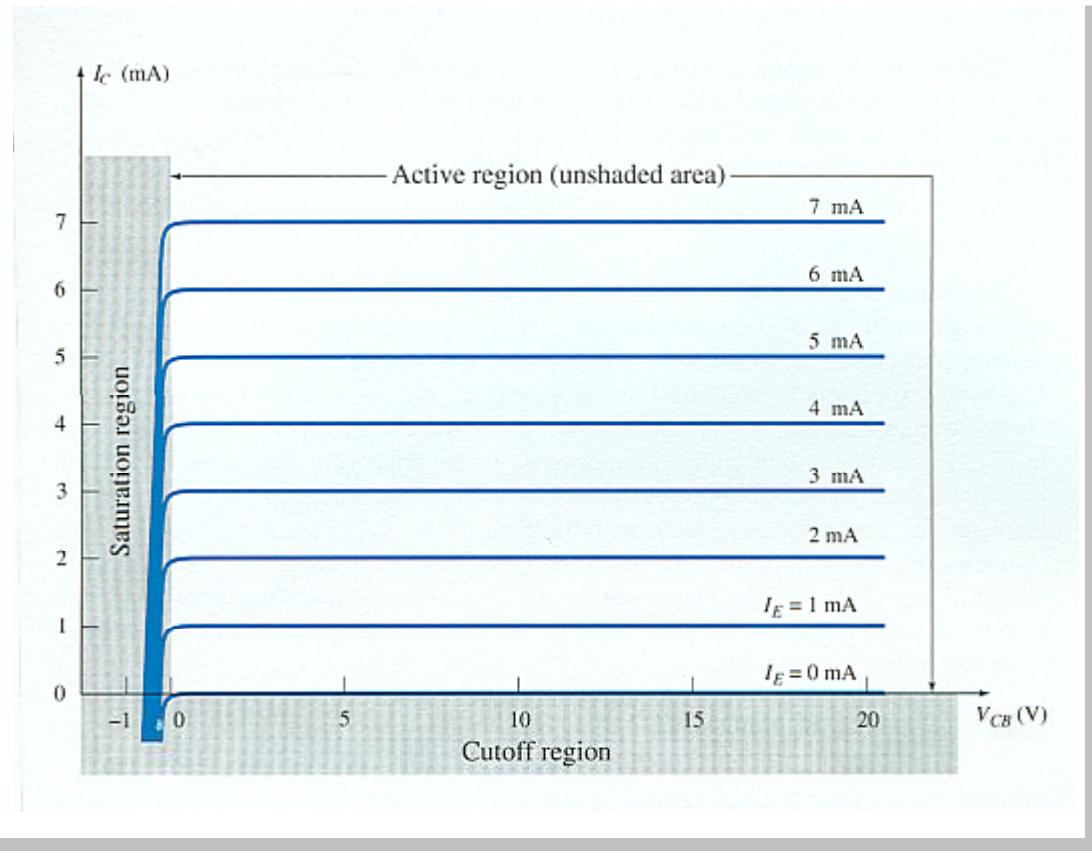
This curve shows the relationship between of input current (I_E) to input voltage (V_{BE}) for three output voltage (V_{CB}) levels.



Common-Base Amplifier

Output Characteristics

This graph demonstrates the output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E).



Operating Regions

- **Active** – Operating range of the amplifier.
- **Cutoff** – The amplifier is basically off. There is voltage, but little current.
- **Saturation** – The amplifier is full on. There is current, but little voltage.

Approximations

Emitter and collector currents:

$$I_C \cong I_E$$

Base-emitter voltage:

$$V_{BE} = 0.7 \text{ V (for Silicon)}$$

Alpha (α)

Alpha (α) is the ratio of I_C to I_E :

$$\alpha_{\text{dc}} = \frac{I_C}{I_E}$$

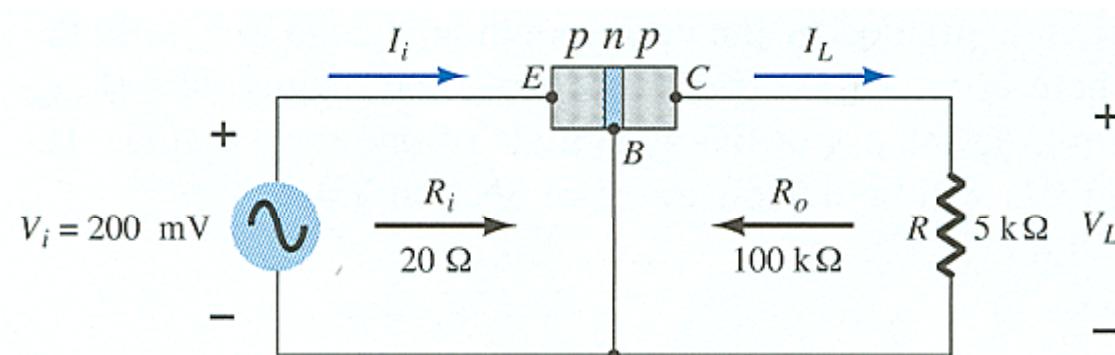
Ideally: $\alpha = 1$

In reality: α is between 0.9 and 0.998

Alpha (α) in the AC mode:

$$\alpha_{\text{ac}} = \frac{\Delta I_C}{\Delta I_E}$$

Transistor Amplification



Currents and Voltages:

$$I_E = I_i = \frac{V_i}{R_i} = \frac{200 \text{ mV}}{20 \Omega} = 10 \text{ mA}$$

$$I_C \approx I_E$$

$$I_L \approx I_i = 10 \text{ mA}$$

$$V_L = I_L R = (10 \text{ mA})(5 \text{ k}\Omega) = 50 \text{ V}$$

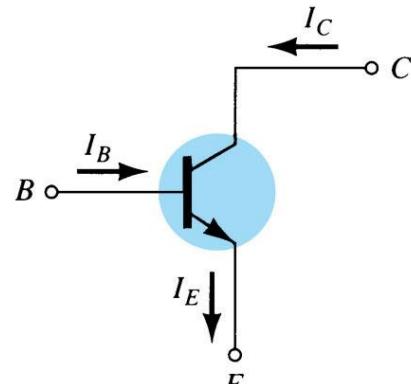
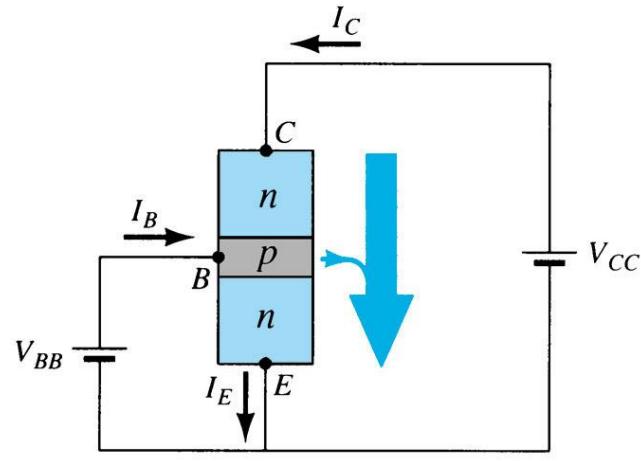
Voltage Gain:

$$A_V = \frac{V_L}{V_i} = \frac{50 \text{ V}}{200 \text{ mV}} = 250$$

Common-Emitter Configuration

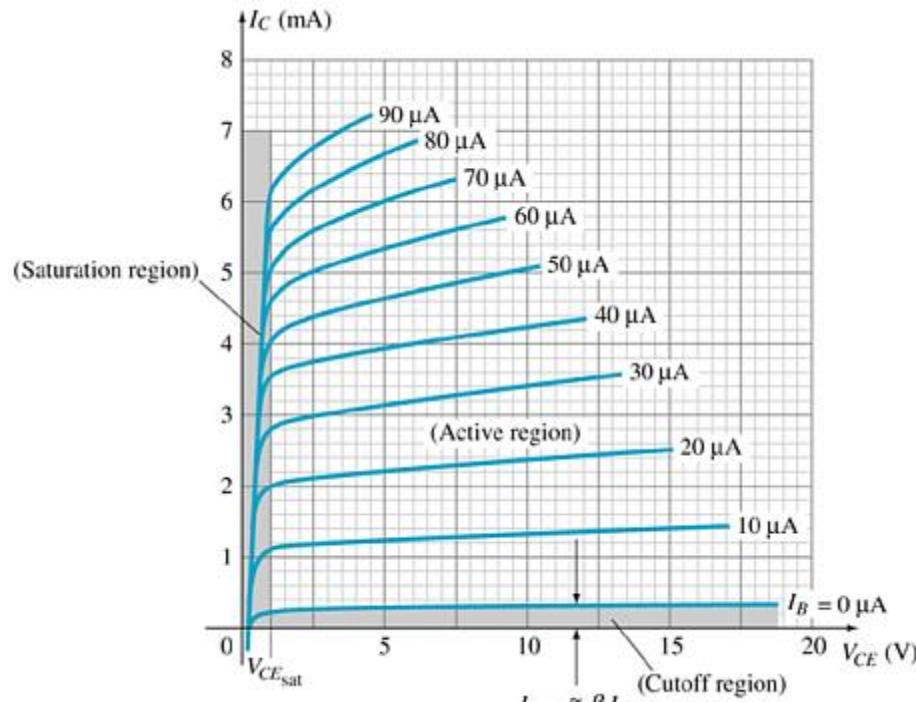
The emitter is common to both input (base-emitter) and output (collector-emitter).

The input is on the base and the output is on the collector.

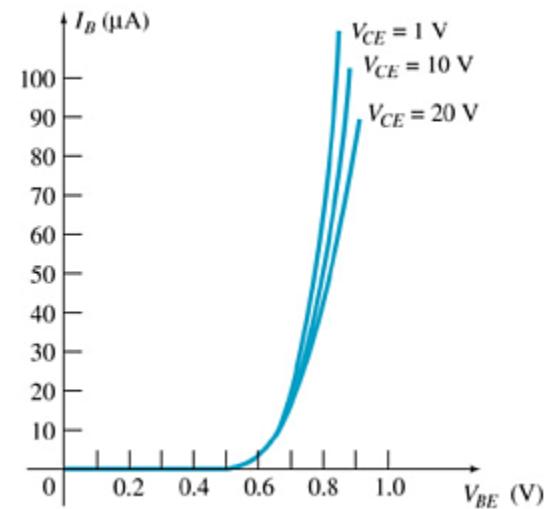


(a)

Common-Emitter Characteristics



Collector Characteristics



Base Characteristics

Common-Emitter Amplifier Currents

Ideal Currents

$$I_E = I_C + I_B$$

$$I_C = \alpha I_E$$

Actual Currents

$$I_C = \alpha I_E + I_{CBO} \quad \text{where } I_{CBO} = \text{minority collector current}$$

I_{CBO} is usually so small that it can be ignored, except in high power transistors and in high temperature environments.

When $I_B = 0 \mu\text{A}$ the transistor is in cutoff, but there is some minority current flowing called I_{CEO} .

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha} \Big|_{I_B=0 \mu\text{A}}$$

Beta (β)

β represents the amplification factor of a transistor. (β is sometimes referred to as h_{fe} , a term used in transistor modeling calculations)

In DC mode:

$$\beta_{dc} = \frac{I_C}{I_B}$$

In AC mode:

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Big|_{V_{CE}=\text{constant}}$$

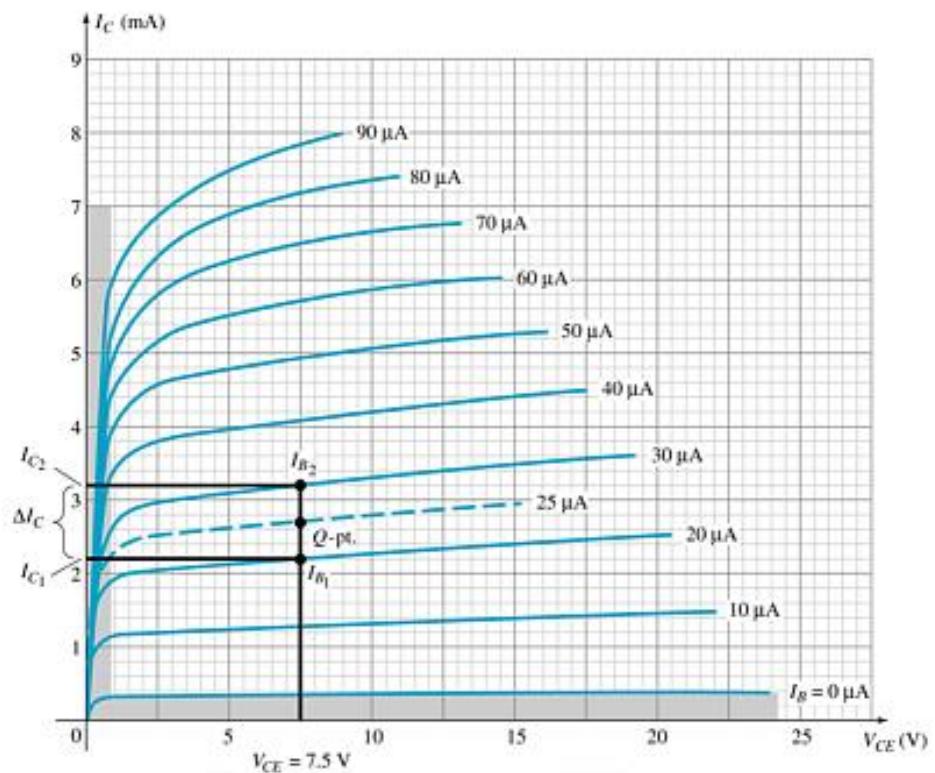
Beta (β)

Determining β from a Graph

$$\beta_{AC} = \frac{(3.2 \text{ mA} - 2.2 \text{ mA})}{(30 \mu\text{A} - 20 \mu\text{A})}$$

$$= \frac{1 \text{ mA}}{10 \mu\text{A}} \Big| V_{CE} = 7.5 \\ = 100$$

$$\beta_{DC} = \frac{2.7 \text{ mA}}{25 \mu\text{A}} \Big| V_{CE} = 7.5 \\ = 108$$



Beta (β)

Relationship between amplification factors β and α

$$\alpha = \frac{\beta}{\beta + 1} \quad \beta = \frac{\alpha}{\alpha - 1}$$

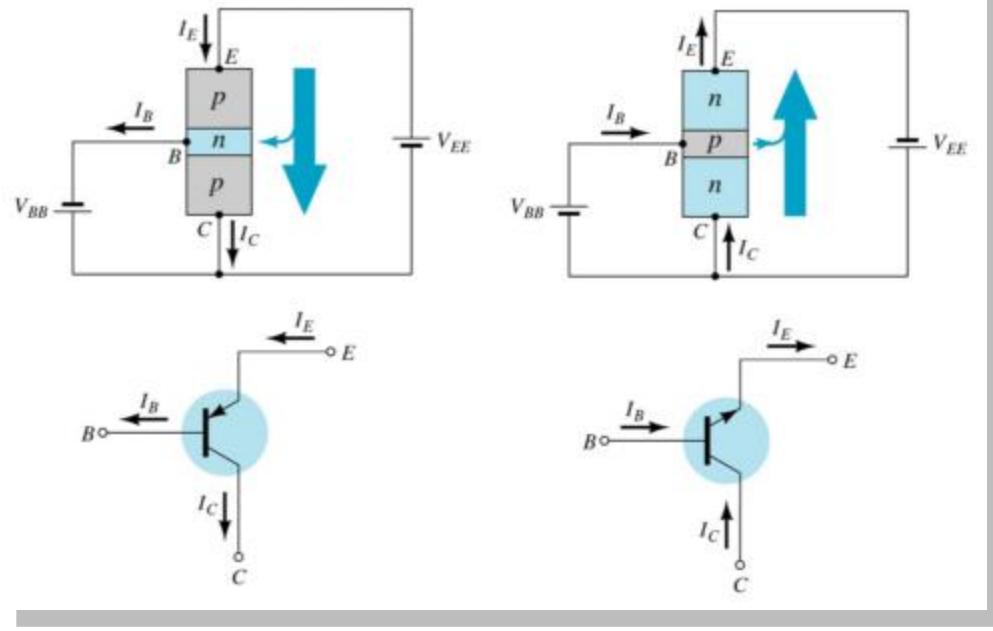
Relationship Between Currents

$$I_C = \beta I_B$$

$$I_E = (\beta + 1) I_B$$

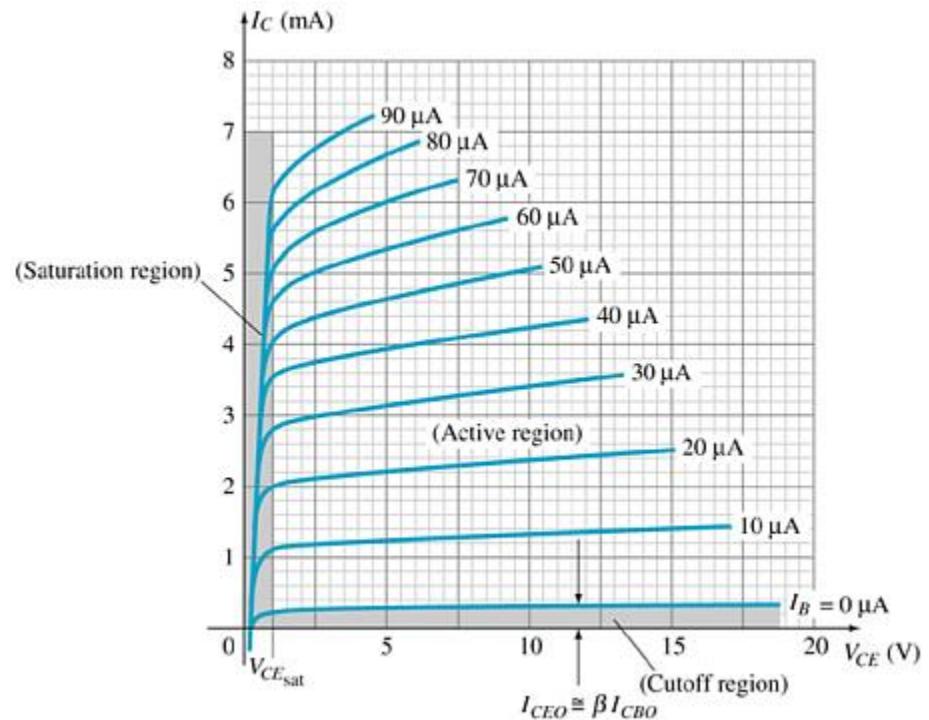
Common–Collector Configuration

The input is on the base and the output is on the emitter.



Common–Collector Configuration

The characteristics are similar to those of the common-emitter configuration, except the vertical axis is I_E .

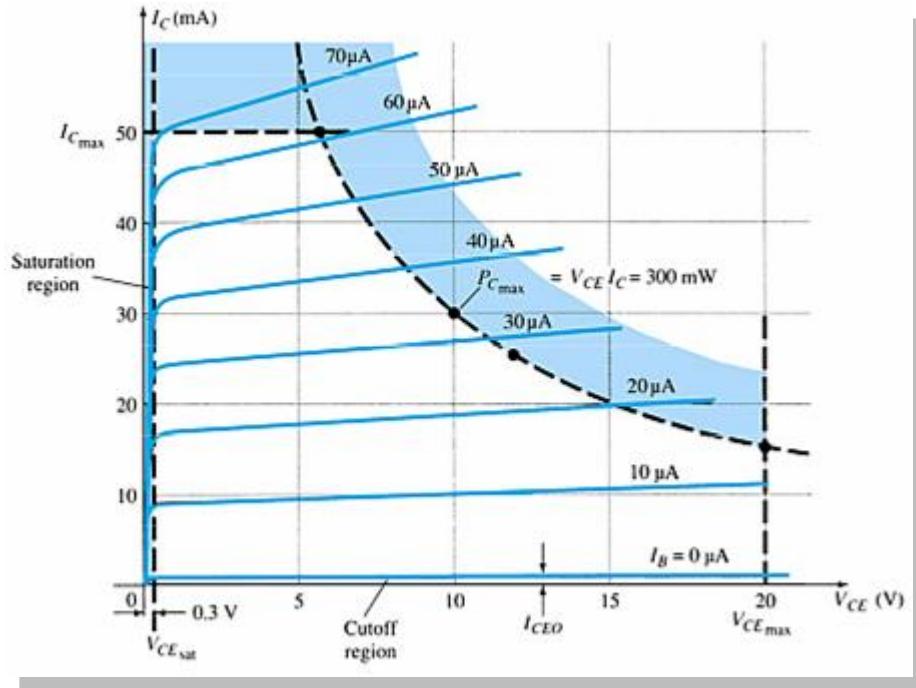


Operating Limits for Each Configuration

V_{CE} is at maximum and I_C is at minimum ($I_{Cmax} = I_{CEO}$) in the cutoff region.

I_C is at maximum and V_{CE} is at minimum ($V_{CE\ max} = V_{CESat} = V_{CEO}$) in the saturation region.

The transistor operates in the active region between saturation and cutoff.



Power Dissipation

Common-base:

$$P_{Cmax} = V_{CB} I_C$$

Common-emitter:

$$P_{Cmax} = V_{CE} I_C$$

Common-collector:

$$P_{Cmax} = V_{CE} I_E$$

Transistor Specification Sheet

MAXIMUM RATINGS

| Rating | Symbol | 2N4123 | Unit |
|--|---------------|-------------|------------|
| Collector-Emitter Voltage | V_{CEO} | 30 | Vdc |
| Collector-Base Voltage | V_{CEO} | 40 | Vdc |
| Emitter-Base Voltage | V_{EBO} | 5.0 | Vdc |
| Collector Current - Continuous | I_C | 200 | mAdc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 625 5.0 | mW mW/C |
| Operating and Storage Junction Temperature Range | T_J, T_{SJ} | -55 to +150 | °C |

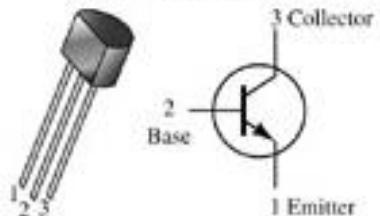
THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------|------|------|
| Thermal Resistance, Junction to Case | R_{jdc} | 83.3 | °C/W |
| Thermal Resistance, Junction to Ambient | R_{jda} | 200 | °C/W |

2N4123

CASE 29-04, STYLE 1

TO-92 (TO-226AA)



GENERAL PURPOSE
TRANSISTOR
NPN SILICON

Transistor Specification Sheet

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|-----------------------------|-----------|----------|------|
| OFF CHARACTERISTICS | | | | |
| Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0 \text{ mAdc}, I_E = 0$) | $V_{(\text{BR})\text{CEO}}$ | 30 | | Vdc |
| Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{Adc}, I_E = 0$) | $V_{(\text{BR})\text{CBO}}$ | 40 | | Vdc |
| Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{Adc}, I_C = 0$) | $V_{(\text{BR})\text{EBO}}$ | 5.0 | - | Vdc |
| Collector Cutoff Current ($V_{CB} = 20 \text{ Vdc}, I_E = 0$) | I_{CBO} | - | 50 | nAdc |
| Emitter Cutoff Current ($V_{BE} = 3.0 \text{ Vdc}, I_C = 0$) | I_{EBO} | - | 50 | nAdc |
| ON CHARACTERISTICS | | | | |
| DC Current Gain(1) ($I_C = 2.0 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 50 \text{ mAdc}, V_{CE} = 1.0 \text{ Vdc}$) | h_{FE} | 50 25 | 150 | - |
| Collector-Emitter Saturation Voltage(1) ($I_C = 50 \text{ mAdc}, I_B = 5.0 \text{ mAdc}$) | $V_{CE(\text{sat})}$ | - | 0.3 | Vdc |
| Base-Emitter Saturation Voltage(1) ($I_C = 50 \text{ mAdc}, I_B = 5.0 \text{ mAdc}$) | $V_{BE(\text{sat})}$ | - | 0.95 | Vdc |
| SMALL-SIGNAL CHARACTERISTICS | | | | |
| Current-Gain – Bandwidth Product ($I_C = 10 \text{ mAdc}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$) | f_T | 250 | | MHz |
| Output Capacitance ($V_{CB} = 5.0 \text{ Vdc}, I_E = 0, f = 100 \text{ MHz}$) | C_{obs} | - | 4.0 | pF |
| Input Capacitance ($V_{BE} = 0.5 \text{ Vdc}, I_C = 0, f = 100 \text{ kHz}$) | C_{in} | - | 8.0 | pF |
| Collector-Base Capacitance ($I_E = 0, V_{CB} = 5.0 \text{ V}, f = 100 \text{ kHz}$) | C_{cb} | - | 4.0 | pF |
| Small-Signal Current Gain ($I_C = 2.0 \text{ mAdc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ kHz}$) | h_{fi} | 50 | 200 | - |
| Current Gain – High Frequency ($I_C = 10 \text{ mAdc}, V_{CE} = 20 \text{ Vdc}, f = 100 \text{ MHz}$) ($I_C = 2.0 \text{ mAadc}, V_{CE} = 10 \text{ V}, f = 1.0 \text{ kHz}$) | h_{ie} | 2.5 50 | - 200 | - |
| Noise Figure ($I_C = 100 \mu\text{Adc}, V_{CE} = 5.0 \text{ Vdc}, R_S = 1.0 \text{ k ohm}, f = 1.0 \text{ kHz}$) | NF | - | 6.0 | dB |

(1) Pulse Test: Pulse Width = 300 μs . Duty Cycle = 2.0%

Transistor Testing

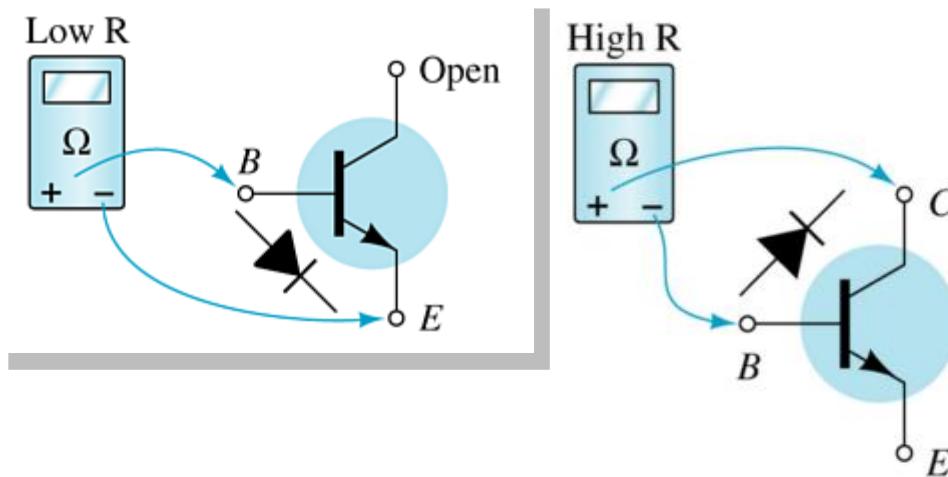
- **Curve Tracer**

Provides a graph of the characteristic curves.

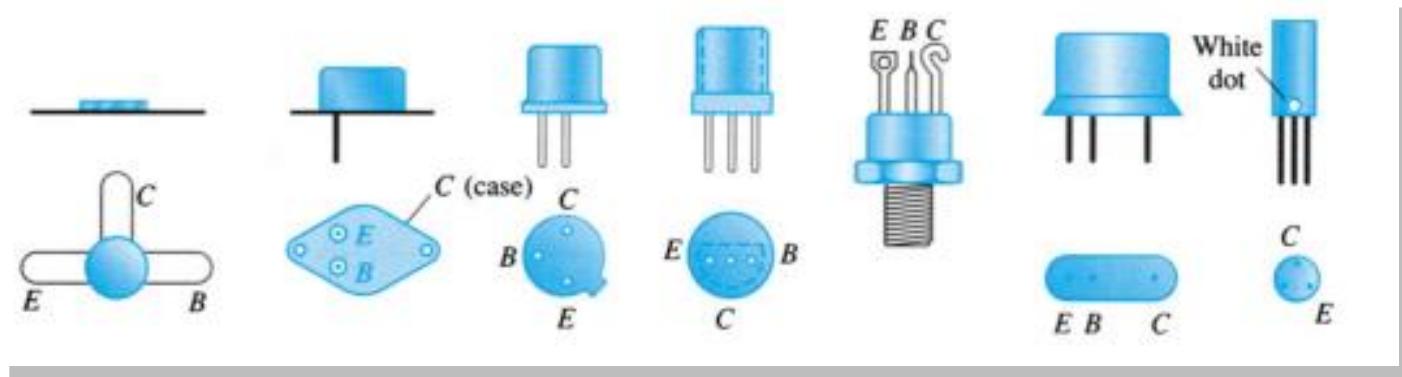
- **DMM**

Some DMMs measure β_{DC} or h_{FE} .

- **Ohmmeter**



Transistor Terminal Identification

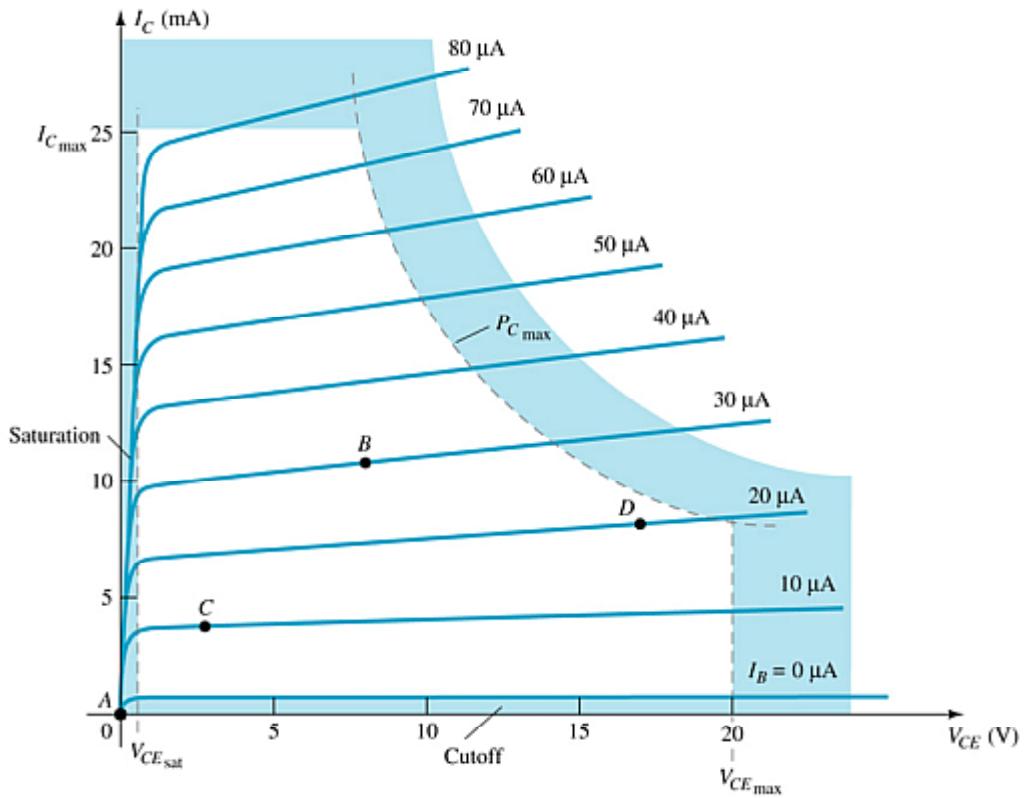


Biassing

Biassing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

Operating Point

The DC input establishes an operating or *quiescent point* called the ***Q-point***.



The Three States of Operation

- **Active or Linear Region Operation**

Base–Emitter junction is forward biased
Base–Collector junction is reverse biased

- **Cutoff Region Operation**

Base–Emitter junction is reverse biased

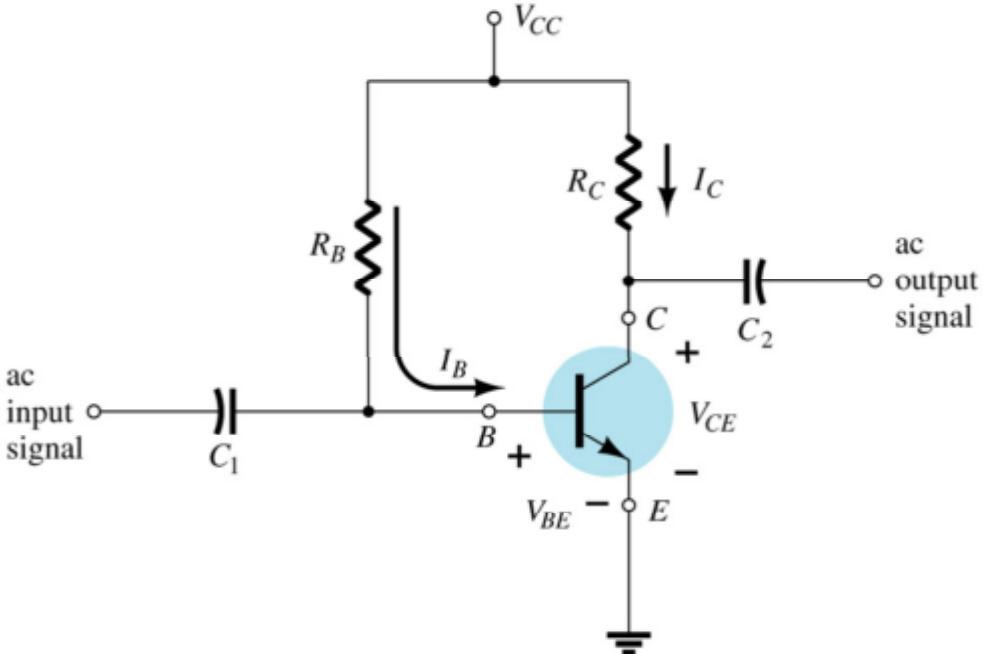
- **Saturation Region Operation**

Base–Emitter junction is forward biased
Base–Collector junction is forward biased

DC Biasing Circuits

- **Fixed-bias circuit**
- **Emitter-stabilized bias circuit**
- **Collector-emitter loop**
- **Voltage divider bias circuit**
- **DC bias with voltage feedback**

Fixed Bias



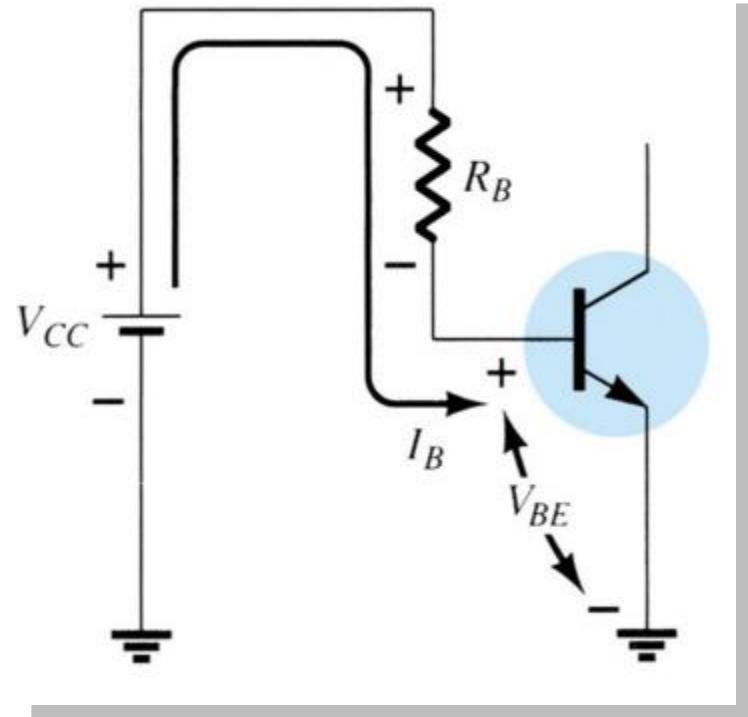
The Base-Emitter Loop

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



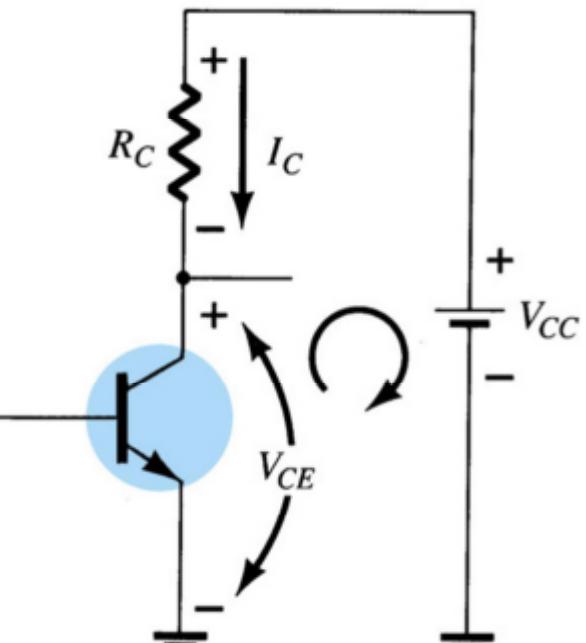
Collector-Emitter Loop

Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Saturation

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

$$I_{C\text{sat}} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0 \text{ V}$$

Load Line Analysis

The end points of the load line are:

$I_{C\text{sat}}$

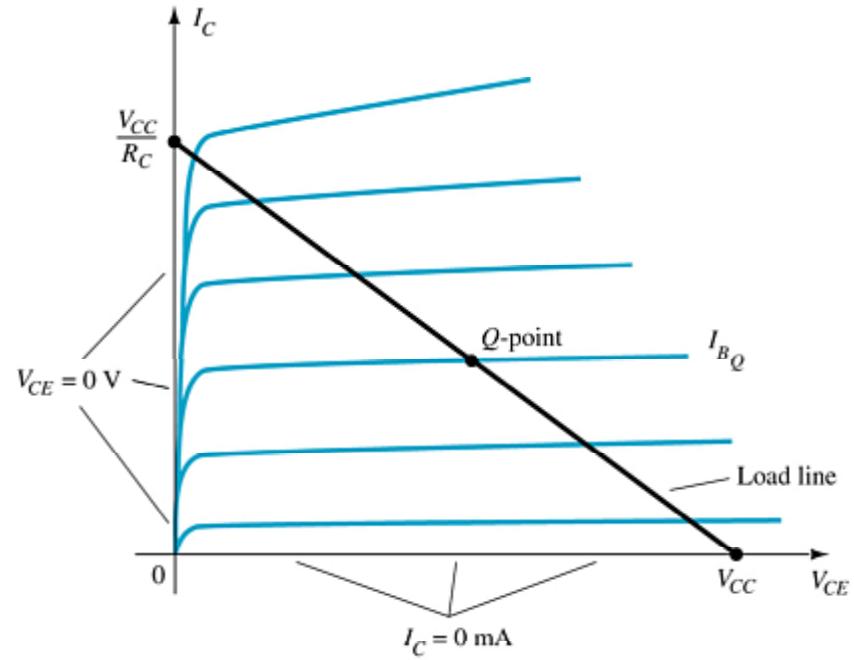
$$I_C = V_{CC} / R_C$$

$$V_{CE} = 0 \text{ V}$$

$V_{CE\text{cutoff}}$

$$V_{CE} = V_{CC}$$

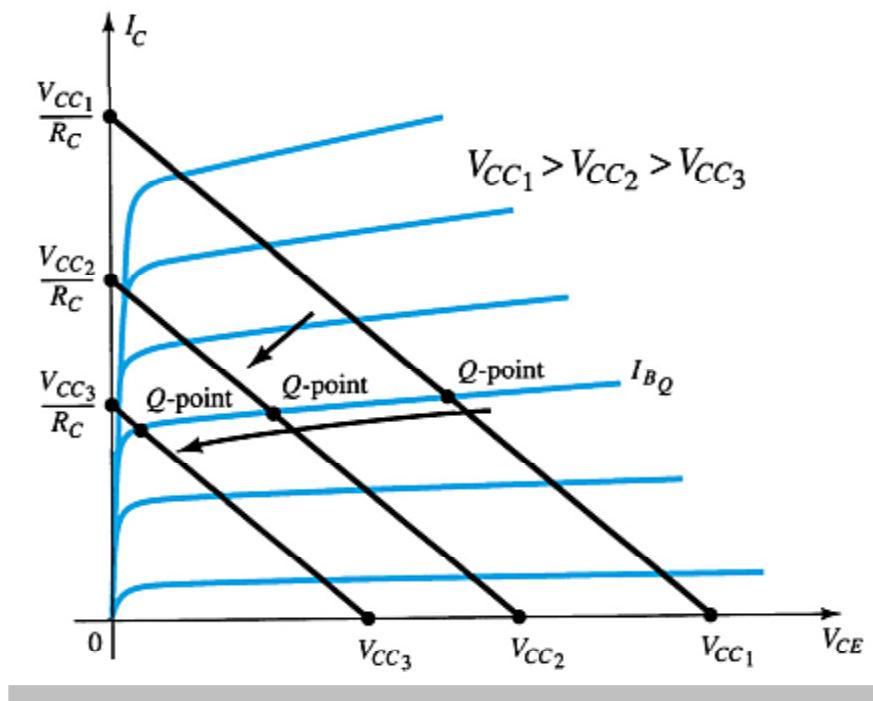
$$I_C = 0 \text{ mA}$$



The Q -point is the operating point:

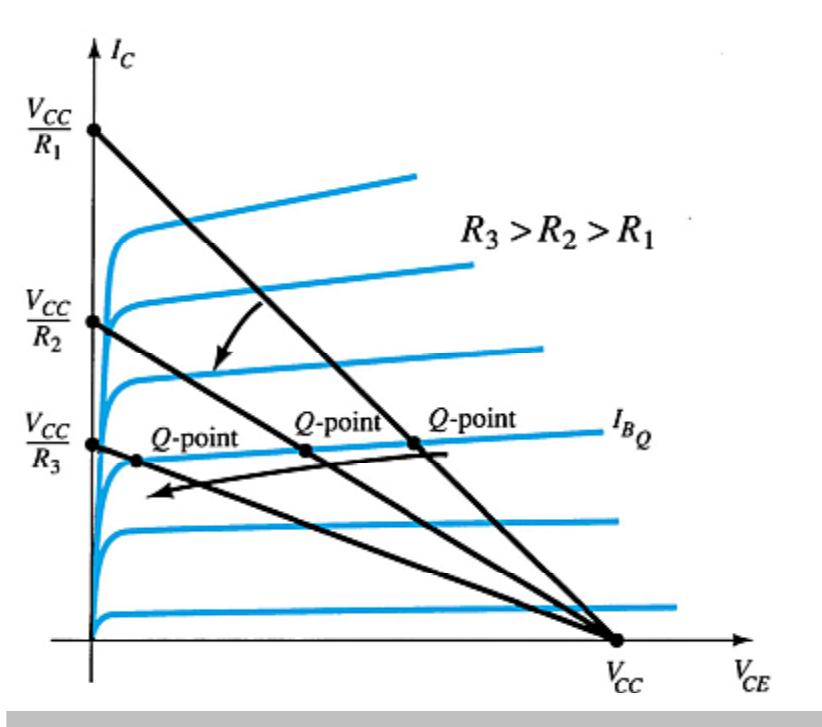
- where the value of R_B sets the value of I_B
- that sets the values of V_{CE} and I_C

Circuit Values Affect the Q-Point



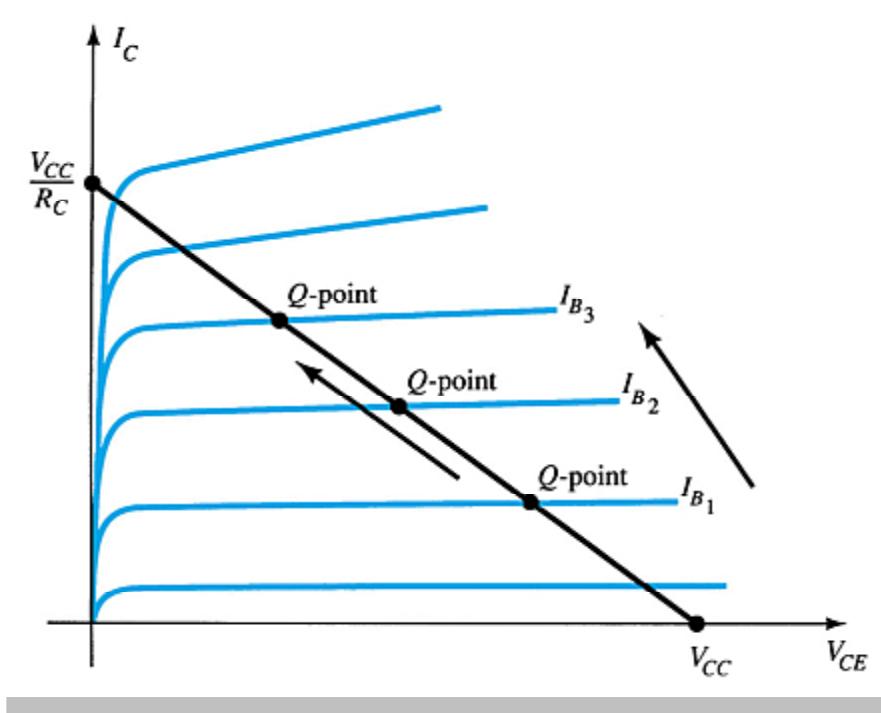
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Circuit Values Affect the Q-Point



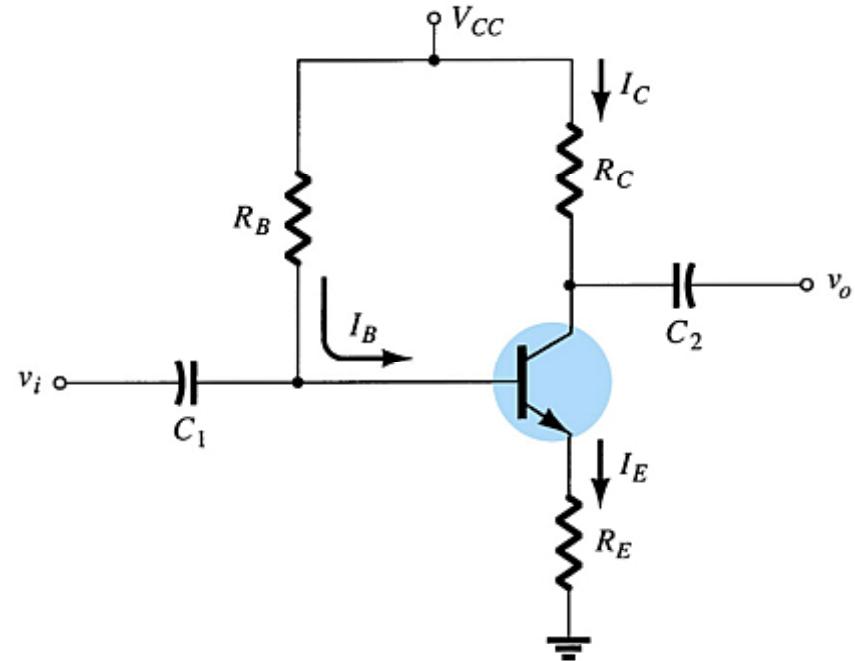
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Circuit Values Affect the Q-Point



Emitter-Stabilized Bias Circuit

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



Base-Emitter Loop

From Kirchhoff's voltage law:

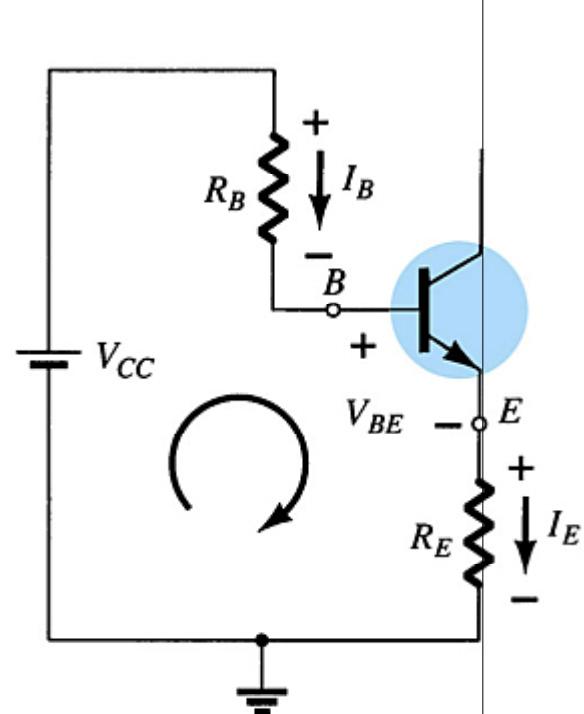
$$+V_{CC} - I_E R_E - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - (\beta + 1)I_B R_E = 0$$

Solving for I_B :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$



Collector-Emitter Loop

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \approx I_C$:

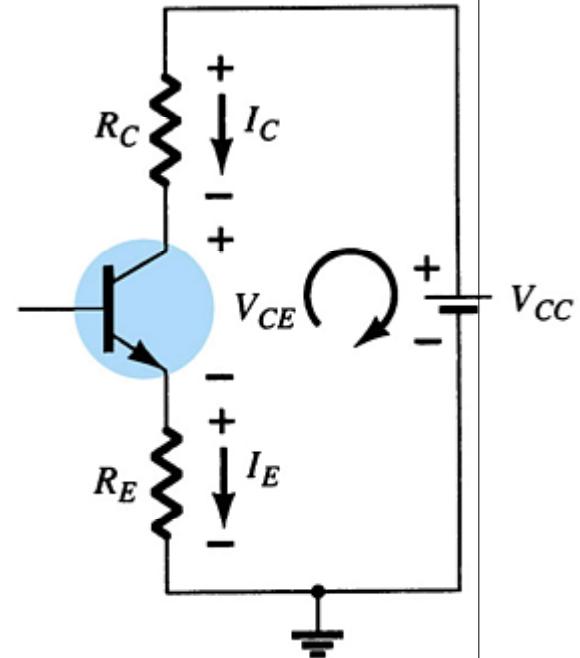
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$

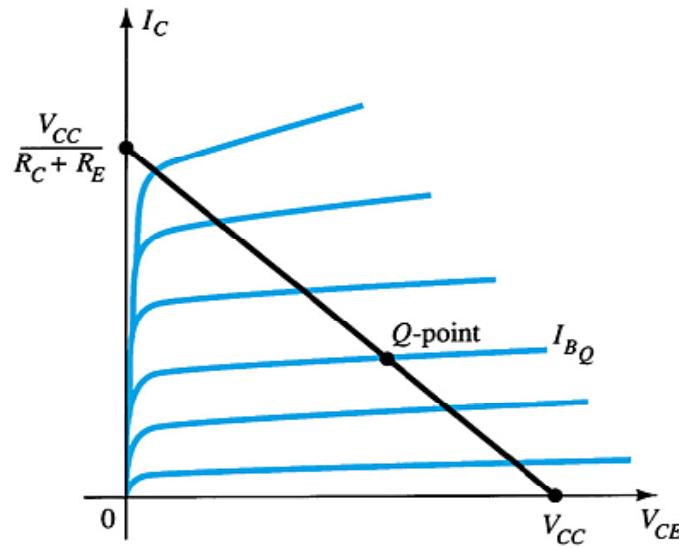
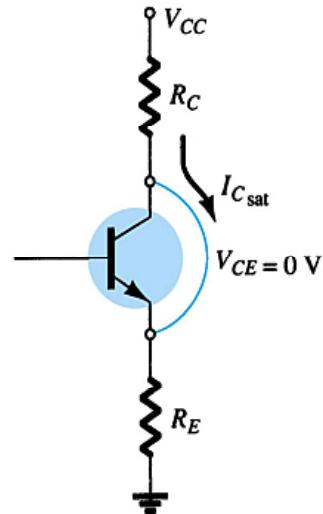


Improved Biased Stability

Stability refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.

Adding RE to the emitter improves the stability of a transistor.

Saturation Level



The endpoints can be determined from the load line.

$V_{CE\text{cutoff}}$:

$$V_{CE} = V_{CC}$$
$$I_C = 0 \text{ mA}$$

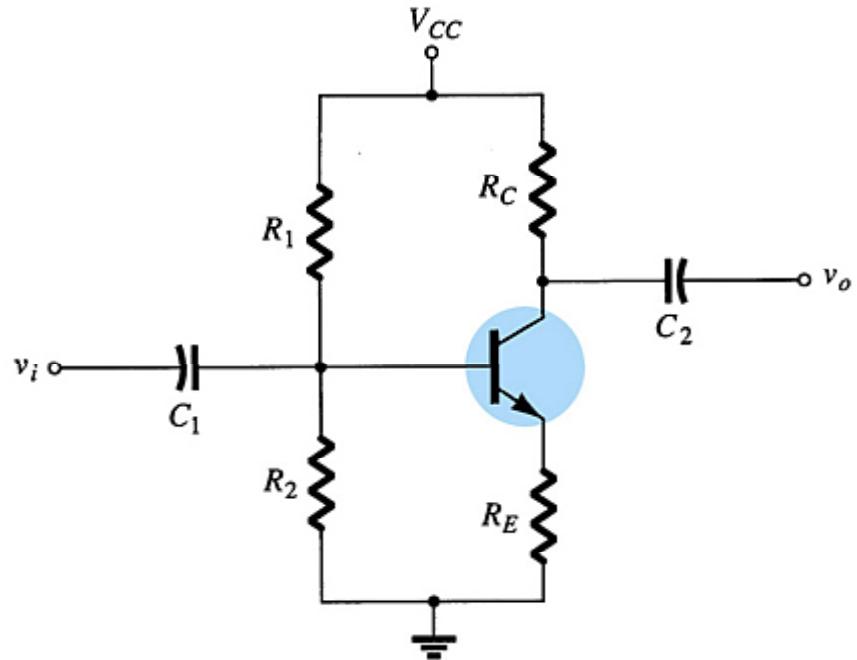
$I_{C\text{sat}}$:

$$V_{CE} = 0 \text{ V}$$
$$I_C = \frac{V_{CC}}{R_C + R_E}$$

Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in β .



Approximate Analysis

Where $I_B \ll I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

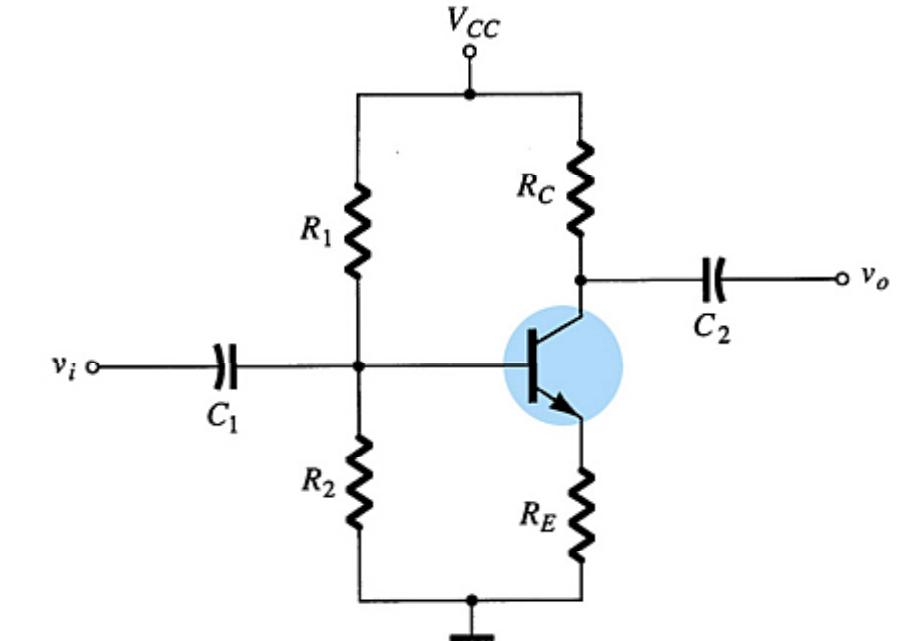
$$V_E = V_B - V_{BE}$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$



Voltage Divider Bias Analysis

Transistor Saturation Level

$$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0\text{mA}$$

Saturation:

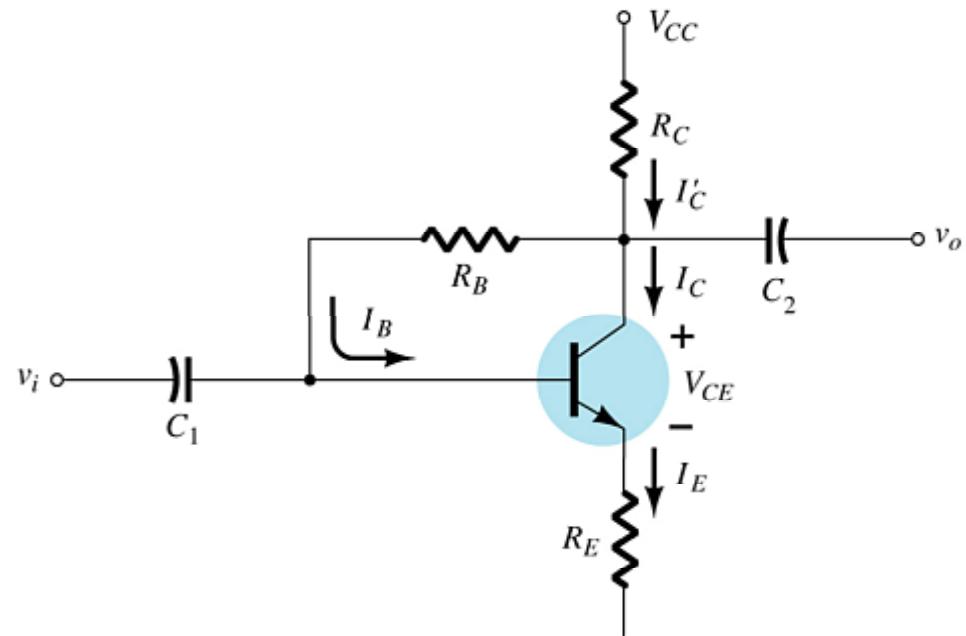
$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0\text{V}$$

DC Bias with Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, β .



Base-Emitter Loop

From Kirchhoff's voltage law:

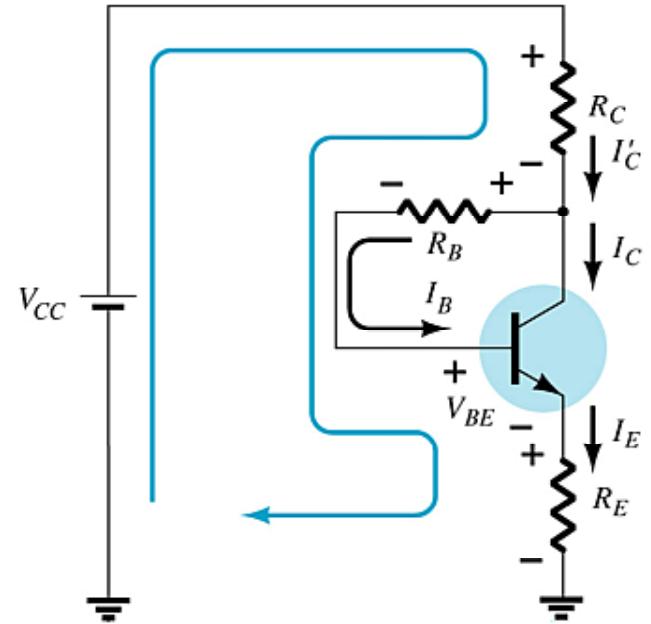
$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Where $I_B \ll I_C$:

$$I'_C = I_C + I_B \approx I_C$$

Knowing $I_C = \beta I_B$ and $I_E \approx I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$



Solving for I_B :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

Collector-Emitter Loop

Applying Kirchoff's voltage law:

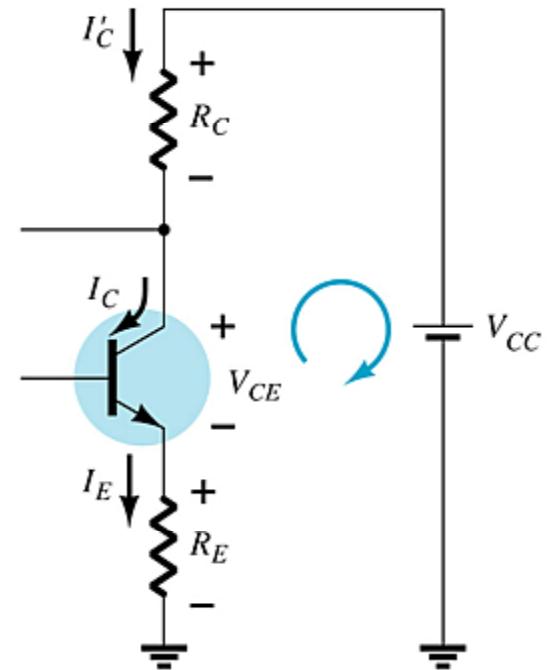
$$I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE} :

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Base-Emitter Bias Analysis

Transistor Saturation Level

$$I_{C\text{sat}} = I_{C\text{max}} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0 \text{ mA}$$

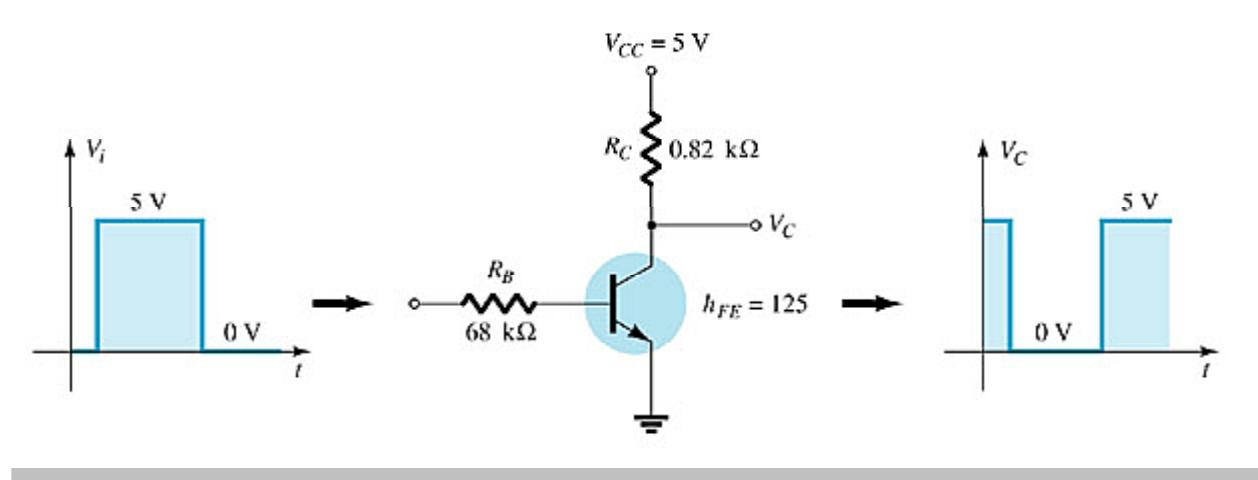
Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0 \text{ V}$$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



Switching Circuit Calculations

Saturation current:

$$I_{C\text{sat}} = \frac{V_{CC}}{R_C}$$

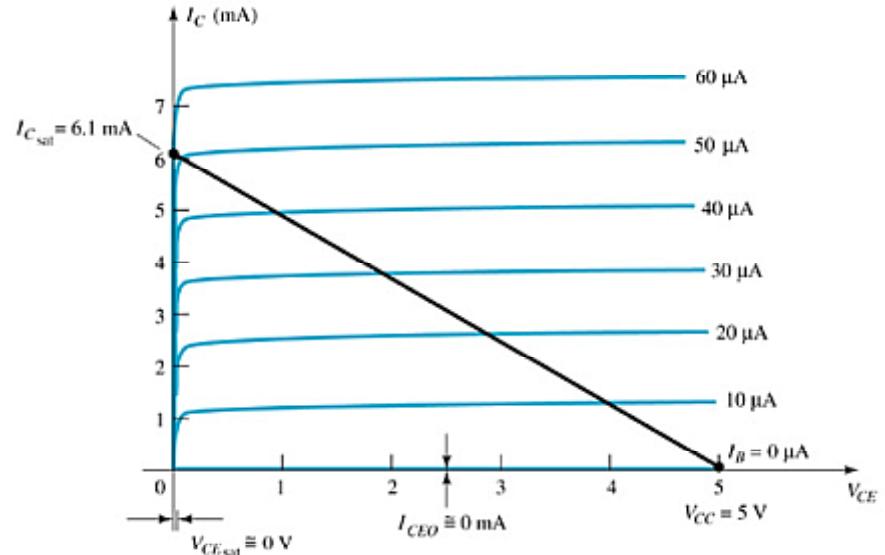
To ensure saturation:

$$I_B > \frac{I_{C\text{sat}}}{\beta_{dc}}$$

Emitter-collector resistance at saturation and cutoff:

$$R_{\text{sat}} = \frac{V_{CE\text{sat}}}{I_{C\text{sat}}}$$

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}}$$

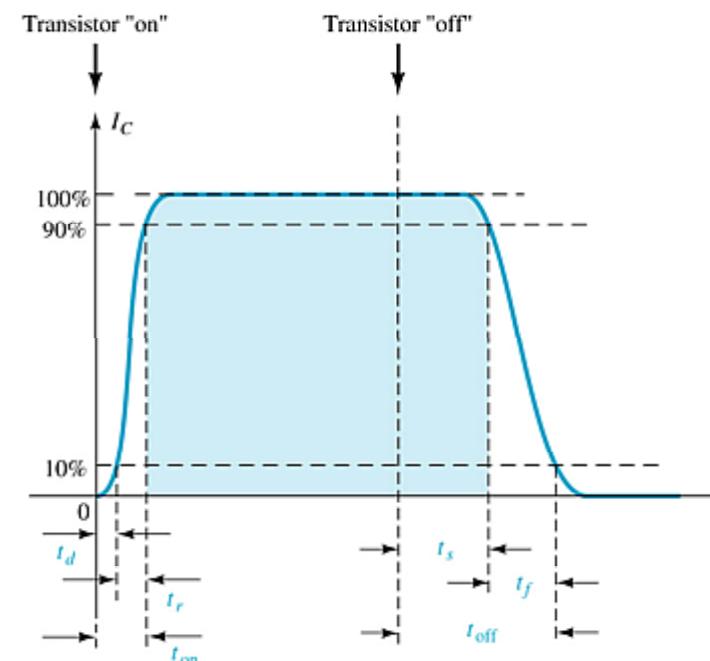


Switching Time

Transistor switching times:

$$t_{\text{on}} = t_r + t_d$$

$$t_{\text{off}} = t_s + t_f$$



Troubleshooting Hints

- Approximate voltages
 - $V_{BE} \approx .7$ V for silicon transistors
 - $V_{CE} \approx 25\%$ to 75% of V_{CC}
- Test for opens and shorts with an ohmmeter.
- Test the solder joints.
- Test the transistor with a transistor tester or a curve tracer.
- Note that the load or the next stage affects the transistor operation.

PNP Transistors

The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.