

# **BLM1033 - Circuit Theory and Electronics**

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# FETs vs. BJTs

## Similarities:

- Amplifiers
- Switching devices
- Impedance matching circuits

## Differences:

- FETs are voltage controlled devices. BJTs are current controlled devices.
- FETs have a higher input impedance. BJTs have higher gains.
- FETs are less sensitive to temperature variations and are more easily integrated on ICs.
- FETs are generally more static sensitive than BJTs.

# FET Types

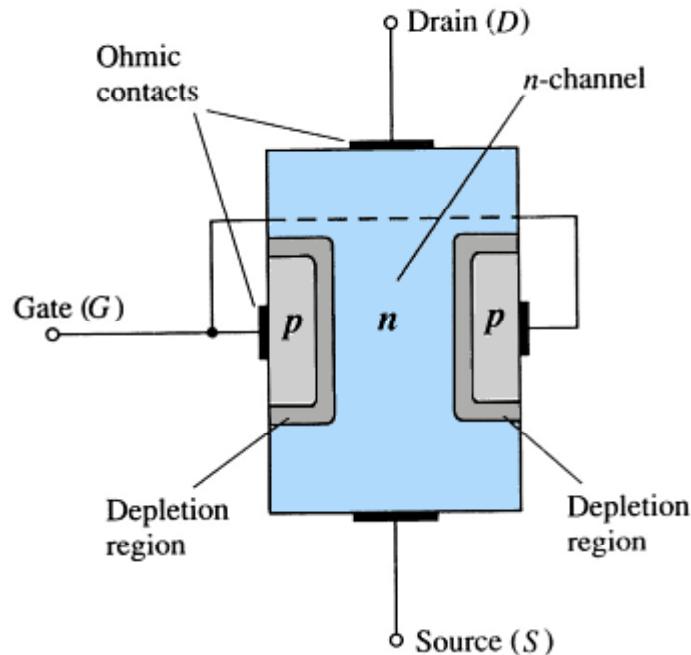
- **JFET:** Junction FET
- **MOSFET:** Metal–Oxide–Semiconductor FET
  - **D-MOSFET:** Depletion MOSFET
  - **E-MOSFET:** Enhancement MOSFET

# JFET Construction

There are two types of JFETs

- n-channel**
- p-channel**

The n-channel is more widely used.



There are three terminals:

- Drain (D)** and **Source (S)** are connected to the *n*-channel
- Gate (G)** is connected to the *p*-type material

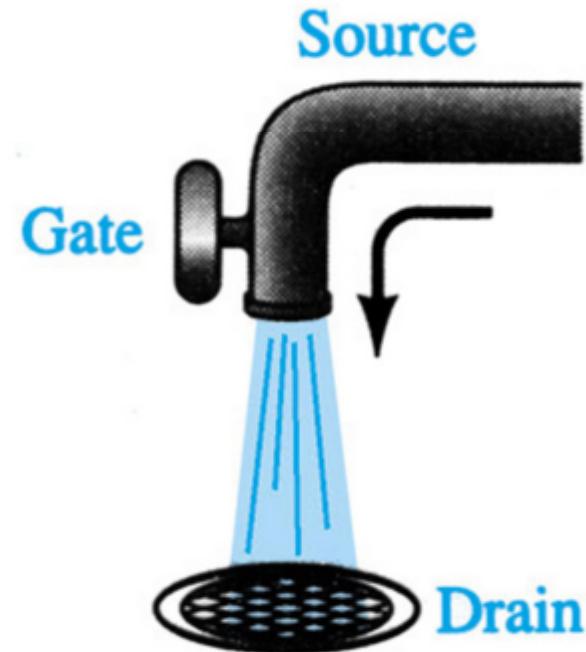
# JFET Operation: The Basic Idea

JFET operation can be compared to a water spigot.

**The source** of water pressure is the accumulation of electrons at the negative pole of the drain-source voltage.

**The drain** of water is the electron deficiency (or holes) at the positive pole of the applied voltage.

**The control** of flow of water is the gate voltage that controls the width of the n-channel and, therefore, the flow of charges from source to drain.



# JFET Operating Characteristics

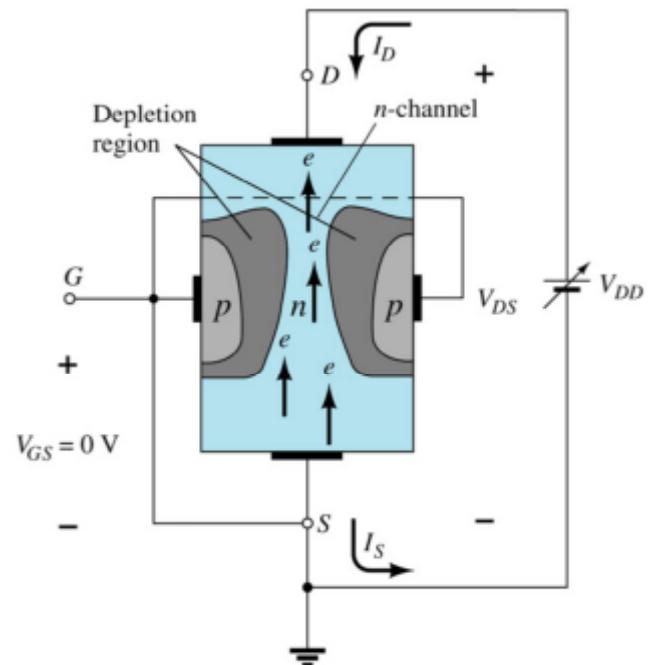
There are three basic operating conditions for a JFET:

- $V_{GS} = 0$ ,  $V_{DS}$  increasing to some positive value
- $V_{GS} < 0$ ,  $V_{DS}$  at some positive value
- Voltage-controlled resistor

# JFET Operating Characteristics: $V_{GS} = 0 \text{ V}$

Three things happen when  $V_{GS} = 0$  and  $V_{DS}$  is increased from 0 to a more positive voltage

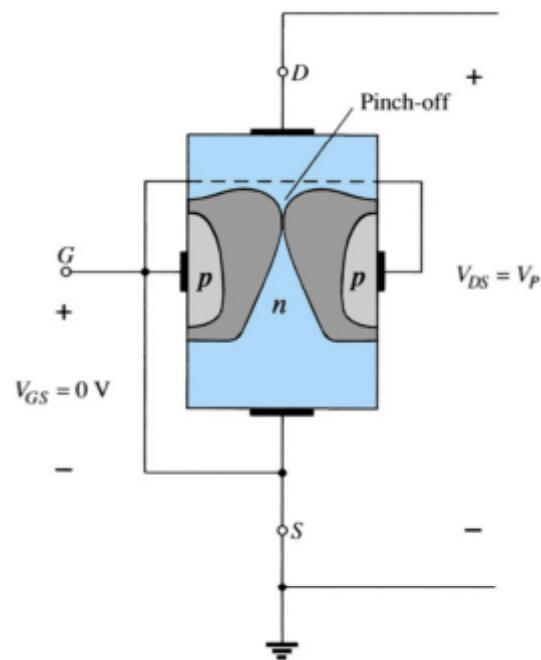
- The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- Even though the n-channel resistance is increasing, the current ( $I_D$ ) from source to drain through the n-channel is increasing. This is because  $V_{DS}$  is increasing.



# JFET Operating Characteristics: Pinch Off

If  $V_{GS} = 0$  and  $V_{DS}$  is further increased to a more positive voltage, then the depletion zone gets so large that it **pinches off** the n-channel.

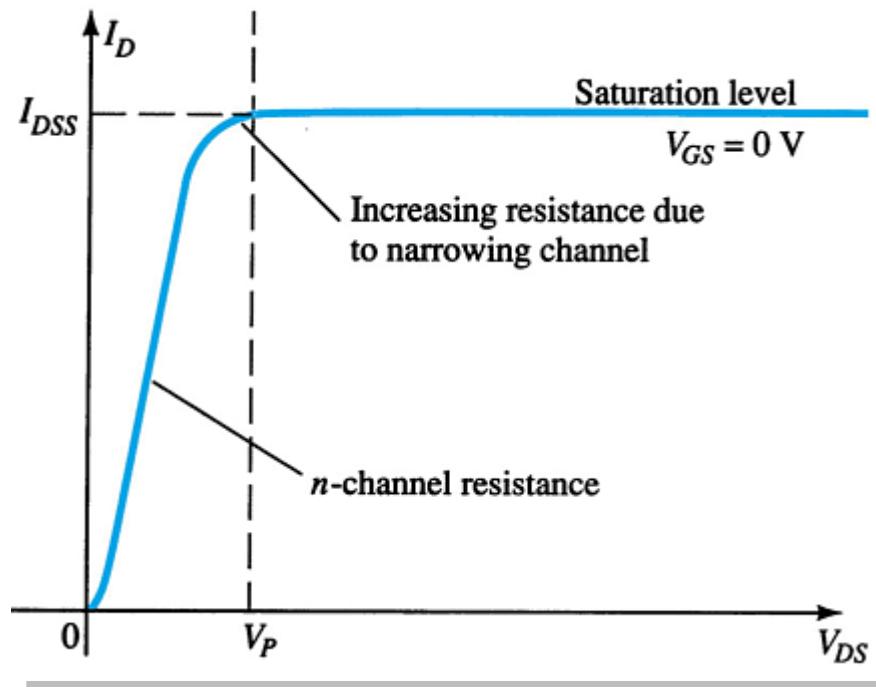
This suggests that the current in the n-channel ( $I_D$ ) would drop to 0A, but it does just the opposite—as  $V_{DS}$  increases, so does  $I_D$ .



# JFET Operating Characteristics: Saturation

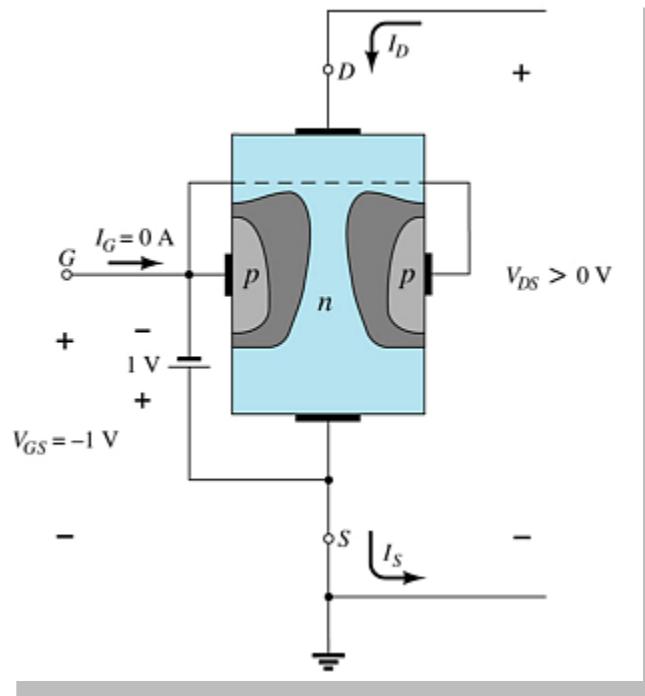
At the pinch-off point:

- Any further increase in  $V_{GS}$  does not produce any increase in  $I_D$ .  $V_{GS}$  at pinch-off is denoted as  $V_p$ .
- $I_D$  is at saturation or maximum. It is referred to as  $I_{DSS}$ .
- The ohmic value of the channel is maximum.



# JFET Operating Characteristics

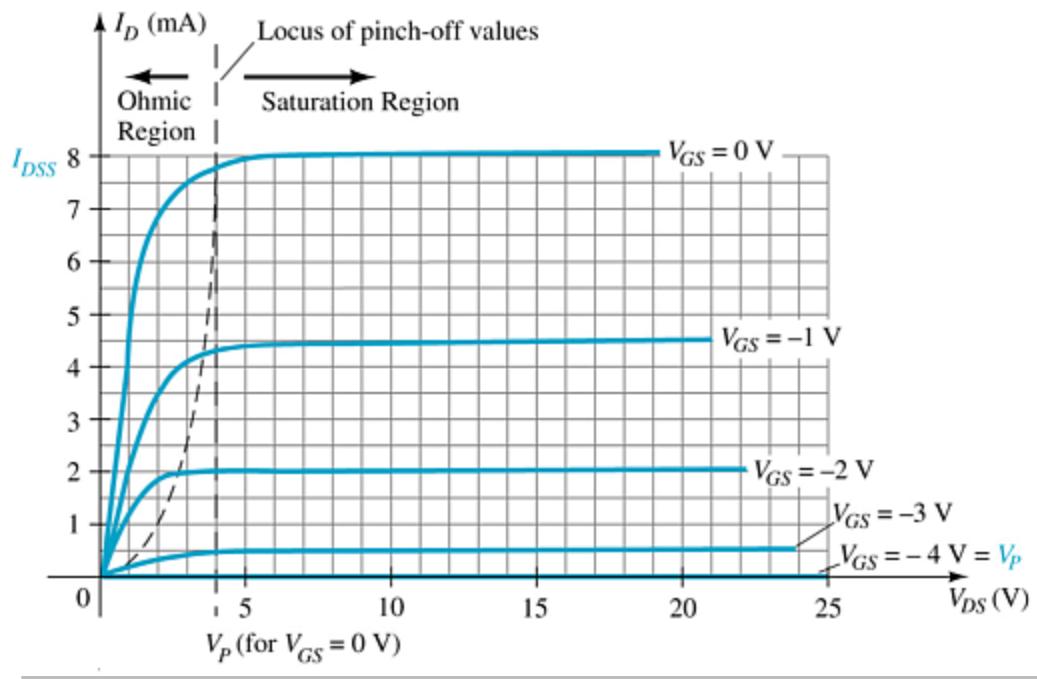
As  $V_{GS}$  becomes more negative, the depletion region increases.



# JFET Operating Characteristics

As  $V_{GS}$  becomes more negative:

- The JFET experiences pinch-off at a lower voltage ( $V_p$ ).
- $I_D$  decreases ( $I_D < I_{DSS}$ ) even though  $V_{DS}$  is increased.
- Eventually  $I_D$  reaches 0 A.  $V_{GS}$  at this point is called  $V_p$  or  $V_{GS(\text{off})}$ .



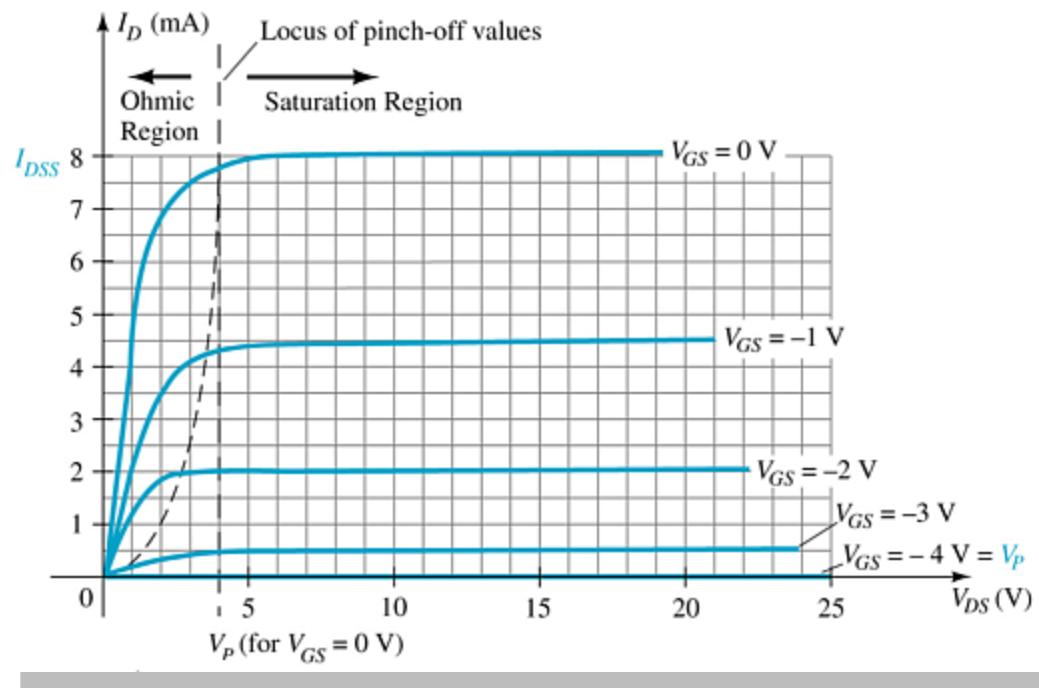
Also note that at high levels of  $V_{DS}$  the JFET reaches a breakdown situation.  $I_D$  increases uncontrollably if  $V_{DS} > V_{DS\text{max}}$ .

# JFET Operating Characteristics: Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the **ohmic region**.

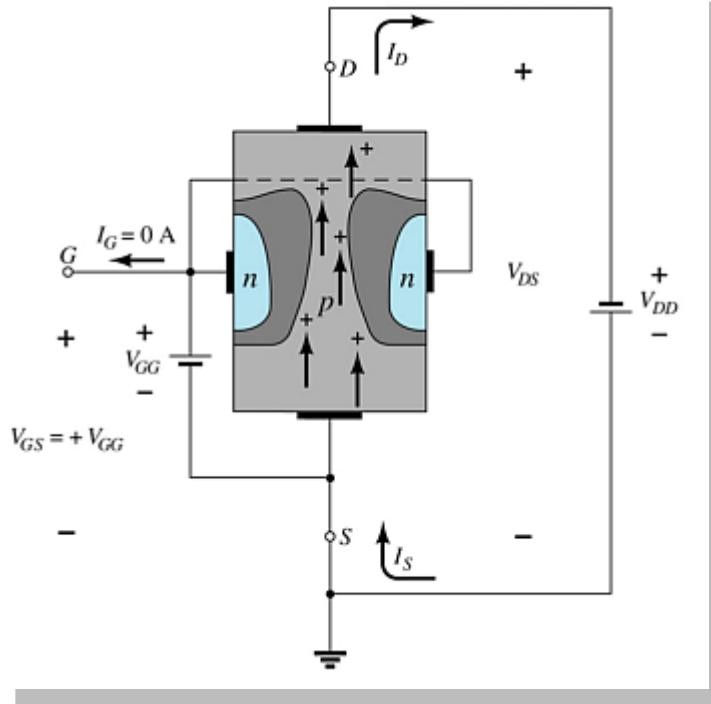
The JFET can be used as a variable resistor, where  $V_{GS}$  controls the drain-source resistance ( $r_d$ ). As  $V_{GS}$  becomes more negative, the resistance ( $r_d$ ) increases.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$



# p-Channel JFETs

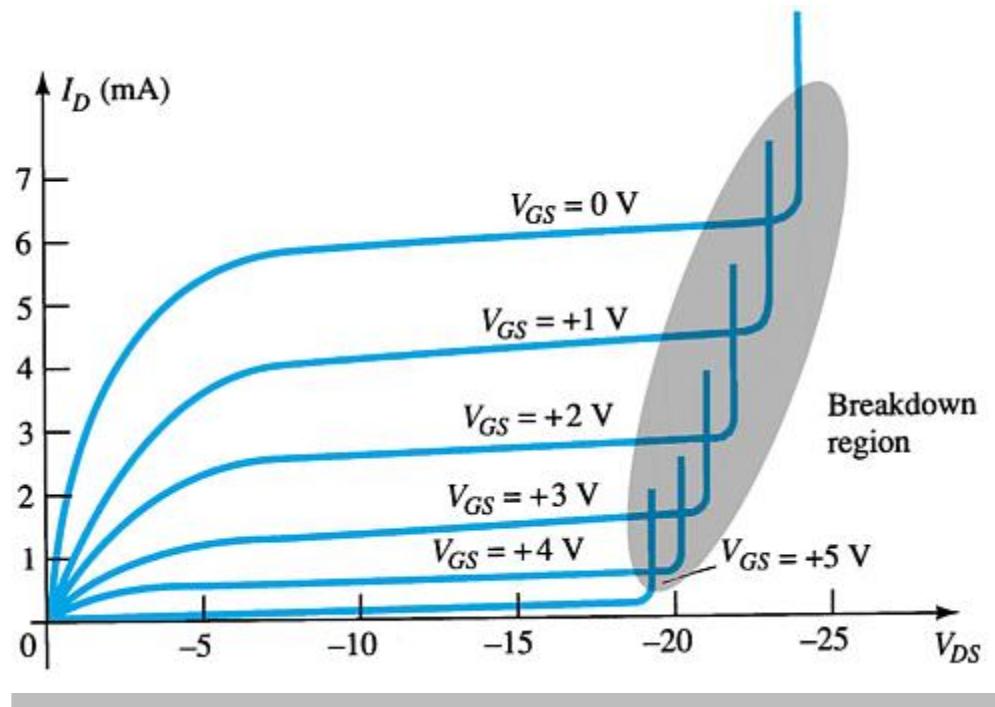
The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.



# p-Channel JFET Characteristics

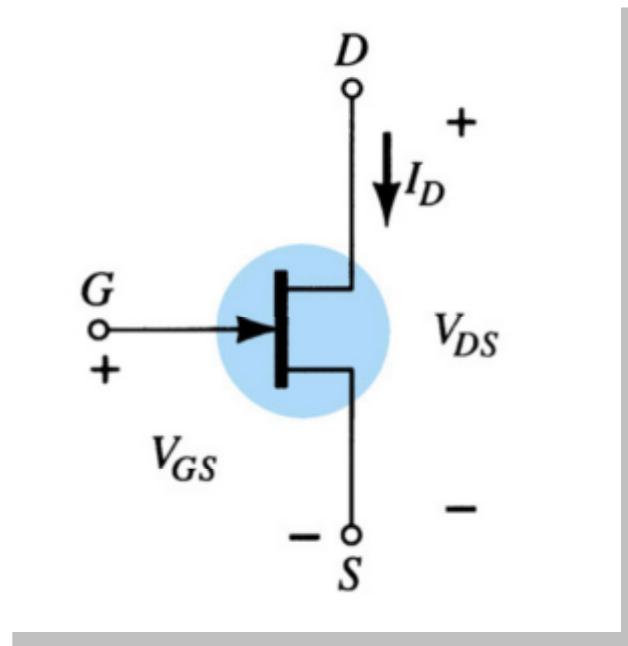
As  $V_{GS}$  increases more positively

- The depletion zone increases
- $I_D$  decreases ( $I_D < I_{DSS}$ )
- Eventually  $I_D = 0 \text{ A}$



Also note that at high levels of  $V_{DS}$  the JFET reaches a breakdown situation:  $I_D$  increases uncontrollably if  $V_{DS} > V_{DS\max}$ .

# N-Channel JFET Symbol



# JFET Transfer Characteristics

The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.

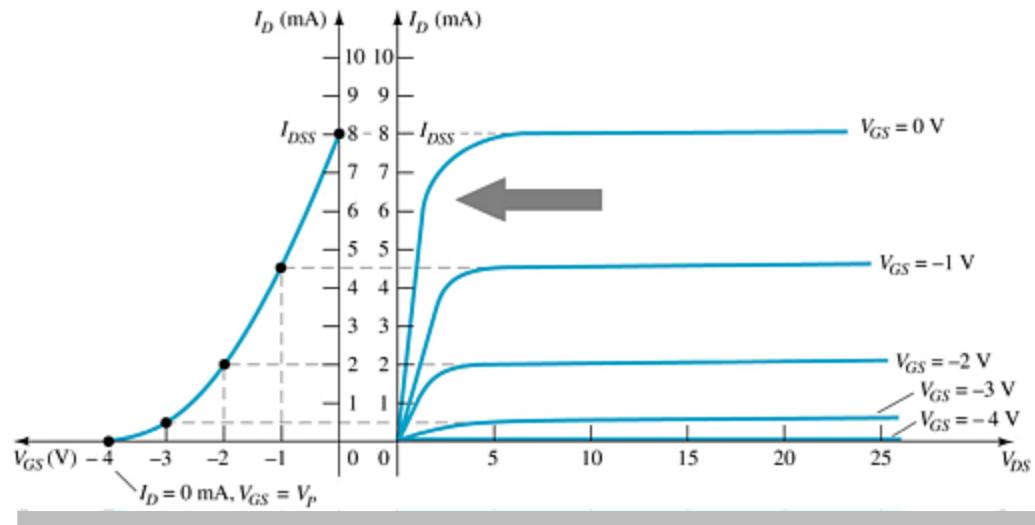
In a BJT,  $\beta$  indicates the relationship between  $I_B$  (input) and  $I_C$  (output).

In a JFET, the relationship of  $V_{GS}$  (input) and  $I_D$  (output) is a little more complicated:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

# JFET Transfer Curve

This graph shows the value of  $I_D$  for a given value of  $V_{GS}$ .



# Plotting the JFET Transfer Curve

Using  $I_{DSS}$  and  $V_p$  ( $V_{GS(off)}$ ) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

## Step 1

Solving for  $V_{GS} = 0V$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$
$$I_D = I_{DSS}$$

## Step 2

Solving for  $V_{GS} = V_p$  ( $V_{GS(off)}$ )  $I_D = 0A$

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

## Step 3

Solving for  $V_{GS} = 0V$  to  $V_p$   $I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$

# JFET Specifications Sheet

## Electrical Characteristics

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Gate-Source Breakdown Voltage ( $I_G = -10 \mu\text{Adc}$ , $V_{DS} = 0$ )	$V_{(BR)GSS}$	-25	-	-	Vdc
Gate Reverse Current ( $V_{GS} = -15 \text{ Vdc}$ , $V_{DS} = 0$ ) ( $V_{GS} = -15 \text{ Vdc}$ , $V_{DS} = 0$ , $T_A = 100^\circ\text{C}$ )	$I_{GSS}$	-	-	-1.0 -200	nAdc
Gate Source Cutoff Voltage ( $V_{DS} = 15 \text{ Vdc}$ , $I_D = 10 \text{ nAdc}$ )	$V_{GS(off)}$	-0.5	-	-6.0	Vdc
Gate Source Voltage ( $V_{DS} = 15 \text{ Vdc}$ , $I_D = 100 \mu\text{Adc}$ )	$V_{GS}$	-	-2.5	-	Vdc
<b>ON CHARACTERISTICS</b>					
Zero-Gate-Voltage Drain Current* ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ )	$I_{DSS}$	1.0	3.0	5.0	mAdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>					
Forward Transfer Admittance Common Source* ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	$y_{sd}$	1000	-	5000	$\mu\text{mhos}$
Output Admittance Common Source* ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	$y_{os}$	-	10	50	$\mu\text{mhos}$
Input Capacitance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{iss}$	-	4.5	7.0	pF
Reverse Transfer Capacitance ( $V_{DS} = 15 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{rss}$	-	1.5	3.0	pF

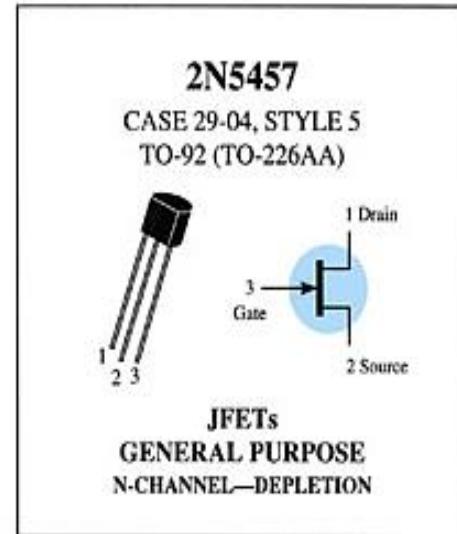
\*Pulse Test: Pulse Width  $\leq 630 \text{ ms}$ ; Duty Cycle  $\leq 10\%$

# JFET Specifications Sheet

## Maximum Ratings

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	25	Vdc
Drain-Gate Voltage	$V_{DG}$	25	Vdc
Reverse Gate-Source Voltage	$V_{GSR}$	-25	Vdc
Gate Current	$I_G$	10	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	310 2.82	mW mW/ $^\circ\text{C}$
Junction Temperature Range	$T_J$	125	$^\circ\text{C}$
Storage Channel Temperature Range	$T_{sig}$	-65 to +150	$^\circ\text{C}$



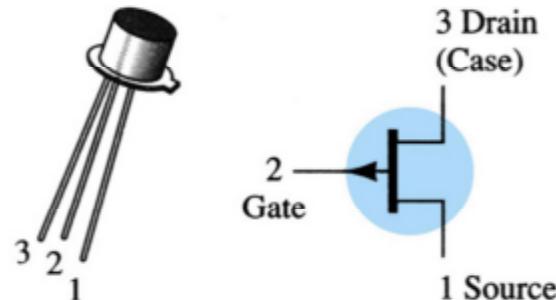
Refer to 2N4220 for graphs.

more...

# Case and Terminal Identification

**2N2844**

CASE 22-03, STYLE 12  
TO-18 (TO-206AA)



**JFETs**  
**GENERAL PURPOSE**  
**P-CHANNEL**

# Testing JFETs

- **Curve Tracer**

A curve tracer displays the  $I_D$  versus  $V_{DS}$  graph for various levels of  $V_{GS}$ .

- **Specialized FET Testers**

These testers show  $I_{DSS}$  for the JFET under test.

# MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful.

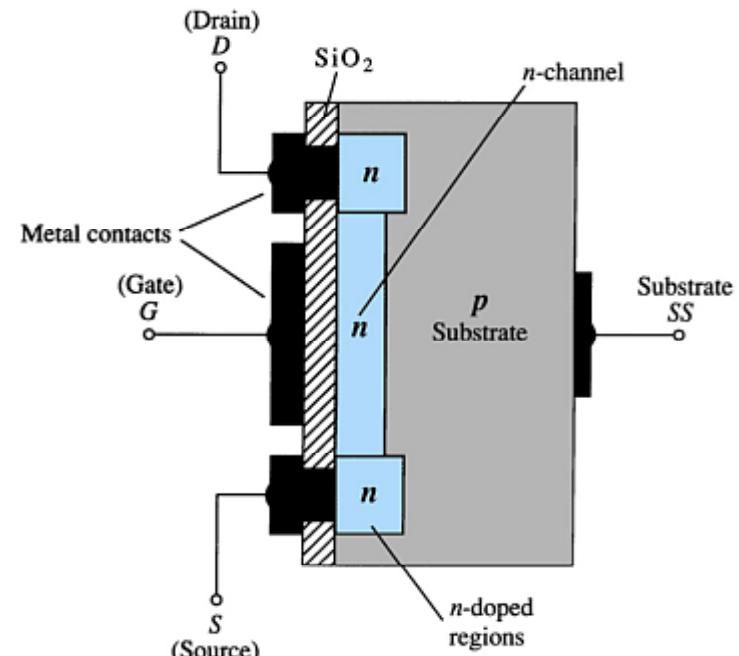
There are two types of MOSFETs:

- Depletion-Type
- Enhancement-Type

# Depletion-Type MOSFET Construction

The **Drain (D)** and **Source (S)** connect to the two *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the **Gate (G)** via a thin insulating layer of  $\text{SiO}_2$ .

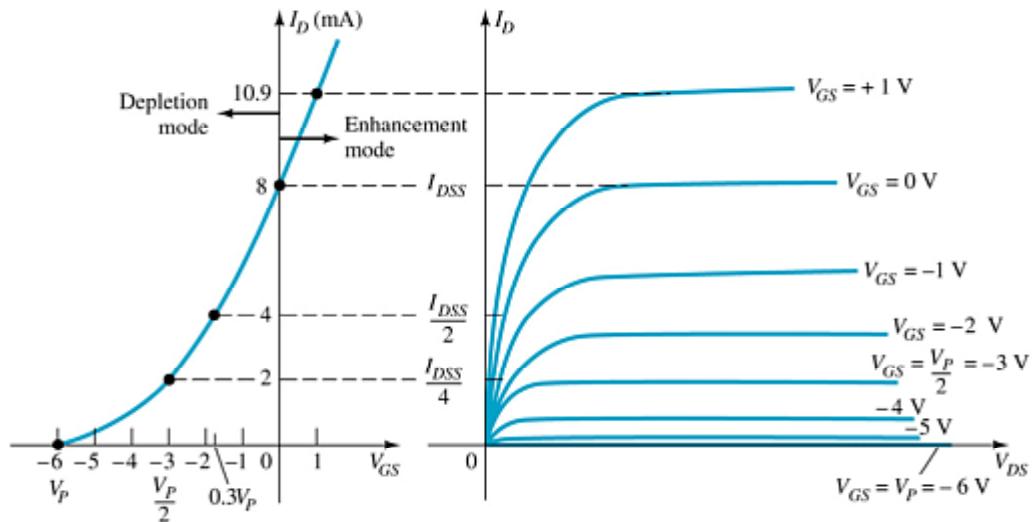
The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called **Substrate (SS)**.



# Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

- Depletion mode
- Enhancement mode



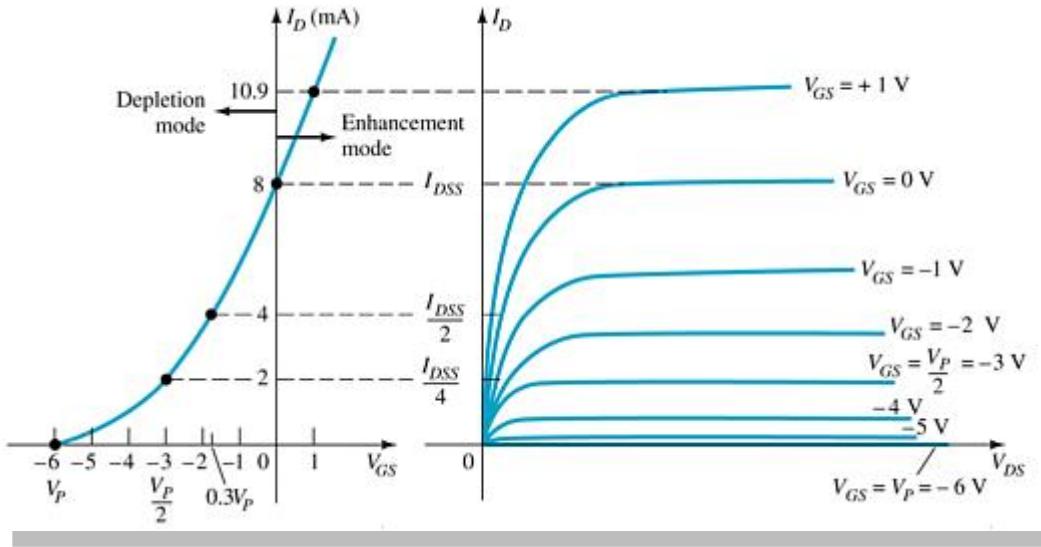
# D-Type MOSFET in Depletion Mode

## Depletion Mode

The characteristics are similar to a JFET.

- When  $V_{GS} = 0 \text{ V}$ ,  $I_D = I_{DSS}$
- When  $V_{GS} < 0 \text{ V}$ ,  $I_D < I_{DSS}$
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

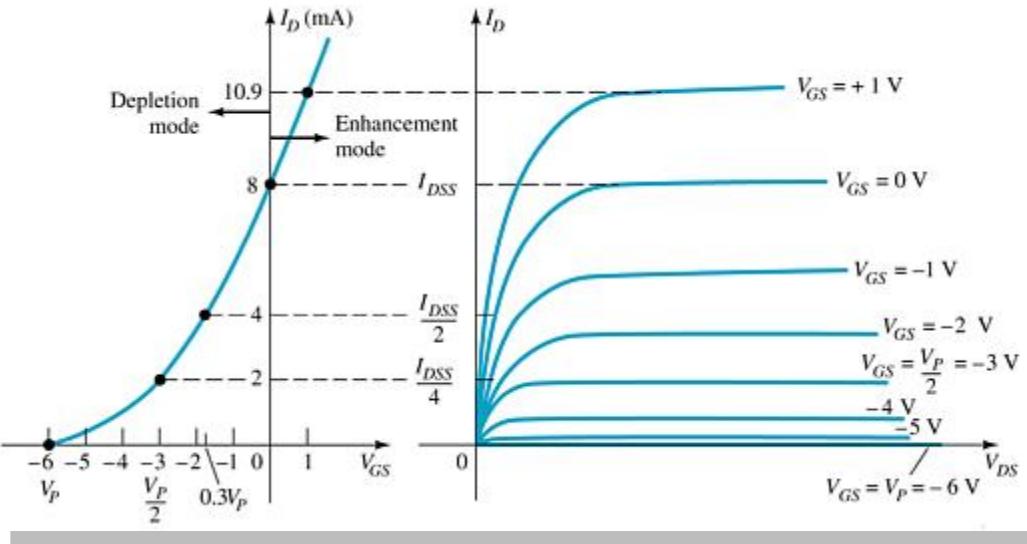


# D-Type MOSFET in Enhancement Mode

## Enhancement Mode

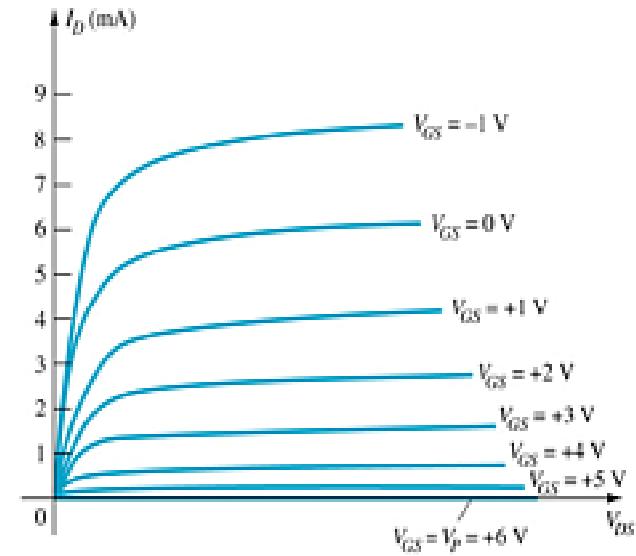
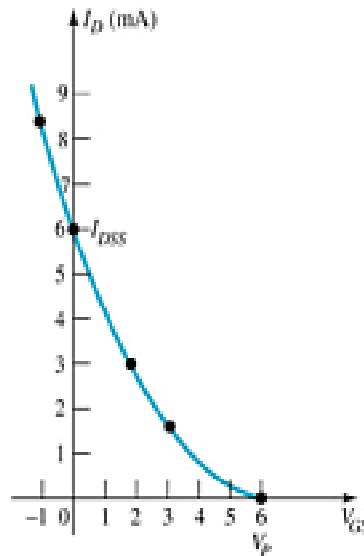
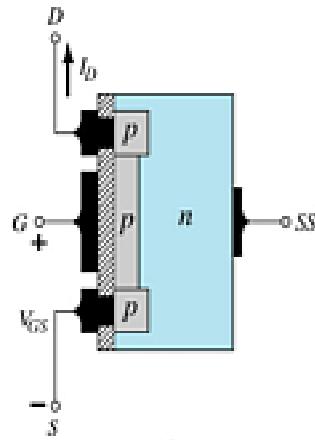
- $V_{GS} > 0 \text{ V}$
- $I_D$  increases above  $I_{DSS}$
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$



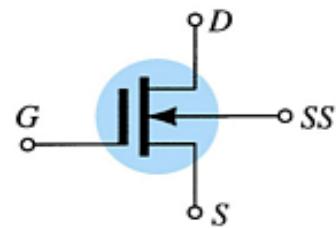
Note that  $V_{GS}$  is now a positive polarity

# p-Channel D-Type MOSFET

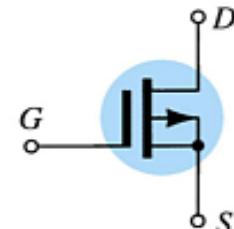
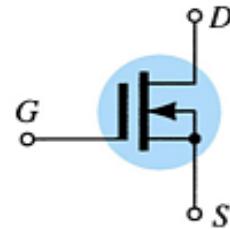
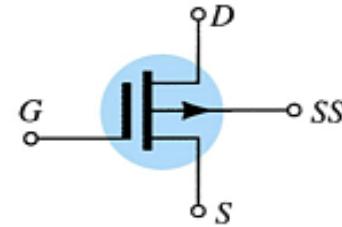


# D-Type MOSFET Symbols

*n*-channel



*p*-channel



# Specification Sheet

## Maximum Ratings

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage 2N3797	$V_{DS}$	20	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 10$	Vdc
Drain Current	$I_D$	20	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	mW mW/C
Junction Temperature Range	$T_J$	+175	'C
Storage Channel Temperature Range	$T_{sg}$	-65 to +200	'C



[more...](#)

# Specification Sheet

## Electrical Characteristics

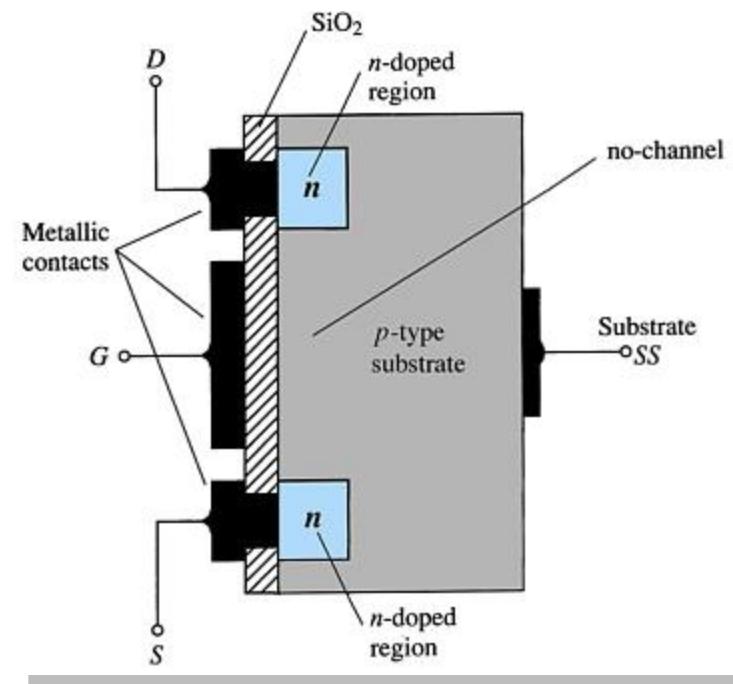
ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain Source Breakdown Voltage ( $V_{GS} = -7.0 \text{ V}$ , $I_D = 5.0 \mu\text{A}$ )	2N3797	$V_{(BR)DSX}$	20	25	—	Vdc
Gate Reverse Current (1) ( $V_{GS} = -10 \text{ V}$ , $V_{DS} = 0$ ) ( $V_{GS} = -10 \text{ V}$ , $V_{DS} = 0$ , $T_A = 150^\circ\text{C}$ )		$I_{GSS}$	— —	— —	1.0 200	pAdc
Gate Source Cutoff Voltage ( $I_D = 2.0 \mu\text{A}$ , $V_{DS} = 10 \text{ V}$ )	2N3797	$V_{GS(\text{off})}$	—	-5.0	-7.0	Vdc
Drain-Gate Reverse Current (1) ( $V_{DG} = 10 \text{ V}$ , $I_S = 0$ )		$I_{DGG}$	—	—	1.0	pAdc
<b>ON CHARACTERISTICS</b>						
Zero-Gate-Voltage Drain Current ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ )	2N3797	$I_{DSS}$	2.0	2.9	6.0	mAdc
On-State Drain Current ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = +3.5 \text{ V}$ )	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>						
Forward Transfer Admittance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	2N3797	$ Y_{fs} $	1500	2300	3000	$\mu\text{mhos}$
( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	2N3797		1500	—	—	
Output Admittance ( $I_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	2N3797	$ Y_{os} $	—	27	60	$\mu\text{mhos}$
Input Capacitance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	2N3797	$C_{in}$	—	6.0	8.0	pF
Reverse Transfer Capacitance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )		$C_{rs}$	—	0.5	0.8	pF
<b>FUNCTIONAL CHARACTERISTICS</b>						
Noise Figure ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ , $R_S = 3 \text{ megohms}$ )		NF	—	3.8	—	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

# E-Type MOSFET Construction

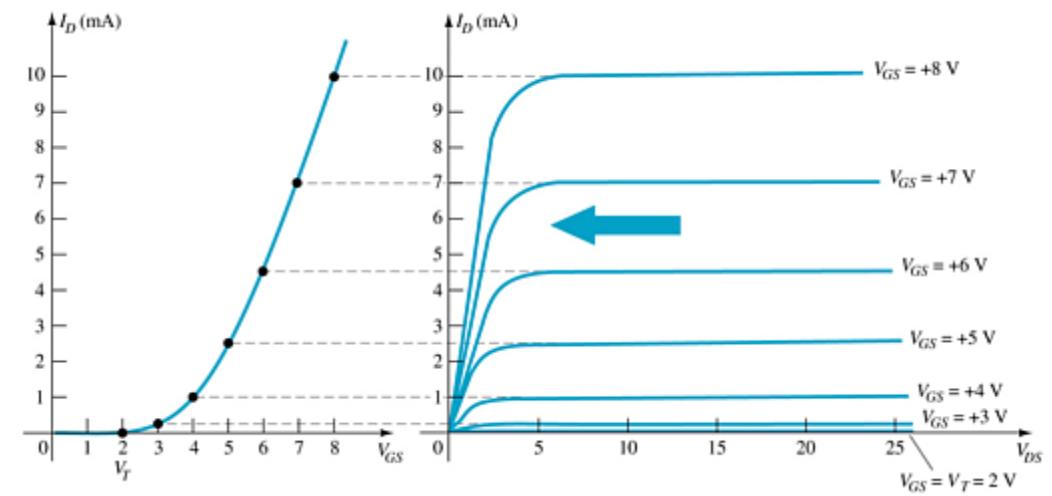
- The **Drain (D)** and **Source (S)** connect to the *n*-doped regions. These *n*-doped regions are connected via an *n*-channel
- The **Gate (G)** connects to the *p*-doped substrate via a thin insulating layer of  $\text{SiO}_2$
- There is no channel
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the **Substrate (SS)**



# Basic Operation of the E-Type MOSFET

The enhancement-type MOSFET operates only in the enhancement mode.

- $V_{GS}$  is always positive
- As  $V_{GS}$  increases,  $I_D$  increases
- As  $V_{GS}$  is kept constant and  $V_{DS}$  is increased, then  $I_D$  saturates ( $I_{DSS}$ ) and the saturation level,  $V_{DSsat}$  is reached



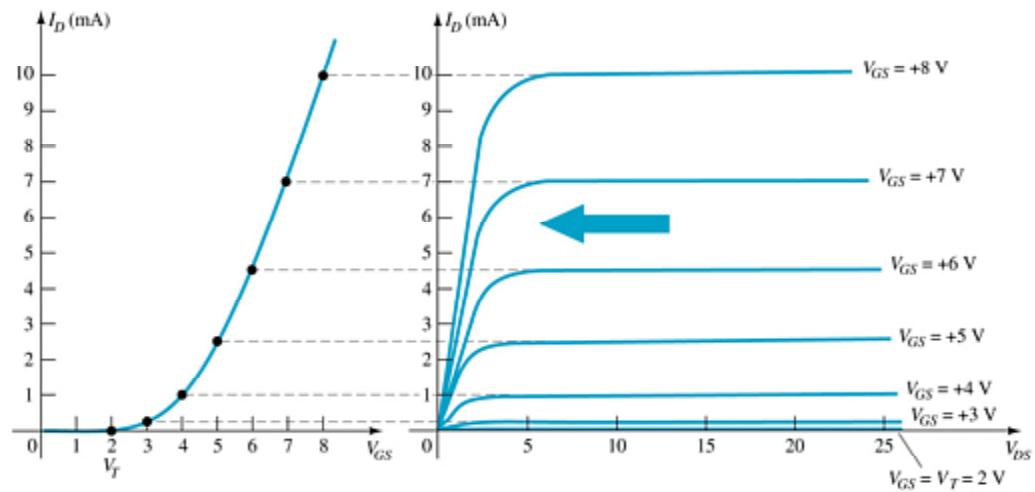
# E-Type MOSFET Transfer Curve

To determine  $I_D$  given  $V_{GS}$ :

$$I_D = k(V_{GS} - V_T)^2$$

Where:

$V_T$  = threshold voltage  
or voltage at which the  
MOSFET turns on



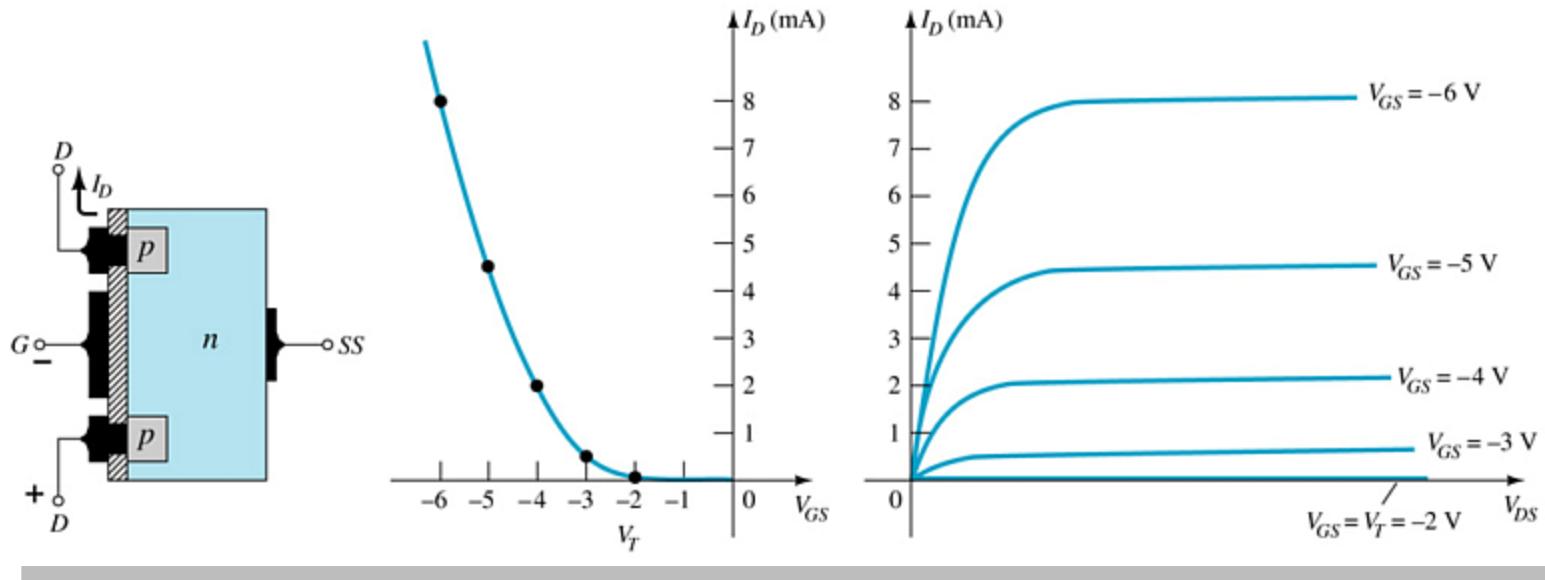
$k$ , a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

$V_{DSsat}$  can be calculated by:

$$V_{DSsat} = V_{GS} - V_T$$

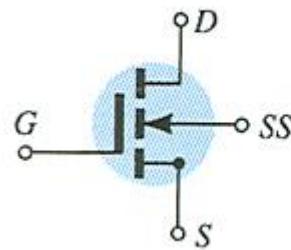
# *p*-Channel E-Type MOSFETs



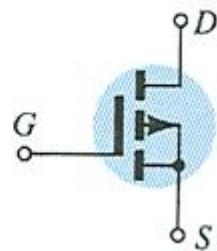
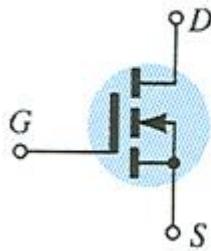
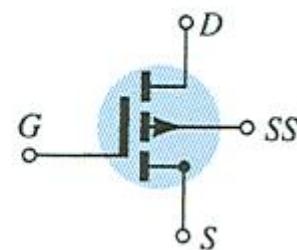
The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

# MOSFET Symbols

*n*-channel



*p*-channel



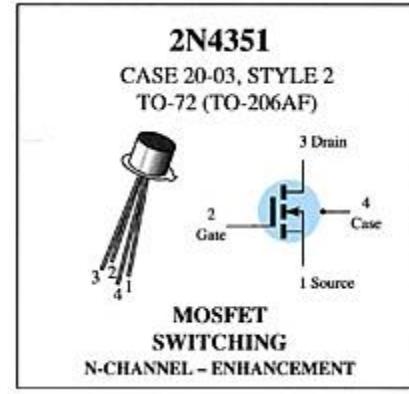
# Specification Sheet

## Maximum Ratings

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DS</sub>	25	Vdc
Drain-Gate Voltage	V <sub>DG</sub>	30	Vdc
Gate-Source Voltage*	V <sub>GS</sub>	30	Vdc
Drain Current	I <sub>D</sub>	30	mAdc
Total Device Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	300 1.7	mW mW/°C
Junction Temperature Range	T <sub>J</sub>	-175	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +175	°C

\* Transient potentials of  $\pm 75$  Volt will not cause gate-oxide failure.



more...

# Specification Sheet

## Electrical Characteristics

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Drain-Source Breakdown Voltage ( $I_D = 10 \mu\text{A}$ , $V_{GS} = 0$ )	$V_{(BR)DSX}$	25	—	Vdc	
Zero-Gate-Voltage Drain Current ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ ) $T_A = 25^\circ\text{C}$ $T_A = 150^\circ\text{C}$	$I_{DSS}$	— —	10 10	nAdc $\mu\text{Adc}$	
Gate Reverse Current ( $V_{GS} = \pm 15 \text{ Vdc}$ , $V_{DS} = 0$ )	$I_{GSS}$	—	$\pm 10$	pAdc	
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage ( $V_{DS} = 10 \text{ V}$ , $I_D = 10 \mu\text{A}$ )	$V_{GS(\text{Th})}$	1.0	5	Vdc	
Drain-Source On-Voltage ( $I_D = 2.0 \text{ mA}$ , $V_{GS} = 10 \text{ V}$ )	$V_{DS(on)}$	—	1.0	V	
On-State Drain Current ( $V_{GS} = 10 \text{ V}$ , $V_{DS} = 10 \text{ V}$ )	$I_{D(on)}$	3.0	—	mAdc	
<b>SMALL-SIGNAL CHARACTERISTICS</b>					
Forward Transfer Admittance ( $V_{DS} = 10 \text{ V}$ , $I_D = 2.0 \text{ mA}$ , $f = 1.0 \text{ kHz}$ )	$ y_{fs} $	1000	—	$\mu\text{mho}$	
Input Capacitance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 140 \text{ kHz}$ )	$C_{iss}$	—	5.0	pF	
Reverse Transfer Capacitance ( $V_{DS} = 0$ , $V_{GS} = 0$ , $f = 140 \text{ kHz}$ )	$C_{rss}$	—	1.3	pF	
Drain-Substrate Capacitance ( $V_{DSUB} = 10 \text{ V}$ , $f = 140 \text{ kHz}$ )	$C_{d(sub)}$	—	5.0	pF	
Drain-Source Resistance ( $V_{GS} = 10 \text{ V}$ , $I_D = 0$ , $f = 1.0 \text{ kHz}$ )	$r_{ds(on)}$	—	300	ohms	
<b>SWITCHING CHARACTERISTICS</b>					
Turn-On Delay (Fig. 5)	$I_D = 2.0 \text{ mAdc}$ , $V_{DS} = 10 \text{ Vdc}$ , $(V_{GS} = 10 \text{ Vdc})$ Turn-Off Delay (Fig. 7) (See Figure 9; Times Circuit Determined)	$t_{dt}$	—	45	ns
Rise Time (Fig. 6)		$t_r$	—	65	ns
Turn-Off Delay (Fig. 7)		$t_{d2}$	—	60	ns
Fall Time (Fig. 8)		$t_f$	—	100	ns

# Handling MOSFETs

MOSFETs are very sensitive to static electricity. Because of the very thin  $\text{SiO}_2$  layer between the external terminals and the layers of the device, any small electrical discharge can create an unwanted conduction.

## Protection

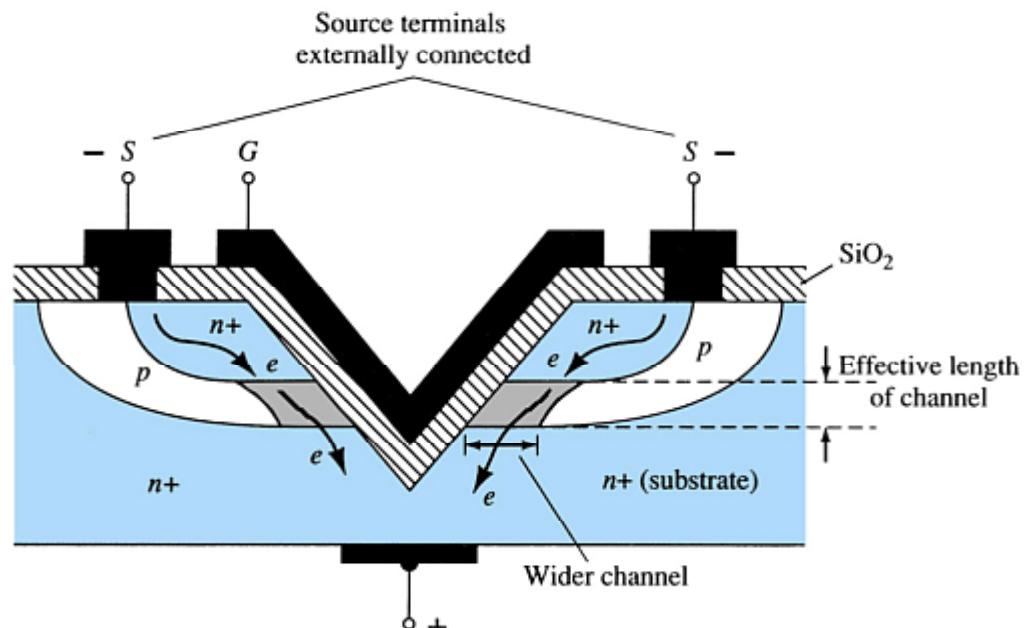
- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- 
- Apply voltage limiting devices between the gate and source, such as back-to-back Zeners to limit any transient voltage.

# VMOS Devices

VMOS (vertical MOSFET) increases the surface area of the device.

## Advantages

- VMOS devices handle higher currents by providing more surface area to dissipate the heat.
- VMOS devices also have faster switching times.

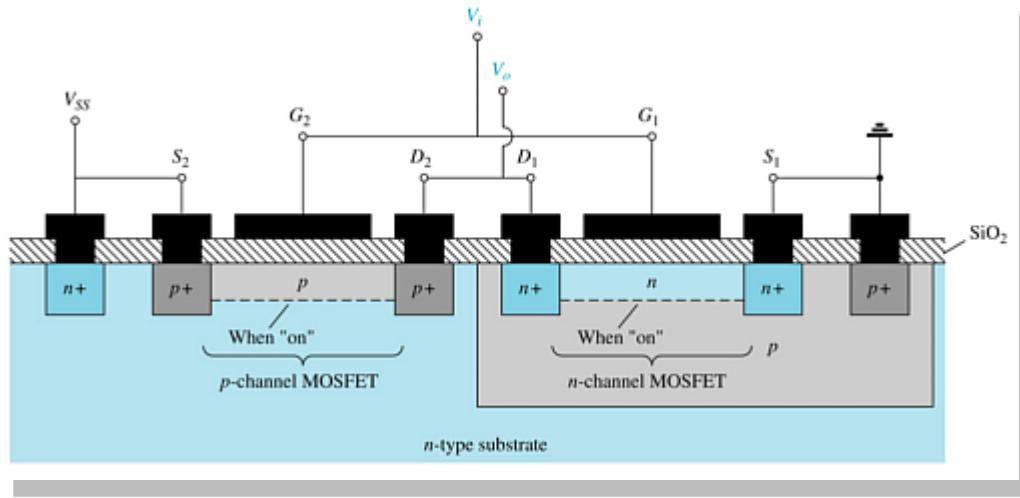


# CMOS Devices

CMOS (complementary MOSFET) uses a *p*-channel and *n*-channel MOSFET; often on the same substrate as shown here.

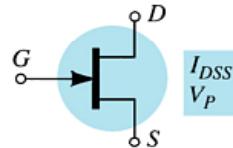
## Advantages

- Useful in logic circuit designs
- Higher input impedance
- Faster switching speeds
- Lower operating power levels

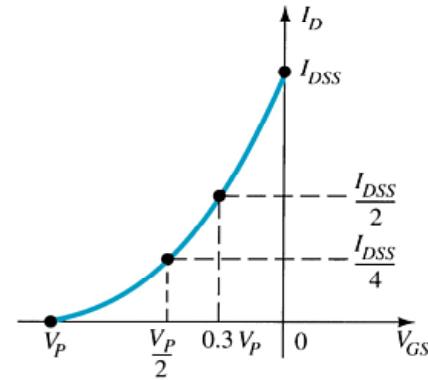


# Summary Table

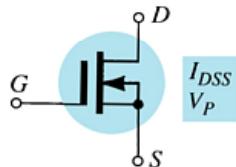
$$I_G = 0 \text{ A}, I_D = I_S$$



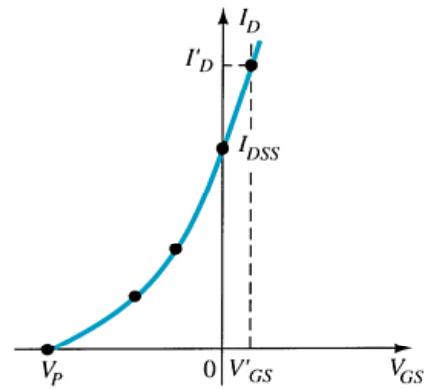
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$



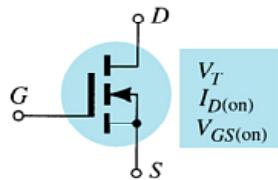
$$I_G = 0 \text{ A}, I_D = I_S$$



$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

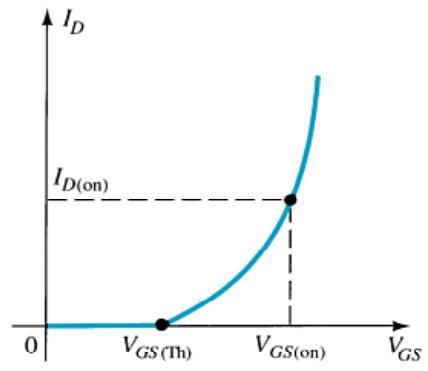


$$I_G = 0 \text{ A}, I_D = I_S$$



$$I_D = k \left( \frac{V_{GS} - V_{GS(\text{Th})}}{I_{D(\text{on})}} \right)^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$



# Common FET Biasing Circuits

## JFET Biasing Circuits

- Fixed – Bias
- Self-Bias
- Voltage-Divider Bias

## D-Type MOSFET Biasing Circuits

- Self-Bias
- Voltage-Divider Bias

## E-Type MOSFET Biasing Circuits

- Feedback Configuration
- Voltage-Divider Bias

# Basic Current Relationships

For all FETs:

$$I_G \cong 0A$$

$$I_D = I_S$$

For JFETs and D-Type MOSFETs:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

For E-Type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

# Fixed-Bias Configuration

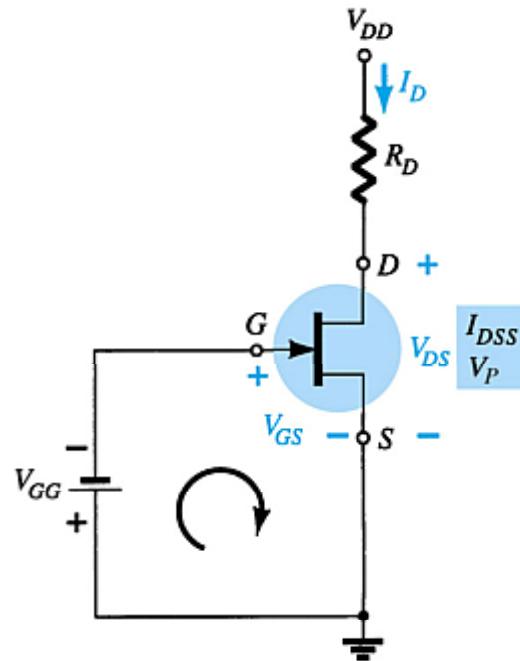
$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0V$$

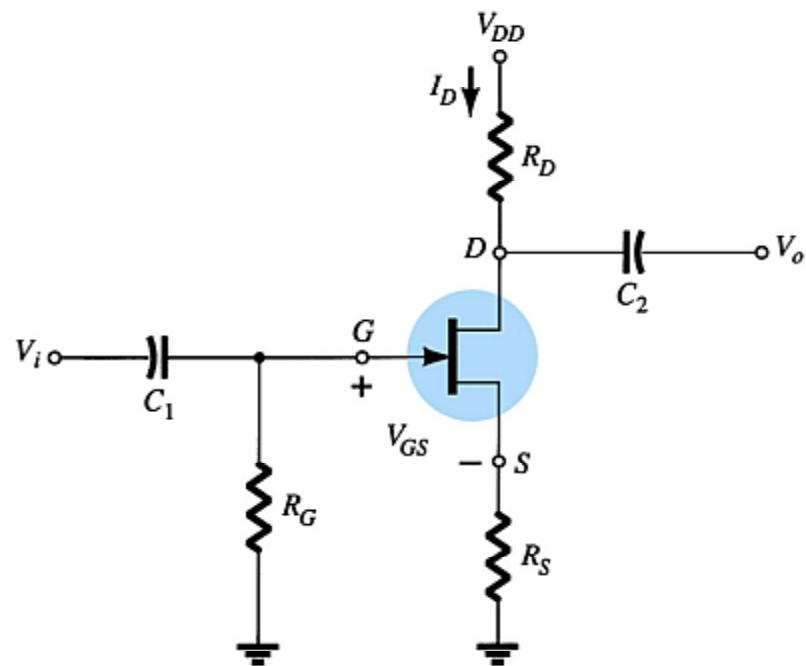
$$V_C = V_{DS}$$

$$V = V_{GS}$$

$$V_{GS} = -V_{GG}$$



# Self-Bias Configuration



# Self-Bias Calculations

For the indicated loop,  $V_{GS} = -I_D R_S$

To solve this equation:

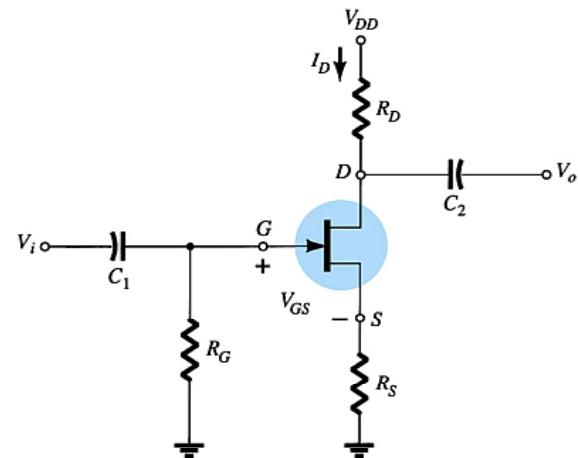
- Select an  $I_D < I_{DSS}$  and use the component value of  $R_S$  to calculate  $V_{GS}$
- Plot the point identified by  $I_D$  and  $V_{GS}$ . Draw a line from the origin of the axis to this point.
- Plot the transfer curve using  $I_{DSS}$  and  $V_P$  ( $V_P = V_{GSoff}$  in specification sheets) and a few points such as  $I_D = I_{DSS}/4$  and  $I_D = I_{DSS}/2$  etc.

The Q-point is located where the first line intersects the transfer curve. Use the value of  $I_D$  at the Q-point ( $I_{DQ}$ ) to solve for the other voltages:

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

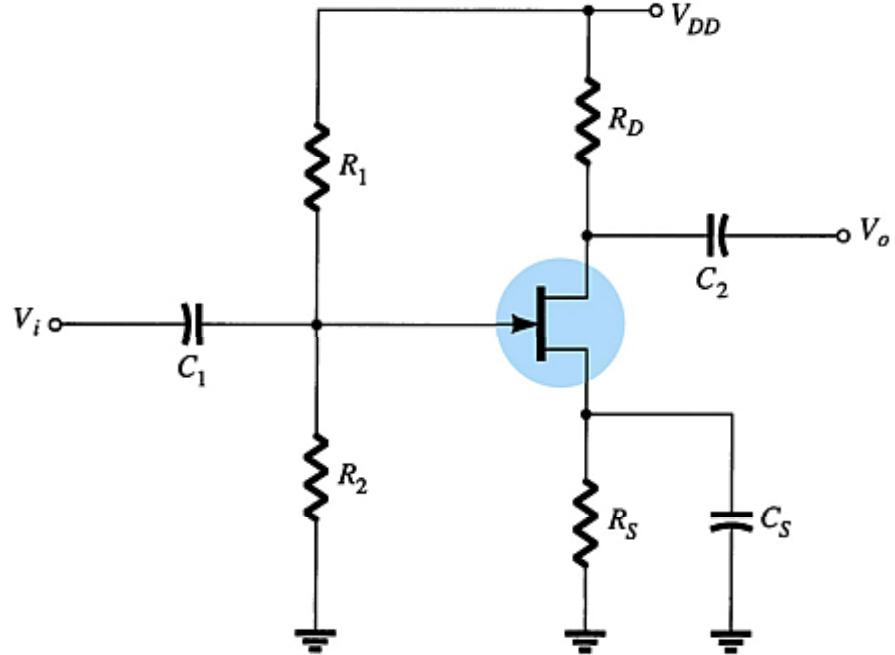
$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$



# Voltage-Divider Bias

$$I_G = 0 \text{ A}$$

$I_D$  responds to changes in  $V_{GS}$ .



# Voltage-Divider Bias Calculations

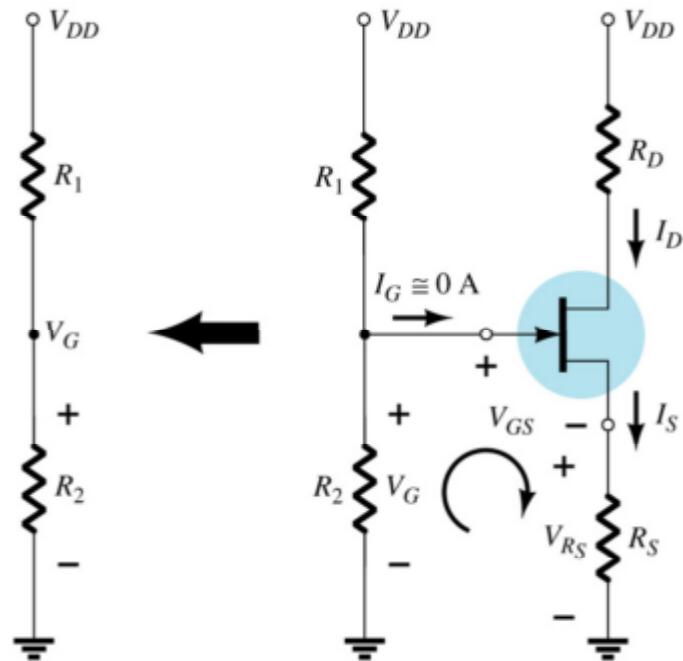
$V_G$  is equal to the voltage across divider resistor  $R_2$ :

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

The Q point is established by plotting a line that intersects the transfer curve.



# Voltage-Divider Q-point

## Step 1

Plot the line by plotting two points:

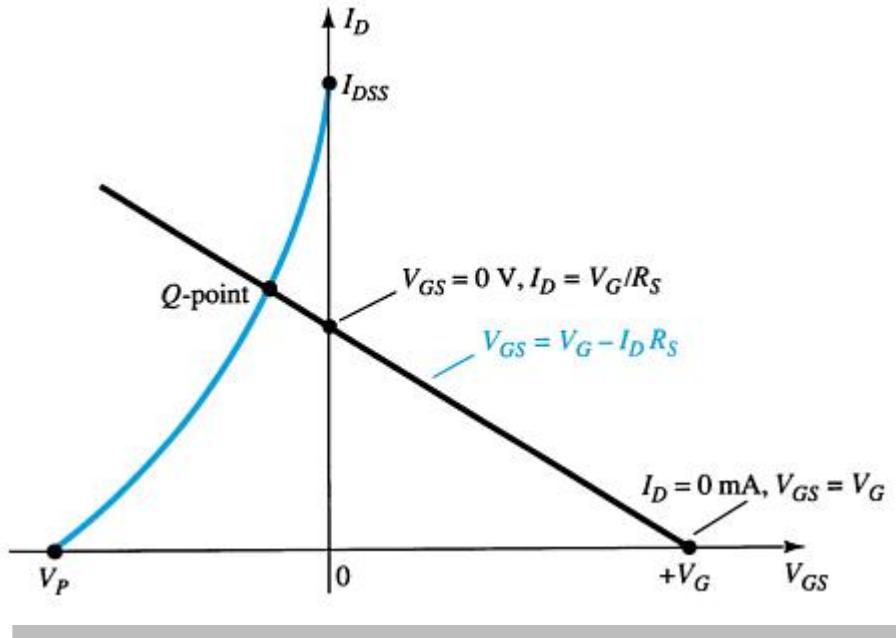
- $V_{GS} = V_G, I_D = 0 \text{ A}$
- $V_{GS} = 0 \text{ V}, I_D = V_G / R_S$

## Step 2

Plot the transfer curve by plotting  $I_{DSS}$ ,  $V_P$  and the calculated values of  $I_D$

## Step 3

The Q-point is located where the line intersects the transfer curve



# Voltage-Divider Bias Calculations

Using the value of  $I_D$  at the Q-point, solve for the other variables in the voltage-divider bias circuit:

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

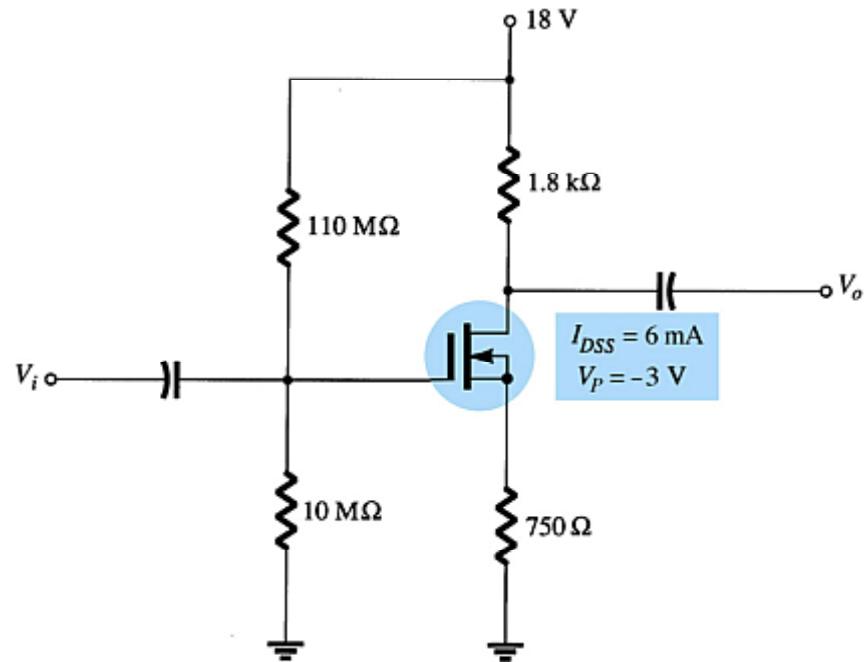
$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

# D-Type MOSFET Bias Circuits

Depletion-type MOSFET bias circuits are similar to those used to bias JFETs. The only difference is that depletion-type MOSFETs can operate with positive values of  $V_{GS}$  and with  $I_D$  values that exceed  $I_{DSS}$ .



# Self-Bias

## Step 1

Plot line for

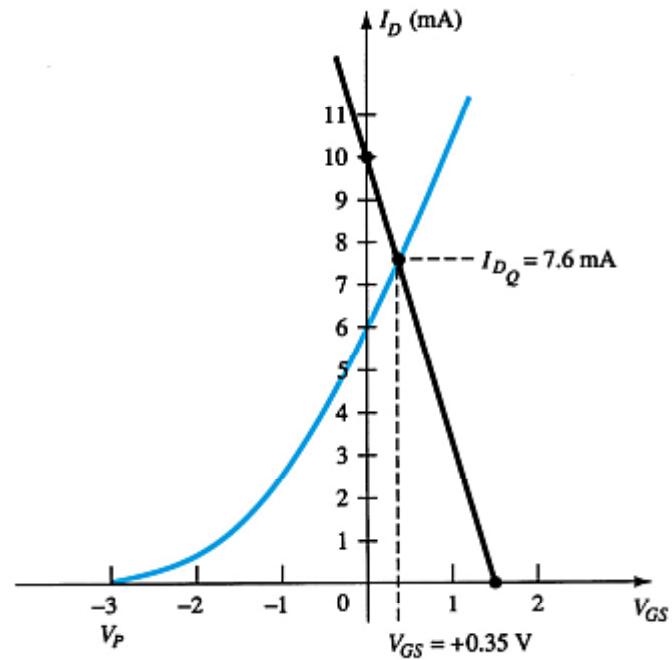
- $V_{GS} = V_G, I_D = 0 \text{ A}$
- $I_D = V_G/R_S, V_{GS} = 0 \text{ V}$

## Step 2

Plot the transfer curve using  $I_{DSS}$ ,  $V_P$  and calculated values of  $I_D$

## Step 3

The Q-point is located where the line intersects the transfer curve. Use the  $I_D$  at the Q-point to solve for the other variables in the voltage-divider bias circuit.



These are the same steps used to analyze JFET self-bias circuits.

# Voltage-Divider Bias

## Step 1

Plot the line for

- $V_{GS} = V_G, I_D = 0 \text{ A}$
- $I_D = V_G/R_S, V_{GS} = 0 \text{ V}$

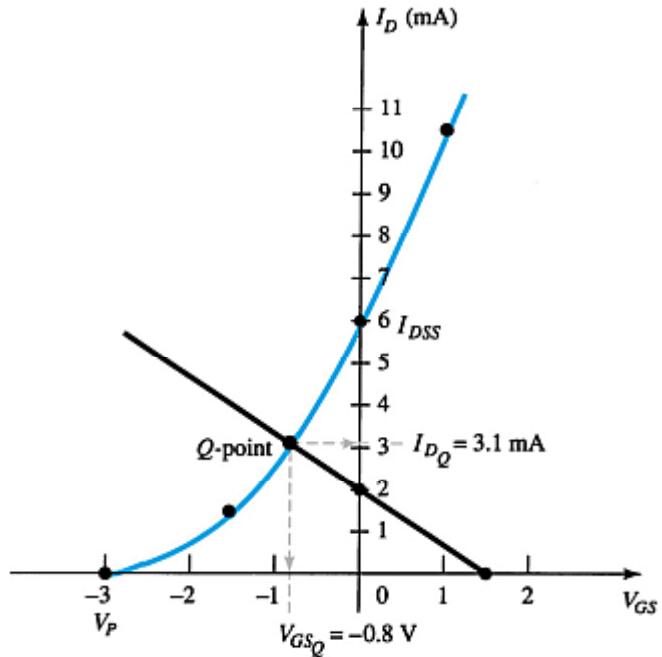
## Step 2

Plot the transfer curve using  $I_{DSS}$ ,  $V_P$  and calculated values of  $I_D$ .

## Step 3

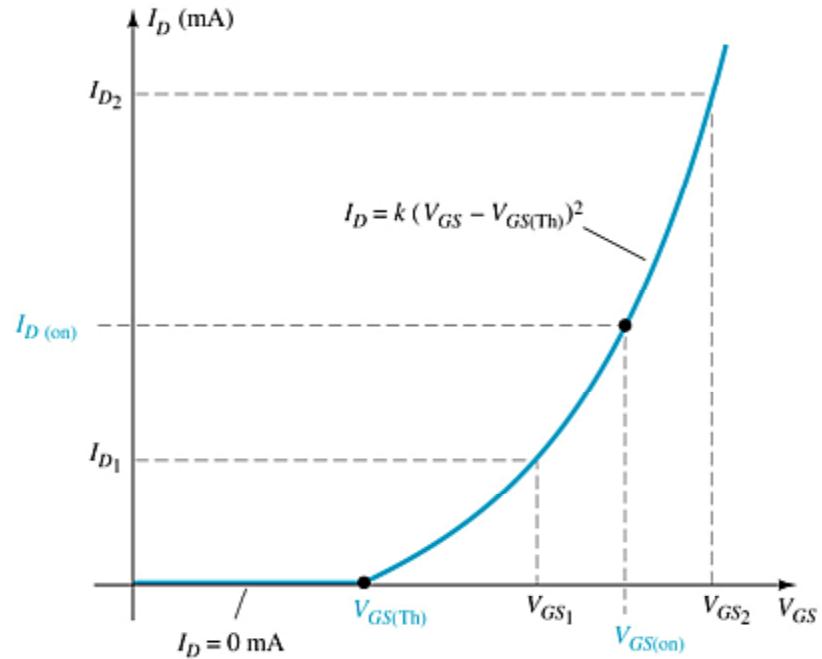
The Q-point is located where the line intersects the transfer curve is. Use the  $I_D$  at the Q-point to solve for the other variables in the voltage-divider bias circuit.

**These are the same steps used to analyze JFET voltage-divider bias circuits.**



# E-Type MOSFET Bias Circuits

The transfer characteristic for the e-type MOSFET is very different from that of a simple JFET or the d-type MOSFET.



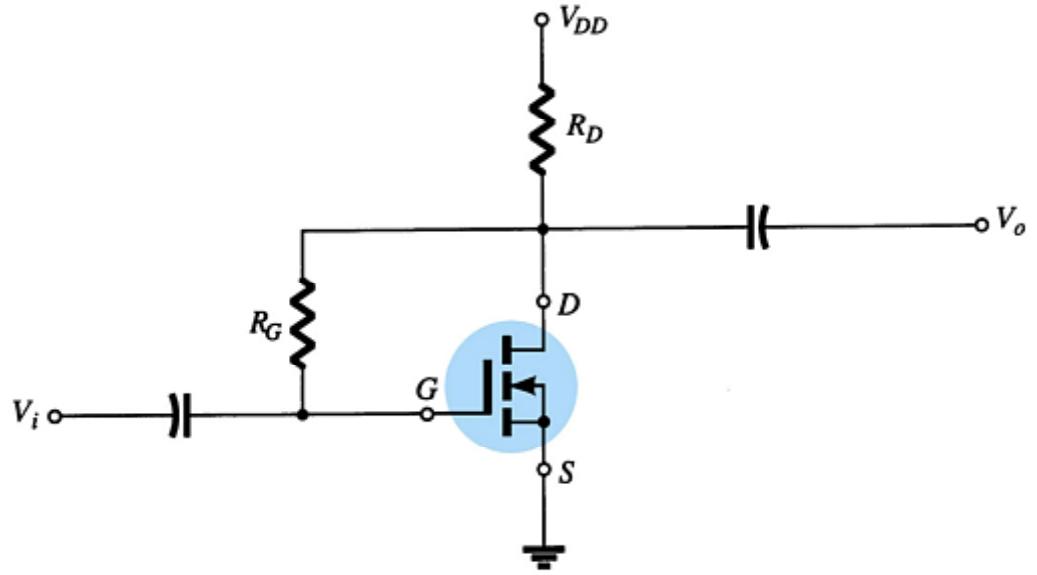
# Feedback Bias Circuit

$$I_G = 0 \text{ A}$$

$$V_{RG} = 0 \text{ V}$$

$$V_{DS} = V_{GS}$$

$$V_{GS} = V_{DD} - I_D R_D$$



# Feedback Bias Q-Point

## Step 1

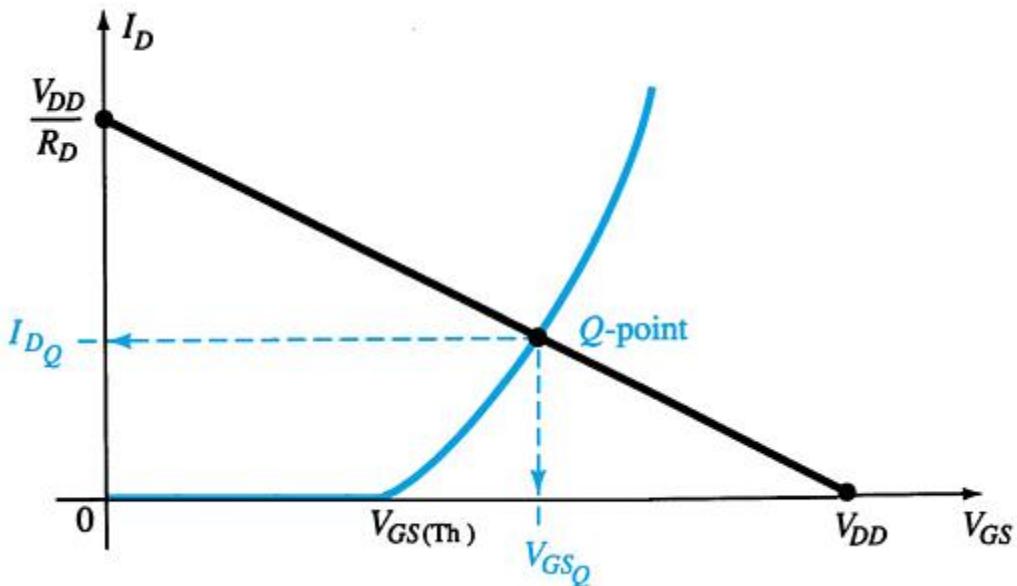
Plot the line using

- $V_{GS} = V_{DD}$ ,  $I_D = 0 \text{ A}$
- $I_D = V_{DD} / R_D$ ,  $V_{GS} = 0 \text{ V}$

## Step 2

Using values from the specification sheet, plot the transfer curve with

- $V_{GSTh}$ ,  $I_D = 0 \text{ A}$
- $V_{GS(on)}$ ,  $I_{D(on)}$



## Step 3

The Q-point is located where the line and the transfer curve intersect

## Step 4

Using the value of  $I_D$  at the Q-point, solve for the other variables in the bias circuit

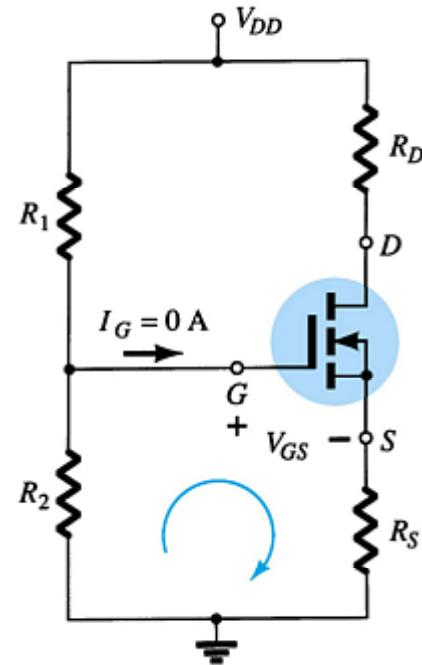
# Voltage-Divider Biasing

Plot the line and the transfer curve to find the Q-point. Use these equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$



# Voltage-Divider Bias Q-Point

## Step 1

Plot the line using

- $V_{GS} = V_G = (R_2 V_{DD}) / (R_1 + R_2)$ ,  $I_D = 0 \text{ A}$
- $I_D = V_G/R_S$ ,  $V_{GS} = 0 \text{ V}$

## Step 2

Using values from the specification sheet, plot the transfer curve with

- $V_{GSTh}$ ,  $I_D = 0 \text{ A}$
- $V_{GS(on)}$ ,  $I_{D(on)}$

## Step 3

The point where the line and the transfer curve intersect is the Q-point.

## Step 4

Using the value of  $I_D$  at the Q-point, solve for the other circuit values.

# *p*-Channel FETs

For *p*-channel FETs the same calculations and graphs are used, except that the voltage polarities and current directions are reversed.

**The graphs are mirror images of the *n*-channel graphs.**

# Applications

Voltage-controlled resistor  
JFET voltmeter  
Timer network  
Fiber optic circuitry  
MOSFET relay driver