Registers Description

NAME: trigger\_type

DESCRIPTION: determine trigger type (rise, fall, '1', '0'), two triggers can not be chosen at the same time, only one can be active and the other will be passive.

ADDRESS: "0x00"

ACCESS: R\W

RESET VALUE: 0x01

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| --- | --- |
| BIT | DESCRIPTION |
| TD[0] | ‘1’ when the chosen trigger is rise. (default trigger) |
| TD[1] | ‘1’ when the chosen trigger is fall. |
| TD[2] | ‘1’ when the chosen trigger is one. (needs to be '1' for 3 clock cycles) |
| TD[3] | ‘1’ when the chosen trigger is zero. (needs to be '0' for 3 clock cycles) |
| TD[4] | ‘1’ when the chosen trigger is a special trigger (second project). |
| TD[5..7] | NA |

NAME: trigger\_position

DESCRIPTION: determine which percent of the recorded data will appear before and after the trigger.

ADDRESS: "0x01"

ACCESS: R\W

RESET VALUE: 0x00

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| --- | --- |
| BIT | DESCRIPTION |
| TD[0..6] | The percent in decimal of the recorded data that will taken **before** the trigger rise. (default: 0- all the data will be recorded after trigger rise) |
| TD[7] | NA |

NAME: clk\_to\_start

DESCRIPTION: debugging register.

ADDRESS: "0x02"

ACCESS: R

RESET VALUE: 0x00

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| BIT | DESCRIPTION |
| TD[0..7] | Counts the number of clk cycles that passed since the system started working until trigger raised. ( if value is bigger then 127, the counter will stay on the max value- 127) |

NAME: system\_status

DESCRIPTION: system is on\off.

ADDRESS: "0x03"

ACCESS: W\R

RESET VALUE: 0x00

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| BIT | DESCRIPTION |
| TD[0] | 0-system off, we don't search for trigger rise (set at the beginning to 0 until all other registers are ready, change in second time after the trigger was found- don't continue to search for trigger rise)  1- system on, start search for trigger rise (changed by write controller after all other registers are in the right mode). |
| TD[1..7] |  |