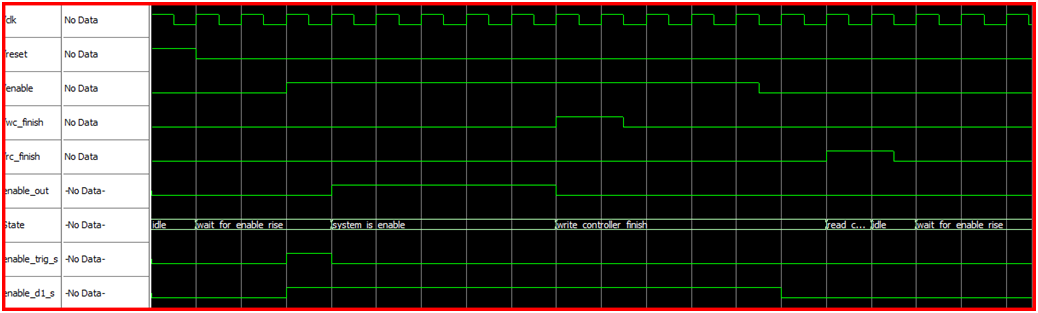
First test



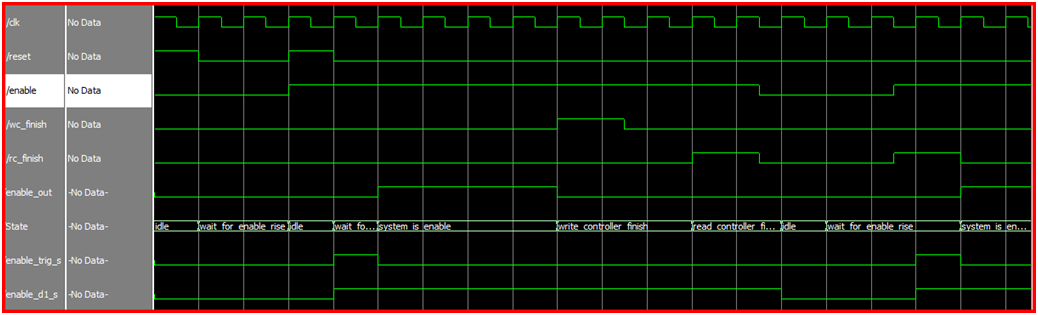
Inputs values

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Values | | | Direction | Signal name |
| 50 duty cycle, 100 period | | | in | Clk |
| 100-2000 | | 0-100 | in | Reset |
| 0 | | 1 |
| 1350-2000 | 300-1350 | 0-300 | in | Enable |
| 0 | 1 | 0 |
| 1050-2000 | 900-1050 | 0-900 | in | Wc\_finish |
| 0 | 1 | 0 |
| 1650-2000 | 1500-1650 | 0-1500 | in | Rc\_finish |
| 0 | 1 | 0 |

Description

At first reset is high and the system is in idle state, second reset is fall and the system is waiting for enable to rise, after enable rise we move into working state (system\_is\_enabl) and enable\_out rise to enable the entity, continuing until wc\_finish rise and the enable\_out is fall when we move to the next state, all due enable input is fall before we will move to the last state (before returning to idle state) just after rc\_finish signal will rise, after that (rc\_finish rise and enable fall) we will return to the initial state (idle) and from there the system will start all over.

Second test



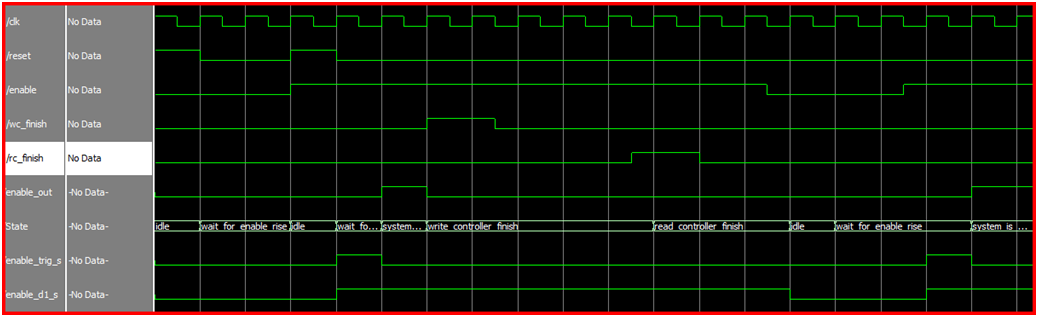
Input values

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Values | | | | | | | | | | Direction | Signal name |
| 50 duty cycle, 100 period | | | | | | | | | | in | Clk |
| 400-2000 | | 300-400 | | | 100-300 | | | 0-100 | | in | Reset |
| 0 | | 1 | | | 0 | | | 1 | |
| 1650-2000 | | 1350-1650 | | | 300-1350 | | | 0-300 | | in | Enable |
| 1 | | 0 | | | 1 | | | 0 | |
| 1050-2000 | | | 900-1050 | | | | 0-900 | | | in | Wc\_finish |
| 0 | | | 1 | | | | 0 | | |
| 1800-2000 | 1650-1800 | | | 1350-1650 | | 1200-1350 | | | 0-1200 | in | Rc\_finish |
| 0 | 1 | | | 0 | | 1 | | | 0 |

Description

We can see that after reset rise, system immediately goes to idle state. After second reset, enable signal is already rise, so after one cycle the system goes into enabled state. After rc\_finish signal rise we move into the last state (rc\_finish), but only after enable is fall, the system change into idle state and looking for new enable rise which come later.

Third test



Input values

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Values | | | | | | Direction | Signal name |
| 50 duty cycle, 100 period | | | | | | in | Clk |
| 400-2000 | 300-400 | | 100-300 | | 0-100 | in | Reset |
| 0 | 1 | | 0 | | 1 |
| 1650-2000 | 1350-1650 | | 300-1350 | | 0-300 | in | Enable |
| 1 | 0 | | 1 | | 0 |
| 750-2000 | | 600-750 | | 0-600 | | in | Wc\_finish |
| 0 | | 1 | | 0 | |
| 1050-2000 | | 1050-1200 | | 0-1050 | | in | Rc\_finish |
| 0 | | 1 | | 0 | |

Description

In this scene we check the case that rc\_finish signal rise first, and after a few cycles enable is fall, all the other characteristic is similar to the preview scene- we rise reset twice, after each time the system returns to idle state, enable rise in the second time that reset signal rise and the system goes into enable state- enable\_out is rise, when wc\_finish signal rise the output (enable\_out) is fall and we go into wc\_finish state, after rc\_finish signal rise we enter the last state and waiting to enable signal to fall, after that happened we returns to idle stste and start all over again.