G. H. Raisoni College of Engineering, Nagpur

(An Autonomous Institute)

Sixth Semester B. E. (Computer Science & Engineering / Information Technology)

Vacation Examination Summer – 2017

Language Processor

Time: 3 hrs.] **[Max. Marks: 60**

Instruction to Candidates:

1) [CO-1/CO-2/CO-3 ...] at the beginning of question/sub-question indicates the course outcome related to the question.
2) All questions carry marks as indicated.

1.			Answer the following questions with explanation:	12
	(a)	[CO-1]	Explain the term cross compiler?	
	(b)	[CO-1]	Write Machine independent code optimization.	
	(c)	[CO-2]	Write the function of lexical analyser.	
	(d)	[CO-2]	Explain shift-reduce, and reduce-reduce conflict	
	(e)	[CO-3]	List different representations of three address code.	
	(f)	[CO-6]	Explain specification of YACC.	
2.	(a)	[CO-1]	Explain all the phases of Compiler with block diagram.	5
	(b)	[CO-1]	Explain the term Backtracking with suitable example, and its disadvantages.	5
3.	(a)	[CO-2]	Consider the following grammar, and check the given grammar is SLR(1) or not? $S \longrightarrow CC$ $C \longrightarrow {}_1c_dC$	5
	(b)	[CO-2]	Construct the CLR(1) Parsing Table for the following Grammar. S -> AaAb S-> BbBa A -> ϵ B -> ϵ	5
			OR	
	(c)	[CO-2]	Write the Predictive Parsing Table for the following Grammar S -> aABb A -> c | ϵ B -> d | ϵ	5
4.	(a)	[CO-3]	Explain synthesized attribute and S-attribute & L-attribute in details.	5
	(b)	[CO-3]	Write SDTS, there address code for the following programming construct____ p < q OR r > s AND t<u	5
5.	(a)	[CO-4]	Explain Loop unrolling and Loop Jamming with example.	5
	(b)	[CO-6]	Explain one of the recent trends in language Processor.	5
6.			Write a short note on **(Any Two)**	8
	(a)	[CO-4]	Various approaches to Symbol Table Organization	
	(b)	[CO-5]	Elimination of Induction Variable	
	(c)	[CO-6]	Peephole Optimization	

G. H. Raisoni College of Engineering, Nagpur

(An Autonomous Institute)

Sixth Semester B. E. (Computer Science and Engineering)

Vacation Examination Summer – 2017

Parallel and Distributed Computing

Time: 03 hrs.] [Max. Marks: 60

Instructions to Candidate:

1) All questions carry marks as indicated.
2) Assume suitable data wherever necessary.
3) Due credit will be given to neatness and adequate dimensions..

1. (a) What will be the output upon executing below OpenMP source file? Justify your answer. 2

```
void test(int val)
{  #pragma omp parallel if (val)
   if (omp_in_parallel()) {
      #pragma omp single
      printf_s("val = %d, parallelized with %d threads\n", val, omp_get_num_threads());
   }
   else {
      printf_s("val = %d, serialized\n", val);
   }
}
int main( )
{  omp_set_num_threads(2);
   test(0);
   test(2);
}
```

(b) Suppose that the following MPI source file is compiled and executed with "mpirun -np 5 <executable>". What will the o/p? Why? 2

```
int main(int argc, char* argv[])
{
int my_rank;
int p;
MPI_Init(&argc, &argv);
MPI_Comm_rank(MPI_COMM_WORLD, &my_rank);
MPI_Comm_size(MPI_COMM_WORLD, &p);
printf("Hello world, I am process %d of %d!\n", my_rank, p);
MPI_Finalize();
}
```

(c) Indicate whether each of the following statements is true or false with proper justification: 2

1. In a MIMD computer, all processors must execute the same instruction at the same time synchronously.
2. As far as scalability is concerned, multicomputers with distributed memory are more scalable than shared-memory multiprocessors.

(d) Write miss: A partial cache line write is handled as a read miss (if necessary to fetch the unwritten portion of the cache line) followed by a write hit. This leaves all other caches in the Invalid state, and the current cache in the Reserved state follows which of the following snooping protocol: 2

a)Write-once b) Write update and Partial Write Through
c) Write Invalidate and Write Through d) Write Invalidate and Write Back

(e) The VLIW architecture follows _____ approach to achieve parallelism. 2

a) MISD b) SISD
c) SIMD d) MIMD

(f) What will be the output of the following OpenMP source code? Justify. 2

```
int main() {
  #pragma omp parallel num_threads(2)
  {
    int var;
    #pragma omp single
        { printf("Read input\n");
          scanf("%d", &var);
        }
```

```
    printf("compute results: %d\n", ++var);
  #pragma omp single
    printf("Write output %d\n", var);
} }
```

2. Solve any **TWO**

(a) State the advantages and disadvantages of message passing architectures and compare them with those found in shared memory architectures. 6

(b) A 80 MHz processor was supposed to execute 10000 instructions with following instruction mix and CPI needed for each instruction. 6

Instruction type	CPI	Instruction count
Integer arithmetic	3	50%
Data transfer	4	16%
Floating point	8	14%
Control transfer	6	20%

Determine the effective **CPI**, **MIPS** rate and execution time (**T**).

(c) Explain clearly what each one of the following MPI commands does. You need to specify the input and output parameters and what they store before and after the call. 6

i) MPI_Comm_rank (comm, rank)

ii) MPI_Bcast (buffer, count, datatype, root, comm)

iii) MPI_IRecv (buf,count,datatype,source,tag,comm, request)

iv) MPI_Allgather (sendbuf, sendcount, sendtype, recvbuf, recvcount, recvtype, comm)

v) MPI_Scatter (sendbuf, sendcnt, sendtype, recvbuf, recvcnt, recvtype, root, comm)

vi) MPI_Reduce (sendbuf, recvbuf, count, datatype, op, root, comm)

3. (a) Why there is a need to define the data types during the send of a message? Discuss the basic data types supported by MPI. 6

(b) Write an OpenMP program segment that shows parallel computation for sum of the products of two arrays. Display the final scalar sum. 6

4. Solve any **TWO**

(a) Perform a data dependence analysis on the following program fragment, 7
a) Show the dependence graph among the statements (Apply Bernstein's Rules),
b) Indicate the pair of instructions with RAW, WAR, and WAW dependence,

S1:	Add R_1, R_2, R_3	$R_1, \leftarrow R_2 + R_3$
S2:	Add R_4, R_1, R_4	$R_4, \leftarrow R_1 + R_4$
S3:	Add R_3, R_1, R_2	$R_3, \leftarrow R_1 + R_2$
S4:	Add R_1, R_1, R_4	$R_1, \leftarrow R_1 + R_4$

(b) For following set of Instructions, Implement a Write Once Protocol and show the listed updates: 7

- Requests from processors, bus requests/responses from snooper.
- Updated state of block, response with data on Processor Cache and Shared Memory.
- Assume initial cache blocks are empty; block A3 and A4 maps to the same cache block.

P1: Read A3
P1: Write 50 to A3
P2: Read A4
P2: Write 30 to A4
P2: Write 20 to A4

(c) Illustrates a matrix multiplication program requiring 8 multiplications and 7 additions for Static Multiprocessor Scheduling. 7

5. (a) Write a C program segment that sets the number of threads equal to the number of processors that are available for computing the addition of two arrays and store it into the third array. Display the elements of resultant array and the thread ID of the thread which has computed the respective element. 5

(b) Write an OpenMP program to demonstrate the use of: 5
PARALLEL for DIRECTIVE and CLAUSES: private, shared and schedule

G. H. Raisoni College of Engineering, Nagpur

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Fourth Term / Sixth Semester B. E. (Computer Science & Engineering)

Vacation Examination Summer – 2017

Design and Analysis of Algorithm

Time: 3 hrs.] **[Max. Marks: 60**

Instruction to Candidates:

1) [CO-1/CO-2/CO-3 ...] at the beginning of question/sub-question indicates the course outcome related to the question.
2) All questions carry marks as indicated.
3) Illustrate your answer wherever necessary with the help of neat sketches.

1.	(a)	[CO-1]	What are the characteristics of an algorithm?	2
	(b)	[CO-2]	Differentiate Time complexity from Space complexity.	2
	(c)	[CO-2]	Find the number of comparisons made by the sequential search in the worst case and best case.	2
	(d)	[CO-3]	Is insertion sort better than the merge sort?	2
	(e)	[CO-3]	Write the difference between the Greedy method and Dynamic programming.	2
	(f)	[CO-4]	What are the requirements that are needed for performing Backtracking?	2
2.	(a)	[CO-1]	How aggregate and accounting method in amortized analysis works? Explain with suitable example.	4
	(b)	[CO-1]	Explain divide and conquer approach and discuss it with the Quick sort. Also write the recurrence relation for quick sort.	4
			OR	
	(b)	[CO-1]	Create Max-Heap and Min Heap for the following sequence {23,17,14,7,13,10,1,5,6,12}	4
3.	(a)	[CO-2]	Write an algorithm for Optimal parenthesization of matrix chain multiplication and find the optimal solution for matrices A=5 X 10,B=10 X 13 and C=13 X 4	5
	(b)	[CO-2]	Find longest common sequence for X=<A,B,C,B,D,A,B> AND Y=< B,D,C,A,B,A>	5
4.	(a)	[CO-3]	Write a greedy algorithm for sequencing unit time jobs with deadlines and profits. Using this algorithm, find the optimal solutions when n=5,(p1,p2,p3,p4,p5,p6,p7)=(3,5,20,18,1,6,30)) and (d1,d2,d3,d4,d5,d6,d7) = (1,3,4,3,2,1,2)	5
	(b)	[CO-3]	Why are Huffman codes needed? Explain construction of Huffman codes using Huffman's algorithm	5
5.	(a)	[CO-4]	Differentiate explicit constraint and implicit constraint	5
	(b)	[CO-5]	Using backtracking enumerate how can you solve the following problems. 1) 8 queen problem 2) Hamiltonian cycle problem.	5
6.	(a)	[CO-6]	What are the two classes of non polynomial time problems? Explain each class in detail with suitable Example	5
	(b)	[CO-1]	Discuss various methods of sorting network with suitable examples	3
	(c)	[CO-2]	Determine the complexity of following recursive function	2

```
Algorithm rsum (a, n)
{
        if (n <= 0) then
        return 0;
        else
        return (rsum(a, n–1) + a[n]);
}
```

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Fourth Term / Sixth Semester B. E. (Computer Science & Engineering)

Vacation Examination Summer – 2017

Embedded Systems

Time: 3 hrs.] **[Max. Marks: 60**

Instruction to Candidates:

1) [CO-1/CO-2/CO-3 ...] at the beginning of question/sub-question indicates the course outcome related to the question.
2) All questions carry marks as indicated.
3) Assume suitable data wherever necessary.
4) Due credit will be given to neatness and adequate dimensions.
5) Illustrate your answer wherever necessary with the help of neat sketches.
6) Use of non-programmable calculator is permitted.

1.			Solve with justification	
	(a)	[CO-1]	Explain cross compiler in embedded systems.	2
	(b)	[CO-3]	Deadline-driven constraints so called i) Reality-time constraints ii) Real-time constraints iii) Real-data constraints iv) None of above	2
	(c)	[CO-3]	Wider frequency makes it more difficult to block and is called i) Trellis codes ii) Spread spectrum iii) NMA data iv) Cellular telephony	2
	(d)	[CO-3]	Networks can be created out of thin air as well as out of copper and glass, creating i) Wireless networks ii) Wired networks iii) Wifi iv) Both i. and ii.	2
	(e)	[CO-2]	Processor must accept and process frame before next frame arrives, typically called i) Hard real-time systems ii) Real-time constraints iii) Real-data constraints iv) Soft real-time systems	2
	(f)	[CO-2]	Two partitions must be insulated to prevent operations on one half from affecting other, such floating-point operations are called i) Single-instruction operation ii) Vector operation iii) Paired single operations iv) Fetch operation	2
2.	(a)	[CO-2]	Write & explain assembly level program to demonstrate direct addressing mode in 8051.	4
	(b)	[CO-2]	List down and explain TCON function register in detail.	4
	(c)	[CO-2]	Explain program Status word with its format in detail.	4
3.	(a)	[CO-3]	Explain in detail serial communication Bus mostly used for automotive products.	6
	(b)	[CO-3]	Illustrate the bus mechanism with which ICs are interconnected with each other	6
4.	(a)	[CO-4]	Describe PIC Architecture with detail Diagram	6
	(b)	[CO-4]	Compare Stack,, Function and Interrupt service routine	6
5.	(a)	[CO-5]	Describe THUMB in ARM compare with ARM instructions	6
	(b)		What do you mean by Pipeline architecture, explain in detail	6
			OR	
	(b)	[CO-5]	Write down the program to generate square wave of 10ms on port pin P01 continuously with 50%duty cycle	6