

Appendix A

MIL-STD-275E: Printed Wiring for Electronic Equipment

This is an important and commonly referenced industry standard. Many companies base their own internal design standards on this document. All incoming artwork and blueprints should be inspected against the criteria established here. The document is divided into six sections plus an appendix. The sections are described below. During the discussion of each section, references are made to various tables and paragraphs. If the specified table or paragraph is not reproduced in the discussion, it is found in the military standard itself.

SECTION 1. SCOPE

The scope and purpose of this standard are explained by paragraph 1.1 and 1.2 of MIL-STD-275E. This standard establishes design requirements governing rigid printed wiring boards. It establishes three classifications of boards:

- Class 1—single-sided boards
- Class 2—double-sided boards
- Class 3—multilayer boards

Also covered are design standards for printed wiring assemblies (using the above types of boards) and design considerations for mounting parts and assemblies thereon. This standard assumes that all of the above boards will be conformally coated, in accordance with MIL-I-46058.

SECTION 2. REFERENCED DOCUMENTS

There is a tabulation of documents published by the federal government and branches of the military, American National Standards Institute (ANSI), American Society for Testing and Materials (ASTM), Institute of Electrical and Electronics Engineers (IEEE), and the Institute for Interconnecting and Packaging

Electronic Circuits (IPC). These documents are referenced throughout MIL-STD-275E and other specifications and standards. They form part of the text. Where they conflict with this standard, the provisions of MIL-STD-275E take precedence.

The documents referenced cover such items as materials, drawings, film preparation, plating, testing, definitions, packaging, marking, and other important considerations. Inclusion of references to these documents allows for greater clarity and brevity in this standard or any other standard which makes reference to them.

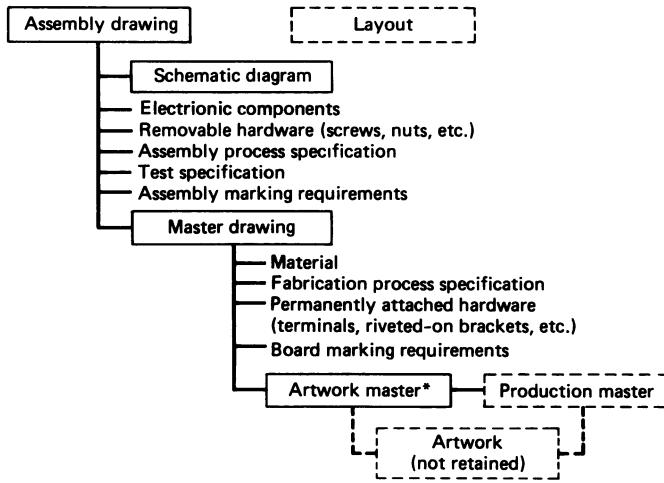
SECTION 3. DEFINITIONS

This section simply states that "The terms and definitions used herein shall be in accordance with this standard and IPC-T-50."

SECTION 4. GENERAL REQUIREMENTS

This section establishes a number of requirements which all planners, designers, and quality assurance people must be aware of:

1. Quality conformance test coupons must be included in the design and layout of the printed circuit board. The requirements of these coupons are listed in Section 5.9 of this standard.
2. The contents of the entire set of drawings for the printed circuit boards and assemblies are called out. Figure A-1 shows what must be covered by the set of drawings and indicates their relationships.



*Includes circuit and silk screen masters.

Fig. A-1 Block diagram depicting typical printed-wiring drawing relationships.

3. Component reference designations must meet the requirements of IEEE-STD-200.
4. Procedures to be followed by designers who are requesting deviations from the requirements of this standard are listed.
5. Items which must be covered by the master drawing are listed in paragraph 4.3 (See Table A-1). There is a list of 22 items, which are also important to the printed circuit manufacturer, since he/she cannot properly plan for manufacturing without knowing what these requirements are.
6. Hole location tolerances for various types of holes are discussed, such as plated-through holes, tooling holes, mounting holes, windows, access holes, via holes, and component holes.
7. Processing allowances are discussed and defined. Table A-2 is a composite of design features and their manufacturability. Manufacturability is expressed as follows:
 - a. Preferred—easiest to conform to, most cost effective.
 - b. Standard—greater difficulty of conformance.
 - c. Reduced producibility—not likely to be attained without greater effort, care, and/or expense.

Table A-2 is such an import design summary that it is reproduced below in full. All manufacturing planners, designers, and quality assurance people should be familiar with its content and refer to it as needed. It is a mistake to ignore the contents of this table.

8. The use of a datum point is established. Two mutually perpendicular lines are drawn through a single hole. All dimensions for holes, slots, hardware, board outlines, etc. are referenced from these datum lines. The use of these datum lines makes it possible to establish acceptable tolerances.
9. Assembly drawing requirements are listed in paragraph 4.4. This book is primarily concerned with planning for printed circuit manufacturing. However, there is frequently some amount of assembly which a board manufacturer will perform. For this reason, paragraph 4.4 is reproduced (see Table A-3).
10. Production masters, film for each layer needed to build the printed circuit, shall be prepared on .0075-inch, dimensionally stable film according to the requirements of MIL-D-8510, type II, L-F-film.

SECTION 5. CONDUCTOR PATTERN

This section covers the design requirements for all conductive patterns, dielectric spacing, material thickness tolerance, and other physical features. This section is important; all planning, design, and quality assurance people must have an understanding of the information covered here. Paragraph 5.1.1 establishes

Table A-1 Required Information for the Master Drawing

The master drawing shall be prepared in accordance with DOD-STD-100; shall include all appropriate detail board requirements (see Section 5), and the following:

- a. The type, size, and shape of the printed wiring board.
- b. The size, location, and tolerance of all holes therein.
- c. Etchback allowances, when required or permitted.
- d. Location of traceability marking.
- e. Dielectric separation between layers.
- f. Shape and arrangement of both conductors and nonconductor patterns defined on each layer of the printed wiring board. Copies of the production masters or copies of the artwork may be used to define these patterns.
- g. Separate views of each conductor layer.
- h. Any and all pattern features not controlled by the hole sizes and locations shall be dimensioned either specifically or by reference to the grid system (see n).
- i. Processing allowances that were used in the design of the printed wiring board (see 5.1.1, 5.1.4, 5.2.1.2, 5.2.2, and 5.2.2.6).
- j. All notes either included on the first sheet(s) of the master drawing or by specifying the location of the notes on the first sheet.
- k. Conductor layers numbered consecutively, starting with the component side as layer 1. If there are no conductors or lands on the component side, the next layer shall be layer 1. For assemblies with components on both sides, the most densely populated side shall be layer 1.
- l. Identification marking (see 5.8).
- m. Size, shape, and location of reference designation and legend markings, if required (see h).
- n. A modular grid system to identify all holes, test points, lands, and overall board dimensions with modular units of length of 0.100, 0.050, 0.025, or other multiples of 0.005 inch in that order of preference. For designs where the majority component locations are metric based (SI), the basic modular units of length shall be 2.0, 1.0, 0.5, or other multiples of 0.1 mm in that order of preference. The grid system shall be applied in the X and Y axes of the Cartesian coordinates. The grid shall not be reproduced on the master drawing; but may be indicated using grid scales or X, Y control dimensions.
- o. Dimensions for critical pattern features which may effect circuit performance because of distributed inductance or capacitance effects within the tolerance required for circuit performance.
- p. All terms used on the master drawing shall be in conformance with the definitions of ANSI/IPC-T-50 or ANSI Y14.5 (see 3.1 and 2.2).
- q. Deviations to this standard (see 4.2.2).
- r. Minimum line width and spacing of the finished printed-wiring board.
- s. Maximum rated voltage (maximum voltage between the two nonconnected adjacent conductors with the greatest potential difference) for type 3 boards only.
- t. Plating and coating material(s) and thickness(es).
- u. Identification of test points required by the design (see 5.1.8).
- v. Applicable fabrication specification with date(s), revision letter, and amendment number.

an important concept: the need to compensate artwork for processing tolerances so that the finished product may come as close as possible to nominal design requirements. Table A-2 summarizes much of what is discussed in this section.

Table A-2 Composite Board Design Guidance

	<i>Preferred</i>	<i>Standard</i>	<i>Reduced Productivity</i>
Number of conductor layers (maximum ¹)	6	12	20
Thickness of total board (maximum) (inch)	.100 (.254)	.150 (.381)	.200 (.508)
Board thickness tolerance	$\pm 10\%$ of above nominal or .0007 (.18), whichever is greater		
Thickness of dielectric (minimum)	.008 (.20)	.006 (.15)	.004 (.10)
Minimum conductor width (or Figure 4 value, whichever is greater)			
Internal	.015 (.38)	.010 (.25)	.004 (.10)
External	.020 (.51)	.015 (.38)	.004 (.10)
Conductor width tolerance			
Unplated 2 oz/ft ²	+ .004 (.10) - .006 (.15)	+ .002 (.05) - .005 (.13)	+ .001 (.025) - .003 (.08)
Unplated 1 oz/ft ²	+ .002 (.05) - .003 (.08)	+ .001 (.025) - .002 (.05)	+ .001 (.025) - .001 (.025)
Protective plated (metallic etch resist over 2 oz/ft ² copper)	+ .008 (.20) - .006 (.15)	+ .004 (.10) - .004 (.10)	+ .002 (.05) - .002 (.05)
Minimum conductor spacing (or Table I, whichever is greater)	.020 (.51)	.010 (.25)	.005 (.013)
Annular ring plated-through hole (minimum)			
Internal	.008 (.20)	.005 (.13)	.002 (.05)
External	.010 (.25)	.008 (.20)	.005 (.13) ²
Feature location tolerance (master pattern, material movement, and registration (rtp))			
Longest board dimension 12 inches or less	.008 (.20)	.007 (.18)	.006 (.15)
Longest board dimension over 12 inches	.010 (.25)	.009 (.23)	.008 (.20)
Master pattern accuracy (rtp)			
Longest board dimension 12 inches or less	.004 (.10)	.003 (.08)	.002 (.05)
Longest board dimension over 12 inches	.005 (.13)	.004 (.10)	.003 (.08)
Feature size tolerance	$\pm .003 (.08)$	$\pm .002 (.05)$	$\pm .001 (.025)$
Board thickness to plated hole diameter (maximum)	3:1	4:1	5:1
Hole location tolerance (rtp)			
Longest board dimension 12 inches or less	.005 (.13)	.003 (.08)	.002 (.05) ³
Longest board dimension over 12 inches	.007 (.18)	.005 (.13)	.003 (.08) ³
Unplated hole diameter tolerance (unilateral)			
Up to 0.032 (.81)	.004 (.10)	.003 (.08)	.002 (.05)
0.033 (.84)-0.063 (1.61)	.006 (.15)	.004 (.10)	.002 (.05)
0.064 (1.63)-0.188 (4.77)	.008 (.20)	.006 (.15)	.004 (.10)
Plated hole diameter tolerance (unilateral) for minimum hole diameter maximum board thickness ratios greater than 1:4 add 0.004 (0.01)			
.015 (.38)-0.030 (.76)	.008 (.20)	.005 (.13)	.004 (.10)
.031 (.79)-0.061 (1.56)	.010 (.25)	.006 (.15)	.004 (.10)
.062 (1.59)-0.186 (4.75)	.012 (.31)	.008 (.20)	.006 (.15)
Conduction to edge of board (minimum)			
Internal layer	.100 (.254)	.050 (.127)	.025 (.064)
External layer	.100 (.254)	.100 (.254)	.100 (.254)

¹ The number of conductor layers should be the optimum for the required board function and good producibility

² See 5.2.3

³ To be used only in extreme situations warranted by the application

NOTE: Unless otherwise specified, all dimensions and tolerances are in inches, data in parentheses () is expressed in millimeters

Other tables and figures referred to herein are found in MIL-STD-275E. The reader is advised to obtain copies of this, and other standards, listed in the appendixes

Table A-3 Required Information for the Printed Wire Assembly Drawing

The printed wiring assembly drawing shall cover printed wiring on which separately manufactured parts have been added. The printed wiring assembly drawing shall be in accordance with DOD-STD-100 and should include at least the following:

- a. Parts and material list.
- b. Component mounting and installation requirements.
- c. Cleanliness requirements per MIL-P-28809.
- d. Location and identification of materials or components (or both).
- e. Component orientation and polarity.
- f. Applicable ordering data from MIL-P-28809.
- g. Structural details when required for support and rigidity.
- h. Electrical test requirements.
- i. Marking requirements.
- j. Electrostatic discharge protection requirements.
- k. Special solder plug requirements.
- l. Eyelets and terminals.
- m. Lead forming requirements.
- n. Type of conformal coating and masking.
- o. Solder mask.
- p. Traceability.

The printed wiring assembly drawing shall include the definition of any conditions considered in the design where the manufacturing variation between the end product and the assembly configuration plays a role in the producibility or performance of the printed wiring assemblies.

Design Features

1. Line widths on master artwork must be compensated for processing allowances to meet or maintain conductor width on the master drawing.
2. Conductors which change direction with less than 90 degree angles shall have the external corner of the bend rounded.
3. Conductor lengths should be held to a minimum. Conductors running along the X axis, the Y axis, and at 45 degrees to these axes are preferred to facilitate computer-aided designing.
4. Conductor spacings shall be as large as allowable. Minimum spacing shall be kept in accordance with Table A-1 of MIL-STD-275E. This table references conductor spacing for internal and external layers as a function of voltage.
5. Minimum spacing between conductors and the board edges shall be as listed in Table A-I of this specification plus .015 inch.
6. Large conductive areas and the problems they cause are discussed. The layout of large metal areas is specified, along with the use of nonfunctional metal areas to balance the construction.

7. Interfacial connections are to be made by the plated-through hole, not by eyelets or other types of hardware.
8. Holes are to be designed to facilitate solder wicking into holes around component leads and to provide solder plugs of holes without leads. Paragraph 5.1.7.1 has an extensive discussion of the requirements for forming solder fillets and solder plugs or plugging the holes with solder mask.
9. The presence of test points, when required by the design, is discussed. These shall be plated-through holes.
10. The minimum annular ring (land area around a plated or nonplated hole) is discussed, as well as the method used to calculate it (paragraph 5.2.1.2).
11. Minimum land area for surface mounted components are discussed.
12. Eyelets are specifically forbidden in new designs without approval of the federal government (paragraph 5.3.3).
13. Drilling directly into internal power and ground planes is forbidden, without some kind of thermal relief (see Figure 14 in the Appendix, not reproduced here).
14. All hole and land areas shall be located on a grid intersection specified on the master drawing. It is permissible to have holes in a group which are off this master grid pattern, provided at least one hole in that group is on the grid and serves as a datum for the other holes in the grouping.
15. Specifications for eyelets and other forms of hardware are discussed (see paragraphs 5.4 to 5.4.3).
16. All metal-clad laminates shall be per MIL-P-13949.
17. Minimum laminate thickness is discussed in paragraph 5.6.1.1.
18. Prepreg bonding materials shall be per MIL-P-13949. GE and GF prepreg (epoxy/fiberglass) shall not be used with GI (polyimide) prepreg.
19. Finished conductors must have at least 1 oz of thickness (.0012 inch) and must be made from at least $\frac{1}{2}$ oz copper foil plated to at least 1 oz finish.
20. Plating requirements (paragraph 5.6.4)
 - a. All external conductive patterns shall be covered with solder, unless covered by solder mask, a heat sink, or other approved plating.
 - b. When other metal plating is approved, no copper shall be exposed as the interface of the two metals.
 - c. No other metals shall be plated over tin-lead or tin.
 - d. Unless otherwise specified on the master drawing, through-hole and surface metal thicknesses shall be per paragraphs 5.6.4 through 5.6.4.6.
21. Solder mask coating shall be per class 3 of IPC-SM-840. It shall not be used unless specified on the master drawing. The use of chemical treatments to improve solder mask adhesion is specifically allowed per paragraph 20.5 of the Appendix.
22. Board thickness shall include plated metals and solder mask coating.
23. Multilayer printed circuits shall have a minimum dielectric spacing of .0035

inch between conductive layers. There must be at least two sheets of prepreg.

24. Maximum bow and twist shall be 1.5%.

SECTION 6. DETAIL PART MOUNTING REQUIREMENTS

This section presents in-depth descriptions of design parameters which affect assembly. The information here is of great importance to printed circuit designers and to quality assurance people involved with design approval and assembly. It will not be covered in depth here because this book is primarily concerned with manufacturing the bare printed circuit board once it has been designed and artwork generated.

SECTION 10. APPENDIX

The purpose of the Appendix is to provide further guidance to the designer of printed wiring boards. Planners and quality assurance people should be familiar with much of the information presented here. The Appendix contains the following:

1. The Table A-2 composite design summary (reproduced in this chapter as well).
2. Design and layout of quality conformance test coupons. These coupons are required to be present on the working film of the printed circuit board manufacturer.
3. A block diagram depicting the relationship of all drawings for printed circuit boards.
4. A diagram of how a grid pattern is used to define pattern requirements.
5. Graphs to be used for determining conductor widths and copper foil thicknesses as a function of amperes and the resulting temperature of the conductor.
6. Land pattern requirements for surface-mounted chip carriers.
7. Pad shapes and minimum annular ring measuring requirements.
8. Where to measure minimum dielectric spacing between conductive layers.
9. Where to locate quality conformance coupons on the printed circuit panel as a function of the number of boards on the panel.

Appendix B

IPC-D-300G: Printed Board Dimensions and Tolerances

This is an invaluable document for anyone who needs to understand some of the most basic information presented on blueprints: dimensions and tolerances. Those who must understand the information presented here include designers, quality assurance people, and manufacturing planners. Measurements are presented in metric units, together with U.S. conversions to inches.

The information presented in this standard is based on industry capability, which, of course, must not be disregarded. This document contains five sections, including the Appendix: (1) Scope, (2) Applicable Documents, (3) Requirements, (4) Summarization, (50) Appendix.

SECTION 1.0 SCOPE

The purpose of this section is expressed in paragraph 1.1 as follows: “The purpose of this standard is to establish rules, principles, and methods of dimensioning and tolerancing used to define the end product requirements of a printed board on a master drawing.” It establishes three classes (A, B, and C) of progressively more difficult requirements. These classes should not be confused with classes 1, 2, and 3 of end item use, which are listed in other IPC standards and specifications. Selection of dimensional classes A, B, and C should be determined by the minimum need for precision, whereas selection of classes 1, 2, and 3 should be based on the purpose of the end product: consumer, general industrial, or high reliability.

IPC-D-300G provides for two types of dimensioning systems:

Type 1—Nominal dimensioning (tolerances apply to dimensions).

Type 2—Basic dimensioning (tolerances are expressed as an allowable variation from the basic dimensions specified).

Paragraph 1.5 lists numerous terms and definitions which have precise technical meaning.

SECTION 2.0 APPLICABLE DOCUMENTS

This section lists other documents which contain information necessary to understand fully the scope of IPC-D-300G, since IPC-D-300G is also referenced in other documents.

SECTION 3.0 REQUIREMENTS

1. The main features that are typically dimensioned and toleranced are listed below, from paragraph 3.1. These are:
 - a. Minimum conductor width
 - b. Minimum conductor spacing
 - c. Minimum annular ring
 - d. Lands
 - e. Plated-through holes
 - f. Nonplated-through holes
 - g. Printed board length, width, and thickness
 - h. Connectors
2. Paragraph 3.1.1 discusses the use of data and provides diagrams of several examples.
3. All holes, lands, and features of printed circuits shall be dimensioned by the use of a grid system, except when necessary for mating with parts that are not on a grid system. Preferred grids are .100, .050, and .025 inch.
4. The annular ring is defined as the minimum distance from the edge of a functional land to the edge of the drilled hole (single-sided boards and inner layer of multilayer boards) or to the inner edge of a plated-through hole for all others. Table B-1 lists the minimum requirement of the annular ring for classes A, B, and C.

Table B-1 Annual Rings (Minimum)

<i>Annular Ring</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Internal supported	.15 [.006]	.05 [.002]	.03 [.001]
External supported	.25 [.010]	.15 [.006]	.05 [.002]
External unsupported	.40 [.016]	.25 [.010]	.15 [.006]

5. Minimum land size around a hole is determined by considering the following:

- A. Maximum diameter of the drilled hole.
- B. Minimum annular ring requirement.
- C. Maximum allowance for etchback, when required.
- D. A standard manufacturing allowance, which must take into account tooling and processing variations. Table B-2 lists standard tolerances which can be applied to each class, depending on the size of the board.

This is summarized by the formula below and discussed in much greater detail in the appendix.

$$\text{Minimum land} = A + 2B + D + 2C \text{ (if required)}$$

6. Bow and twist is discussed in paragraph 3.1.4, together with information on each tolerance class (see Table B-3).

Table B-2 Standard Manufacturing Allowances

Greatest Board/Panel Dim.	Class A	Class B	Class C
Up to 300 [12.00]	.70 [.028]	.50 [.020]	.30 [.012]
More than 300 [12.00]	.85 [.034]	.60 [.024]	.40 [.016]

Table B-3A Bow and Twist Tolerance, Paper Base and Composite Materials

Pattern	Thickness Code	Class A	Class B	Class C
1				
S	T1	No req.	2.5%	1.5%
I	T2	2.5%	2.0%	1.0%
D	T3	2.0%	1.2%	0.8%
E	T4	1.5%	0.8%	0.6%
D				
2				
S	T1	No req.	2.0%	1.0%
I	T2	2.0%	1.5%	0.8%
D	T3	1.5%	1.0%	0.6%
E	T4	1.0%	0.7%	0.7%
D				

Table B-3B Bow and Twist Tolerance, Glass Base Material

<i>Pattern</i>	<i>Thickness Code</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
1				
S	T1	2.5%	2.0%	1.5%
I	T2	2.0%	1.5%	1.0%
D	T3	1.5%	1.0%	0.8%
E	T4	0.8%	0.6%	0.6%
D				
2				
S	T1	2.0%	1.5%	1.5%
I	T2	1.5%	1.0%	0.9%
D	T3	1.0%	0.7%	0.6%
E	T4	0.6%	0.5%	0.5%
D				
M				
U				
L	All categories	3.0%	2.0%	1.0%
T				
I				

7. Type 1, the Nominal Dimensioning System, is discussed beginning with paragraph 3.2. This system assigns a desired (nominal) dimension to each feature of the board and then assigns a tolerance to that dimension. Typically, a board edge serves as a datum.

There is a discussion of each type of dimension and a table with the tolerance values of each. The types of dimensions listed are:

- a. Board edges (see Table B-4).
- b. Board connector tangs (contact finger areas).
- c. Cutouts, notches, and keying slots.

NOTE: Radii should be provided for all slots and notches.

- d. Board thickness (see Table B-5).
- e. Board edge chamfering.

Table B-4 Board Edge Tolerances

<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
±.40 [±.016]	±.25 [±.010]	±.15 [±.006]

Table B-5 Board Thickness Tolerances

<i>Thickness</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
T1	$\pm .20$ [$\pm .008$]	$\pm .10$ [$\pm .004$]	$\pm .05$ [$\pm .002$]
T2	$\pm .30$ [$\pm .012$]	$\pm .20$ [$\pm .008$]	$\pm .10$ [$\pm .004$]
T3	$\pm .40$ [$\pm .016$]	$\pm .25$ [$\pm .010$]	$\pm .15$ [$\pm .006$]
T4	$\pm 15\%$ of nom.	$\pm 10\%$ of nom.	$\pm 5\%$ of nom.

For edgeboard connector, use classes B and C

- f. Unsupported hole diameters (see Table B-6).
- g. Unsupported hole-to-lead ratio.
- h. Finished diameter of the plated-through hole (see Table B-7).

NOTE: More tolerance is added over that shown in Table B-7, if the hole diameter is less than one-third to one-fourth of the board thickness.

NOTE: For any class, the larger the hole, the greater the tolerance; three size ranges are listed.

- i. Supported hole-to-lead ratio.
- j. Hole, feature location (see Table B-8).

NOTE: The information in Table B-8 was developed for epoxy/fiberglass. Less dimensionally stable materials may require that more tolerance be allowed.

Table B-6 Unsupported Holes

<i>Hole Dia.</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
0-.8 [0-.032]	$\pm .08$ [$\pm .003$]	$\pm .05$ [$\pm .002$]	$\pm .03$ [$\pm .001$]
.85-1.6 [.033-.063]	$\pm .10$ [$\pm .004$]	$\pm .08$ [$\pm .003$]	$\pm .05$ [$\pm .002$]
1.65-5.0 [.064-.188]	$\pm .15$ [$\pm .006$]	$\pm .10$ [$\pm .004$]	$\pm .08$ [$\pm .003$]
Ratio of min. hole dia. to base material thick- ness	2:3 or 66%	1:2 or 50%	1:4 or 25%

Table B-7 Plated-Through Hole Diameter Tolerances

<i>Hole Dia.</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
0-.8 [0-.032]	±.10 [±.004]	±.08 [±.003]	±.05 [±.002]
.81-1.6 [.033-.063]	±.15 [±.006]	±.10 [±.004]	±.05 [±.002]
.61-5.0 [.064-.195]	±.20 [±.008]	±.15 [±.006]	±.10 [±.004]

Table B-8 Hole Location Tolerances

<i>Related Board Size</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Where greatest dimension is less than 300.0 [12.00]	±.15 [±.006]	±.10 [±.004]	±.05 [±.002]
Where greatest dimension is greater than 300.0 [12.00]	±.20 [±.008]	±.15 [±.006]	±.10 [±.004]

- k. Conductive pattern feature location tolerance (see Table B-9).

NOTE: Minimum annular ring requirements are a measure of conductor pattern registration.

- l. Solder mask apertures feature location tolerance (see Table B-10).
m. Conductor width and spacing tolerances (see Table B-11).

NOTE: Tolerances listed in Table B-11 are for 1-oz copper conductor thickness. Allow .001 inch conductor variation for each additional ounce of conductor thickness.

NOTE: Conductor spacing requirements are the inverse of the conductor widths; apply the same tolerances.

Table B-9 Conductive Pattern Location Tolerances

<i>Related Board Size</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Where greatest dimension is less than 300.0 [12.00]	±.30 [±.012]	±.20 [±.008]	±.10 [±.004]
Where greatest dimension is greater than 300.0 [12.00]	±.40 [±.016]	±.30 [±.012]	±.20 [±.008]

Table B-10 Feature Location Tolerances for Solder Mask Aperture

<i>Related Board Size</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Where greatest dimension is less than 300.0 [12.00]	$\pm .40$ [$\pm .016$]	$\pm .25$ [$\pm .010$]	$\pm .15$ [$\pm .006$]
Where greatest dimension is greater than 300.0 [12.00]	$\pm .45$ [$\pm .018$]	$\pm .30$ [$\pm .012$]	$\pm .20$ [$\pm .008$]

Table B-11 Conductor Width Tolerances

<i>Feature</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Without plating	+ .10	+ .05	+ .03
	− .15	− .10	− .05
	[+ .004]	[+ .002]	[+ .001]
	[− .006]	[− .004]	[− .002]
With plating	+ .20	+ .10	+ .08
	− .15	− .10	− .08
	[+ .008]	[+ .004]	[+ .003]
	[− .006]	[− .004]	[− .003]

8. Type 2, the Basic Dimension System, is discussed beginning with paragraph 3.3. The exact dimension for a feature size or location is established, along with permissible variations. The same types of dimensions covered under type 1, Nominal Dimensioning, are also discussed in detail (see Tables B-12 to B-16). Only one example will be provided. (See Figure B-1 and Table B-17 from IPC-D-300G for an example of how tolerance may be expressed.)

Table B-12 Tolerance for Basic Dimensions of Cutouts, Notches, and Keying Slots, as Machined

<i>Tolerances to Be Applied To:</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Feature (slot or notch).	.15 [.006]	.10 [.004]	.05 [.002]
Location where greatest basic location dimension is less than 300.0 [12.00]	.20 [.008]	.15 [.006]	.10 [.004]
Location where greatest basic location dimension is greater than 300.0 [12.00]	.25 [.010]	.20 [.008]	.15 [.006]

NOTE Radii should be provided in all slots or notches

Table B-13 Board Thickness Tolerances

<i>Basic Code</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
T1	.40 [.016]	.20 [.008]	.10 [.004]
T2	.60 [.024]	.40 [.016]	.20 [.008]
T3	.80 [.030]	.50 [.020]	.30 [.012]
T4	30%	20%	10%

Table B-14 Hole Location Tolerances

<i>Related Board Size</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Where greatest basic dimension is less than 300.0 [12.00]	.40 [.016]	.30 [.012]	.15 [.006]
Where greatest basic dimension is greater than 300.0 [12.00]	.55 [.022]	.40 [.016]	.30 [.012]

Table B-15 Feature Location Tolerances (Lands, Conductor Pattern, Etc.)

<i>Related Board Size</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Where greatest dimension is less than 300.0 [12.00]	.85 [.034]	.55 [.022]	.30 [.012]
Where greatest dimension is greater than 300.0 [12.00]	1.15 [.046]	.85 [.034]	.55 [.022]

NOTE: Conductor pattern registration may be expressed in terms of minimum annular ring violation, which establishes manufacturing registration allowances.

Table B-16 Feature Location Tolerances for Solder Mask Apertures

<i>Related Board Size</i>	<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
Where greatest dimension is less than 300.0 [12.00]	1.15 [.046]	.70 [.028]	.40 [.016]
Where greatest dimension is greater than 300.0 [12.00]	1.30 [.052]	.85 [.034]	.55 [.022]

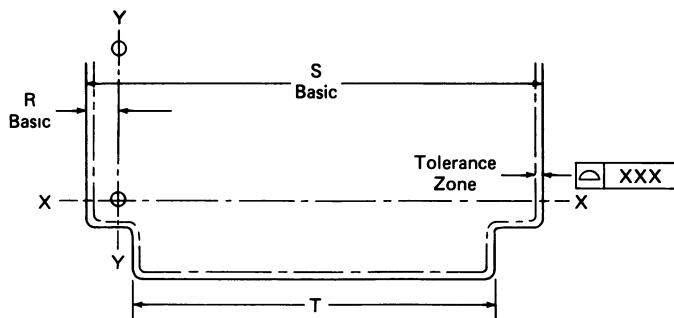


Fig. B-1 Tolerancing at contact finger tabs.

**Table B-17 Board Edge Tolerance
(Profile Tolerancing)**

<i>Class A</i>	<i>Class B</i>	<i>Class C</i>
.40 [.016]	.25 [.010]	.15 [.005]

Table B-18 Summary of the Type 1 Dimensioning System

<i>Applicable Characteristics</i>	<i>Paragraph Number</i>	<i>Figure Number</i>	<i>Table Number</i>	<i>Range of Dimensional Requirements</i>
1 Board edges	3 2 1	6	4	.15-.40 [0.006-0.016]
2 Board connector tang	3 2 1 1	6	—	—
3 Board thickness	3 2 2	—	6	05- 40 [002- 016]
4 Board edge chamfering	3 2 2 1	8	—	—
5 Bow and twist (flatness)	3 1 4	—	3a, 3b, 3c	5%-2 5%
6 Standard manufacturing allowances	3 1 3 2	—	2	30- 85 [012- 034]
7 Annular ring	3 1 3 1	—	1	03- 40 [.001- 016]
8 Cutouts, notches, and keys	3 2 1 2	7	5	05- 25 [002-010]
9 Unsupported holes	3 2 3	—	7	03- 15 [001- 006]
10 Plated-through holes	3 2 4	—	8	05- 20 [002-.008]
11 Hole locating tolerances	3 2 5	5	9	05- 20 [002- 008]
12 Conductive pattern tolerances	3 2 6	—	10	10- 40 [009- 016]
13 Conductor width tolerances	3 2 8	—	12	.03- 20 [001- 008]
14. Solder mask apertures	3 2 7	—	11	.15- 45 [006- 018]

SECTION 4.0 SUMMARY

Tables B-18 and B-19 provide summaries of each dimensioning system. The paragraph and applicable table number are referenced. Since these table do not list all classes, most of the tables from IPC-D-300G are also reproduced.

SECTION 50.0 APPENDIX

1. Geometric characters and symbols (see Figures B-2 and B-3).
2. Hole-to-land relationship (50.2).
3. Detailed discussion of the feature size determination equation (50.2.1)
4. Conversion table of coordinate tolerance to positional (circular) tolerance.

Table B-19 Summary of the Type 2 Dimensioning System

<i>Applicable Characteristics</i>	<i>Paragraph Number</i>	<i>Figure Number</i>	<i>Table Number</i>	<i>Range of Dimensional Requirements</i>
1. Board edges	3.3.1	9	13	.15–40 [.006–.016]
2. Board connector tang	3.3.1.1	9	—	—
3. Board thickness	3.3.2	—	15	.10–.80 [.004–.030]
4. Board edge chamfering	3.2.2.1	8	—	—
5. Bow and twist (flatness)	3.1.4	—	3a, 3b, 3c	.5%–2.5%
6. Standard manufacturing allowances	3.1.3.2	—	2	.30–.85 [.012–.034]
7. Annular ring	3.1.3.1	—	1	.03–.40 [.001–.016]
8. Cutouts, notches, and keys	3.3.1.2	7	14	.05–.25 [.002–.010]
9. Unsupported holes	3.3.3	—	7	.03–.15 [.001–.006]
10. Plated-through holes	3.3.4	—	8	.05–.20 [.002–.008]
11. Hole locating tolerances	3.3.5	—	16	.15–.55 [.006–.022]
12. Conductive pattern tolerances	3.3.6	—	17	.30–1.15 [.012–.046]
13. Conductor width tolerances	3.3.8	—	12	.03–.20 [.001–.008]
14. Solder mask apertures	3.3.7	—	18	.40–1.30 [.016–.052]

"For editorial reasons certain tables and figures listed in *(name of document goes here)* has been re-numbered. The reader is advised to obtain copies of those military and IPC documents."

	TYPE OF TOLERANCE	CHARACTERISTIC	SYMBOL
FOR INDIVIDUAL FEATURES	FORM	Straightness	—
		Flatness	□
		Circularity (roundness)	○
		Cylindricity	○
FOR INDIVIDUAL OR RELATED FEATURES	PROFILE	Profile of a line	⌞
		Profile of a surface	⌞
FOR RELATED FEATURES	ORIENTATION	Angularity	↙
		Perpendicularity	⊥
		Parallelism	//
	LOCATION	Position	○±
		Concentricity	○
	RUNOUT	Circular runout	↗*
		Total runout	↗↗*
*Arrowhead(s) may be filled in.			

Fig. B-2 Geometric characteristic symbols.

Term	Abbreviation	Symbol
At maximum material condition	MMC	(M)
Regardless of feature size	RFS	(S)
At least material condition	LMC	(L)
Projected tolerance zone	TOL ZONE PROJ	(P)
Diameter	DIA	Ø
Spherical diameter	SPHER DIA	S Ø
Radius	R	R
Spherical radius	SPHER R	SR
Reference	REF	()
Arc length	A/C	⌞
All around	A/A	Ø

Fig. B-3 Other symbols.

5. Microsectioning procedure
6. Thickness, plating in holes, micro-ohms method
7. Method for measuring bow and twist

Appendix C

MIL-P-55110D: General Specification for Printed Wiring Boards

This is an important document for a number of reasons which will become apparent. All printed circuit planning, manufacturing, and quality assurance personnel should have an understanding of and familiarity of its requirements. MIL-P-55110D and IPC-A-600C are perhaps the best presentation on end product acceptability and inspection guidelines available. IPC-A-600C is covered in Appendix D. No quality or planning persons should consider themselves competent and knowledgeable without having learned the information contained in both of these documents.

MIL-P-55110D also has another purpose. It stipulates that printed circuit boards being procured under government contract shall be procured only from manufacturers who have been qualified by the Defense Electronics Supply Center (DESC) as having met all documentation, manufacturing, and testing requirements listed in Table C-1. This document defines the exact qualification procedure to be followed. See paragraphs 4.5 and 6.6.

SECTION 1. SCOPE

This section states that this specification establishes the qualification and performance requirements of rigid single-sided, double-sided, and multilayer printed-wiring boards with plated-through holes. It also establishes three classifications and defines them as follows:

- Type 1: Single-sided boards
- Type 2: Double-sided boards
- Type 3: Multilayer boards

Table C-1 Qualification Inspection

Material	Inspection	Requirement Paragraph	Method Paragraph	Qualification Test Specimen Number (see 4.5.1)	Test Coupon by Board Type ¹			Whole Specimen
					1	2	3	
Visual	3.4, 3.4.1-3.4.9	—	—	—	—	—	—	—
Edges of laminate	3.5	4.8.2	—	1, 2, 3, 4	—	—	—	X
Surface imperfections	3.5.1	4.8.2.1	—	1, 2, 3, 4	—	—	—	X
Subsurface imperfections	3.5.2	4.8.2.2	—	1, 2, 3, 4	—	—	—	X
Marking	3.5.3	4.8.2.3	—	1, 2, 3, 4	—	—	—	X
Traceability	3.5.4	4.8.2.4	—	1, 2, 3, 4	—	—	—	X
Workmanship	3.5.4.1	4.8.2.4	—	1, 2, 3, 4	—	—	—	X
Solderability	3.5.5	4.8.2.5	—	1, 2, 3, 4	—	—	—	X
Solderability	3.5.6	4.8.2.6	—	—	A-1	—	—	—
Surface	3.5.6.1	4.8.2.6.1	1	C-1	—	—	—	—
Hole	3.5.6.2	4.8.2.6.2	1	—	—	—	—	—
Thermal stress	3.5.7	4.8.2.7	1	B-3	—	—	—	—
Dimensional	3.6, 3.6.1	4.8.3	—	—	—	—	—	—
Hole pattern	3.6.2	4.8.3.1	—	—	—	—	—	X
Bow and twist	3.6.3	4.8.3.2	1, 2, 4	—	—	—	—	X
Conductor spacing	3.6.4	4.8.3.3	1, 2, 4	E-1 to E-5	E-1 to E-5	E-1 to E-5	E-1 to E-5	—
Conductor pattern	3.6.5	4.8.3.4	1, 2, 4	E-1 to E-5	E-1 to E-5	E-1 to E-5	E-1 to E-5	X
Layer-to-layer registration	3.6.6	4.8.3.5	1, 2, 3, 4	—	—	—	—	X

Table C-1 (Continued)

Inspection	Requirement Paragraph	Method Paragraph	Qualification Test Specimen Number (see 4.5.1)	Test Coupon by Board Type ¹			Whole Specimen
				1	2	3	
<i>Dimensional (Continued)</i>							
Annular ring (external)	3.6.7	4.8.3.6	1, 4	A-3	—	—	X
Unsupported hole	3.6.7.1	4.8.3.6	1, 4	A-3	—	—	X
Plated-through hole	3.6.7.2	4.8.3.6	1, 4	—	—	—	X
Plating and coating thickness	3.6.9	4.8.3.8	3	C-1, C-4, C-5	C-1, C-4, C-5	C-1, C-4, C-5	—
Physical requirements	3.7	4.8.4	—	—	—	—	—
Plating adhesion	3.7.2	4.8.4.2	1, 2, 3, 4	C	C	C	X
Conductor edge outgrowth	3.7.3	4.8.4.3	—	—	—	—	X
Bond strength	3.7.4	4.8.4.4	1	A-2	—	—	—
Construction integrity (microsection)	3.8	4.8.5	1, 4	—	—	—	—
Plated-through hole	3.8.1	4.8.5.1	1, 4	—	A-1 or A-5	A-1 or A-5	—
Plated copper thickness	3.8.2	4.8.5.2	1, 4	—	A-1 or A-5	A-1 or A-5	—
Layer to layer ²	3.6.6	4.8.3.5	1, 4	—	—	—	—
Plating voids	3.8.3	4.8.5.3	1, 4	—	A-1 or A-5	A-1 or A-5	—
Conductor thickness	3.8.4	4.8.5.4	1, 4	—	A-1 or A-5	A-1 or A-5	—
Resin smear and etchback	3.8.5	4.8.5.5	—	—	—	—	—
Hole cleaning (smear removal)	3.8.5.1	4.8.5.5	1, 4	—	—	—	A-1 or A-5
Negative etchback	3.8.5.2	4.8.5.5	1, 4	—	—	—	A-1 or A-5
Etchback	3.8.5.3	4.8.5.5	1, 4	—	—	—	A-1 or A-5

Undercutting	3.8.6	4.8.5.6	1, 4	—	A-1 or A-5	A-1 or A-5	—
Annular ring (internal)	3.8.7	4.8.5.7	1, 4	—	—	A-1 or A-5	—
Dielectric layer thickness	3.8.8	4.8.5.8	1, 4	—	A-1 or A-5	A-1 or A-5	—
Laminate voids	3.8.9	4.8.5.9	1, 4	—	A-1 or A-5	A-1 or A-5	—
Resin recession	3.8.10	4.8.5.10	1, 4	—	A-1 or A-5	A-1 or A-5	—
Lifted lands	3.8.11	4.8.5.11	1, 4	—	A-1 or A-5	A-1 or A-5	—
Plated-through holes	3.9	4.8.6	—	—	—	—	—
Thermal stress	3.9.1	4.8.6.1	1	—	B-2	B-2	—
Layer to layer²	3.6.6	4.8.3.5	1	—	—	B-2	—
Rework simulation	3.9.2	4.8.6.2	1, 2	—	A-2	A-2	—
Thermal shock	3.9.3	4.8.6.3	1, 2	—	A-2	A-2	—
Lifted lands	3.9.4	4.8.6.4	1	—	D-3	D-3	—
Electrical and environmental requirements	3.10	4.8.7	—	—	—	—	—
Moisture and insulation resistance	3.10.1	4.8.7.1	1	E-1	E-1	E-1	—
Dielectric withstanding voltage	3.10.2	4.8.7.2	1	E-1	E-1	E-1	—
Circuitry	3.10.3	4.8.7.3	—	—	—	—	—
Circuit continuity	3.10.3.1	4.8.7.3.1	2	D-3	D-3	D-3	—
Circuit shorts ³	3.10.3.3	4.8.7.3.2	2	E-1	E-1	E-1	—
Cleanliness ⁴	3.10.4	4.8.7.4	1, 2, 4	A11	A11	A11	X
Ionic	3.10.4.1	4.8.7.4.1	1, 2, 4	A11	A11	A11	X
Repair	3.10.5	4.8.7.5	1, 2, 3, 4	A11	A11	A11	X

¹See MIL-STD-275, paragraph 1.2 and Figures 11, 12, and 13 herein.²The two layer-to-layer microsections shall be at 90 degree angles >200 Volts.⁴Cleanliness shall be performed prior to any other inspection

SECTION 2. APPLICABLE DOCUMENTS

The purpose of these other documents is as discussed in MIL-STD-275E under "Referenced Documents." The planning and quality departments should have a copy of these documents on hand for reference as needed. Without these documents, there is no way to verify a requirement which may arise on any job.

SECTION 3. REQUIREMENTS

This section details all manufacturing and other requirements for rigid printed circuit boards. They are discussed below.

1. Quality conformance test coupons shall be included on all panels. Defects noted in the coupons shall be considered indicative of defects in the printed circuit boards themselves, and corrective action must be taken.
2. Metal-clad laminates used are to be in accordance with MIL-P-13949 (plastic sheet, metal-clad, for use in printed wiring boards):
 - a. No base material (dielectric) shall be used which is thinner than .002 inch, not including copper foil, for single-sided cladding.
 - b. Minimum base material width with double-sided cladding shall be .0035 inch.

Other materials such as fluxes, copper foil, solder, solder mask, marking inks, and adhesives are specified in paragraph 3.4.
3. Visual requirements are discussed in paragraph 3.5. A very brief and only partial summary of them is provided below. All of the requirements in paragraph 3.5 should be studied and known well by planners and quality assurance personnel.
 - a. Haloing along board edges shall be limited to .100 inch or 50% of the edge spacing called out on the drawing.
 - b. Surface imperfections (such as scratches, dents, and haloing) are allowed, provided that laminate fiber is not damaged or exposed and the imperfection does not bridge conductors or reduce dielectric spacing requirements.
 - c. Subsurface imperfections (blistering, haloing, measles) are allowed, provided that the imperfection is nonconductive, does not bridge more than 25% of the distance between conductors, does not reduce conductor spacing below requirements, and does not propagate as a result of testing.
 - d. Foreign particles included in laminate are allowed, provided they are at least .010 inch from conductors, do not reduce spacing more than 50%,

- are smaller than .032 inch, and are limited to a maximum of two such defects per side of the printed circuit board. Gelation particles (pieces of epoxy resin from prepreg) are permitted, regardless of their location.
- e. Measuring is allowed within the restricted guidelines of paragraph 3.5.3.3.
 - f. All boards and quality conformance coupon strips should be marked per the drawing and contain the following:
 - (1) Part number and revision level.
 - (2) Date of manufacture.
 - (3) Manufacturer's Federal Supply Code for Manufacturers (FSCM).
 - (4) Lot number.
 - (5) Serial number, which identifies each coupon and board made on a given panel.

NOTE: Markings A, B, C, and D can be etched/plated on by inclusion with the outer layer artwork during imaging, or they can be applied by an appropriate ink.

NOTE: The serial number must be stamped on with an appropriate ink or scribed onto a metal square provided for that purpose. It is required that all boards and coupons be traceable to the panels from which they were manufactured.

- g. The boards shall exhibit good workmanship when inspected in accordance with other requirements and methods called out in this specification.
- h. The boards must meet minimum solderability requirements.
- i. Dimensional requirements and hole pattern accuracy shall meet the drawing specifications.
- j. Maximum bow and twist shall be 1.5% when tested according to the method described in paragraph 4.8.3.2.
- k. Conductor width and spacing shall be per the drawing. If nothing is specified on the drawing, minimum external spacing shall be .005 inch and minimum internal spacing .004 inch. Internal or external conductor width should not be less than .004 inch.
- l. Conductor pattern defects shall not reduce conductors more than 20% below the minimum width requirement on the drawing. These isolated defects must be confined to a .500-inch section or less of a conductor's length.

NOTE: Thus, isolated defects which violate the minimum conductor width requirements may be permissible.

- m. Layer-to-layer registration cannot deviate more than .014 inch for a multilayer board. Registration must be confirmed by two mutually per-

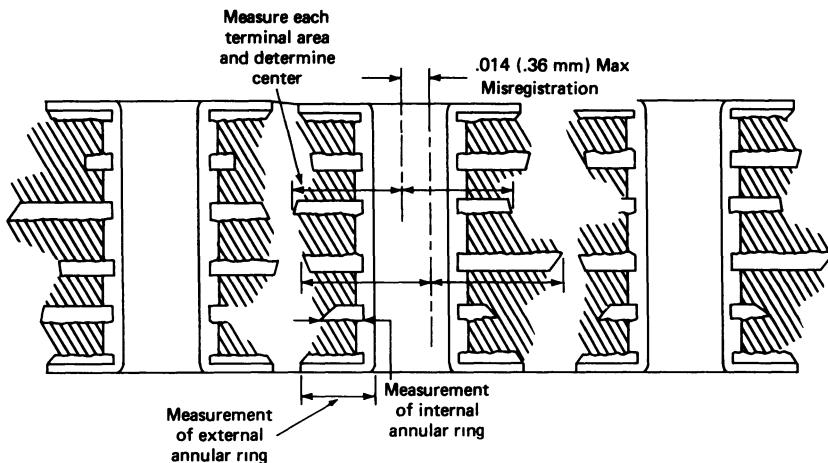


Fig. C-1 Layer-to-layer registration and annular ring measurement.

perpendicular microsections or by special coupons which allow visual assessment (see Figure C-1).

- n. Minimum annular ring requirements may be violated by up to 20% due to isolated defects on external layers. Other requirements for the minimum annular ring are as follows:
 - (1) External plated-through hole: .005 inch where the conductor meets the hole; .002 inch elsewhere; unsupported hole: .015 inch.
 - (2) Internal: .002 inch (see Figure C-2).
- o. Solder mask thickness at the crest of a conductor shall be .001 inch minimum. It is permissible to have a certain amount of solder mask peel off when tape tested, unless that mask is on bare copper or bare laminate (see Table C-2). If solder mask is required, the boards are to be tested for ionic contamination prior to applying the solder mask.
- p. Plating thicknesses shall be per Table C-3. Note that tin-lead is to be measured before reflow not afterward.
- q. Construction integrity shall be determined by microsection prior to thermal stress testing. The requirements are listed in paragraph 4.8.5 (see Figures C-3 to Figure C-9).

The plated-through hole is examined by microsectioning of three holes in a coupon section. Good workmanship should be evident and the following requirements apply:

- (a) No cracks in conductive foil, plating, or coating.
- (b) No separation at conductor interfaces.
- (c) Nail heading shall not exceed 1.5 times the foil thickness.

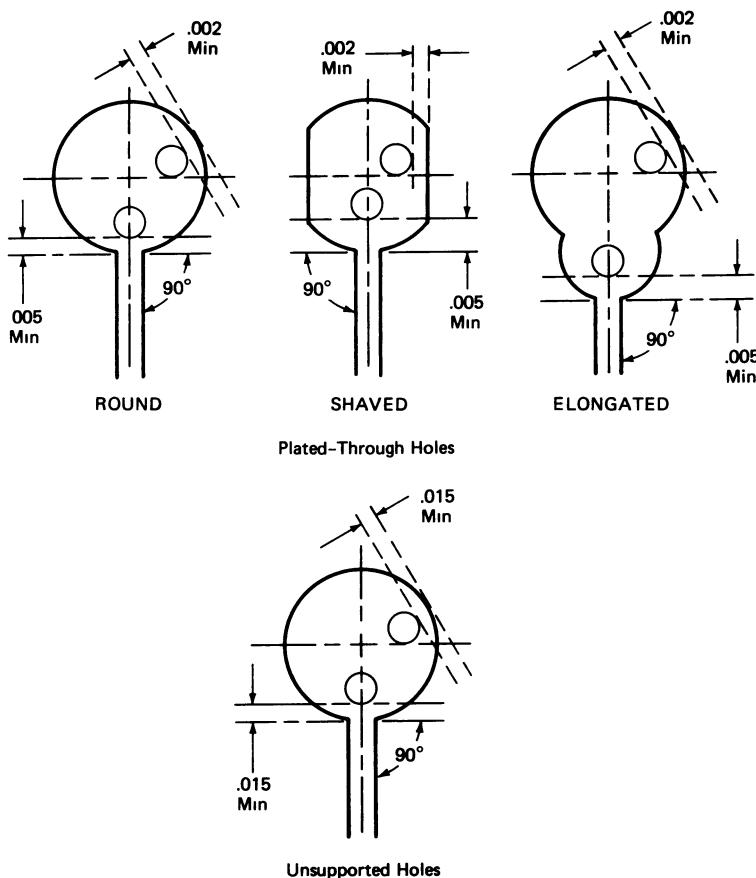


Fig. C-2 Land areas (external minimum annular ring).

Table C-2 Solder Mask Adhesion to Printed Wiring Boards

Material	Maximum Percentage of Lifting: Melting and Nonmelting Metals Nonscribed Test
Bare copper	0
Gold or nickel	5
Tin-lead plating	10
Reflowed tin-lead	10
Base laminate	0

Table C-3 Plating and Coating Thickness¹

<i>Plating Material</i>	<i>Surface and Through-Hole Thickness</i>
Gold	.000050 inch minimum
Nickel	.0002 inch minimum
Tin-lead	.0003 inch minimum at the surface as plated
Solder coating	.0003 inch minimum at the crest on the surface as coated

¹A coupon prior to reflow may be required (see paragraph 4 6 and Table C-7)

- (d) Nodules, plating folds, or plated glass fiber protrusion are acceptable, provided that hole diameter and copper thickness requirements are not violated.
- r. Surface and through-hole copper thickness shall be .001 inch minimum, except that isolated areas down to .0008 inch are permissible. Isolated areas less than .0008 inch shall be treated as a void.
- s. Plating voids in the hole wall require 100% visual inspection. Allowable voids are limited to the following (three voids maximum in a hole):
 - (1) The combined length of voids shall not exceed 5% of the total hole wall length.

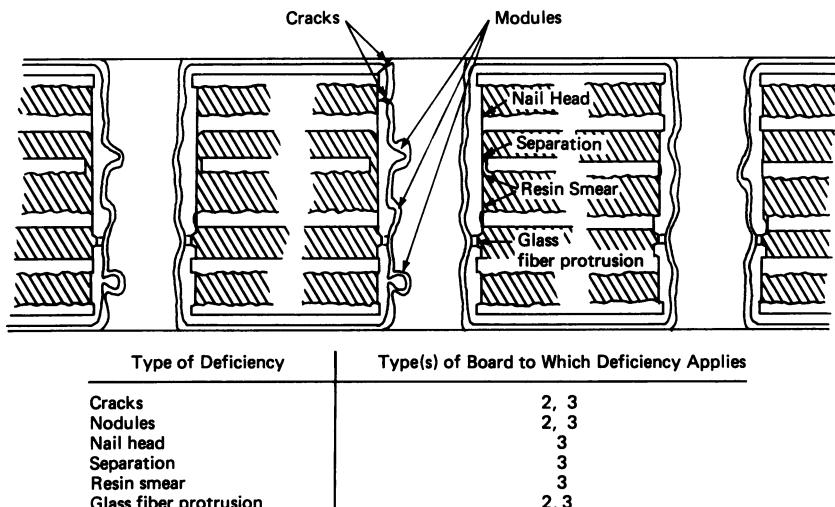


Fig. C-3 Deficiencies in plated-through hole workmanship.

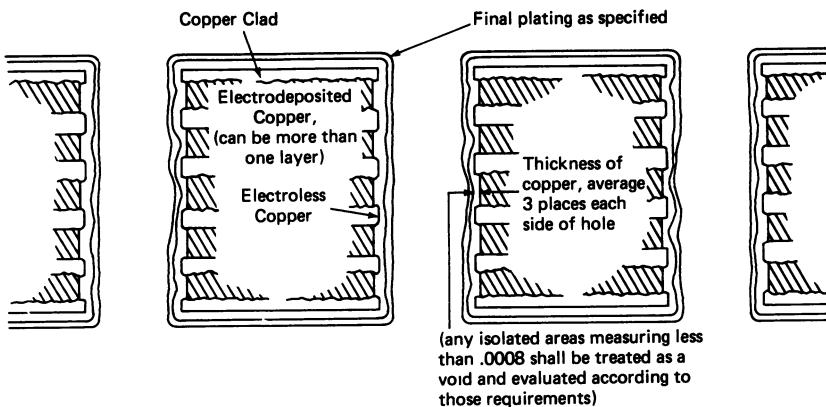


Fig. C-4 Plating thickness.

- (2) The combined area shall not exceed 10% of the hole wall area.
- (3) No circumferential voids (ring voids or lip voids) are permitted.
- t. Etchback and smear removal requirements
 - (a) Type 3 boards shall be free of resin smear at inner layer connections.
 - (b) When etchback is not specified, lateral removal of hole wall material (etchback) shall not exceed .001 inch.
 - (c) When etchback is specified on the drawing, lateral removal of hole wall material shall be .0002 inch minimum to .003 inch maximum. Material removal may take place on one or both sides of the inner layer foil. Wicking or copper back an additional .003 inch maximum is allowable, provided that conductor spacing requirements are not violated.

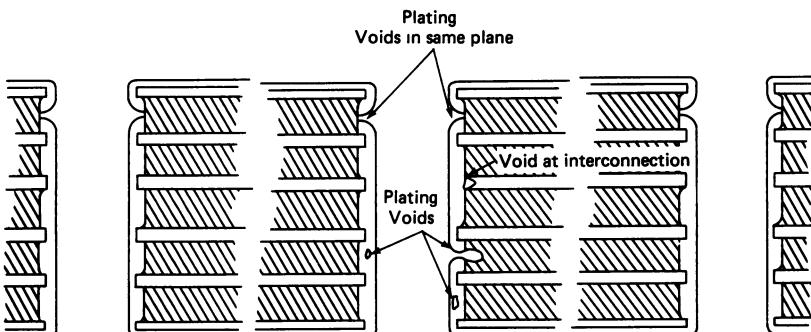
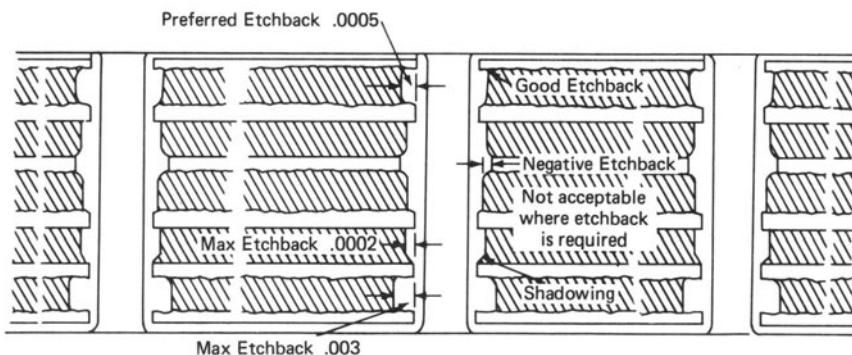


Fig. C-5 Typical plating voids.



NOTES:

1. Dimensions are in inches.

Fig. C-6 Forms of etchback.

- u. Negative etchback is the lateral removal of inner layer copper foil at the plated-through hole. It should not exceed .0005 inch.
- v. Undercutting shall not exceed the total thickness of foil and plating or 10% of the conductor width, whichever is less.
- w. Dielectric layer thickness shall be per the drawing. Type 3 boards shall have .0035-inch minimum spacing between any two conductive layers (see Figure C-7). There must be a minimum of two sheets of prepreg or laminate between any two conductive layers.
- x. Laminate voids .003 inch or less in the longest direction shall be permitted.

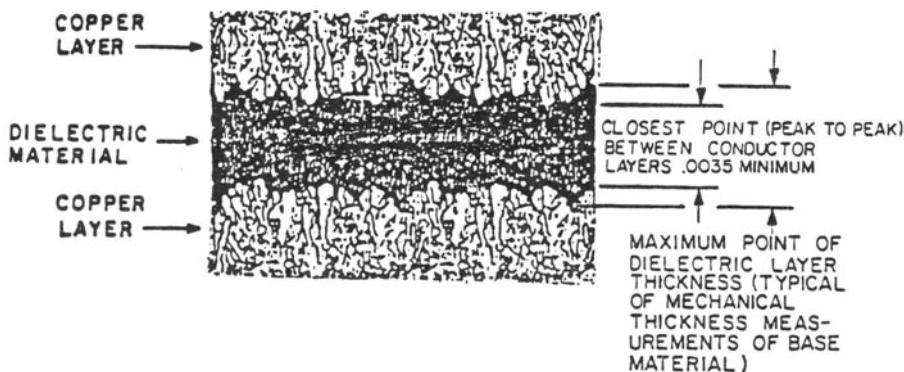
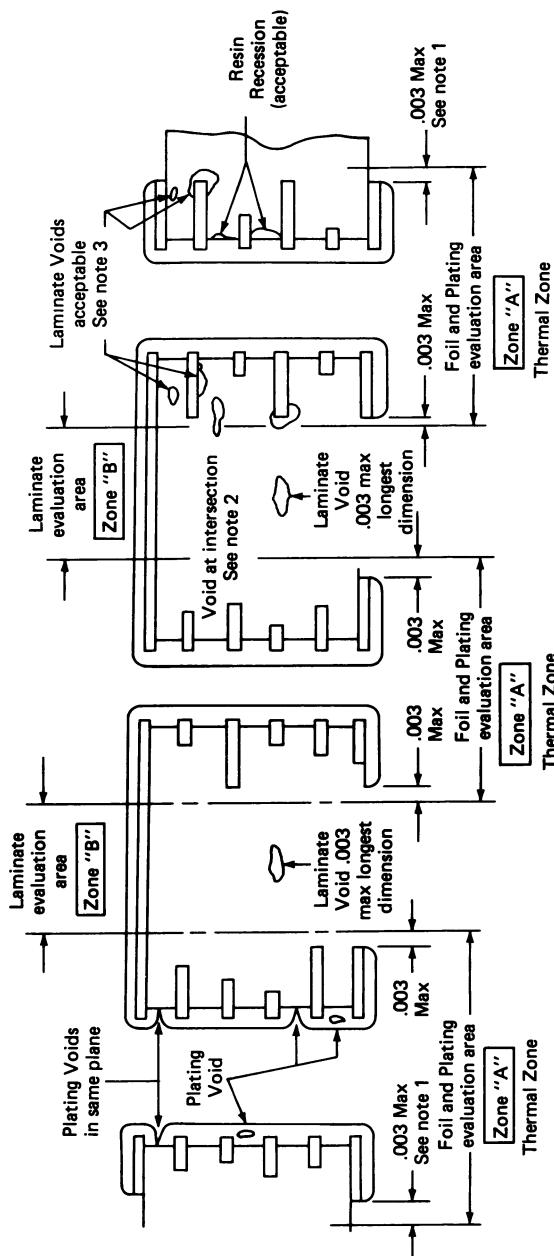
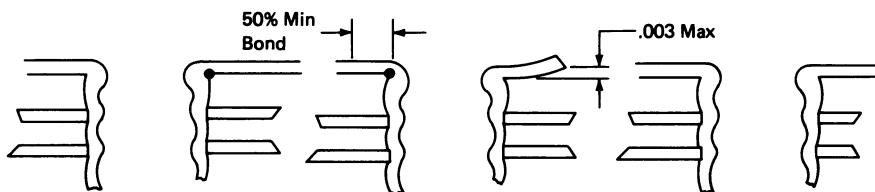


Fig. C-7 Dielectric layer thickness measurement.



- NOTES:**
1. Typically beyond land edge most radially extended.
 2. Void at intersection of Zone A and Zone B. Laminate voids greater than .003 (0.08 mm) in length which extend into the laminate evaluation area are rejectable.
 3. Laminate voids are not evaluated in Zone A, laminate voids greater than .003 (0.08 mm) that extend into Zone B are rejectable.
 4. Dimensions are in inches.

Fig. C-8 Typical microsection of plated-through holes after thermal stress and rework simulation.

**NOTES:**

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

Fig. C-9 Lifted lands.

- y. Resin recession from the hole wall shall be permitted as long as it is less than 40% of the hole wall length and does not recede more than .003 inch from the hole wall copper in the unthermal stress sample. Resin recession exceeding these requirements is permitted in the thermal stressed sample.
- z. There shall be no lifted land (metal areas) in the microsection sample prior to thermal stress. After thermal stress, lifting is allowed, provided at least 50% of the land is bonded and the lifted portion is less than .003 inch off the surface.
 - aa. Thermal stressed microsections shall be examined in two zones, A and B. (see Figure C-8).
 - bb. Electrical continuity testing shall be performed on all production boards.
 - cc. Repair is not permitted on boards being built to MIL-P-55110D requirements. When boards are inspected, there shall be no evidence of repair.

NOTE: Touchup is permitted. Touchup is defined as repeating a manufacturing operation manually to increase the yield on acceptable boards.

SECTION 4. QUALITY ASSURANCE PROVISIONS

This section spells out all inspection and testing requirements needed to operate a MIL-P-55110D program. There are four types of inspection: (1) materials inspection, (2) qualification inspection, (3) in-process inspection, (4) quality conformance inspection (groups A and B).

1. Materials inspection. This consists of certifications from the manufacturers together with verifying data. The verifying data (laboratory/inspection reports) must be available upon request. Table C-4 lists those items which must be covered by this requirement and the specification which they must meet.

Table C-4 Materials Inspection

<i>Material</i>	<i>Requirement Paragraph</i>	<i>Applicable Specification</i>
Metal-clad laminate	3.4.1	MIL-P-13949
Bonding material	3.4.2	MIL-P-13949
Solder coating	3.4.4	QQ-S-571
Soldering flux	3.4.5.3	MIL-F-14256
Permanent solder mask	3.4.6	IPC-SM-840
Copper foil	3.4.3	IPC-CF-150

2. Qualification inspection. This is performed at a laboratory acceptable to the government and is part of the procedure for becoming a DESC qualified manufacturer of printed circuit boards. Table C-1 lists all requirements. The entire qualification program is discussed beginning with paragraph 4.5.
3. In-process inspection. The requirements are listed in Table C-5. Most of them are met simply by performing group A inspections (see Table C-6). However, tin-lead thickness must be measured and recorded as the job is being plated. Also, a minimum of five boards per shift must have ionic contamination testing performed. This testing shall be considered an ongoing program required of all DESC qualified producers (see Table C-5).
4. Quality conformance inspection. This is the group A and group B listed in Tables C-6 and C-7. Group A must be performed on each lot of boards being run. Group B must be performed, as a minimum, on the most complicated pattern of printed circuits produced during a month. For group B, two coupon strips and the associated boards are submitted to a government-approved laboratory for testing.

SECTION 5. PACKAGING

Three levels of preservation are discussed: A, B, and C.

Table C-5 In-Process Inspection

<i>Test</i>	<i>Requirement Paragraph</i>	<i>Method Paragraph</i>
Cleanliness	3.10.4, 3.10.4.1	4.8.7.4, 4.8.7.4.1
Plating deposit ¹	3.4.3 and 3.6.9	4.8.1, 4.8.3.8
Solder mask	3.4.6	4.8.3.7
Conductor pattern	3.6.5	4.8.3.4
Plating adhesion	3.7.2	4.8.4.2

¹A nonreflowed coupon may be required by contract.

Table C-6 Group A Inspection

Inspection	Requirement Paragraph	Method Paragraph	Production Board	Test Coupon by Board Type ¹			AQL (Percent Defective)	
				1	2	3	Major	Minor
Material	3.4, 3.4.1 to 3.4.7	—	—	—	—	—	—	—
Visual	3.5	4.8.2	²	—	—	—	1.0	4.0
Edges of printed wiring board	3.5.1	4.8.2.1	X	—	—	—	—	—
Surface imperfections	3.5.2	4.8.2.2	X	—	—	—	1.0	4.0
Subsurface imperfections	3.5.3	4.8.2.3	X	—	—	—	1.0	4.0
Marking	3.5.4	4.8.2.4	X	—	—	—	1.0	4.0
Traceability	3.5.4.1	4.8.2.4	X	—	—	—	1.0	4.0
Workmanship	3.5.5	4.8.2.5	X	—	—	—	1.0	4.0
Solderability	3.5.6	4.8.2.6	— ³	—	—	—	—	—
Surface	3.5.6.1	4.8.2.6.1	C	—	—	—	1.0	4.0
Hole	3.5.6.2	4.8.2.6.2	—	A	A	A	1.1	4.0
Thermal stress	3.5.7	4.8.2.7	—	B	—	—	1.0 ⁶	4.0
Dimensional	3.6, 3.6.1	4.8.3	—	—	—	—	1.0	4.0
Hole pattern	3.6.2	4.8.3.1	X	—	—	—	1.0	4.0
Bow and twist	3.6.3	4.8.3.2	X	—	—	—	1.0	4.0
Conductor spacing	3.6.4	4.8.3.3	X	—	—	—	1.0	4.0
Conductor pattern	3.6.5	4.8.3.4	X ⁷	—	—	—	1.0	4.0
Layer-to-layer registration	3.6.6	4.8.3.5	—	—	—	F	1.0	4.0
Anular ring (external)	3.6.7	4.8.3.6	X	—	—	—	1.0	4.0
Unsupported hole	3.6.7.1	4.8.3.6	X	—	—	—	1.0	4.0
Plated-through hole	3.6.7.2	4.8.3.6	X	—	—	—	1.0	4.0

Solder mask thickness	3.6.8	4.8.3.7	X ³	E ³	E ³	1.0	4.0
Plating and coating thickness	3.6.9	4.8.3.8	X ³	C ³	C ³	1.0	4.0
Physical requirements	3.7	4.8.4	—	—	—	—	—
Solder mask cure and adhesion	3.7.1	4.8.4.1	—	J ³	J ³	1.0	4.0
Plating adhesion	3.7.2	4.8.4.2	X ³	C ³	C ³	1.0	4.0
Conductor edge outgrowth ⁹	3.7.3	4.8.4.3	X	—	—	1.0	4.0
Construction integrity (microsection) ⁴	3.8	4.8.5	—	—	—	—	—
Plated-through hole	3.8.1	4.8.5.1	—	B	B	4	4
Plated copper thickness	3.8.2	4.8.5.2	—	B	B	4	4
Plating voids	3.8.3	4.8.5.3	—	B	B	4	4
Conductor thickness	3.8.4	4.8.5.4	—	B	B	4	4
Resin smear and etchback	3.8.5	4.8.5.5	—	—	—	—	—
Hole cleaning (smear removal)	3.8.5.1	4.8.5.5	—	—	B	4	4
Negative etchback	3.8.5.2	4.8.5.5	—	—	B	4	4
Etchback	3.8.5.3	4.8.5.5	—	—	B	4	4
Undercutting	3.8.6	4.8.5.6	—	B	B	4	4
Annular ring (internal)	3.8.7	4.8.5.7	—	—	B	4	4
Dielectric layer thickness	3.8.8	4.8.5.8	—	B	B	4	4
Laminate voids	3.8.9	4.8.5.9	—	—	B	4	4
Resin recession	3.8.10	4.8.5.10	—	—	B	4	4
Lifted lands	3.8.11	4.8.5.11	—	B	B	4	4
Plated-through holes	3.9	4.8.6	—	—	—	5	—
Thermal stress	3.9.1	4.8.6.1, 4.8.1	—	—	B	4	4
Electrical and environmental requirements	3.10	4.8.7	—	—	—	—	—

Table C-6 (Continued)

Inspection	Requirement Paragraph	Method Paragraph	Production Board	Test Coupon by Board Type ⁱ			AQL (Percent Defective)	
				1	2	3	Major	Minor
Circuitry	3.10.3	4.8.7.3	—	—	—	—	—	—
Circuit continuity	3.10.3.2	4.8.7.3.1	X	—	—	—	100% inspection ^j	—
Circuit shorts	3.10.3.3	4.8.7.3.2	X	—	—	—	100% Inspection ^j	—
Repair	3.10.5	4.8.7.5	X	A11	A11	A11	100% Inspection	—

ⁱSee MIL-STD-275 and paragraph 1.2.^jVisual examination (4.8.1) of production board surface for all three board types (1, 2, and 3).^kTest coupon or production board; manufacturer's option coupon shall be processed with production board.^lOne coupon per panel shall be microsectioned for type 3 boards; the number of coupons to be microsectioned for types 1 and 2 boards shall be based on a statistical sample in accordance with MIL-STD-105 General Inspection level II of the number of panels produced and shall meet an AQL of 2.5% defective.^mFor type 3 boards, microsection 1 coupon per panel 100% of the time in any one direction, and microsection perpendicular to that direction on a sampling of the microsectioned coupons based on MIL-STD-105 General Inspection level II with an AQL of 2.5% defective. Type 2 boards shall be microsectioned in only one direction.ⁿSee 4.7.1.2 of MIL-P-55110.^oInspected prior to lamination^pProduction board shall be used for type 2.^qMay be inspected by examination of microsectioned coupon associated with production board^rIf the printed assembly drawing required the circuitry tests to be run with 100% inspection on the printed wiring assembly, a sampling plan (4.7.1.2.1) based on an AQL of 2.5% defective shall be used on the bare unassembled printed wiring board

Table C-7 Group B Inspection

<i>Inspection</i>	<i>Requirement Paragraph</i>	<i>Method Paragraph</i>	<i>Test Coupon by Type¹</i>		
			<i>I</i>	<i>2</i>	<i>3</i>
Bond strength	3.7.4	4.8.4.4	B	—	—
Rework simulation	3.9.2	4.8.6.2	—	B	B
Moisture and insulation resistance	3.10.1	4.8.7.1	E	E	E
Dielectric withstanding voltage	3.10.2	4.8.7.2	E	E	E

¹See MIL-STD-275 and 1.2 herein

SECTION 6. NOTES

This section has isolated pieces of information which supplement the other sections. Included are definitions and explanations.

Appendix D

IPC-A-600C: Guidelines for Acceptability of Printed Boards

Technically this document is part of inspection literature for quality assurance. It was compiled to help "standardize individual interpretations to specifications on printed boards." Because of the need to place standards and specifications within the visual context of the end product, it is desirable that design, quality, planning, and manufacturing personnel know what certain conditions look like and how those conditions are viewed by the electronics/printed circuit industry (i.e., IPC members). Without a knowledge of this document and the other standards and specifications in this chapter, a design, planning, quality assurance, or manufacturing person would have no basis for evaluating a company specification, a set of artwork, or a set of blueprints for a given printed circuit board.

This document establishes three conditions: preferred, acceptable, and rejectable. The meaning of "preferred" is obvious. "Acceptable" means that the product is reliable and functional, although poor workmanship is evident. "Rejectable" means that the product has a very poor aesthetic appearance and may not meet reliability requirements.

IPC-A-600C is divided into 15 sections. Each section should be read and understood by people involved in any aspect of printed circuit manufacturing. This document is perhaps the most well-known and often-cited one in printed circuit literature. It forms part of the internal specifications for many government and industrial organizations (see Table D-1).

SECTION 1. PLATED-THROUGH HOLES

This section contains drawings and photographs of microsectioned holes showing numerous conditions related to the acceptability of the plated-through hole. It is prefaced by a list of methods used for inspecting and measuring. This list is important because it establishes certain methods and techniques as standard.

SECTION 2. SURFACE PLATING

1. Adhesion is tape tested. The only acceptable condition is that no metal is removed by the tape. There is a comment that slivering is often associated

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with plating adhesion. Slivering is the breaking off of metallic etch resist along conductor edges.

2. Nodules (burned-on excessive plating) are acceptable, provided they are not loose and easily broken off, and provided minimum conductor spacing requirements are not violated.
3. Pitting should be cause for rejection if pits are large, numerous, and omnipresent or if they result in exposure of the base metal. Except in these situations, acceptability should be based on the intended function of the end product. A distinction is made between pitting in contact fingers and pitting elsewhere in the circuitry. This section makes it clear that pitted plating is not an automatic cause for rejection; accept/reject decisions should be based instead of functionality and intended use.

SECTION 3. SOLDER COATING

1. Acceptability is based on the ability of the coating to provide a reliable electrical and mechanical joint. The solder also provides some protection to the copper surface. Visual examination is the only requirement. It is usually performed after the edge dip solderability test called out in paragraph 2.4.14 of IPC-TM-650.
2. Dewetting is allowed, provided it is not widespread.
3. The thickness of fused solder is measured at the crest of the conductor.

NOTE: IPC-A-600C does not address the quality requirements of SMOBC circuitry. These requirements are discussed in another separate chapter of this book.

SECTION 4. LAMINATE BASE MATERIAL

This section contains a detailed discussion of laminate defects and conditions. There are some important areas which have been neglected, such as discussions of included particles, damaged laminate, stains or discolorations, and darkened laminate as a result of baking.

1. Measles and crazing. There is an extensive discussion of these defects. Measles are white dots caused by separation of the resin and the glass fibers; they generally result from thermal processing. Crazing is more severe and has the appearance of connected measles. These defects are generally considered to result from mechanical processing. Some rather technical guide-

lines are set up for determining the acceptability of these conditions (see Tables D-1, D-2, and D-3). A paragraph is also added which states that the IPC has no data showing that a board with even severe measles has ever failed due to this defect, even with extended use under harsh conditions (see Figure D-1).

TABLE D-2 Acceptability Guidelines for Measling and Crazing: Raw Material—Bare Laminate

<i>Class I: Consumer</i>	<i>Class II: General—Industrial</i>	<i>Class III: High-Reliability Life Support</i>
Measling and crazing shall not exceed 2% of the total usable area. (See Notes.)	Measling and crazing shall not exceed .5% of the total usable area. (See Notes.)	Measling and crazing shall not exceed .1% of the total usable area. (See Notes.)

NOTE 1: The area of measling or crazing is determined by combining the area of each measles or craze and dividing by the total area of the printed board. A separate determination is made for each side of the board.

NOTE 2: The referee test (destructive) to determine propagation of measling or crazing is to precondition the test specimen and solder float the specimen on a solder bath at a temperature of $288^{\circ}\text{C} \pm 6^{\circ}\text{C}$ ($550^{\circ} \pm 10^{\circ}\text{F}$) for a period of 10 seconds. Measling/crazing shall not propagate into a lesser class requirement or other defect category. (See IPC Test Method 2.6.8.)

Courtesy of the IPC.

Table D-3 Acceptability Guidelines for Measling and Crazing: Ball Printed Board (Completely Processed and Fused)

<i>Class I: Consumer</i>	<i>Class II: General—Industrial</i>	<i>Class III: High-Reliability Life Support</i>
Measling or crazing does not bridge electrically uncommon conductors.	Total area affected by measles or crazing shall not exceed 5% of the board area.	Total area affected by measles or crazing shall not exceed 1% of the board area.
Test for dielectric resistance: 10,000 megohms/ 500 VDC between conductive surfaces where measles occur (dry board). (See Notes.)	There shall be no more than 70% reduction in space between electrically uncommon conductors. (See Notes.)	There shall be no more than 25% reduction in space between electrically uncommon conductors. (See Notes.)

NOTE 1: Repairs to boards are permissible provided that the repaired board meets the above criteria.

NOTE 2: The area of measling or crazing is determined by combining the area of each measles or craze and dividing by the total area of the printed board. A separate determination is made for each side of the board.

NOTE 3: The referee test (destructive) to determine propagation of measling or crazing is to precondition the test specimen and solder float the specimen on a solder bath at a temperature of $260^{\circ}\text{C} \pm 6^{\circ}\text{C}$ ($500^{\circ} \pm 10^{\circ}\text{F}$) for a period of 5 seconds. Measling/crazing shall not propagate into a lesser class requirement or other defect category. (See IPC Test Method 2.6.8., except that the time and temperature shall be as shown above)

Courtesy of the IPC.

Table D-4 Acceptability Guidelines for Measling and Crazing: Printed Board Assemblies

<i>Class I: Consumer</i>	<i>Class II: General—Industrial</i>	<i>Class III: High-Reliability Life Support</i>
The only criterion for measling and crazing is that the assembly is functional.	Total area affected by measles or crazing shall not exceed 10% of the board area.	Total area affected by measles or crazing shall not exceed 2% of the board area.
This may be determined through functional testing or dielectric resistance measurements. (See Notes.)	There shall be no more than 80% reduction in space between electrically uncommon conductors. (See Notes.)	There shall be no more than 50% reduction in space between electrically uncommon conductors. (See Notes.)

NOTE 1: Repairs to boards are permissible provided that the repaired board meets the above criteria.

NOTE 2: The area of measling or crazing is determined by combining the area of each measles or craze and dividing by the total area of the printed board. A separate determination is made for each side of the board.

Courtesy of the IPC.

The evidence to date is that even boards with severe MEASLES have functioned adequately over long periods of time and in harsh environments. In fact, the IPC has no data which shows that a board which is "MEASLED" (and not subjected to other more serious conditions) has failed.

The committee established 3 classes of measles, one as applied to consumer products, one for general industrial use, and one for high reliability: life support systems. These findings and deliberations are detailed on pages 24 and 25.

Fig. D-1 IPC statement on measles.

Definitions, drawings, and photographs are provided for other conditions, but, acceptability guidelines are left to other documents.

2. Blistering and delamination are the same, except that delamination is small, localized areas is called "blistering."
3. Weave texture and weave exposure. Weave texture that is noticeable at the laminate surface is not a problem. When the glass fibers are not completely covered by resin, weave exposure is the result and may be cause for concern.
4. Haloing consists of light areas in the laminate around machined areas of the board.

SECTION 5. ETCHING CHARACTERISTICS

This section defines the terms used to discuss and measure the cross-sectional characteristics of conductors. It is noted that the trace width will generally increase (called "outgrowth") when screened-on resist is used for pattern plating and that the conductor width will generally decrease (called "undercut") when photoresist imaging is used for pattern plating. Thus, conductors will have a different cross-sectional appearance depending on the choice of imaging method.

1. Etch factor. This is the ratio of total copper thickness to overhang. Etch factor = copper/overhang (see Figure D-2, top right-hand corner).
2. Minimum conductor width (MCW), overall conductor width (OCW), and designed conductor width (DCW) are shown in Figure D-3.
3. Numerous photographs of etching conditions are shown.

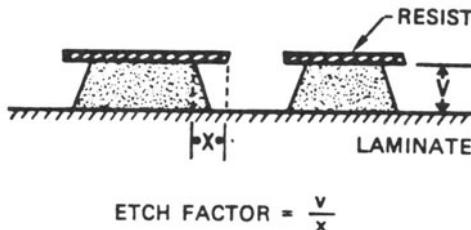


Fig. D-2 An etch factor of 1:1 is usually considered practical. Higher factors may be specified for some applications.

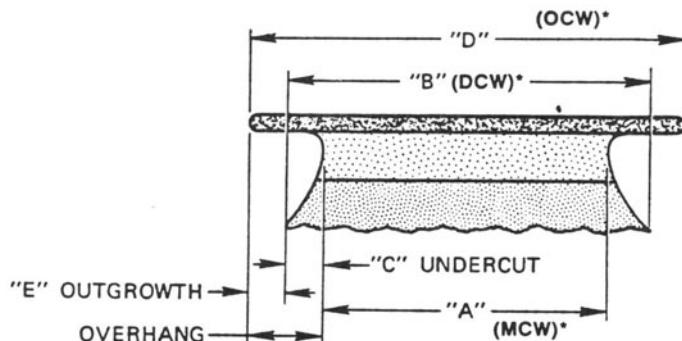


Fig. D-3 Cross section of a pattern plated conductor after dry film photoresist imaging.

SECTION 6. CONDUCTOR

This section defines conditions which may affect conductors, and presents drawings and photographs of these conditions. It also describes how these conditions are to be measured.

1. Various conditions are explained in Figures D-4 and D-5 from this document. They include edge roughness, indentations, and isolated projections measured along a span of the conductor, usually a .500-inch section.

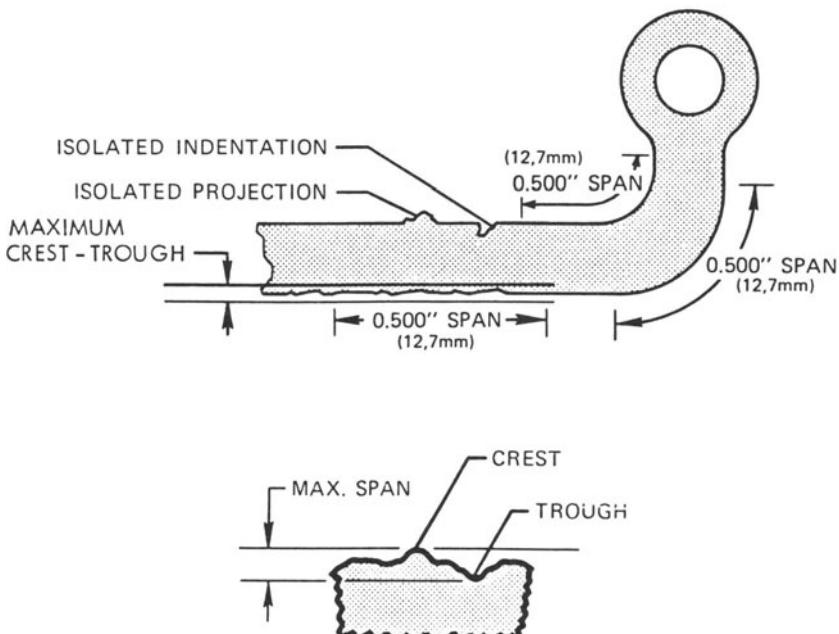


Fig. D-4 Irregular conditions on conductor edges.

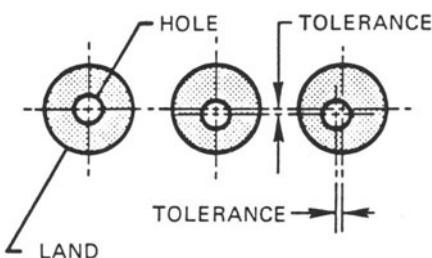


Fig. D-5 Misregistration.

2. Isolated projections are permissible as long as minimum conductor spacing is not violated.
3. Edge roughness is defined here but allowable limits are set by other documents, usually specified by contract or blueprint/procurements specifications.
4. Registration is determined by measuring the distance from the center of the hole to the center of the land area about that hole (see Figure D-5).
5. Conductor edge definition is defined as preferred, acceptable, or rejectable.

SECTION 7. FABRICATION

Drilling and machining of holes and edges are discussed, together with the appropriate measuring method. Preferred, acceptable, and rejectable conditions are depicted.

1. Land registration. Misregistration is acceptable provided minimum annular ring requirements are not violated.
2. Sawing/routing edge conditions. Only smooth edges are acceptable. No burrs are acceptable; they must be filed or sanded.
3. Solder mask registration. Solder mask on the pads is acceptable provided sufficient land is exposed to form an adequate solder fillet during soldering.

NOTE: This is often interpreted to mean that a minimum annular ring requirement must be met for the land area exposed by the solder mask.

4. Chamfering (beveling along edges of contact fingers). Slight burrs are acceptable provided bridging due to burrs does not violate any specified conductor tolerance or spacing requirement. Lifted metal and loose glass fibers are rejectable, along with excessive burring.
5. Nonplated drill holes. Slight burrs and glass fibers are acceptable. Excessive degrees of these conditions indicate lack of process control and are rejectable.

SECTION 8. EYELETING

Acceptability guidelines, together with appropriate photographs, are displayed for funnel, flat, and rolled eyelets. There is a caution against using eyelets for through connections, as improper assembly may result in intermittent open circuits.

SECTION 9. LEGENDS

Legends may be either etched on or applied by screen printing or stamping. They must be legible and permanent and must not interfere with the function of the circuit in any way.

SECTION 10. FLUSH PRINTED BOARDS

The acceptability guidelines for these boards, which are identical to those for traditional printed circuit boards, are listed in this section by page number. Flush printed circuit conductors are rejectable if they are not flush, with the height above the base material or the surrounding insulating material exceeding allowable tolerances.

SECTION 11. FLEXIBLE PRINTED BOARDS

Guidelines for these boards are similar to those for rigid boards. There is a set of photographs which show examples of delamination of the cover coat and the plated-through holes. Flexible and rigid-flex circuits are covered in Chapter 6 of this book.

SECTION 12. MULTILAYER PRINTED BOARDS

Most of the acceptability guidelines discussed thus far also apply to multilayer printed circuits. There are, however, additional concerns related to the plated-through holes and to inner layer integrity and registration. Coupons should be run with multilayer circuitry. This allows destructive testing (such as microsectioning) to be performed without having to sacrifice an otherwise acceptable circuit.

1. Integrity of the plating junction of the plated hole and inner layer must be assured by the use of chemical cleaning or etchback processing.
2. Minimum annular rings at plated holes and layer-to-layer registration are measured by X-ray photography or mutually perpendicular microsections.
3. Lamination integrity is verified by inspecting for air entrapment, layer-to-layer delamination, and localized blisters (delamination).
4. Electrical integrity is verified by checking for power-to-ground shorts; followed by continuity testing of the circuitry.
5. Photographs of preferred, acceptable, and rejectable conditions are shown.

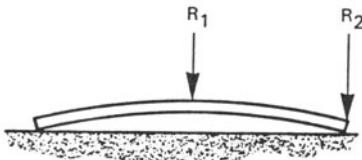
SECTION 13. BOW AND TWIST

This section presents charts which show allowable variations for single, double, and multilayered circuitry according to the type of material and board thickness. The techniques to be used for determining bow and twist are shown. This section is reproduced here (see Figure D-6).



The board shall be placed unrestrained on a flat horizontal surface (surface plate) with the convex surface of the panel upward, the maximum vertical displacement shall be measured.

METHOD A INDICATOR HEIGHT GAGE —



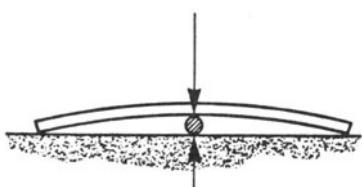
BOW

- 1 Place the printed board on a flat surface
- 2 Take reading at edge of the printed board contacting flat surface R₂
- 3 Take reading at maximum vertical displacement R₁
- 4 Subtract R₂ from R₁

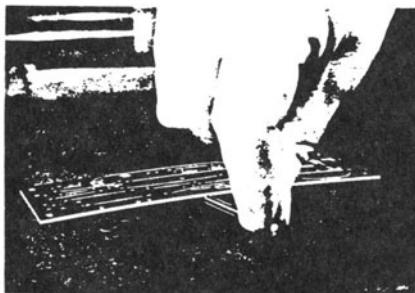
NOTE Care must be taken to make both readings on circuitry or base material

- 5 Multiply length of printed board by allowable inch per inch bow (Table I, II or III)
- 6 The difference of R₂ from R₁ should be equal to or less than the product in step 5

METHOD B FEELER GAGE —



- 1 Place the printed board on a flat surface
- 2 Multiply length or width of the printed board by inch inch bow (Table I, II or III)
- 3 Select feeler gage (gage blocks, or gage blanks), for the maximum allowance
- 4 Attempt to slide feeler gage under printed board at point of greatest deviation
- 5 If the feeler gage does not enter under the printed board the printed board is within tolerance. If gage enters under the printed board, the printed board is out of tolerance



TWIST

Use either method described above, but measure diagonally (corner to corner) for inch per inch multiplier

Fig. D-6 How to measure bow and twist on finished printed circuits. (Courtesy IPC)

IPC-TMM-650

2 1 1	Microsectioning
2 1 5	Surface Examination
2 2 7	Hole Size Measurement, Plated
2 2 9	Overhang & Undercut Measurement
2 2 10	Registration of Conductors
2 2 11	Registration, Terminal Pads (Layer to Layer)
2 2 13 1	Thickness, Plating in Holes, Micro-Ohm Method
2 3 4	Chemical Resistance, Legend Paints & Inks
2 3 11	Glass Fabric Examination
2 4 1	Adhesion, Plating
2 4 14	Solderability of Metallic Surfaces
2 4 22	Warp & Twist
2 5 4	Current Carrying Capacity, Multilayer Printed Boards
2 5 7	Dielectric Withstanding Voltage, Printed Board Material
2 5 16	Shorts, Internal on Multilayer Printed Boards
2 6 10	X-Ray (Radiology) Multilayer Printed Boards
5 8 1	Flexible Circuit Test Pattern
5 8 4	Rigid Multilayer Test Pattern

Fig. D-7 Tabulation of related test methods.

SECTION 14. FLAT CONDUCTOR, FLAT CABLE

Some areas of these types of circuitry are the same as those for printed circuits. These areas of commonality are listed, with a brief discussion.

SECTION 15. APPENDIX

This is a tabulation of test methods from IPC-TMM-650 (see Figure D-7). The appendix reproduces that actual test method.

Appendix E

MIL-P-13949F: Plastic Sheet, Laminated, Metal Clad (for Printed Wiring Boards)

This document is the industry standard for referencing materials for rigid printed circuit boards. It contains information on laminate and prepreg for all military recognized material types. The material designation is different from that of the National Electronics Manufacturing Association (NEMA) and must be understood; for example, instead of FR-4, the military designation is GF.

This specification has six sections plus an extensive appendix. The sections will not be fully discussed separately; but they are listed here: (1) Scope, (2) Applicable Documents, (3) Requirements, (4) Quality Assurance Provisions, (5) Packaging, (6) Notes, (7) Appendixes.

SECTION 1. SCOPE

Paragraph 1.1 states: “This specification covers the requirements for fully cured, metal-clad laminated, plastic sheets (glass and paper base) and semicured (B stage), resin-preimpregnated glass cloth (prepreg) to be used primarily for the fabrication of printed-wiring boards for electrical and electronic circuits (see 3.1 and 6.1). For the purposes of this specification, the term ‘laminate’ will be used hereafter to denote metal-clad plastic sheets and the term ‘prepreg’ will be used to denote resin preimpregnated glass cloth (B stage). The term ‘reinforced’ will be used to denote a glass laminate and ‘nonreinforced’ will denote a laminate with no glass reinforcement.”

The two materials, laminate and prepreg, each have their own type designation system. Also, in the back of this specification is a set of material specification sheets for each type of material. Designers often specify material on drawings as, for instance, MIL-P-13949F/4. This designation actually specifies GF material (NEMA designation: FR-4). This subject will be covered below.

1. Laminate, reinforced and nonreinforced, type designation.

<i>GFN</i>	<i>0310</i>	<i>CH/DI</i>	<i>A</i>	<i>I</i>	<i>A</i>
Base material	Nominal base thickness	Type and nominal weight of copper foil	Grade of pits and dents	Class of thickness tolerance	Class of bow and twist
(A)	(B)	(C)	(D)	(E)	(F)

- a. Base materials are separated into 11 types. Unless otherwise designated, glass fiber is woven, compared to nonwoven, matte fibers.
- (1) PX—Paper base, epoxy resin, flame resistant.
 - (2) GB—Glass base, epoxy resin, heat resistant, retains strength when hot.
 - (3) GE—Glass base, epoxy resin, general purpose.
 - (4) GF—Glass base, epoxy resin, flame retardant.
 - (5) GH—Glass base, epoxy resin, heat resistant (retains strength when hot) and flame retardant.
 - (6) GP—Glass base (nonwoven fiber), polytetrafluoroethylene resin, flame retardant.
 - (7) GR—Glass base (nonwoven fiber), polytetrafluoroethylene resin, flame retardant, for microwave application.
 - (8) GT—Glass base, polytetrafluoroethylene resin, flame retardant.
 - (9) GX—Glass base, polytetrafluoroethylene resin, flame retardant, for microwave application.
 - (10) GI—Glass base, polyimide resin, high temperature, heat resistant.
 - (11) GY—Glass base, polytetrafluoroethylene resin, flame resistant, for microwave application.

The third letter (example: N in GFN) designation:

N—Base material without coloring agent or opacifier; frequently referred to as “natural.”

P—Base material with coloring agent or opacifier. When P is specified on a drawing, as in “GFP,” the planner or quality assurance person must look for a designated color, such as blue.

- b. Nominal base thickness is designated by a four-digit number. This identifies the thickness to a ten-thousandth of an inch. Note that this excludes any metal cladding and refers strictly to the base (often referred to as “core”) thickness.

EXAMPLES: 0050 = .0050 inch = 5.0 mils

: 0140 = .0140 inch = 14.1 mils

: 0305 = .0305 inch = 30.5 mils

- c. Type and nominal weight of copper foil five characters. There are two characters, a slash mark, and two more characters. Note that the slash mark is the third character. Example: CH/D1

- (1) The letters C and D (first and fourth characters) indicate the type of copper foil cladding. Copper foil will be of the following types:

A — Rolled
 B — Rolled (treated)
 C — Drum side out, electrodeposited
 D — Drum side out (double treated), electrodeposited
 E — Matte side out, electrodeposited
 F — Matte side out (double treated), electrodeposited
 O — Unclad

- (2) The H and 1 (second and fifth characters) indicate the nominal copper foil weight in ounces per square foot. If the foil cladding is 1 oz/sq ft or more, the actual ounce number shall be used in the designation. If the foil cladding is less than 1 oz/sq ft one of the letter indicators shown below shall be used.

Foil Thickness Designations

E—1/8 oz/sq ft	1 = 1 oz/sq ft
Q—1/4 oz/sq ft	2 = 2 oz/sq ft
T—3/8 oz/sq ft	
H—1/2 oz/sq ft	
O—unclad	

- d. The grade of pits and dents is designated by letter A, B, or C. These grades differ by the point count allowed.

Grade A: The total point count in any 12 × 12-inch area shall be less than 30.

Grade B: The total point count in any 12 × 12-inch area shall be less than 30. There shall be no pits greater than .015 inch in the longest dimension. There shall be no more than three pits in a 12 × 12-inch area with the longest dimension over .005 inch.

Grade C: The total point count in any 12 × 12-inch area shall be less than 100.

Point count for pits and dents is as follows:

<i>Longest Dimension (Inches)</i>	<i>Point Value</i>
.005 to .010 inch inclusive	1
.011 to .020 inch inclusive	2
.021 to .030 inch inclusive	4
.031 to .040 inch inclusive	7
Over .040 inch	30

- e. The class of thickness tolerance is designated by the number 1, 2, 3, or 4; these are the four classes. Thickness and tolerances do not apply to the outer 1.0 inch of a trimmed full-sized sheet. At least 90% of the sheet must meet the thickness class requirement, and no portion of the sheet shall vary more than 125% of the specified tolerance. Cut sheets of GP, GR, GT, GX, and GY shall meet the thickness tolerance requirement for the specified class in 100% of the area.

NOTE: The tolerance varies in each class with the nominal thickness of the laminate. Table E-1 lists the nominal thicknesses and tolerances.

- f. The class of bow and twist is designated by letter A, B, C, or X. Classes A and B apply to full-size sheets of laminate. Class C applies only to laminate which has been cut to panel size. Class X indicates that bow and twist requirements are not applicable to single-sided laminates or to any other laminate with a base thickness of less than .020 inch. Table E-2 shows permissible bow and twist for full-size sheet classes A and B. Table E-3 shows the requirements for cut panels.
2. Prepregs and copper foils will not be discussed in depth here. However, Table E-4 is reproduced. This contains some information on glasses and prepregs. Table E-5 contains information on copper foil thickness and tolerance. Table E-5 is also reproduced here. Both the copper foil manufacturer and the laminate manufacturer must go through a certification process for their materials which is similar to the certification process called out under MIL-P-55110D for the printed circuit manufacturer. A discussion of this

Table E-1 Nominal Thickness and Tolerances for Laminates (Inch)

<i>Thickness</i>	<i>Class</i>		<i>Class 2 Glass Reinforced</i>	<i>Class 3¹ Glass Reinforced</i>	<i>Class 4 for Microwave Application</i>
	<i>Paper Base Only</i>	<i>Glass Reinforced</i>			
.0010 to .0045	—	±.0010	±.00075	±.0005 ²	—
.0046 to .0065	—	±.0015	±.0010	±.00075 ²	—
.0066 to .0120	—	±.0020	±.0015	±.0010 ²	—
.021 to .0200	—	±.0025	±.0020	±.0015 ²	—
.001 to .0299	—	±.0030	±.0025	±.0020 ²	—
.030 to .040 ²	±.0045	±.0065	±.0040	±.0030	±.002
.041 to .065 ²	±.0060	±.0075	±.0050	±.0030	±.002
.066 to .100 ²	±.0075	±.0090	±.0070	±.0040	±.003
.101 to .140 ²	±.0090	±.0120	±.0090	±.0050	±.0035
.141 to .250 ²	±.0120	±.0220	±.0120	±.0060	±.0040

¹These tighter tolerances are available only through product selection.

²Overall thickness including the copper foil (see 1.2.1.1.2).

Table E-2 Permissible Bow and Twist

Thickness (Inch) (see Table E-1)	Total Variation, Maximum, Percent (on Basis of 36-Inch Dimension) ¹					
	Class A			Class B		
	All Types, All Weights Metal (One Side)	All Types, All Weights Metal (Two Sides)	Glass	All Types, All Weights Metal (One Side)	All Types, All Weights Metal (Two Sides)	Glass
Over 0.020—	—	5	—	—	2	—
.030 or .031—	12	5	6	10	2	5
.060 or .062—	10	5	6	5	1	2.5
.090 or .093—	8	3	3	5	1	2.5
.120 or .125—	8	3	3	5	1	2.5
.240 or .250—	5	1.5	1.5	5	1	1.5

¹These values apply only to sheet sizes as manufactured and to cut pieces having either dimension not less than 18 inches.

²For nominal thicknesses not shown in this table (see 6.2), the bow or twist for the next lower thickness shown shall apply.

Table E-3 Bow and Twist or Cut-to-Size Panels

Thickness ² (inch) (See Table E-1)	Panel Size (Maximum Dimension, Inches)	Total Variation, Maximum, Percent			
		Laminate—Class C			
		All Weights of Foil, One Side	All Weights of Foil, Two Sides	All Other Types	Types GP, GR GT, GX, GY
Over .020	8 or less	2.0	—	1.0	—
	8 to 12	2.0	—	1.5	—
	Greater than 12	2.5	—	1.5	—
.030 or .031	8 or less	1.5	3.0	.5	3.0
	8 to 12	1.5	3.0	1.0	3.0
	Greater than 12	2.0	3.0	1.0	3.0
.060 and over	12 or less	1.0	1.5	.5	1.5
	Greater than 12	1.5	1.5	.5	1.5

¹Except when otherwise specified (see 3.1).

²For nominal thicknesses not shown in this table (see 6.2), the bow and twist for the next lower thickness shown shall apply.

process begins at paragraph 4.0. Only materials certified to MIL-P-13949F (or latest revision) should ever be used in printed circuits which must be certified to MIL-P-55110D.

Table E-4 Construction Characteristics

Range of Thicknesses ⁴	Glass Cloth						Prepreg		
	Glass Style		Representative Thickness (Inch) ¹	Thread Count per Inch		Weight per Sq. Yd. (Ounces) ^{1,2}			
	Plied	Unplied		Warp	Fill				
Range A	—	104	.0012 ±.0005	60 ± 3	52 ± 3	0.59 ± 10%	60–85 .0010–.0025		
	—	106	.0014 ±.0005	56 ± 3	56 ± 3	0.73 ± 10%	60–95 .0010–.0030		
Range B	107	—	.0019 ±.0005	60 ± 3	35 ± 3	1.10 ± 10%	55–75 .0020–.0035		
	108	1080	.0022 ±.0005	60 ± 3	47 ± 3	1.40 ± 10%	55–75 .0020–.0035		
Range C	112	2112	.0031 ±.0010	40 ± 3	39 ± 3	2.10 ± 10%	50–70 .0030–.0045		
	113	—	.0028 ±.0005	60 ± 3	64 ± 3	2.50 ± 10%	50–70 .0030–.0045		
—	2113	—	.0030 ±.0005	60 ± 3	56 ± 3	2.40 ± 10%	50–70 .0030–.0045		
	1125	—	.0033 ±.0010	40 ± 3	39 ± 3	2.60 ± 10%	N/A N/A		
Range D	2125	—	.0037 ±.0010	40 ± 3	39 ± 3	2.60 ± 10%	N/A N/A		
	116	—	.0037 ±.0010	60 ± 3	58 ± 3	3.20 ± 10%	40–60 .0035–.0050		
—	2116	—	.0040 ±.0010	60 ± 3	58 ± 3	3.20 ± 10%	40–60 .0035–.0050		

	—	1675	.0040 ±.0010	40 ± 3 36 ± 3	32 ± 3 34 ± 3	2.90 ± 10% 3.70 ± 6%	45–65 N/A	.0035–.0050 N/A
Range E	1528	—	.0065 ±.0010	42 ± 3 44 ± 3	32 ± 3 32 ± 3	6.10 ± 6% 6.00 ± 6%	35–50 35–50	.0060–.0085 .0060–.0085
N/A	127	—	.0074 ±.0010	42 ± 3 42 ± 3	32 ± 3 32 ± 3	6.10 ± 6% 6.00 ± 6%	— —	— —
	128	—	.0067 ±.0010	42 ± 3 44 ± 3	32 ± 3 22 ± 3	6.00 ± 6% 7.00 ± 6%	— —	— —
	—	7637	.0092 ±.0010	44 ± 3 44 ± 3	20 ± 3 20 ± 3	6.80 ± 6% 6.80 ± 6%	— —	— —
	—	7642	.0099 ±.0010					

¹Based on greige goods state.

²Based on overall width excluding selvages.

³Cured thickness is dependent upon the combined factors of resin content and resin flow percent, and, as such, no nominal thickness for any prepreg can be considered meaningful. These values should not be used for computation of dielectric thickness in multilayer board design.

⁴Each range includes glass styles and/or prepreg that will result in equivalent cured thicknesses. The range groupings are provided for extension of qualification purposes (see 4.5.3).

Table E-5 Copper Thickness and Tolerance

<i>Nominal Weight (oz./ft²)</i>	<i>Tolerance by Weight (Percent)</i>		<i>Nominal¹ Thickness, Inches (Microns)</i>	<i>Tolerance¹ Inches (Microns)</i>
	<i>Class I</i>	<i>Class II</i>		
1/8	±10	±5	.00020 (5.0)	—
1/4	±10	±5	.00036 (9.0)	—
3/8	±10	±5	.00052 (13.0)	—
1/2	±10	±5	.0007 (17.5)	±.0001 (2.5)
3/4	±10	±5	.0010 (25.0)	±.0002 (5.0)
1	±10	±5	.0014 (35.0)	±.0002 (5.0)
2	±10	±5	.0028 (70.0)	±.0003 (7.5)
3	±10	±5	.0042 (105.0)	±.0004 (10.0)
4	±10	±5	.0056 (140.0)	±.0006 (15.0)
5	±10	±5	.0070 (175.0)	±.0007 (17.5)
6	±10	±5	.0084 (210.0)	±.0008 (20.0)
7	±10	±5	.0098 (245.0)	±.0010 (25.0)
10	±10	±5	.0140 (350.0)	±.0014 (35.0)
14	±10	±5	.0196 (490.0)	±.0020 (50.0)

¹Derives by weight test method 2.2.12 of IPC-CF-150.

3. Paragraph 4.8.2 begins a section on prepreg inspection that will be of use to quality assurance people. Areas of concern and testing include:
 - a. Presence of dicyanodiamide crystals. See note at paragraph 6.11.
 - b. Thread count, glass cloth thickness, and fabric weight.
 - c. Resin gel time.
 - d. Volatiles content.
 - e. Resin content.
 - f. Resin flow.
 - g. Cured thickness.
 - h. Electrical strength.
 - i. Dielectric constant and dissipation factor.

4. Paragraph 4.8.3 begins a section on laminate inspection which will be of use to quality assurance people. Areas of concern and testing include:
 - a. Pits and dents.
 - b. Scratches.
 - c. Solderability.
 - d. Etch characteristics of the metal-clad surfaces.
 - e. Plastic surface contamination (unclad side).
 - f. Bow and twist.
 - g. Thermal stress.
 - h. Peel strength of foil
 - Before and after thermal stress.

- Before and after temperature cycling.
- At elevated temperatures.
- After exposure to process conditions.
- i. Volume and surface resistivity.
- j. Dimensional stability.
- k. Water absorption.
- l. Dielectric breakdown voltage.
- m. Electrical strength.
- n. Dielectric constant and dissipation factor.

15. PACKAGING

- 5.1 *Preservation.* Unless otherwise specified (see 6.2), clean and dry metal-clad laminates shall be interleaved with noncorrosive sheets to prevent abrasion. Unless otherwise specified (see 6.2), preimpregnated glass cloth shall be unit packaged and sealed in polyethylene bags in a manner that will afford adequate protection against corrosion, deterioration and physical damage during shipment and storage. The unit packaging shall be in a manner that will afford adequate protection against corrosion, deterioration, and physical damage during shipment from the supply source to the first receiving activity. This may conform to the contractor's commercial practice when such meets the requirements specified herein. The unit contractor shall be as specified in 5.2.
- 5.2 *Packing.* The metal-clad laminates and preimpregnated glass cloth shall be packed in shipping containers in a manner that will afford adequate protection against damage during direct shipment from the supply source to the first receiving activity. These packs shall conform to the applicable carrier rules and regulations and may be the contractor's commercial practice if these requirements are met.
- 5.3 *Marking.* In addition to any special marking required on the contract (see 6.2), each unit package and exterior container shall be marked with the following information (when applicable):
 - a. Specification number and type of material.
 - b. Manufacturer's material designation and lot number.
 - c. Quantity, unit of issue and roll or sheet dimensions.
 - d. Gross weight and cube.¹
 - e. Date packed.¹
 - f. Contract number.
 - g. Manufacturer's (contractor's) name and address.
 - h. Name and address of consignee.¹
 - i. Cloth batch number and contractor's designation.²
 - j. Resin batch number and contractor's designation.²
 - k. Date of manufacture (impregnation) and manufacturer's recommended storage conditions (see 3.6.10).²
- 5.4 *General.* Exterior containers shall be of a minimum tare and cube consistent with the protection required and contain equal quantities of identical items to the greatest extent practicable.

¹ Required for shipping containers only.

² Required for resin preimpregnated glass cloth materials only.

Fig. E-1 Packaging requirements for materials.

- o. Measurements of base materials GR and GX at X-band frequency.
- p. Q (resonance) when applicable.
- q. Flexural strength: ambient and elevated temperatures.
- r. Arc resistance.
- s. Flammability, when applicable.

**SECTION 5. PACKAGING, COVERS PRESERVATION,
PACKAGING, AND MARKING OF MATERIAL CERTIFIED TO MIL-
P-13949F**

This section is important and will be reproduced here. If a printed circuit manufacturer is buying materials which must be certified to MIL-P-13949F, all of these requirements must be met as the material comes into the shipping department (see Figure E-1).

SECTION 6. NOTES

This section contains useful notes, explanations, and definitions.

APPENDIXES

Appendix A: X-Band Effective Stripline Dielectric Constant and Dissipation Factor for Copper Clad Glass Woven Fabric GR and GX Laminate

Appendix B: Two Fluid, Three Terminal Method for the Measurement of Dielectric Properties at 1 MHz

Appendix C: Two Terminal, Contacting Electrodes Method for Measurement of Dielectric Properties

Appendix F

MIL-STD-2118: Design Requirements for Flex and Rigid-Flex Printed Wiring for Electronic Equipment

MIL-STD-2118 is one of the cornerstone documents in the world of flex and rigid-flex circuitry. If design, quality assurance, and planning personnel wish to become familiar with only one document to govern their flex programs, this is the one they should know. Many pitfalls in design can be avoided by following the design rules laid out here. No incoming/artwork inspection can be considered complete or accurate without a review of blueprints and artwork for conformance to the rules of this standard. The person who provides job quotations must perform a cursory engineering review to this standard in order to fully understand the consequences of what is being quoted.

This document is composed of six sections and an appendix: (1) Scope, (2) Referenced Documents, (3) Definitions, (4) General Requirements, (5) Detail Requirements, (6) Detail Part Mounting Requirements, and Appendix: Design Considerations.

SECTION 1. SCOPE

This section states the purpose of the standard and lists the classifications of flex circuitry. The purpose (from paragraph 1.1) is to accomplish the following:

1. To establish design requirements governing the following types of printed wiring:
 - a. Flexible printed wiring, with or without shields or stiffeners.
 - b. Rigid to flexible wiring (to be called “rigid-flex”), with or without plated-through holes.

2. To establish design considerations for mounting parts and assemblies thereon.
3. To establish the following requirements:
 - a. For rigid-flex applications, conductor layers that are in the flexible portion are also to be considered conductor layers in the rigid multilayer board.
 - b. All board types shall have the conductor patterns protected by an insulating layer, with two exceptions:
 - (1) Land areas do not have to be covered by an insulating layer.
 - (2) External conductors on the rigid portion of a type 4 rigid-flex circuit do not have to be covered by an insulating layer.
 - c. When components are mounted on flex or rigid-flex circuits, the mounting area must be conformally covered in accordance with MIL-I-46058.

There are five types of circuitry, depending on the number of layers. Types 1, 2, and 3 correspond to types 1, 2, and 3 listed in MIL-STD-275 and MIL-P-55110D: single-sided, double-sided, and multilayer. Type 4 is rigid-flex multilayer with plated-through holes, and type 5 is rigid-flex multilayer without plated-through holes. The five types of circuitry are:

- Type 1—Single-sided flex, with or without shields or stiffeners (one conductive layer).
- Type 2—Double-sided flex, with or without shields or stiffeners (two conductive layers).
- Type 3—Multilayer flex with plated-through holes, with or without shields or stiffeners (more than two conductive layers).
- Type 4—Multilayer rigid and flex combinations with plated-through holes (more than two conductive layers).
- Type 5—Bonded rigid or flex combinations without plated-through holes.

For each of the five types, there are two classifications:

- Class A—Capable of withstanding flexing during installation.
- Class B—Capable of withstanding continuous flexing for the number of cycles specified on the master drawing (generally not used for more than two conductive layers).

SECTION 2. REFERENCED DOCUMENTS

This section lists the titles and numbers of numerous federal, military, ANSI, and IPC specifications and standards. These are referenced throughout this stan-

dard. To fully understand all requirements of MIL-STD-2118, the reader must have a copy of these documents available for consultation.

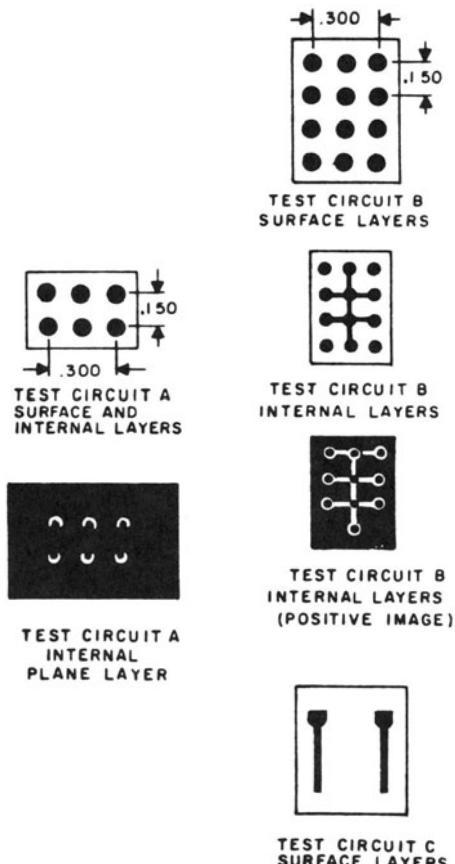
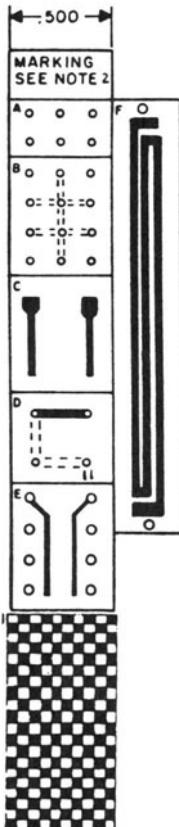
SECTION 3. DEFINITIONS

This section does two things. It defines "splay" (which is the tendency of a rotating drill to drill holes which are off-center, out of round, or nonperpendicular) and it states that all other terms and definitions shall be in accordance with IPC-T-50.

SECTION 4. GENERAL REQUIREMENTS

1. **Design Features.** Paragraph 4.1 states that quality conformance test coupons shall be included on the production master, master drawing, and artwork. The coupons are shown in Figure F-1. The coupons are to be .250 to .500 inch from the board edges and must reflect all of the manufacturing processes which the boards themselves will undergo.
2. **Master drawing.** Paragraph 4.2 establishes the requirements to be met by the master drawing. These requirements include:
 - a. Type, size, and shape of the flex or rigid-flex circuit.
 - b. Size and location of all holes.
 - c. Whether or not etchback is required.
 - d. Location of traceability markings.
 - e. Dielectric separation between layers.
 - f. Number and location of quality conformance test coupons.
 - g. Shape and arrangement of conductor and nonconductor patterns or elements.
 - h. Separate views of each conductor layer for flex and rigid-flex layers.
 - i. All pattern features not controlled by the hole size and locations shall be adequately dimensioned, either by specific dimensions or by notes on the blueprint.
 - j. Step or repeat of circuit patterns or quality conformance test coupons (that is, generation of working film) shall meet the requirements for production master accuracy (paragraph 4.3).
 - k. Definitions of all terms used on the drawing shall be in accordance with IPC-T-50.
 - l. Plating and coating thickness shall be specified on the master drawing.
 - m. The master drawing shall list all artwork considerations that were used in the design of the flex or rigid-flex printed circuit. This means that processing tolerances (minimum and maximum values) for trace width, conductor spacing, annular ring, etc. shall be noted somewhere on the

INCH	MM
.150	3.81
.300	7.62
.500	12.70



Quality conformance test circuitry (individual coupons).

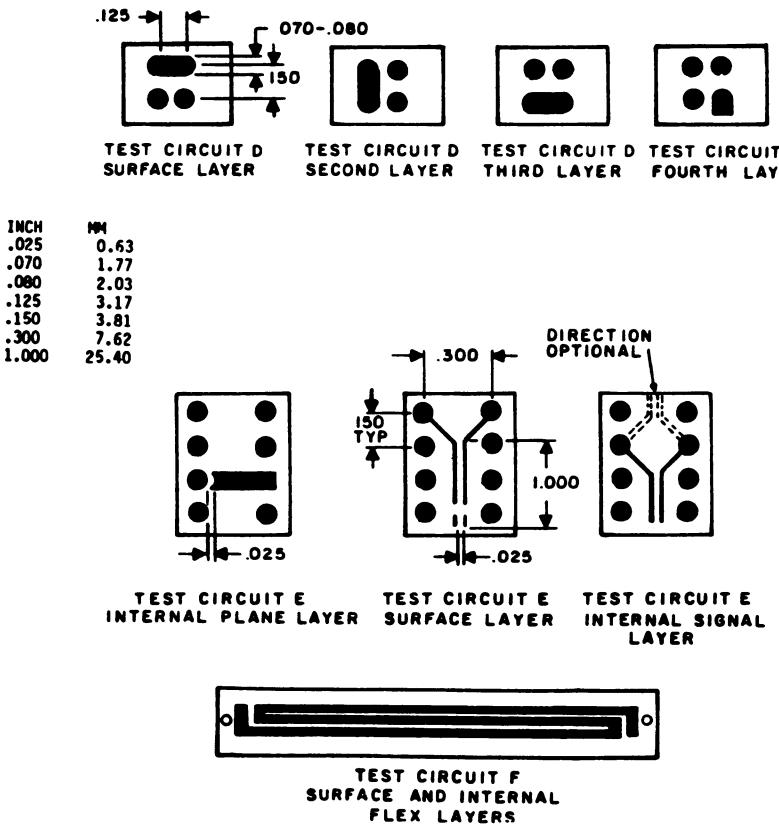
Quality conformance test circuitry layout.

Fig. F-1 Quality conformance test circuitry.

master drawing. This standard recognizes that the end product will not match the artwork exactly and that the allowable variations must be spelled out. All feature detail requirements (to be discussed in Section 5) shall be spelled out.

3. Number of Sheets for the Master Drawing

- If practical, the master drawing shall be kept to one sheet.
- Requirements for multisheet master drawings

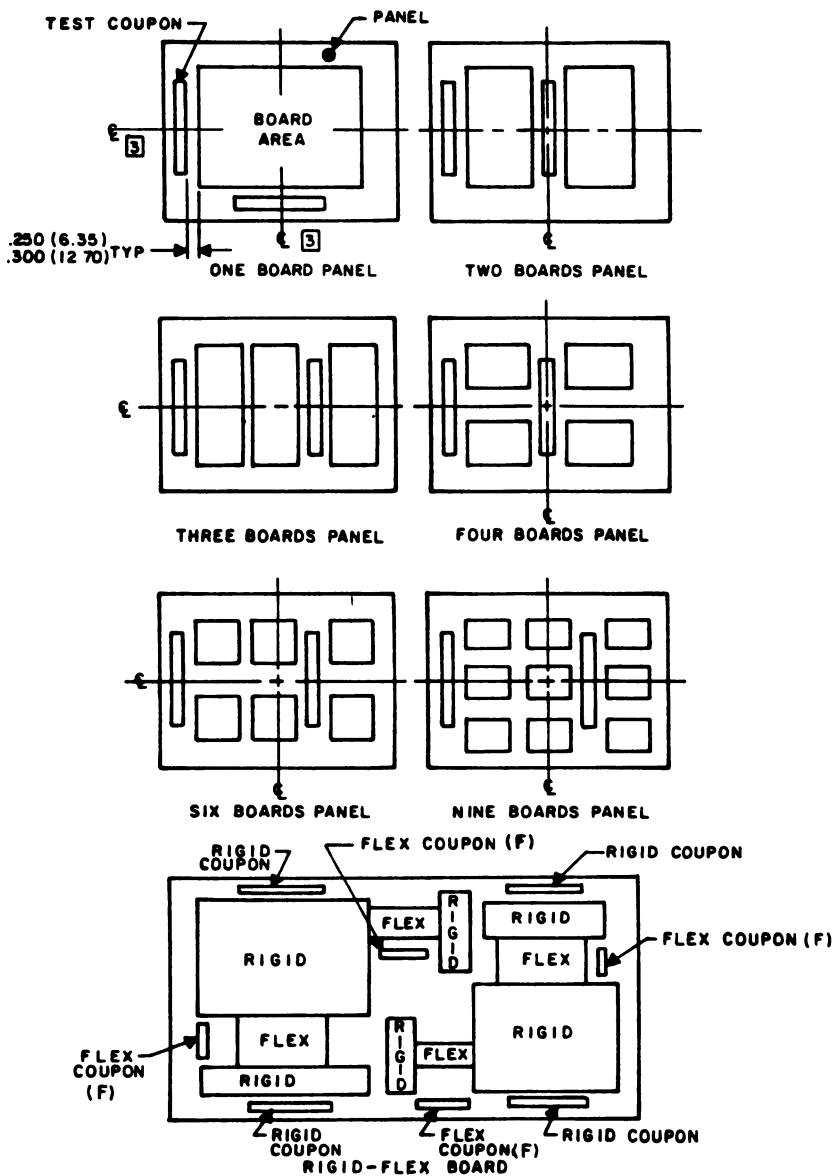


Quality conformance test circuitry (individual coupons).

Fig. F-1 (Continued)

The first sheets shall establish the size and shape of the printed circuit, stiffeners, hole diameters, tolerances and locations, and all notes. Pattern features not controlled by hole locations shall be dimensioned specifically, or by notes, on these first sheets.

- c. Subsequent sheets shall establish the shape and arrangement of conductor and nonconductor layers.
- d. Conductor layers are to be numbered sequentially from the component side. The first conductor layer is to be layer 1.
- e. Locations of manually applied markings (scribed or hand stamped) shall be described in notes.



Typical location of test coupon based on number of boards fabricated per panel.

Fig. F-1 (Continued)

NOTES:

1. Dimensions are in inches.
2. Test coupons are to be identified with the following:
 - a. FSCM.
 - b. Part number and revision letter.
 - c. Board traceability or lot number.
3. All lines shall be .020 (0.51 mm) $\pm .003$ (0.08 mm), unless otherwise specified.
4. Unless otherwise specified, the tolerances shall meet the requirements of this standard.
5. The minimum land dimensions shall be .070 (1.78 mm) $\pm .005$ (0.13 mm) and represent the land shape used on the associated board. Holes in lands shall be the diameter of the smallest component hole in the associated board.
6. All first layers and internal layers shall be as specified on the master drawing. Copper plane areas shall be used on all coupons on appropriate plane layers, except for the D and E segments. When shields are used (see 5.11) appropriate layers shall be added to the coupons.
7. The lengths of test circuits D and E are dependent upon the number of layers in the panel. For test circuits D, a pair of holes and a conductor between same shall be provided for each layer. Electrical connection shall be in series, stepwise, through each conductor layer of the board. For test circuit E, a pair of holes and conductors shall be provided for the first layer and each internal layer.
8. Coupon F shall be positioned in the flexible area on the associated board.
9. The quality conformance test circuitry may be segmented; however, test circuitry A and B shall be joined together. Test circuit C, D, E, and F may be arranged to optimize board layout. All test coupons illustrated shall appear on each panel. The number of layers shall be identical to the number of layers in the boards derived from the panel.
10. Letters on coupons are for identification purposes only and shall be etched or applied by the use of a permanent ink which will withstand board processing. Location of letters on applicable coupons is optional.
11. Number of layers shown in these test coupons are for illustration purposes only. Conductor layer number 1 shall be the first layer on the component side, and all other conductor layers shall be counted consecutively downward through the laminated board to the bottom conductor layer which is the solder side. Surface layers shall consist of the outer layers of a printed-wiring board, the first layer (component side) and the last layer (solder side).

Fig. F-1 (Continued)

- f. Photographically applied markings (legend and solder mask) shall have locations and methods specified on a separate sheet, preferably the last sheets in the set.
4. Other Requirements for the Master Drawing
 - a. Location dimensioning. Holes, test points, lands, and overall dimensions shall be specified by the use of a grid pattern. The grid shall be .100, .050, or inch .025 or another multiple of .005 inch. There is other information in paragraph 4.2.3 which is of interest to a designer.
 - b. Hole patterns. Each distinctive set of holes shall be dimensioned from a primary or secondary grid system. Types of holes include plated-through holes, tooling holes, mounting holes, windows, access holes, etc. Each

Table F-1 Board Design Guidelines

	<i>Preferred</i>	<i>Standard</i>	<i>Reduced Producibility</i>
Number of conductive layers (types 3 and 4)	6	12	20
Composite thickness tolerance (types 1, 2, 3, and 4)	+, -20% of nominal	+, -15% of nominal	+, -10% of nominal or +, -0.010 inch, whichever is greater
Thickness of dielectric rigid materials—type 4 (min.)	.008 (.20)	.006 (.15)	.0035 (.089)
Flex-polyimide—types 1, 2, 3, and 4 (min.)	.002 (.05)	.002 (.05)	.0015 (.038)
Stiffeners	.031 (.79)	.062 (.6)	.090 to .125 (2.3 to 3.2)
Minimum conductor width (or Figure 4 value, whichever is greater)			
Internal	.15 (0.38)	.008 (0.20)	.004 (.10)
External	.20 (0.51)	.015 (0.38)	.008 (.20)
Conductor width tolerance			
Unplated 2 oz/ft ²	+.004 (.10) -.006 (.15)	+.002 (.05) -.005 (.13)	+.001 (0.025) -.003 (0.08)
Unplated 1 oz/ft ²	+.002 (.05) -.003 (.08)	+.001 (.025) -.002 (.05)	+.001 (.025) -.001 (.025)
Unplated 1/2 oz/ft ²	—	—	+.0005 / -.001 (.013/.03)
Metallic etch resist in external layers			
Over 2 oz/ft ² Cu	+.008 (.20) -.006 (.15)	+.004 (.10) -.004 (.10)	+.002 (.05) -.002 (.05)
Minimum conductor spacing (or Table 1, whichever is greater)	.015 (.38)	.008 (.20)	.004 (.10)
Annular ring plated-through hole (min.) (See 5.2.2)			
Internal	.008 (.20)	.005 (.13)	.002 (.05)
External	.010 (.25)	.008 (.20)	.005 (.13)
Annular ring unsupported hole, rigid and flex (min.)	.020 (.51)	.015 (.38)	.010 (.25)
Feature location tolerance (rtp) (types 1, 2, 3, and 4) (master pattern and registration)			
Longest dimension (12 inches or less)			
Feature pattern (rtp) area of types 3 and 4	.006 (.15)	.005 (.13)	.004 (.10)
Feature pattern (rtp) area of types 1 and 2	.015 (.38)	.010 (.25)	.008 (.20)

Table F-1 (*Continued*)

	<i>Preferred</i>	<i>Standard</i>	<i>Reduced Producibility</i>
Longest dimension (over 12 inches) (rtp)			
Feature pattern (rtp)			
area of types 3 and 4	.008 (.20)	.007 (.18)	.006 (.15)
Feature pattern (rtp)			
area of types 1 and 2	.025 (.64)	.020 (.51)	.015 (.38)
Predicted on total board configuration (see 4.2.6)			
Master pattern accuracy (rtp)			
Longest board dimension 12 inches or less	.004 (.10)	.003 (.08)	.002 (.05)
Longest board dimension over 12 inches	.005 (.13)	.004 (.10)	.003 (.08)
Feature size tolerance	+, - .003 (.08)	+, - .002 (.05)	+, - .001 (.025)
Composite thickness to hole diameter	3:1	4:1	5:1
Rigid (types 3 and 4) max.			
Hole location tolerance (rtp)			
Component mounting area—dimension of 12 inches or less	.007 (.18)	.005 (.13)	.003 (.08)
Component mounting area—dimension of over 12 inches	.010 (.25)	.008 (.20)	.005 (.13)
Unplated hole diameter tolerance (unilateral)			
Up to .032 (.81)	.004 (.10)	.003 (.08)	.002 (.05)
.033			
.063	.006 (.15)	.004 (.10)	.002 (.05)
.064			
.188	.008 (.20)	.006 (.15)	.004 (.10)
Plated hole diameter tolerance (unilateral); for minimum hole diameter maximum board thickness ratios greater than 1.4, add .004 (.10) inch			
.015 (.38)			
.030 (.76)	.008 (.20)	.005 (.13)	.003 (.08)
.031 (.79)			
.061 (1.56)	.010 (.25)	.006 (.15)	.004 (.10)
.062 (1.59)			
.186 (4.75)	.012 (.31)	.008 (.20)	.006 (.15)
Conductor, including terminal pads to edge of composite (min)			

Table F-1 (Continued)

	<i>Preferred</i>	<i>Standard</i>	<i>Reduced Producibility</i>
Conductor, including terminal pads to edge of composite (min) (Continued)			
Types 3 and 4	.100 (2.54)	.075 (1.90)	.050 (1.27)
Types 1 and 2	.100 (2.54)	.050 (1.27)	.025 (.63)
Bending of flex (internal radius) thickness			
Class A .003 to .010 (.08 to .25)	6 × material thickness	1 × material thickness	
Over .010 (.25)	12 × material thickness	2 × material thickness	1 × material thickness
Class B .020 max (.51)	1 inch	1/2 inch	1/4 inch
Continuous flex cycles (based 1 oz./ft² copper, .002 inch dielectric) thickness			
.003 to .008 (.08 to .20)	1000	100,000	500,000
Over .008 to .014 (.20 to 0.36)	500	50,000	250,000
Over .014 (.36)	250	25,000	100,000

NOTE: Unless otherwise specified, all dimensions and tolerances are in inches. Data in parentheses () are expressed in millimeters.

NOTE: This figure is not shown. The reader should reference MIL-STD-2118.

- set may require separate dimensional tolerance considerations. Table F-1, which summarizes design guidelines, is reproduced here. These guidelines are based, like other military specifications, on producibility. Preferred, Standard, and Reduced Producibility are the three classes.
- c. **Data.** There shall be a minimum of two mutually perpendicular datum lines. Critical features with critical location requirements may be referenced by a secondary datum.
 - d. **Government-furnished master drawings** must be in accordance with this standard. Any deviations must be recorded on the government-approved master drawing.
5. **Assembly Drawings.** Requirements for assembly drawings are discussed beginning with paragraph 4.4. It is common for manufacturers of flex and rigid-flex to be required to perform some assembly. For this reason, it is a good idea to know the basic drawing requirements. Minimum requirements include:

- a. Lead-forming requirements.
- b. Cleanliness requirements per MIL-P-28809.
- c. Types of materials (conformal contain, masking, and potting).
- d. Location and identification of all components.
- e. Component orientation and polarity.
- f. Applicable ordering data from MIL-P-28809.
- g. Structural details, when required, for support and rigidity.
- h. Electrical circuitry test requirements.
- i. Marking requirements.
- j. All appropriate assembly requirements shall be listed and defined on the assembly drawing, including allowances and necessary manufacturing data.

SECTION 5. DETAIL REQUIREMENTS

This section covers requirements for conductors, spacing, test points, cover sheets, bends, holes, plated metals, and solder mask. It is important that planners, designers, and quality assurance people have an understanding of this material.

1. Conductor Pattern

- a. Conductor thickness and width shall be determined in accordance with Figure F-2. Widths and spacings shall be maximized for manufacturability and operating durability, consistent with good design practice. The minimum allowable conductor width is .004 inch. Working film (production master) shall be modified to compensate for processing tolerances. Conductor width tolerances are listed in Table F-1.
- b. Conductors with exterior angles less than 90 degrees shall be rounded.
- c. Conductor lengths shall be held to a minimum, with the following considerations:
 - (1) Conductors shall run parallel with the X or Y axis directions or at a 45 degree angle to these directions.
 - (2) Parallel conductors on opposite sides of a dielectric that will be flexed shall be offset from each other.
 - (3) Flexing, or bending, shall be allowed only in areas where the conductors are straight and the bend radius is at 90 degrees to the conductor paths (see Figure F-3).
- d. Conductor spacing shall be as large as possible. Minimum conductor spacing shall be in accordance with Table F-2.
- e. Jumper wires are permitted only with prior approval of the procuring agency. Paragraph 5.1.5 lists other requirements for jumper wires.
- f. Minimum edge spacing from any conductive feature to the board edges shall be per Table F-2—only if the edges are protected from physical harm in the installed assembly. Otherwise, the minimum conductor-to-

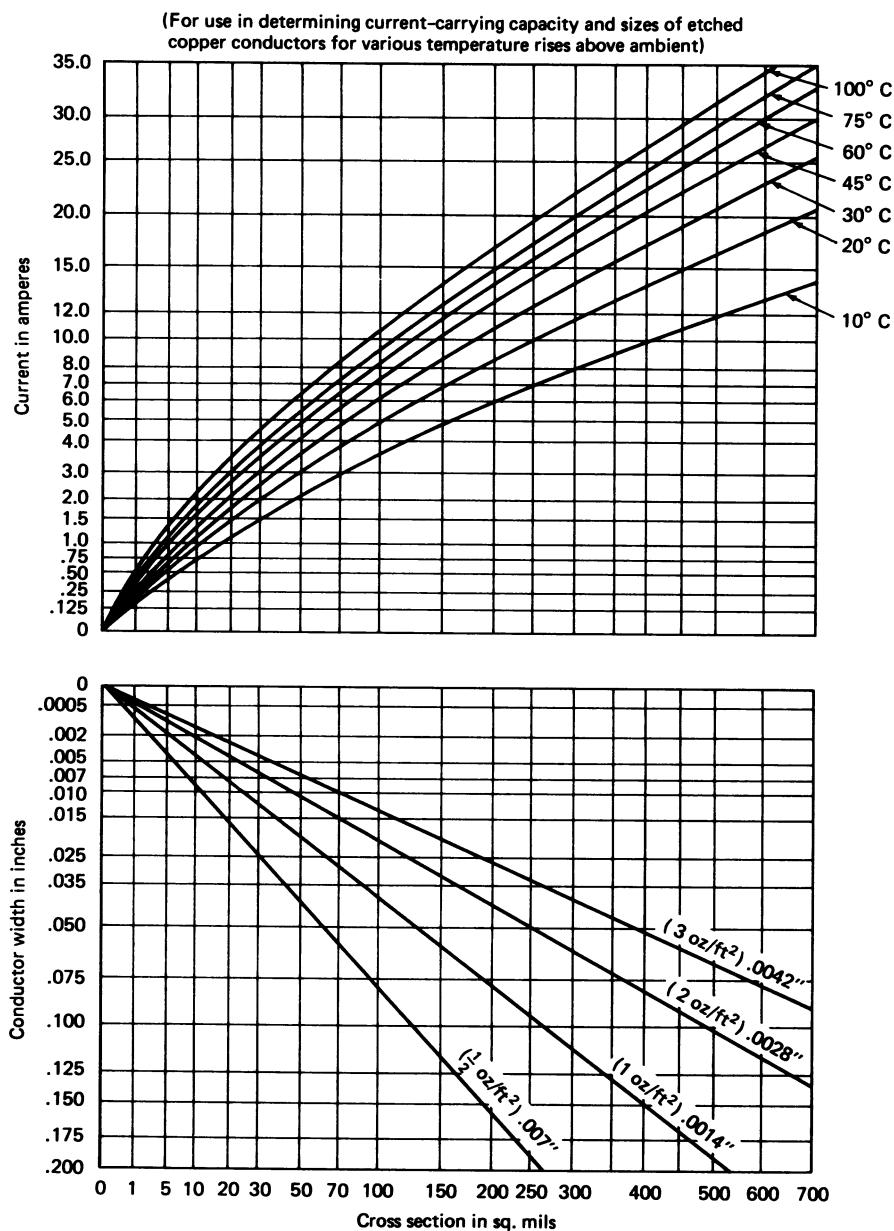


Fig. F-2 Current-carrying capacity of conductors.

NOTES:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs. current for various cross-sectional areas of etched copper conductors. It is assumed that normal design conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10% derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
2. Additional derating of 15% (current-wise) is suggested under the following conditions:
 - (a) For panel thickness of 1/32 inch or less.
 - (b) For conductor thickness of 0.0042 inch (3 oz/ft²) or thicker.
3. For general use, the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature in the location where the panel will be used.
4. For single conductor applications the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current. The equivalent cross section is equal to the sum of the cross sections of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power-dissipating parts is not included.
7. The conductor thicknesses in the design chart do not include conductor overplating with metals other than copper.

Fig. F-2 (*Continued*)

- board edge shall be .100 inch. Edge spacing does not apply to shield/ground planes or heat sinks.
- g. Large external conductive areas, exceeding 1.0 inch in diameter, shall be broken up by etched-out areas. Large conductive areas should be on the component side of type 3 and type 4 circuits.
 - h. Large internal conductive areas, exceeding 1.0 inch in diameter, shall be broken up by etched-out areas and located near the center of the board. If more than one such layer is used, these layers must be located to provide for balanced construction.
 - i. Interfacial connections on type 2 boards can be made by plated-through holes or clinched wires. Clinched wires being used to make interfacial connections are not considered part of the assembly. Interfacial connections on type 3 and 4 boards shall be made only with plated-through holes.
 - j. Solder plugs in holes which do contain leads are permissible after wave soldering. See paragraph 5.1.8.1 for other rules about solder plugs.
 2. Lands shall be provided at each location where a part lead occurs or at any other location where an electrical connection is made, including a test point.

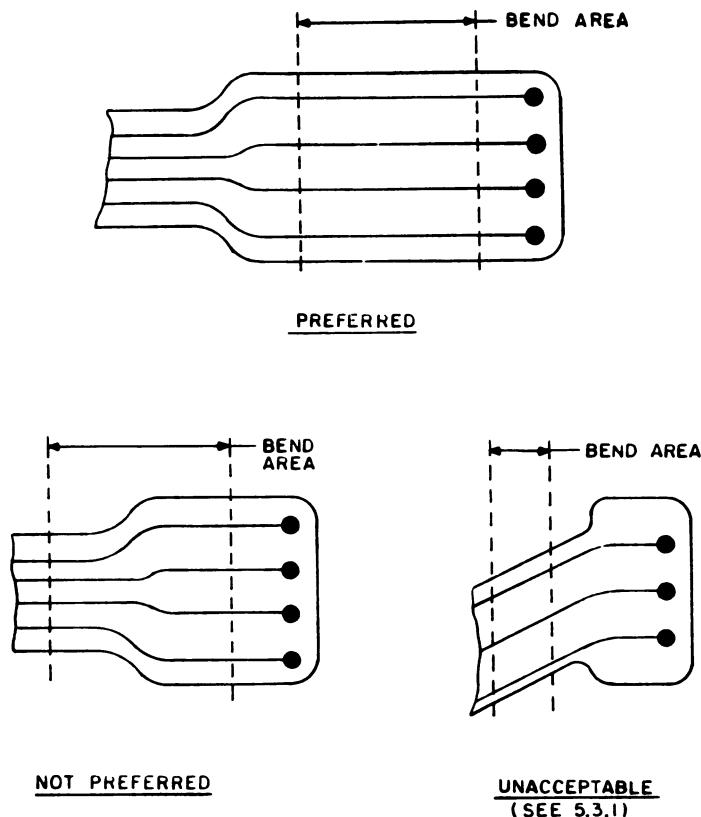


Fig. F-3 Bending rules for conductors.

Table F-2 Conductor Spacing

<i>Voltage Between Conductors DC or AC Peak (Volts)</i>	<i>Minimum Spacing (Inches)</i>	
	<i>Surface</i>	<i>Encapsulated</i> ²
0-100	.005 (.13 mm)	.004 (.10 mm)
101-300	.015 (.38 mm)	.008 (.20 mm)
301-500	.030 (.76 mm)	.010 (.25 mm)
Greater than 500 ¹	.00012 (.0030 mm) per volt	.0001 (.003 mm) per volt

¹For reference only, voltage greater than 500 volts should be evaluated for the specific design application.²"Encapsulated" means the internal layers bonded together or the external layers with cover coat or potting, as opposed to conformal coating or solder mask.

Lands for surface-terminated flat packs shall be rectangular (preferably) and shall have the following dimensions:

- a. Minimum width: equal to or greater than the maximum lead width.
 - b. Minimum length: equal to or greater than twice the minimum width.
3. Etchback. When required, etchback shall be specified on the master drawing. It shall be at least .0001 inch minimum and .003 inch maximum.
 4. Negative etchback at the internal layers shall be allowed to a maximum of .003 inch.
 5. Land areas shall be as large as possible. Minimum land areas shall be calculated as follows:

$$\text{Minimum land area} = a + 2b + 2c \text{ (when required)} + d$$

a = Maximum diameter of the drilled hole for internal lands or maximum diameter of the finished hole for external lands.

b = Minimum annular ring requirement.

c = Maximum allowance for etchback, when required.

d = Standard fabrication allowance, determined by statistical survey. See Table F-3 for allowable standard fabrication tolerances which can be used.

6. Annular ring considerations. The minimum annular ring for flexible circuits is determined in the same manner as for rigid printed circuits.
 - a. External measurements—from the inside edge of the hole to the outside edge of the land at the narrowest location.
 - b. Internal measurements—from the inside edge of the drilled hole wall to the outside edge of the land at the narrowest location.

Minimum requirements for the annular ring are as follows:

Table F-3 Standard Fabrication Allowances

<i>Greatest Board Dimension</i>	<i>Allowances (inches)</i>		
	<i>Preferred</i>	<i>Standard</i>	<i>Reduced Producibility</i>
Up to 12 inches	.028 (.71 mm)	.020 (.51 mm)	.012 (.30 mm)
12 to 18 inches	.034 (.86 mm)	.024 (.61 mm)	.016 (.41 mm)
More than 18 inches	Drawing tolerances must reflect bend and fold allowances between component mounting rigid areas.		

- a. External
 - (1) Minimum annular ring for plated holes on types 2, 3, and 4 is .005 inch.
 - (2) Minimum annular ring for nonplated holes is .015 inch.
- b. Internal
 - (1) Minimum annular ring at functional lands is .002 inch.

7. Lands in large conductive planes shall be relieved according to the examples shown in Figure F-4.

8. Bends

- a. Bends should be kept to a minimum.
- b. Conductors must be perpendicular to bend lines.
- c. Component holes, plated-through holes, and surface mounting lands must be at least .100 inch from a bend.
- d. Class B, continuous flexing applications must not have plating in the bend area.

9. The bend radius should be as large as possible. Suggested minimum allowed radii are:

- a. Type 1 and 2 boards—minimum radii should be at least 6 times the maximum overall thickness.
- b. Type 3, 4, and 5 boards—minimum radii should be at least 12 times the maximum overall thickness.

10. Strain reliefs should be used, when applicable, to relieve pressure on solder joints.

11. Prebending should be avoided, per paragraph 5.3.3.

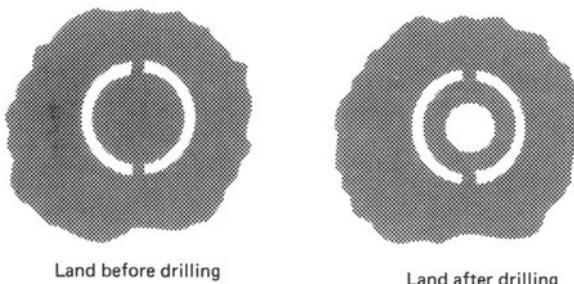


Fig. F-4 Ground plane lands.

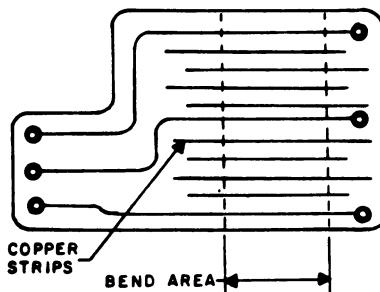


Fig. F-5 Method of increasing bend strength.

12. Bend strengtheners are permissible to increase the strength of circuits when bends occur in an area with few conductors. Bend strengtheners are strips of copper added in parallel with conductors (see Figure F-5).
13. Periphery of circuits (see Figure F-6). Good rules to follow are the following:
 - a. Keep the shape as simple as possible.
 - b. Avoid sharp corners.
 - c. Inside corners and slots should have tear stop holes or copper dams added.
 - d. Outside corners may be chamfered or formed with a radius (minimum radius, .015 inch).
14. Cover sheets and access holes. Access holes are holes in the cover sheets which allow access to the circuitry or other holes. Good design rules are as follows:
 - a. Access holes should have a diameter at least .030 inch greater than the diameter of the component hole in the conductive layer.

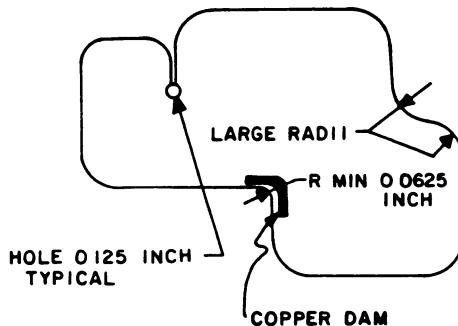


Fig. F-6 Flexible printed-wiring shape.

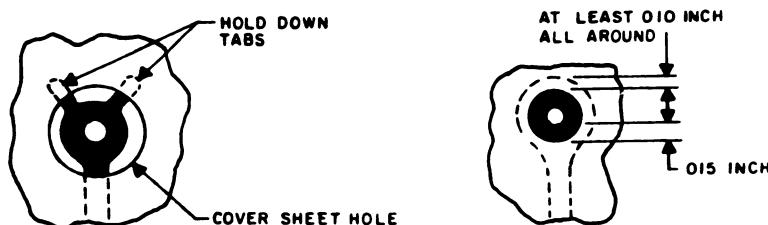
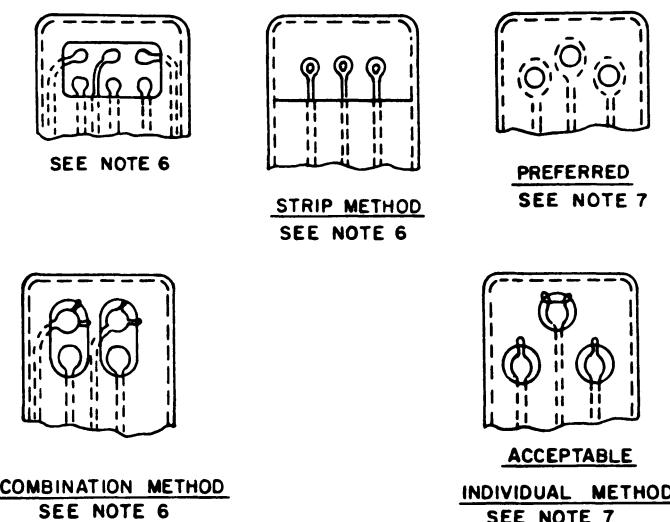


Fig. F-7 Coverlay sheet must capture pads.

- b. Pads must be held down by the cover sheet. If the cover sheet does not overlap at least .010 inch on the pads of unsupported holes, anchoring spurs must be added to those pads (see Figure F-7).
 - c. When using reduced producibility per Table F-3 (standard fabrication allowances), all lands shall have anchoring spurs added.
 - d. Forms of access holes for tightly spaced holes (see Figure F-8). When individual access holes are not practical, the access holes may take the form shown in Figure F-8. However, unsupported holes must have anchoring spurs added.
15. Holes of various types will now be discussed.
- a. For unsupported holes, the maximum diameter should not be .020 inch greater than the diameter of the lead to be inserted. When a rectangular pin is to be inserted, the hole diameter shall not exceed the nominal diagonal of the pin by more than .028 inch.
 - b. Holes which will have eyelets inserted shall have diameters no more than .010 inch greater than the outside diameter of the eyelet. The inside diameter of the eyelet shall not be more than .028 inch greater than the lead which will be inserted.
 - c. Indexing holes must be dimensioned on the master drawing.
 - d. Plated-through holes
 - (1) Plated-through holes shall not be used for mounting eyelets or standoffs.
 - (2) Plated-through holes which will have leads terminating in them shall be solder coated or plated. The minimum solder thickness shall be .0001 inch.
16. Flexible metal-clad materials shall be per IPC-FC-241, with a minimum base thickness of .001 inch. Other metal-clad materials shall be GF or GI per MIL-P-13949, with a minimum base thickness of .002 inch (see Table F-4).



NOTES:

1. The combination and individual methods are the most costly. The strip method creates a weak spot where the copper and the base material may crack.
2. The individual method shall be used for flexible printed-wiring with low density lands ($> .15$ centers).
3. Strip or combination methods shall be used for flexible printed-wiring with high density lands ($< .15$ centers).
4. Strip method (baring conductors) shall always be encapsulated at assembly and be provided with strain relief.
5. Combination method (baring conductors) shall always be conformal coated or encapsulated at assembly.
6. For use with plated through holes only.
7. For use with unsupported and plated through holes.

Fig. F-8 Forms of access holes.

Table F-4 Flexible Metal-Clad Dielectric

<i>Specification Sheet</i>	<i>Material Identification</i>
IPC-FC-241/1	Copper clad, polyimide with acrylic adhesive
IPC-FC-241/2	Copper clad, polyimide with epoxy adhesive
IPC-FC-241/3	Copper clad, fluorinated poly (ethylene-propylene) (FEP) with acrylic adhesive
IPC-FC-241/4	Copper clad, fluorinated poly (ethylene-propylene) (FEP) with epoxy adhesive

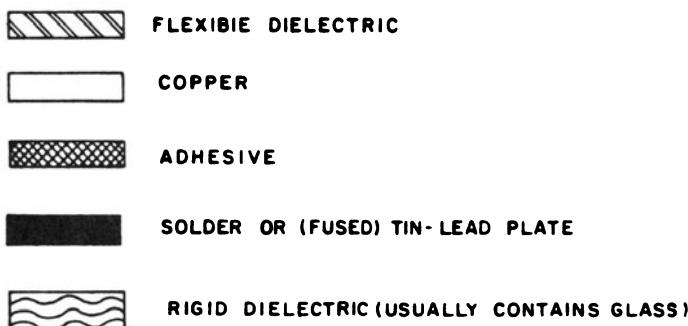
Table F-5 Cover Layer

<i>Specification Sheet</i>	<i>Material Identification</i>
IPC-FC-232/1	Polyimide base dielectric with acrylic adhesive
IPC-FC-232/2	Polyimide base dielectric with epoxy adhesive
IPC-FC-232/3	FEP base dielectric (fluorinated poly [ethylene propylene]) with acrylic adhesive
IPC-FC-232/4	FEP base dielectric (fluorinated poly [ethylene propylene]) with epoxy adhesive

17. Coverlayer material shall be per IPC-FC-232 and Table F-5. The minimum thickness of the base plus adhesive shall be .001 inch.
18. Adhesives (see Table F-6)
- Prepreg shall be GE, GF, or GI per MIL-P-13949. Areas requiring prepreg or adhesive shall be identified in the master drawing.
 - Flexible adhesive bonding films shall be in accordance with IPC-FC-233. Locations requiring adhesives are to be identified on the master drawing.
 - Adhesives and preps can be used interchangeably in the rigid portion of type 4 boards, provided dielectric requirements are met.
19. Fillets of adhesive may be required as strain reliefs at junctures of stiffeners or rigid-flex junctures. Requirements of the fillet shall be on the master drawing (see Figure F-9).
20. Stiffeners and heat sink materials. Thickness and adhesive shall be specified on the master drawing when required. Registration requirements of stiffener access holes to the printed circuit shall also be specified on the master drawing (see Figure F-10). Stiffeners may be internal or external. The edge of the stiffener shall be chamfered or rounded to prevent damage to conductors where it meets the flexible portion of the circuit (see Figure F-11).
21. Copper circuitry layers shall be in accordance with IPC-FC-150. A minimum of $\frac{1}{2}$ oz/sq ft is required for external layers.

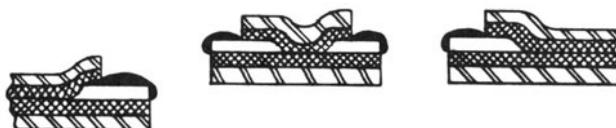
Table F-6 Adhesives

<i>Specification Sheet</i>	<i>Material Identification</i>
IPC-FC-233/1	Acrylic adhesive
IPC-FC-233/2	Epoxy adhesive



MATERIAL LEGEND

WITHOUT STIFFENER



WITH STIFFENER



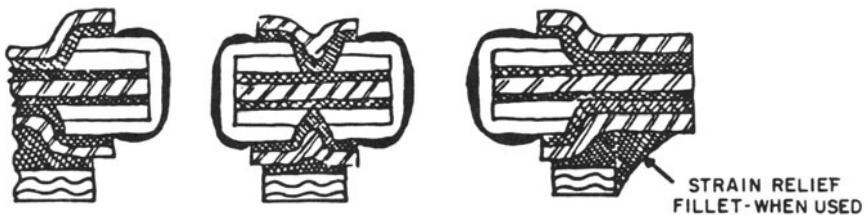
Single-sided flexible printed wiring (type 1).

WITHOUT STIFFENER



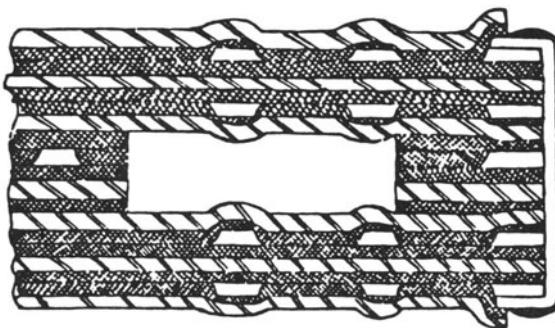
Fig. F-9 Typical constructions of flexible and rigid-flex printed circuits.

WITH STIFFENER



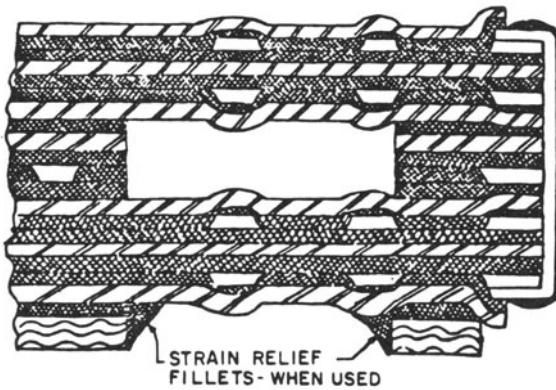
Double-sided flexible printed-wiring (type 2).

FLEXIBLE SECTION WITHOUT STIFFENER



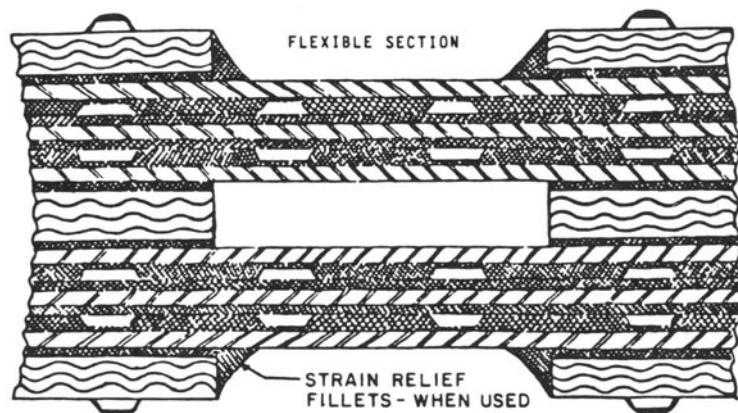
Five layer depicted - 2 Double sided with coverlayers
plus 1 Single layer (encapsulated)

FLEXIBLE SECTION WITH STIFFENER

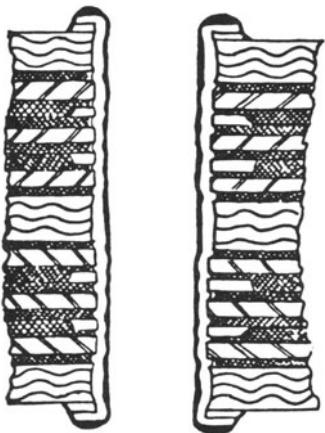


Multilayer flexible printed-wiring (type 3).

Fig. F-9 (Continued)



PLATED THROUGH HOLE SECTION



NOTE:

Varying degrees of preferential etchback amongst the various materials, as depicted is to be expected in finished product.

Multilayer composite combination rigid-flex printed-wiring (type 4).

Fig. F-9 (Continued)

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- a. Flexible layers
 - Type W, class 7
 - b. Rigid layers
 - Type E, class 1, 2, 3, or 4
- or
- c. Class B flexible, and flexible portion of rigid-flex boards
 - Type w, class 7
22. Plating
- a. Electroless copper—for all plated-through holes.
 - b. Electrolytic copper—per MIL-C-14550, with a minimum thickness of .001 inch.
 - c. Gold—per MIL-G-45204, with a minimum thickness of .000050 inch over low-stress nickel.
 - d. Tin/lead—per MIL-P-81728; it shall have a minimum fused thickness of .0003 inch at the crest of the conductor.
23. Solder mask shall be limited to the rigid portions of type 4 boards and shall meet IPC-SM-840, class 3, requirements when specified.
- a. If the mask is to cover tin-lead, metal areas larger than .050 in² should be relieved with at least .010 in². This promotes solder mask adhesion.
 - b. Metal areas which are to be uncovered shall have solder mask overlapping edges by .010 to .250 inch.
24. Flex and rigid-flex thickness tolerances
- a. Keep tolerances as liberal as possible. If a thickness tolerance is required, limit it to the portion where thickness control is critical.
 - b. When parts are being mounted, measure across metal extremities.
 - c. When base material thickness is critical, measure across the dielectric only.
25. Minimum dielectric thicknesses
- a. In type 4 circuits constructed with MIL-P-13949 materials, minimum dielectric spacing between conductive layers shall be .0035 inch. Dielectric includes prepreg and copper-clad material. There shall be at least two sheets of glass material between the conductive layers.
 - b. Circuits constructed using flexible materials and adhesives shall have at least .0015 inch of dielectric spacing. Spacing includes the flexible base plus adhesive.
26. Bow and twist shall be 1.5% of the rigid section of type 4 circuits only.

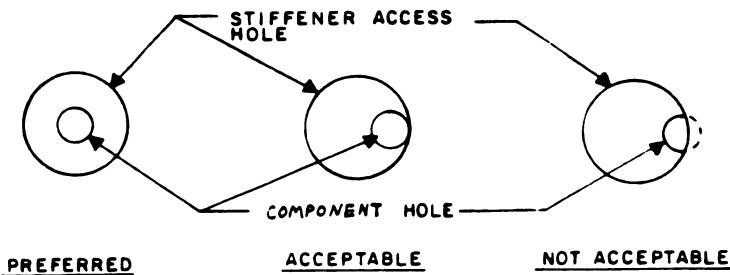


Fig. F-10 Stiffener registration.



Fig. F-11 Radiused edge of stiffener.

27. Shielding materials other than copper foil shall be approved by the procuring agency and included on the quality conformance test coupons and master drawings. Examples of shielding materials are silver epoxy and vapor-deposited metals.

SECTION 6. DETAIL PART MOUNTING REQUIREMENTS

This section begins on page 14 of MIL-STD-2118 and will not be covered here.

APPENDIX

The Appendix contains a few paragraphs on design considerations and Table F-1.

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