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DESIGN OF MODULATORS FOR OVERSAMPLED CONVERTERS

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Oversampled A/D converters have become very popular in recent years. Some of their advantages include relaxed requirements for anti-alias filters, relaxed requirements for component matching, high resolution and compatibility with digital VLSI technology. There is significant amount of literature discussing the principle, theory and implementation of various oversampled converters. Such converters are likely to continue to proliferate in the foreseeable future. Additionally, more recently there is great interest in low voltage and low power circuit design. New design techniques have been proposed for both the digital domain and the analog domain. Both trends point to the importance of the low power design of oversampled A/D converters.

Unfortunately, there has been no systematic study on the optimal design of modulators for oversampled converters. Design has generally focused on new architectures with little attention being paid to optimization. The technique for power estimation for digital circuits can only be applied to the digital filtering circuits of the overall converter but not to the analog modulator. Some opamp design details can be found in literature. However, the choices of opamp topologies in terms of power tradeoff and applications have not been studied. Nonlinearity is a very important performance measure for oversampled converters. Traditionally, the impact of the nonlinearity on the converter performance is studied by computer simulation and/or nonlinear curve fitting. While semi-quantitative information can be obtained through simulation, an analytical expression only consisting of the design and device parameters is not available. What is worse is that there are no measurement results for the nonlinearities which can also be predicted by a theory. The lack of an experimentally verified nonlinearity model forces designers to greatly overdesign their modulators resulting in power wastage.

The goal of this book is to develop a methodology for the optimal design of modulators in oversampled converters. We are mainly interested in two subjects: power consumption and nonlinearity, which are two important design constraints for oversampled converters. There are a number of different types of oversampled converters such as multi-loop, multi-stage and incremental, etc.. While differing in implementation details, they share a similar structure for the modulators. Therefore, the research results gained from this study should benefit the design of a wide range of oversampled converters.

This book is organized as follows.

- **Chapter 1**: Fundamentals of Oversampled A/D Converters
  Reviews fundamentals of oversampled A/D converters. Briefly discusses the principles of multi-loop, multi-stage and incremental oversampled converters. This chapter also introduces two nonideal effects associated with the modulators.

- **Chapter 2**: Opamp Topologies for Oversampled Converters
  Discusses various opamp topologies that can be used in oversampled modulators. We discuss Miller-compensated two-stage opamps, class AB opamps and dynamic opamps. The transient behavior, particularly the large signal behavior of these three opamp topologies are studied. A new low voltage CMOS class AB opamp is proposed. Measurement data from fabricated ICs for the new class AB opamp is also presented.

- **Chapter 3**: Optimal Design of Opamps for Delta-Sigma Modulators
  Addresses three issues related to the optimal design of opamps for oversampled converters: the theoretical minimum power bound for an ideal opamp, the best opamp choice in terms of power consumption and the best design strategy to achieve the minimum power consumption. We develop a model that captures the dynamics of the integrator inside the modulator. Based on this model, power consumption for various opamp topologies are computed and compared with each other. We further demonstrate a design strategy with the help of an example that can be used to achieve the minimum power for class A opamps.

- **Chapter 4**: Nonlinear Settling in Delta-Sigma Modulators
  Presents a new analytical model for opamp induced nonlinearity in oversampled converters. This model incorporates both finite slew rate and finite gain bandwidth effects and is valid for both first order and higher order modulators. Theoretical predictions agree very well with measured results from fabricated ICs.

- **Chapter 5**: Other Nonlinear Phenomena in Delta-Sigma Modulators
  Examines other nonlinear phenomenon in delta-sigma modulators besides

nonlinear settling covered in Chapter 4. The nonlinearities include nonlinear capacitor, nonlinear reference voltage and nonlinear DC gain. Design tradeoffs to minimize overall nonlinearity is discussed.

- **Chapter 6**: Circuit Implementation of Delta-Sigma Modulators
  Examines the design considerations of building blocks for a first-order delta-sigma modulator. The design tradeoffs to minimize power consumption and nonlinearity are evaluated. Measurements from fabricated ICs are compared to computer simulations to demonstrate the principle of the modulator operation.

This book originated from the Ph.D. dissertation of the first author in Department of Electrical Engineering at University of Minnesota.

FENG WANG AND REMASH HARJANI

This book is dedicated to our
wives, Zhen Huang and Savita
Harjani, for their patience and
support throughout the writing
of this book

1 FUNDAMENTALS OF OVERSAMPLED A/D CONVERTERS

1.1 OVERSAMPLED CONVERTERS

In this section, we provide some background for various oversampled converters. We are primarily interested in multi-loop, multi-stage and incremental structures . The fundamental nature of each structure will be briefly described mathematically.

Multi-loop structure

A conceptual block digram of a first order sigma-delta A/D converter and its Z-domain representation are shown in Figure 1.1.

The principle can be better understood in the Z-domain. By linearizing the quantizer as an additive noise source, we can obtain

$$Y(z) = X(z)z^{-1} + (1 - z^{-1})e(z) \tag{1.1}$$

From the above equation, we can see that the output is equal to the delayed version of the input plus the first order difference of the quantization error. The term $(1 - z^{-1})$ is called the noise shaping function and its frequency response
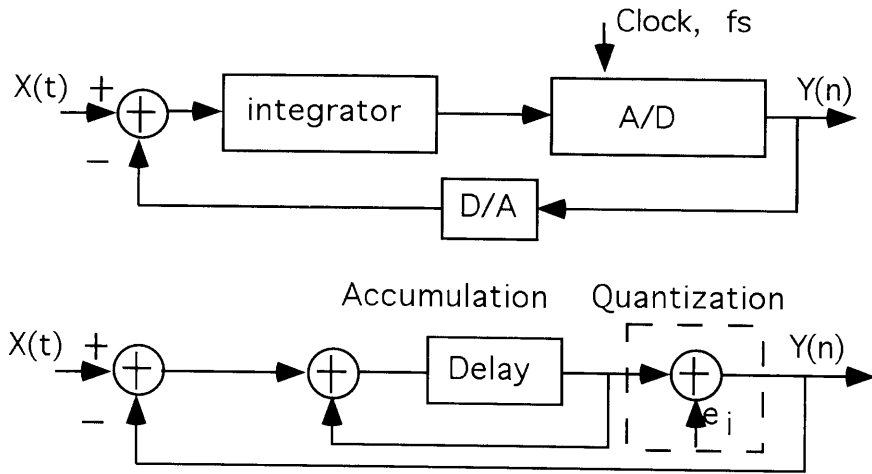
Figure 1.1.   Delta-Sigma converter and its sampled-data representation

Figure 1.2.   Power spectral density of the shaped quantization noise

has a highpass characteristics. The inband modulation noise can be estimated by first calculating the power spectral density $S_q(f)$ of the shaped quantization noise. It can be written as

$$S_q(f) = S_n(f)|1 - e^{-j\omega\tau}|^2 = \frac{\Delta^2}{3f_s}sin^2(\frac{\pi\tau}{2})   \qquad (1.2)$$

where f_s is the sampling frequency and is equal to $1/\tau$. Δ is the smallest quantization step. The total inband noise is the integral of $S_q(f)$ over the signal band, i.e.,

$$n^2 = \int_{-f_{B/2}}^{f_{B/2}} S_q(f)df = \frac{\Delta^2\pi^2}{36}(OSR)^{-3}   \qquad (1.3)$$

where OSR is the oversampling ratio and is equal to $f_s/2f_B$. Clearly, each doubling of the oversampling ratio improves the signal-to-noise ratio by 9dB as opposed to 3dB for a simple oversampled PCM converter. The speed-resolution tradeoff is more advantageous here. Some typical power spectral densities for modulation noise is shown in Figure 1.2 for two different inputs. The envelopes of both spectrum follow the frequency response of highpass function $(1 - z^{-1})$, but have distinct discrete spectral lines. The top figure corresponds to the input that is in the vicinity of an integer divisor of the quantization level while the bottom one corresponds to an integer divisor of the quantization level. This input voltage dependent spectrum is further illustrated in Figure 1.3 where the

modulation noise power is plotted versus the input signal. Note that sharp peaks appear close to plus and minus the reference voltage and the around the zero (midpoint of the full range). There are also peaks adjacent to integer divisions of the space between levels. This characteristic structure is called pattern noise. Pattern noise results in a much worse SNR than that predicted by the theory that assumes that the quantization error is white. It is possible to provide a qualitative explanation for why this occurs. For example, for an input that is an integer divisor of the quantization level the digital output of the quantizer exhibits a periodic pattern repeating itself at a relatively high frequency (bottom in Figure 1.2), noise power with this high frequency components does not get into signal band resulting in low inband noise power. On the other hand, for the input that is close to an integer divisor the digital output repeats itself at a relatively low frequency. This low frequency repetition causes noise power to be introduced into the signal band resulting in a large inband noise power. The pattern noise reflects the strong correlation between the quantization noise and the input signal which has been described mathematically [Candy and Benjamin, 1981]. Actually the general assumption that the quantization is white and not correlated with the input breaks down for the
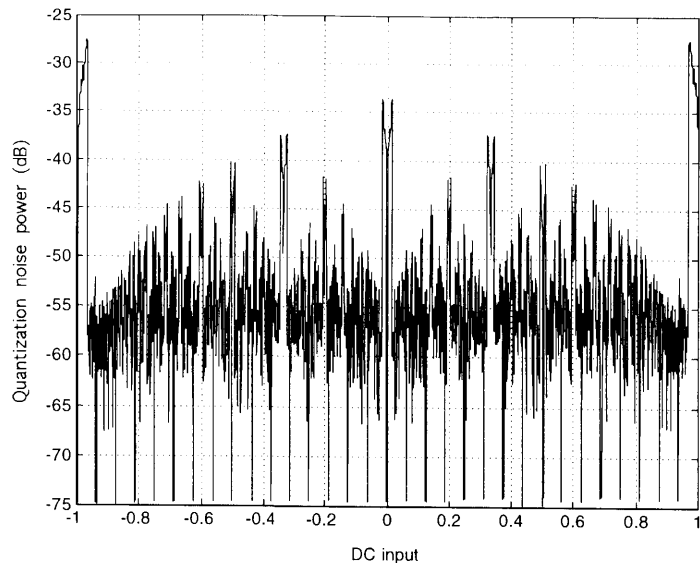
Figure 1.3.   Quantization noise of a first order delta-sigma modulator
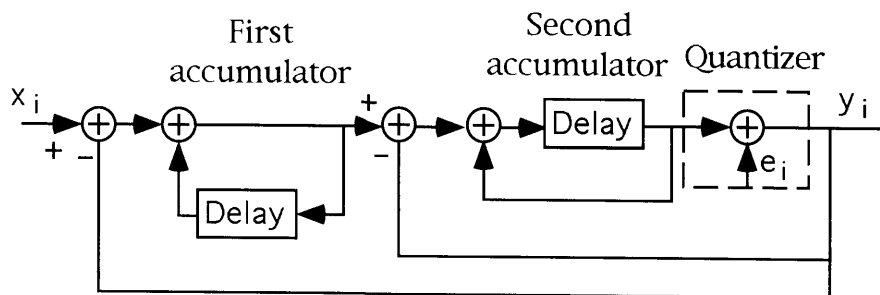
Figure 1.4.   Second order delta-sigma modulator

first order modulator. More rigorous treatment can be found in in [Candy and Benjamin, 1981, Friedman, 1989, Gray, 1989, Gray et al., 1988]. To alleviate the pattern noise problem and increase the speed-resolution tradeoff a second order delta-sigma modulators can be used [Candy, 1985].

A schematic for the second order delta-sigma modulator is shown in Figure 1.4 [Norsworthy et al., 1996]. According to the linear model of the modu-

lator, the Z-domain expression of the modulator output can be written as

$$Y(z) = X(z)z^{-1} + (1 - z^{-1})^2 e(z) \qquad (1.4)$$

The $(1 - z^{-1})^2$ term has a second order highpass filter characteristics. It will suppress more quantization noise in the low frequency range than the first order highpass term for the first order modulator. The total inband quantization noise can be written as

$$n^2 = \frac{\Delta^2 \pi^2}{60}(OSR)^{-5} \qquad (1.5)$$

Clearly each doubling of the oversampling ratio improves the SNR ratio by 15 dB, providing 2.5 extra bits of resolution. Not only does the second order delta-sigma modulator provide better SNR but it also does a better job of decoloring the quantization noise and decorrelating the quantization noise from the input signal. This better performance is reflected in Figure 1.5. Comparing Figure 1.5
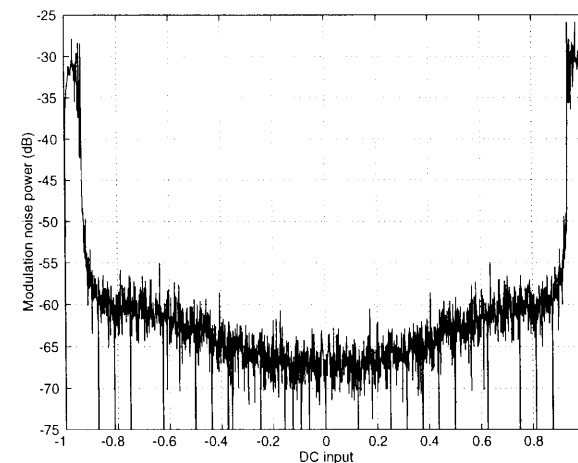
Figure 1.5.   Pattern noise in a second order delta-sigma modulator

with Figure 1.3, we can see that there is no conspicuous spikes for inputs up to 0.8 times the reference voltage. Therefore, second order modulators are less prone to the pattern noise problem. For larger signals, the second integrator will overload and the inband noise will increase.

In general, we can further increase the SNR of the modulators by increasing the order of the loop (multi-loop structure). However, the stability for any order larger than two becomes problematic. Many topologies have been suggested to overcome the instability of the modulators [Welland et al., 1989, Ferguson

et al., 1990, Adams et al., 1991] by carefully choosing loop coefficients and limiting the input range. Alternative way to achieve high resolution is to use a multi-stage structure [Matsuya et al., 1987, Uchimura et al., 1988] as explained in the following section.

Multi-stage structure

A second order multi-stage (MASH) architecture using two cascaded first order sections is shown in Figure 1.6. It can be shown that the output is equal to
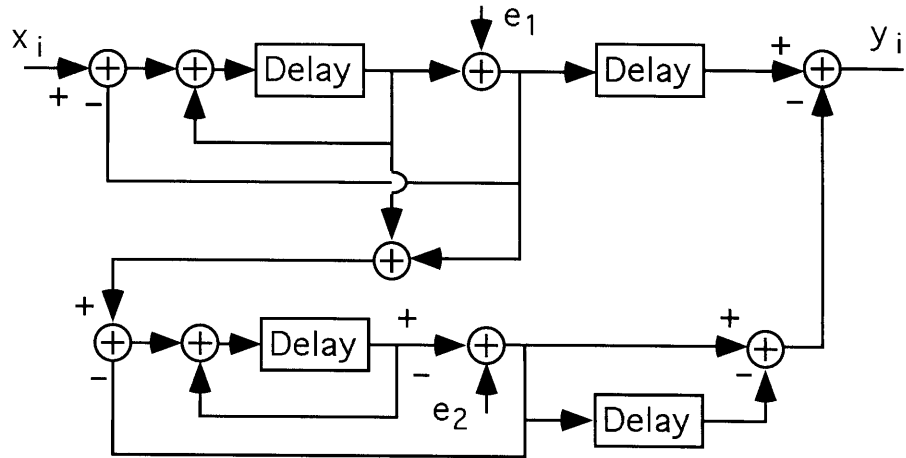
Figure 1.6.   MASH architecture for a second order modulator

$$Y(Z) = Z^{-2}X(Z) - (1 - Z^{-1})^2 E_2(Z) \qquad (1.6)$$

We note that the quantization noise is shaped by a second order high pass filtering. Therefore, a cascade of two first order modulators is equivalent to a second order modulator in terms of the quantization noise spectrum. It also can be shown that for the two-stage modulator operating at a typical oversampling ratio, the quantization noise spectral density is a smooth continuous function of frequency and is independent of the input signal level [Wong and Gray, 1990].

In principle, this MASH topology can be extended to delta-sigma modulators with higher order. However, for complete cancellation of the quantization noise from the first integrator the gain of the first loop needs to be exactly equal to the gain of the second loop. Therefore, the capacitor mismatches between the two loops limits the practical order of the modulator. Higher than three stages is seldom implemented. An alternate but interesting variation of the

MASH topology is to use a second order modulator cascaded with a first order modulator [Longo and Copeland, 1988].

Alternative structure

As we mentioned before, delta-sigma A/D converters that use noise-shaping techniques offer high resolution. They are characterized by AC performance such as signal-to-noise ratio. They are suitable for applications in which offset and finite gain error can be tolerated. On the other hand, measurement and instrumentation application require absolute accuracy, e.g., offset and gain can not be tolerated. Incremental A/D converters have been suggested to achieve such requirements. The circuit schematic is shown in Figure 1.7 [Robert et al., 1987]. Although the incremental converter has a similar structure to the sigma-
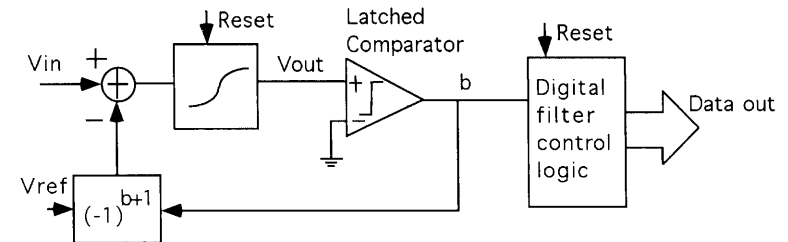
Figure 1.7.   Schematic block diagram of the incremental converter

delta converter, the main difference of the operation includes:

- The input signal is converted at a slow rate, once in every 2^n clock period, where the n is the number of bits of resolution, rather than once in every OSR clock period, where OSR is the oversampling ratio;

- The integrator and counter (digital filter) are both reset before each conversion;

- The digital circuitry following the integrator contains an up/down counter, rather than a decimating digital low-pass filter.

The simple mathematical description regarding the relation between the input signal and the digital output can be given as follows:

$$V_{in} = \frac{N^+ - N^-}{N} V_r + \frac{V_{outf} - V_{outi}}{N} \qquad (1.7)$$

where N^+ and N^- are number of "1"s and "0"s at the output of the comparator. $N = N^+ + N^-$ is the total number of outputs per conversion. V_{outf}

and V_{outi} are the final and initial output voltages of the integrator. Since the integrator is reset before each conversion, V_{outi} becomes zero. The first term of the right hand side of Equation 1.7 is the digital representation of the input signal V_{in} which suggests a simple up/down counter filter. Therefore, the error left in this expression is equal to $V_{outf}/N \propto O(1/N)$. Clearly, if high accuracy
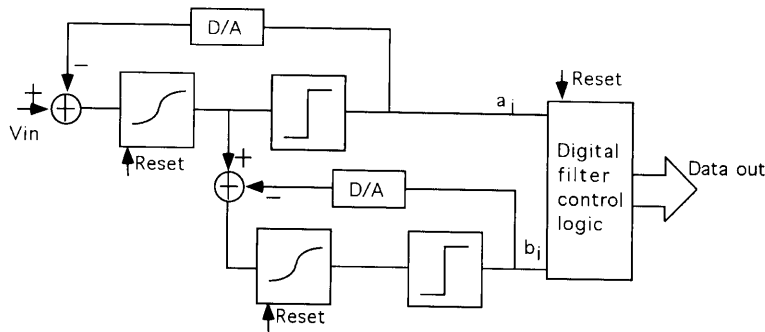
Figure 1.8.   Schematic digram of a second order incremental A/D converter

is required, a large N is needed resulting in a very slow conversion rate. So this particular topology is only suitable for very low frequency applications. The very low conversion rate problem can be solved by using a second order incremental A/D converter. A schematic circuit digram is shown in Figure 1.8 [Robert and Deval, 1988]. A similar mathematical description relating the input signal to the digital output can be found and is shown in Equation 1.8

$$V_{in} = \frac{\sum_{i=1}^{N} a_i(N+1-i) + \sum_{i=1}^{N} b_i}{1/2N(N+1)} V_r + O\left(\frac{1}{N(N+1)}\right) \qquad (1.8)$$

where $a_i(b_i) = 1$ if the top (bottom) comparator yields a logic high. Otherwise, $a_i(b_i) = -1$ if the top (bottom) comparator yields a logic low. Therefore, the resulting accuracy is now bound to $O(1/N(N+1)) \propto O(1/N^2)$ which produces an dramatic reduction in the conversion time. The form of the digital output suggests the digital filter should take a running sum form as opposed to the simple sum in the case of the first order incremental converter. Every doubling of integration periods N will gain an improvement of 12 dB in terms of signal-to-noise ratio. Generally, a mth order incremental converter will gain $6m$ dB improvement for each doubling of the integration period.
Delta-Sigma vs Incremental The theory of sigma-delta converters shows a $6m+3$ dB improvement of signal-to-noise ratio per octave of oversampling. Compared to the result for the incremental converter, the extra 3 dB is gained by using the complex digital filter under the assumption that the input signal

is sufficiently busy such that the quantization error is white enough. Note that these values corresponds to the average noise level on the whole dynamic range of the input signal. As as discussed before, certain idle inputs will produce a drastic increase in the in-band noise as shown in Figure 1.3. Sigma-delta converters generally have a 3dB better resolution than incremental counterparts but they both have the same worst case accuracy. On the other hand, the implementation of digital post processing is quite simple for incremental converters which leads to a savings in power. In another words, sigma-delta converters are more suitable for applications where high signal-to-noise ratio is the primary goal such as in consumer electronics. Incremental converters are suitable for low frequency, high accuracy applications such as found in instrumentation.

1.2   NONIDEALITIES IN DELTA-SIGMA MODULATORS

Up to now, we have explained the basic principle of delta-sigma modulators assuming perfect components. However, all real elements are limited by their nonidealities. The main nonidealities result from operational amplifiers, switches and capacitors and comparators.

For operational amplifiers, finite and nonlinear DC gain, finite gain bandwidth and slew rate and input referred device noise contribute to the nonidealities. The thermal noises generated by the finite on resistances of the switches are sampled and are added to the overall input referred noise. Fortunately, the performance of the comparators is not critical in delta-sigma modulators and therefore they are neglected here.

Most of nonidealities mentioned above will be examined in detail in the following chapters. In this section, we will only briefly review the the impact of finite DC gain and the noise contribution from switches since they are already well understood.

Finite DC gain

The first step to understand the impact of the finite DC gain of the opamp is to find the transfer function of the integrator utilizing such an opamp. It is possible to show [Gregorian and Temes, 1986] that for an inverting integrator the transfer function becomes

$$H(Z) = \frac{\alpha}{1 - \beta Z^{-1}} \qquad (1.9)$$

where

$$\alpha = \frac{-C_1}{C_2 + (C_1 + C_2)/A} \qquad (1.10)$$
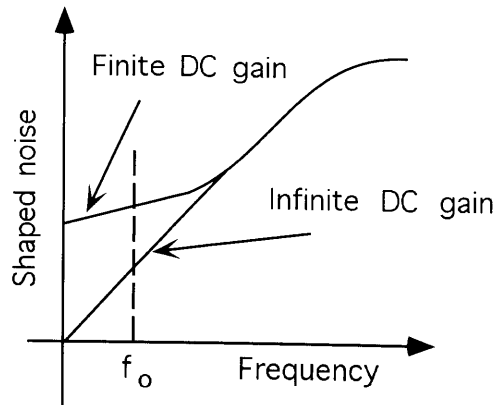
Figure 1.9.   Effect of finite DC gain on noise shaping function

Figure 1.10.   SNR degradation due to finite gain

$$\beta = \frac{C_2(1 + 1/A)}{C_2 + (C_1 + C_2)/A}$$

where A is the DC gain of the opamp, and capacitors C_1 and C_2 are the input and integrating capacitors respectively. When A approaches ∞, α approaches $-C_1/C_2$ and β approaches one as expected. Because β is slightly less than one, the magnitude of the transfer function $H(Z)$ at zero frequency is no longer infinite which in turn makes the noise shaping function have a nonzero value at zero frequency. This is demonstrated graphically in Figure 1.9. The figure shows that the power spectral density of the shaped noise for an ideal opamp (infinite gain) and a real opamp (finite gain). The quantization noise in the signal band f_o is essentially the area under each curve up to frequency f_o. The finite gain curve levels off at low frequency as opposed to declining to zero in the infinite gain curve. This allows the integrator to pick up more quantization noise in the signal band. Therefore, the signal-to-noise ratio (SNR) is reduced. Figure 1.10 illustrates the effect of the finite gain on SNR for different input levels. The plot is generated via difference equation simulation using MATLAB. This method makes no particular assumption about the nature of the quantization noise as opposed to the white noise assumed by the linear model. Normally a DC gain larger than the oversample ratio is required from the linearized noise perspective.

Figure 1.11.   Switched-capacitor integrator with equivalent noise sources

Thermal noise

In this subsection, we investigate the noise induced by the sampled capacitor and the operational amplifier (opamp). The work is based on the analysis by [Gobet and Knob, 1983]. We start the analysis by reviewing some background with the help of Figure 1.11.

- A periodically sampled capacitor can be modeled as a simple RC network with capacitance C and the "on" resistance R of the MOS switch.

- If the switch is on all the time, the total thermal noise is KT/C independent of the "on" resistance R. An equivalent noise with uniform spectral density and equal power can be defined in the frequency band $f_{eq} = 1/2RC$.

- Typically the sampling frequency f_s is much smaller than f_{eq}. Therefore, the wide band noise is greatly undersampled . The total noise power KT/C is folded back into the frequency band $-f_s/2 < f < f_s/2$.

- The noise spectral density of the sampled capacitor can be found as

$$S_n(f) = \frac{KT}{f_s C}\left(\tau\frac{f_s}{f_{eq}} + (1-\tau)^2 sinc^2\left(\pi f\frac{1-\tau}{f_s}\right)\right) \qquad (1.11)$$

where τ is the fraction of clock period when the switch is on, and f_s is the sampling frequency. At low frequencies, the folded back noise dominates.

- Noise generated in a switched-capacitor (SC) integrator at the output consists of three parts: noise contribution from the left MOS switch S_{n1}, noise contribution from the right MOS switch S_{n2}, and noise from the opamp S_{n3}.

$$
\begin{aligned}
S_{n1}(f) &= \frac{KT}{f_s \alpha C}\left[\frac{\alpha}{2\pi\frac{f}{f_s}}\right]^2 & (1.12)\\[2ex]
S_{n2}(f) &= \frac{KT}{f_s \alpha C}\left[\alpha^2\tau\frac{f_s}{f_{eq}} + \left(\frac{\alpha}{2\pi\frac{f}{f_s}}\right)^2\frac{\pi}{\alpha+1}\frac{f_b}{f_{eq}}\right]\\[2ex]
S_{n3}(f) &= S_{ni}(f)\frac{f_b}{f_s}\left[(1+\alpha\tau(\alpha+2))\frac{f_s}{f_b} + \left(\frac{\alpha}{2\pi\frac{f}{f_s}}\right)^2\frac{\pi}{\alpha+1}\right]
\end{aligned}
$$

where f_b is the unity gain bandwidth of the opamp, $\alpha = C_1/C_t$ and S_{ni} is the input referred noise of the opamp.

Let us first carry out some numerical estimates for the individual contributions from above mentioned three noise sources. Let us assume that the sampling frequency is about 200 kHz and the unity gain bandwidth of opamp is about 1 MHz. A typical "on" resistance for the MOS switch is about $10K\Omega$ and a typical sampling capacitance is about 5pf. Therefore $f_{eq} = 1/(2R_{on}C)$ is equal to 10 MHz, $f_b/f_{eq} = 0.1$ and $f_s/f_{eq} = 0.02$. We are primarily concerned with

the low frequency noise. Therefore, the following approximation for the total noise can be reached:

$$S_n(f) = \left(\frac{KT}{f_s C_1} + S_{ni}\frac{f_b}{f_s}\frac{\pi}{\alpha+1}\right)\left(\frac{\alpha}{2\pi\frac{f}{f_s}}\right)^2 \qquad (1.13)$$

When referred to input, the above expression should be divided by the transfer function

$$H(f) = \left(\frac{\alpha}{2\pi\frac{f}{f_s}}\right)^2 \qquad (1.14)$$

The input referred noise spectral density then becomes

$$S_n(f) = \left(\frac{KT}{f_s C_1} + S_{ni}\frac{f_b}{f_s}\frac{\pi}{\alpha+1}\right) \qquad (1.15)$$

and

$$S_{ni}(f) = \frac{8}{3}KT\frac{\beta}{g_m} \qquad (1.16)$$

where β is the effective number of devices that contribute to the input referred noise, and g_m is the transconductance of the input transistors. The flicker noise component has been neglected for our analysis. It is assumed that it is removed via correlated double sampling or chopper stabilization techniques (see Chapter 6. The total input referred noise in the signal band $-f_B < f < f_B$ is

$$
\begin{aligned}
V_n^2 &= \int_{-f_B}^{f_B} S_n(f)df & (1.17)\\[2ex]
&= \frac{KT}{OSR}\left(\frac{1}{C1} + \frac{4\beta}{3(\alpha+1)C_L}\right)
\end{aligned}
$$

where $OSR = f_s/(2f_B)$ is the oversampling ratio, and $f_b = g_m/2\pi C_L$ is used. For the first order delta-sigma A/D converter, there are two capacitors, the sampling capacitor C_1 and the reference capacitor C_2. Let us assume that the noise sources are statistically independent, then the input referred noise becomes

$$V_n^2 = \frac{KT}{OSR}\left(\frac{1}{C1} + \frac{1}{C_2} + \frac{4\beta}{3C_L}\left[\frac{1}{\alpha_1+1} + \frac{1}{\alpha_2+1}\right]\right) \qquad (1.18)$$

where $\alpha_1 = C_1/C_t, \alpha = C_2/C_t$ and C_L is the effective load capacitance. From the above expression, we can calculate the minimum capacitance bound due to the thermal noise given the oversampling ratio and the converter resolution.

The intuitive understanding of Equation 1.18 can be made as follows. The "on" resistance of the switches will generate thermal noise with the spectral

density of $4kRT$, where k is the Boltzman constant, T is the temperature in degrees Kelvin. The thermal noise has a white spectrum but is frequency limited by the low pass filtering of the RC network. The total noise power is calculated as KT/C which is independent of the resistance R. When this KT/C noise is undersampled by the modulator, all the noise power folds back into the Nyquist band of the oversampling converter. This noise is evenly spread across the Nyquist band but only the fraction $2f_o/f_s$ of this noise appears in the signal band. Therefore the overall input referred noise is equal to KT/C divided by the oversampling ratio OSR. Meanwhile, the smallest capacitor will dominate the noise contribution because the noise power is proportional to $1/C_{min}$. At a first glance, Equation 1.18 shows that the noise power is independent of the gain bandwidth of the opamp. This is only true when the flicker noise and noise S_{n2} are neglected. The roll off frequency characteristics of the opamp acts as a lowpass filter. Therefore, the smaller gain bandwidth will allow less noise to corrupt the signal. However, a tradeoff must be made here because a small gain bandwidth will degrade the settling behavior of the integrator.

1.3 CONCLUSIONS

In this chapter, we discussed the fundamentals of oversampled converters. The operation principles for three different kinds of oversampled converters have been reviewed. The optimal design of the modulators for such oversampled converters is made impossible without the thorough understanding of the basic principles. In the following chapters we will address optimal design issues at the circuit level and the system level based on the insight gained here.

2   OPAMP TOPOLOGIES FOR OVERSAMPLED CONVERTERS

2.1 INTRODUCTION

Operational amplifiers play a critical role in delta-sigma modulators. The impacts of the nonlinearities of the opamps on the modulator performance were studied extensively[Medeiro and Perez-Verdu, 1994, Boser and Wooley, 1988, Hauser and Broderson, 1986, Bishop et al., 1990]. These studies are carried out without assuming any particular opamp topology. Nonidealities such as finite gain, finite slew rate and finite gain bandwidth were incorporated into the linearized Z-domain expression of the modulator and/or into the time-domain difference equation. The former approach is suitable for the analytical study while the latter is suitable for the computer simulation. It was found that the modulator can tolerate incomplete settling provided that the settling is linear. This assumption, however, is only valid if a perfect class AB opamp is used where the transient period is not slew-rate limited. Several authors have studied the effect of the finite slew rate on the modulator performance. However, all of them assumed a simple slew rate formula based on class A opamps. Since any practical opamp can not supply infinitely large current, the transient process is more or less slew-rate limited no matter of what kind

of opamp is used. This limitation results in input voltage-dependent settling behavior, which directly degrade the modulator performance. Therefore, the importance of a better understanding of the transient process for the different opamps can not be overlooked.

In this chapter, we carry out a detail analysis of the transient behavior of three classes of opamps: class A, class AB and dynamic opamps. We concentrate on the development of models for the effective slew rate for these opamps. The established slew rate formulas can be easily embedded into existing modulator macromodels or table-based simulations for further processing.

Despite some disadvantages, the two stage Miller-compensated opamp is often used in low voltage delta-sigma modulators due to its high gain. This high gain can be realized without using cascode transistors and therefore without losing voltage headroom. Class AB opamps are particularly suitable for modulators that require large slew rate but moderate bandwidth[Brandt et al., 1991]. In Section 2.2, we introduce a new slew rate model for such opamps. In Section 2.3 in response to the low power low voltage design trend we propose a novel low voltage class AB opamp . Both design principles and experimental results are given. In Section 2.4, we develop an analytical model for the transient behavior for a class of class AB opamps. Usually it is assumed that the use of class AB opamps will result in a linear settling. It is our goal to examine the validity of such claims. In Section 2.5, we examine the transient behavior of dynamic opamps proposed by [Copeland and Rabaey, 1979]. We address the issue of of power consumption, slewing and settling in such opamps. In Section 2.6 we provide some conclusions.

2.2 CLASS A OPAMPS: AN IMPROVED SLEWING MODEL

Background

The settling time for an opamp is an important parameter for switched-capacitor and data converter circuits. The total settling time can be broken up into two distinct regions; a slewing period (T_{SL}) and a settling period (T_{ST}) [Wang and Harjani, 1995, Chuang, 1982]. During the slewing period the opamp operates in a rate limited fashion and the output voltage changes from its original value to a voltage close to its final value. And during the settling period the output voltage settles to its final value in a small-signal linear fashion. Our discussions concentrate on the slewing period.

A unified two-pole model that takes into account the slew rate limitation was developed in [Chuang, 1982] and further extended in [Lin and Nevin, 1986]. Unfortunately, in both these works small signal analysis is used for both the slewing and settling periods. However, slewing is inherently a large signal characteristic. For example, Figure 2.1 shows the $|V_{gs} - V_T|$ of the second stage
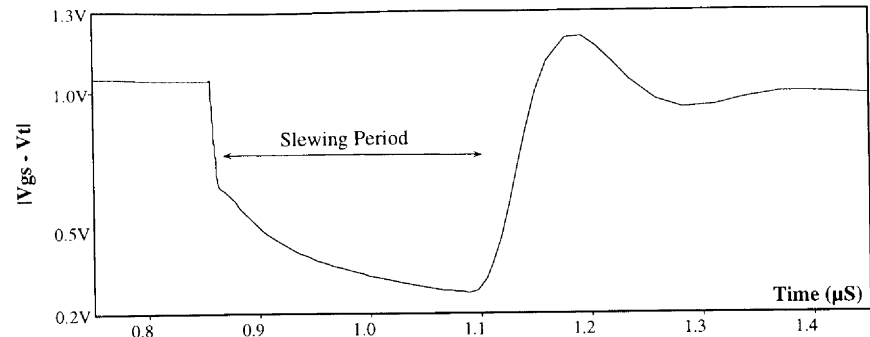
Figure 2.1.   The $|V_{gs} - V_T|$ of transistor Q_5

gain transistor of the opamp (Q_5 in Figure. 2.3). Clearly this voltage and the associated drain-to-source current is not constant during the slewing period. In fact, in our example (see Figure 2.1) it changes by 5X. Therefore, a small-signal analysis in the s-domain cannot be used and a complete time-domain analysis including nonlinear behavior is necessary.

Basic Model

For this study the amplifier is configured as a voltage follower as shown in Figure 2.2. This circuit configuration was chosen for its simplicity, however, the results can be extended to other configurations without much effort. A step input is applied at time $t = 0$. The circuit diagram for the two stage opamp is shown in Figure 2.3.

During the slewing period one of the differential pair transistors is completely off and the feedback loop is open [Kamath et al., 1974]. During this period the entire differential pair tail current, I_1, flows through the compensation capacitor, C_C. This current is constant during the slewing period. Further, to make the final equations tractable we use the simple square-law equations for the transistors during this period. Based on these assumptions, four equations can be developed for a positive step input as follows

$$I_1 = C_c \frac{d(V_o - V_1)}{dt} \qquad (2.1)$$

$$I_L = C_l \frac{dV_o}{dt} \qquad (2.2)$$

$$I_5 = \frac{\beta_5}{2}(V_{DD} - V_1 + V_{Tp})^2 \qquad (2.3)$$

$$0 = I_1 + I_2 + I_L - I_5 \tag{2.4}$$

The initial conditions for the differential equations above are

$$V_1(0^+) = V_1(0^-) - I_1 R_c = \left[V_{DD} + V_{Tp} - \sqrt{\frac{2I_2}{k_p \frac{W_5}{L_5}}}\right] - I_1 R_c \tag{2.5}$$

Using Equations (2.4) - (2.5), we can develop an expression for the output voltage V_o for a positive input step as shown in equation 2.6.

$$V_o(t) = \frac{I_1}{C_c}t - \gamma \tanh\left[\frac{1}{2}\frac{\gamma\beta_5}{C_L}(t + t_o)\right] + \xi \tag{2.6}$$

where

$$I_o = I_1 + I_2 + \frac{C_L}{C_c}I_1 \qquad\qquad t_o = \frac{C_L}{\gamma\beta}ln\frac{\gamma+\kappa}{\gamma-\kappa}$$

$$\gamma = \sqrt{\frac{2I_o}{\beta}} \qquad\qquad \kappa = \sqrt{\frac{2I_2}{\frac{k_p W_5}{L_5}}} + I_1 R_c$$

$$\xi = V_o(0^+) + \sqrt{\frac{2I_2}{k_p \frac{W_5}{L_5}}} + I_1 R_c$$

Similarly, for a negative input step, we can develop an expression for V_o by replacing I_1 and I_L by $-I_1$ and $-I_L$, respectively. In general, I_2 is greater than $I_1(1 + \frac{C_L}{C_c})$ such that I_o is positive.

$$V_o(t)\prime = -\frac{I_1}{C_c}t - \gamma\prime \, ctanh\left[\frac{1}{2}\frac{\gamma\prime\beta_5}{C_L}(t + t_o\prime)\right] - \xi\prime \tag{2.7}$$

where

$$I_o\prime = I_2 - I_1(1 + \frac{C_L}{C_c}) \qquad\qquad t_o\prime = \frac{C_L}{\gamma\prime\beta}ln\frac{\kappa\prime+\gamma\prime}{\kappa\prime-\gamma\prime}$$

$$\gamma\prime = \sqrt{\frac{2I_o\prime}{\beta_5}} \qquad\qquad \kappa\prime = \sqrt{\frac{2I_2}{\frac{k_p W_5}{L_5}}} - I_1 R_c$$

$$\xi\prime = V_o(0^+) + \sqrt{\frac{2I_2}{k_p \frac{W_5}{L_5}}} - I_1 R_c$$

The slew rate for the circuit is given by the derivative of $V_o(t)$ with respect to time t and is itself a function of time. Therefore, the effective slew rate defined as $SR_e = [V_o(T_{SL}) - V_o(0)]/T_{SL}$ is a more useful quantity, where T_{SL} is the time it takes the output voltage to change from its original value to the value when the opamp enters the linear region. The output voltage at $t = 0^+$ and at $t = T_{SL}$ are given by equation 2.8 and equation 2.9 respectively.

Figure 2.2.   Circuit configuration used for slewing model
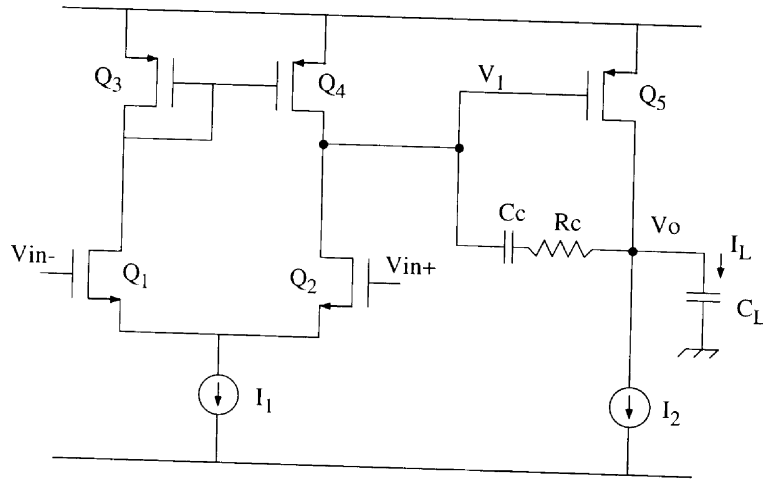
Figure 2.3.   A circuit diagram of a CMOS two stage opamp

$$V_o(0^+) = \xi - \gamma tanh\left[\frac{1}{2}\frac{\gamma\beta}{C_L}t_o\right] \tag{2.8}$$

$$V_o(T_{SL}) \approx \frac{I_1}{C_c}T_{SL} + \xi - \gamma \tag{2.9}$$

By using the approximation $1 - tanh x \approx 2exp(-2x)$ when x is large, SR_e can be simplified as

$$SR_e = \frac{I_1}{C_c} - \frac{2\gamma}{T_{SL}}\frac{\kappa - \gamma}{\kappa + \gamma} \tag{2.10}$$

Likewise, the effective slew rate for a negative input step can be written as

$$SR_e\prime = \frac{I_1}{C_c} - \frac{2\gamma\prime}{T_{SL}}\frac{\kappa\prime - \gamma\prime}{\kappa\prime + \gamma\prime} \tag{2.11}$$

However, since $T_{SL} = \Delta V/SR_e$ the above expressions can further be simplified to

$$SR_e = \frac{\frac{I_1}{C_c}}{1 + 2\frac{\gamma}{\Delta V}\frac{(\gamma - \kappa)}{(\gamma + \kappa)}} \tag{2.12}$$

$$SR_e\prime = \frac{\frac{I_1}{C_c}}{1 + 2\frac{\gamma\prime}{\Delta V}\frac{(\gamma\prime - \kappa\prime)}{(\gamma\prime + \kappa\prime)}} \tag{2.13}$$

where ΔV is equal to the magnitude of the input voltage step minus $\sqrt{2}(V_{gs} - V_T)$ of the input differential pair transistors.

From equations 2.12 and 2.13 and the expressions for γ and κ it is possible to see that the effective slew rate is not only a function of I_1 and C_c, but is also a function of C_L, I_2 and β_5. Additionally, the effective slew rate is less than what is predicted by the simple equation I_1/C_c. To compensate for this degradation, I_1 needs to be over designed. Using the assumption that $I_2 \geq I_1(1 + C_l/C_c)$ and equation 2.12 a closed form expression for I_1 can be developed as follows

$$I_1 \geq \frac{1}{\frac{1}{C_c SR} - 4\frac{\sqrt{2}(\eta+1)[2(\sqrt{2}-1)\eta+2\sqrt{2}-3]tan(\frac{\pi}{2}-\phi_m)}{[2(\sqrt{2}+1)\eta+2\sqrt{2}+3]\eta\,\Delta V\,C_c\,UGF}} \tag{2.14}$$

Here, ϕ_m is the desired phase margin and $\eta = C_c/C_L$. A similar expression for the minimum I_1 that is able to meet the negative slew rate specification is shown in equation 2.15. The maximum of these two values can be used to design the opamp. The negative slew rate is usually always smaller than the positive slew rate for a NMOS input opamp because of the finite channel length modulation of transistors Q_3 and Q_4 such that current sourced during the slewing period is smaller than I_1. To account for this effect the extra term

(ψ) has been added to equation 2.15. For our process (2μ MOSIS CMOS) and the circuit configuration (simple current mirror) a value of $0.92 \leq \psi \leq 0.96$ was found to be adequate. This number will vary with processes and is inversely proportional to the channel modulation parameter λ.

$$I_1 \geq \frac{1/\psi}{\frac{1}{C_c SR} - 4\frac{(\eta+1)\sqrt{1-\psi}[2(\eta+1)\sqrt{1-\psi}-2\eta+\psi-2]tan(\frac{\pi}{2}-\phi_m)}{(2(\eta+1)\sqrt{1-\psi}+2\eta-\psi+2)\psi\eta\Delta V\,C_c\,UGF}} \tag{2.15}$$

From equations 2.12 and 2.13 it is clear that the error caused by the simplified expression for the slew rate (I_1/C_c) is proportional to γ. An approximate expression for γ can be developed and is shown in equation 2.16. It is clear that the value of γ increases as the ratio of the slew rate to bandwidth increases. For 60° of phase margin and $C_c = C_L$, γ is approximately equal to $SR/(2\,UGF)$ if the UGF is given in Hz. If γ is much smaller than 1.0 then the slew rate may be approximated by $I_1 C_c$ else the new expressions for the slew rate (equation 2.12 and equation 2.13) should be used.

$$\gamma \approx \frac{\sqrt{8}(1+\eta)tan(\frac{\pi}{2} - \phi_m)SR}{UGF} \tag{2.16}$$

Discussion and Simulation

The results discussed above have been corroborated using SPICE simulations. The circuit shown in Figure 2.3 was used for these simulations. Other specifications for this experiment are shown in the top section of Table 2.2. Simulation results and values for the output voltage predicted by our model and the traditional simple model are shown in Figure 2.4. There is excellent agreement between the simulation results and our model throughout the voltage range. We also note that the deviation is largest for small input steps as is predicted by equation 2.14 and equation 2.15. The traditional simplified model is only able to approximate the slewing behavior for large phase margin and a small slew rate/bandwidth ratio. Our model on the other hand is general and can predict the slewing behavior for all conditions.

We have designed two circuits, one using the simplified expression for slew rate and the other using our model for slew rate. Both circuits were designed for ($SR = 10V/\mu S$, $C_L = 10pF$, $C_c = 10pF$, $UGF = 6MHz$, $\phi_m = 45^o$). Other design parameters and measured and predicted slew rates are shown in the bottom half of Table 2.2. The numbers in top row of the bottom half correspond to the circuit designed using the simplified model and the numbers in the bottom row correspond to the circuit designed using our model. The
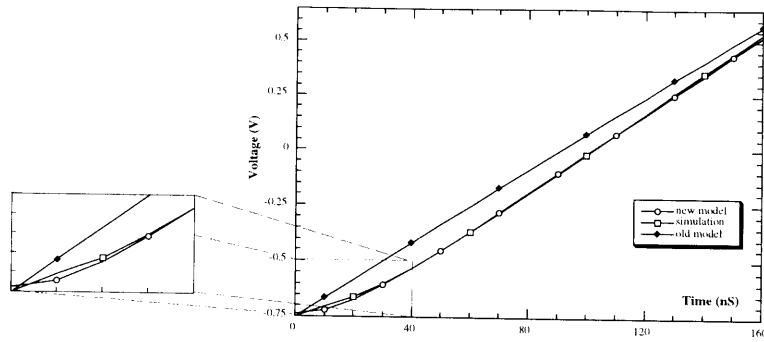
Figure 2.4.   Slew rate behavior: simulation vs model

Table 2.1.   Specifications used for model and verification

C_L(pF)	C_c(pF)	SR+(V/μS)	SR-(V/μS)	$UGF(MHz)$
10	4	10	10	6
$gm_1(\mu A/V)$	$gm_5(\mu A/v)$	$I_1(\mu A)$	$I_2(\mu A/v)$	ϕ_m
152	397	40	142	50

Table 2.2.   Design parameters of the normal and improved opamps

W_1/L_1	W_5/L_5	W_3/L_3	$I_1(\mu A)$	$I_2(\mu A)$
129	119	30	100	200
94	87	22	137.5	275

slew rate numbers in the last two columns are values predicted by our model. It is clear that more predictable slew rates are possible by using our model. The output waveform for a positive and a negative step for the two circuits is shown in Figure 2.5.

Summary

We have analyzed the slewing behavior of a two stage Miller compensated CMOS amplifier. In this section we have presented analytical expressions for the amplifier response during slewing. Using this expression for the output voltage we have developed an improved formula to calculate the effective slew

Table 2.3.   Slew rate from both simulation and model prediction

Simulation results		Model predictions	
SR+(V/μS)	SR-(V/μS)	SR+(V/μS)	SR-(V/μS)
8.91	7.97	8.87	7.76
11.87	10.01	12.06	10.05
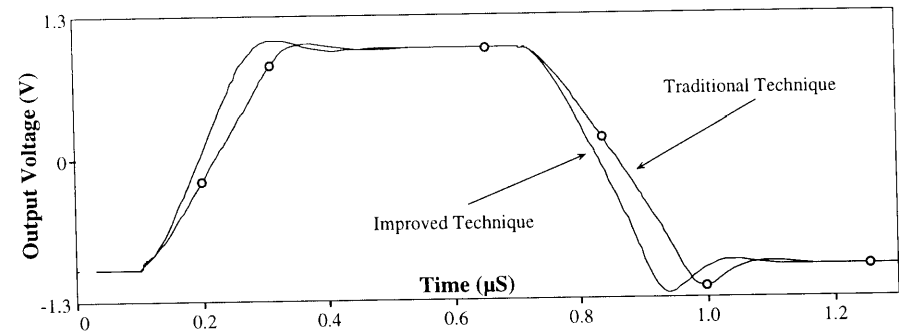
Figure 2.5.   The step response for the traditional and improved designs

rate. We also presented a closed form equation to determine the necessary tail current. The effect of the load capacitance, device sizes and bias currents are included in these new models. It was shown that small-signal models cannot be used to predict slewing behavior. Results from SPICE simulations were used to validate our analysis and design methodology. Our model is general and is applicable for all design parameters and simplifies to the traditional model ($SR = I_1/C_c$) for small values of γ.

2.3 A NEW CLASS AB OPAMP: PRINCIPLE AND DESIGN

Background

The increased complexity of analog and mixed-signal ICs makes it important to optimize the power to performance ratio. Additionally, there is a shift towards lower voltage operation. In order to achieve both these goals new circuit topologies and building blocks need to be explored. The operational amplifier (opamp) is perhaps one of most important and widely used building blocks [Wang and Harjani, 1996b]. Class A opamps have poor large signal behavior since their tail currents are constant resulting in a slew-limited transient response. An alternative solution is to use class AB opamps. They have a low and well-controlled quiescent current which is automatically boosted when a large differential voltage is applied. There are basically two classes of class AB opamps. The first class uses a source-coupled NMOS and PMOS transistors [Castello and Gray, 1985a]. However, this class of circuits is not suitable for low voltage operation. The second class of circuits utilizes a form of positive feedback to boost the tail current when required. Among them, adaptive biasing amplifier[Degrauwe et al., 1982] is based on a class A opamp and uses additional circuitry to obtain the current difference through the input transistor pair. This current difference is then fed back as additional tail current. The feedback current increases with increased input voltage. In [Nagaraj, 1990, Kline et al., 1989], the output current is boosted by measuring the differential input voltage. A large differential input voltage results in a large boosted output current. In [Gallewaert and Sansen, 1990] a new class AB principle is proposed. The circuit uses a current mirror to return a fraction the current through the input pair as additional tail current. Therefore, when a large differential voltage is applied, the total tail current increases. If the current mirror is perfectly matched and the current feedback ratio is equal to one then the output current is proportional to the square of the input voltage difference. Unfortunately, if the current feedback ratio is greater than one the circuit becomes unstable. Therefore, because of device mismatch the current ratio has to be less than one to avoid instability. Then, the output current is no longer proportional to the square of the input voltage difference.
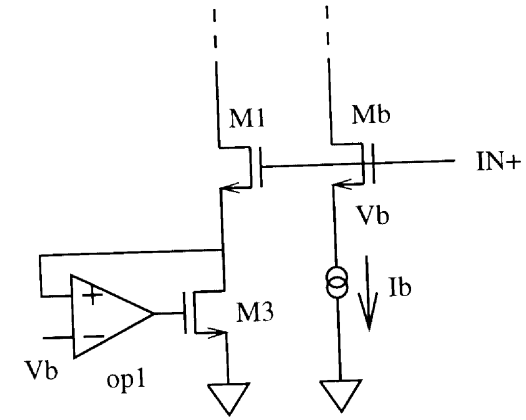
Figure 2.6.   Circuit schematic for self-biasing input transistor

In this section a new general-purpose class AB amplifier is introduced to solve some of the problems mentioned above. We first describe the principle of operation. As will be shown later in the text, our circuit behaves identically to the circuit in [Gallewaert and Sansen, 1990] for ideal current feedback and yet is completely stable. Some design consideration are also addressed and final conclusions are given.

The novel class AB OTA

Self-biasing input transistor.   Before we explain the basic operation of our novel class AB amplifier, let us first understand the operation of the proposed self-biasing input transistor shown in Figure 2.6. Transistor M_1 is the input transistor and transistor M_b is the auxiliary input transistor. Operational transconductance amplifier op1 and transistor M_3 forms a negative feedback loop. The negative feedback mechanism can be understood as follows. Suppose the source voltage of transistor M_1 increases slightly, consequently the output voltage of op1 will also increase. This increment will force voltage V_s to go down. This mechanism enables the source voltage of transistor M_1 virtually equal to the source voltage of transistor M_b. Due to the same gate and source voltage for M_1 and M_b respectively, the current density will be the same for these two transistors if we use square law and neglect channel length modulation. By correctly sizing the device dimension of transistor M_1 and M_b and choosing I_b, the quiescent current flowing through transistor M_1 can be well

controlled. The output voltage of OTA op1 is adjusted automatically to bias transistor M_3 in a such way that the required quiescent current is conducted. In [Gallewaert and Sansen, 1990] a similar self-biasing differential input pair is proposed. There are several differences between our proposed technique and the one in [Gallewaert and Sansen, 1990]. First, although both techniques involve feedback loop, our technique uses negative feedback loop while [Gallewaert and Sansen, 1990] uses positive feedback loop. Second, we use a single self-biasing input transistor as a basic building block while [Gallewaert and Sansen, 1990] use self-biasing differential input pair. Two of our building blocks can be combined into a differential pair explained in the next paragraph. In [Gallewaert and Sansen, 1990] due to the fact that the role of the two input transistor in the self-biasing differential input pair is not interchangeable. Another self-biasing differential input pair with opposite input polarity is required to form a complete opamp. As a consequence a fairly complex topology results.

Principle of new class AB OTA. The basic operation of proposed class AB amplifier can now be illustrated with the help of Figure 2.7. The circuit is constructed upon the principle of the self-biasing input transistor. Two such transistors are combined in a common source configuration. Except the input stage and tail current, the new circuit resembles the symmetrical OTA. Note that the proposed input pair can be extended to other circuit topologies, i.e., miller-compensated OTA without much effort. The key to understanding the circuit operation is to recognize that through the mechanism of negative feedback, the common source voltage of M_1 and M_2 is always forced to track the smaller of the two voltages, V_a and V_b. Without any loss of generality, let us assume that the gate voltage V_{in+} is larger than the gate voltage V_{in-}. Therefore, voltage V_b is larger than V_a. Effectively, the output voltage of opamp op_1 is pulled down, which turns off transistor M_4. Due to the negative feedback, the drain voltage V_s of transistor M_3 is equal to the voltage V_a. In other words, the voltage at the common source of M_1 and M_2 is constant with respect to the gate voltage of transistor M_2 and is only determined by the magnitude of V_{in-}, the device size of transistor M_a and the constant bias current I_b. A SPICE simulation of this condition is shown in Figure 2.8. This simulation shows the voltages V_a, V_b and V_s. Voltage V_a is kept constant and the voltage V_b is altered. In the figure we note that the voltage at V_s first follows V_b and then when V_b is greater than V_a it follows V_a.

Figure 2.7.   Overall circuit for the proposed class AB opamp
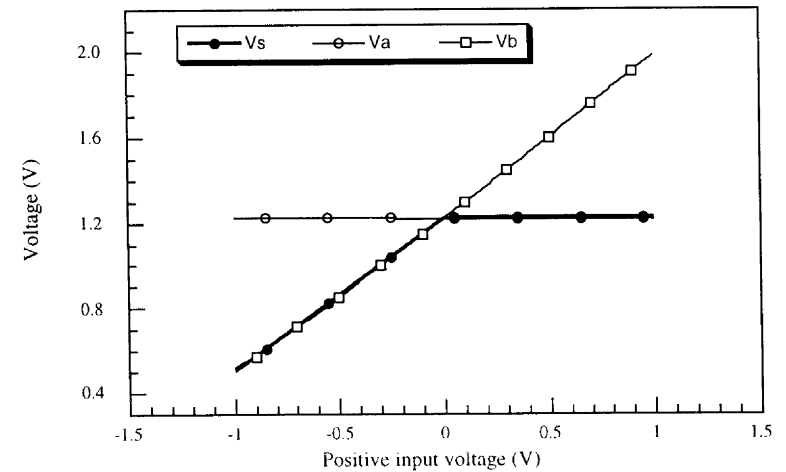
Figure 2.8.   Common source voltage vs. positive input voltage

Using the previous conditions the current through M_1 can be written as shown in equation 2.17

$$
\begin{aligned}
I_{M1} &= \tfrac{1}{2}k_n\left(\tfrac{W}{L}\right)_{M1}(V_{in+} - V_s - V_{Tn})^2 \\
&= \tfrac{1}{2}k_n\left(\tfrac{W}{L}\right)_{M1}(V_{in+} - V_a - V_{Tn})^2
\end{aligned}
\tag{2.17}
$$

Further, using the relationship between V_a and V_{in-}, i.e.,

$$
V_{in-} = V_a + \Delta V + V_{Tna}
\tag{2.18}
$$

the expression for the current I_{M1} can be rewritten as

$$
I_{M1} = \frac{1}{2}k_n\left(\frac{W}{L}\right)_{M1}(V_{in+} - V_{in-} + \Delta V)^2
\tag{2.19}
$$

where $\Delta V = \sqrt{2I_b/K_n(W/L)_a}$. We neglect the body effect by assuming V_{Tn} is equal to V_{Tna}. The above equation shows that I_{M1} is proportional to the square of the differential input voltage. A similar expression can be found in [1,2]. The maximum current, however, is limited by the supply voltage and the maximum current I_{M3} that transistor M_3 can sink. The current through transistor M_2 is the bias current I_b multiplied by the ratio of the device sizes of M_2 and M_a. By interchanging V_{in+} and V_{in-} in equation 2.19 we can derive an expression for the current through transistor M_2 when V_{in-} is larger than V_{in+}. A SPICE simulation of output current verse differential input voltage is shown in Figure 2.9. For this design the quiescent current I_b was set to $0.4\mu A$ and the device ratio $M_2/M_a = 10$. Note, however, that as the differential input voltage increases to 1V the output current increases to approximately $800\mu A$.

The quiescent current of the input stage is very well controlled. For a zero differential input voltage, V_a is equal to V_b and the common source voltage of the input pair (M_1 and M_2) is equal to V_a (V_b). Therefore, the quiescent current through the transistor M_1 (M_2) is given by equation 2.20. The quiescent current for the complete circuit can be kept small by selecting a small value for I_b.

$$
\begin{aligned}
I_{M1_{quiescent}} &= \tfrac{1}{2}k_n\left(\tfrac{W}{L}\right)_{M1}(V_{in+} - V_a - V_{Tn})^2 \\
&= \left(\tfrac{W}{L}\right)_{M1}\left(\tfrac{L}{W}\right)_{MA}I_b
\end{aligned}
\tag{2.20}
$$

In [Castello and Gray, 1985a] a source coupled NMOS and PMOS transistor pair is used to generate a current which is proportional to the square of the
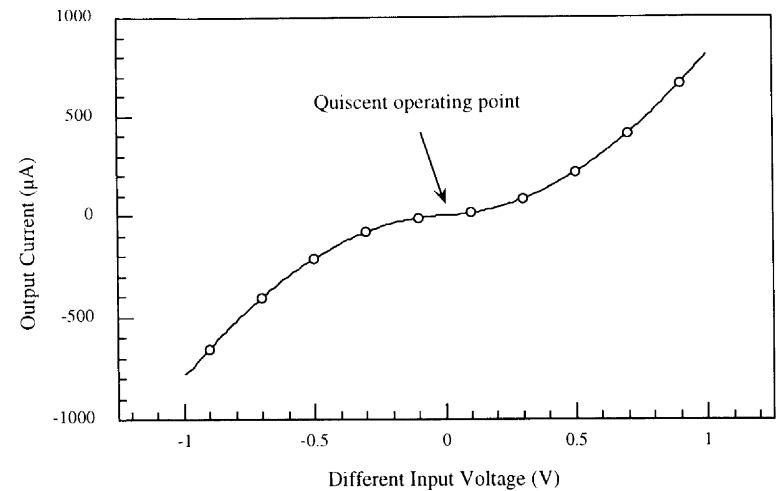
Figure 2.9.   Output current vs. differential input voltage

differential input voltage. However, this circuit suffers from limited common-mode input range and is not suitable for low voltage operation. The minimum supply voltage for this circuit is equal to $2V_T + 3(V_{gs} - V_T)$ [Huijing, 1993]. For our proposed circuit topology, the minimum supply voltage is equal to $V_T + 3(V_{gs} - V_T)$. Given a typical value of $V_{gs} - V_{Tn}$ of 0.2 V (edge of strong inversion) and V_{Tn} of 0.7 V, the former expression yields 2 V and the latter expression yields 1.3 V. The common input voltage range for our circuit is similar to that of a conventional class A opamp. It is clear that the proposed topology is suitable for low voltage operation.

To compare the power consumption of the proposed opamp with other opamp topologies, the current excess factor (CEF) is used [Degrauwe et al., 1982]. This CEF is defined as the ratio of the amplifier's current consumption I_{tot} and the current consumption by an ideal inverter operated in weak inversion with the same gain bandwidth and is given by

$$
CEF = \frac{I_{tot}}{2\pi n U_T C_L GBW}
\tag{2.21}
$$

where U_T is equal to KT/q, and n the weak inversion slope factor. The lower this CEF, the better the opamp uses the current to generate the desired GBW. Since the proposed opamp is built upon the symmetrical OTA, and if the current consumption of the auxiliary opamps and the auxiliary input pair can be made negligibly small, the proposed opamp will virtually have the same CEF

as the symmetrical OTA, i.e.,

$$CEF = \frac{B+3}{B}\frac{V_{gs}-V_T}{2nU_T} \tag{2.22}$$

For low frequency application up to 100 kHz, the proposed opamp exhibits superior CEF over the opamp proposed in [Gallewaert and Sansen, 1990], both with and without the cascode output.

Unlike the circuits in [Degrauwe et al., 1982, Gallewaert and Sansen, 1990], no positive feedback loop is involved in the proposed circuit. The circuit is therefore guaranteed to be stable. The negative feedback loops are only connected to the common source of the input pair. Therefore, to the first order the differential mode small signal behavior will not be affected by the negative feedback loops.

The maximum current through the input transistors can also be estimated. Again, we assume the gate voltage of transistor M_1 is larger that of transistor M_2. The source voltage is V_a which is determined by both the gate voltage V_{in-} and the bias current I_b. To ensure that transistor M_1 operates in the saturation region, we have following equations,

$$V_d \geq V_{in+} - V_{Tn} \tag{2.23}$$
$$V_d = V_{DD} - \Delta V_5 + V_{Tp} \tag{2.24}$$

where V_d is the drain voltage of transistor M_1, V_{Tp} is the threshold voltage for PMOS transistors and has a negative value and $\Delta V_5 = \sqrt{2I_{max}/K_n(W/L)_5}$. Therefore, the maximum achievable input voltage V_{in+} without entering triode operation region and the maximum current are as follows

$$V_{in+} = V_{DD} - \Delta V_5 + V_{Tp} + V_{Tn} \tag{2.25}$$

$$I_{max} = \frac{1}{2}k_n\left(\frac{W}{L}\right)_{M1}(V_{in+} - V_a - V_{Tn})^2 \tag{2.26}$$

By examining Equation 2.26, we can see that larger V_{in+} and smaller V_a will give larger current. However, voltage V_a can not be made too small. Otherwise, transistor M_3 will be forced into triode operation. For a given maximum current I_{max}, the minimum V_a will be equal to $\sqrt{2I_{max}/k_n(W/L)_3}$. To solve the above two equations simultaneously and to keep in mind that ΔV_5 and V_a are functions of I_{max}, the maximum current can now be written as

$$I_{max} = \frac{1}{(1+\alpha+\beta)^2}k_n\left(\frac{W}{L}\right)_{M1}(V_{DD} - V_{Tn})^2 \tag{2.27}$$

where

$$\alpha = \sqrt{k_n W_1 L_5 / k_p W_5 L_1} \tag{2.28}$$
$$\beta = \sqrt{W_1 L_3 / W_3 L_1}$$

The maximum current I_{max} can be made large if device size ratio W/L of transistor M_3 and M_5 are made large with respect to M_1. Normally the gate capacitances associated with these transistors are large too. Tradeoff needs to be made because these capacitances determine respectively the second pole frequency of the overall circuit and how quickly gate of transistor $M_3(M_4)$ can be charged and discharged.

Extension to weak inversion. The principle of the proposed class AB opamp can be easily applied to weak inversion. Assuming the input transistors work in saturation region, we can rewrite Equation 2.19 as

$$\frac{I_{M1}}{I_{M2}} = exp\frac{V_{in+} - V_{in-}}{nU_T} \tag{2.29}$$

where n is weak inversion slop factor and U_T the thermal voltage 26 mV. When only one gate voltage, i.g., V_{in+}, is swept, the current I_{M2} will be kept constant. Therefore, the current I_{M1} will increase exponentially with the differential input voltage as opposed to quadratically when the input transistors operate in strong inversion. If we denote V_{step} as the differential input voltage $V_{in+} - V_{in-}$ and I_{peak} the corresponding peak current, then we have the following relationship regarding peak current versus input step size.

$$\frac{I_{peak1}}{I_{peak2}} = exp\left(\frac{V_{step1} - V_{step2}}{nU_T}\right) \tag{2.30}$$

The above expression can be experimentally verified by measuring the peak currents for different input step sizes. Please note that the actually measured current peak ratio will be somewhat smaller than that predicted by Equation 2.30. This is because that when one gate voltage takes a step jump, the common source voltage V_s is not really fixed. It will tend to follow the gate voltage which in turn reduces the step size.

Negative feedback opamp . The negative feedback opamp (op_1, op_2) is shown in Figure 2.10. Because the input voltage of the feedback opamp is close to the negative rail PMOS input transistors are used. The diode connected transistor M_{5a} is added to prevent the output voltage of feedback opamp from going below V_{Tn}. The reason can be understood as follows. Suppose the input
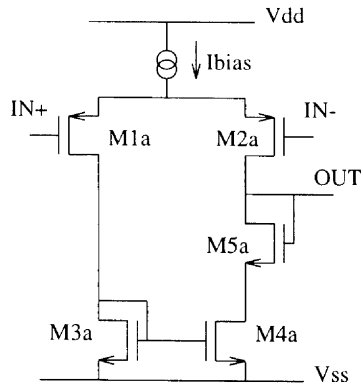
Figure 2.10.   Circuit schematic of negative feedback opamp

voltages change polarity, then each sink transistor (M_3 and M_4) changes state from *on* to *off* or from *off* to *on* respectively. If transistor M_{5a} is not added, the gate voltage of the transistor that was previously *on* (for instance M_4) is pulled down to the negative rail. In other words, it is turned off hard. With the result that turn-on time is large as the gate voltage has to be charged from zero to V_{Tn} before it starts operating. Unfortunately, this results in increased delay and cross-over distortion. Inserting a diode connected transistor ensures that the output voltage of the feedback opamp will not go below V_{Tn}. In this way, transistors M_3 and M_4 are at most weakly turned off when they are in the *off* state. Both signal delay and cross-over distortion are greatly reduced.

Negative feedback loop .   As mentioned before, the common source voltage V_s of transistor M_1 and M_2 tends to track the smaller value of V_a and V_b. This tracking function is provided by the negative feedback mechanism. The behavior of V_s responding to any change of voltage at the negative node of opamp $op1$ ($op2$ will directly affect the performance of the proposed class AB opamp. Let's investigate the small signal behavior of this loop. A small signal model is shown in Figure 2.11 where g_m, g_{m1} and g_{m2} are transconductances of input transistor inside $op1$ ($op2$), input transistor M_1 (M_2) and transistor M_3 (M_4) respectively. C_1 and C_2 are the total gate capacitance and drain capacitance of M_3 (M_4). All the conductances have been neglected. A set of equations governing the currents and the voltages are established as follows

$$g_m(V_o - V_{in}) = SC_2V_1 \qquad (2.31)$$

$$g_{m2}V_1 + g_mV_o = -V_oSC_1 \qquad (2.32)$$
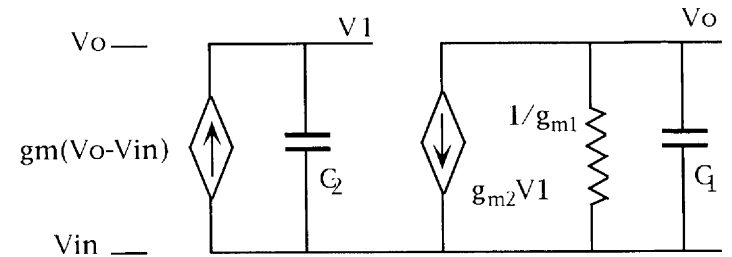
Figure 2.11.   Small signal analysis of negative feedback loop

The transfer function between V_{in} and V_o can be easily found as

$$\frac{V_o}{V_{in}} = \frac{g_mg_{m2}}{S^2C_1C_2 + SC_2g_{m1} + g_{m2}g_m} \qquad (2.33)$$

The rationalized denominator is

$$S^2 + \frac{\omega}{Q}S + \omega^2 \qquad (2.34)$$

where $\omega = \sqrt{g_mg_{m2}/C_1C_2}$ and $Q = \sqrt{g_mg_{m2}C_1/(g_{m1}^2C_2)}$. Depending on the value of Q, the step response of this feedback system will exhibits underdamping, critical damping and overdamping characteristics. For a critically damped transient response, Q needs to be equal to 0.5. This determines the maximum value of g_m which is $C_2g_{m1}^2/4C_1g_{m2}$.

Experimental results

The new class AB opamp shown in Figure 2.7 was fabricated using a MOSIS 2μm N-well process CMOS technology. A micrograph of the chip is shown in Figure 2.12. The opamp is biased with 2.5 V and with a bias current 10 nA. Figure 2.13 displays the DC transfer characteristic of the class AB opamp when operated in the unity gain feedback mode, as well as the offset voltage between the input and the output voltage. The opamp has a linear output range from 250 mV to 2.3 V. The measured offset voltage in the linear region is less than 40 mV. The expected offset value is around $2.5/A$, where A is the DC gain of the opamp. Since the opamp only has a single gain stage without any cascode transistor, the DC gain is normally around 100 which is be confirmed in Figure 2.14. The finite gain related offset is then around 25 mV. Therefore the random offset is approximately 15 mV (40 mV minus 25 mV).

Figure 2.14 shows the AC characteristic of the class AB opamp. The measured DC gain is around 42 dB, and the gain bandwidth is around 100 kHz.
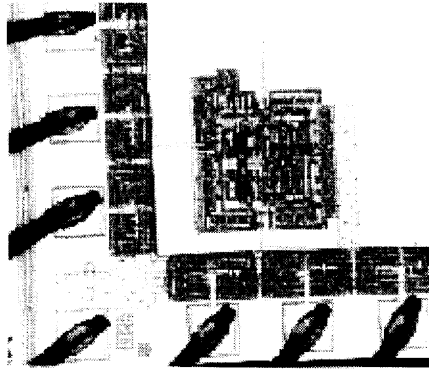
Figure 2.12.   Microphotograph of the chip

Figure 2.13.   Measured DC transfer function

The phase margin is at least 75 degrees for a $10pf$ load. If a cascoded output stage is used, the DC gain is expected to increase 100X. These measured data prove that small signal characteristics of the proposed class AB opamp is comparable to those obtained with conventional amplifiers.

The transient behavior for the opamp is shown in Figure 2.15. The opamp is configured in unity gain mode with a step input of 0.4 V. The supply current is monitored at the same time and is shown in Figure 2.16. From the figure, we can see that the supply current of the opamp (large spike) is substantially boosted when a large input step is encountered while the quiescent current remains low. The peak current versus quiescent current ratio is estimated to be around 100 which clearly demonstrates the superior large signal drive capability. Figure 2.17 shows the supply current for a step input of 0.3 V. In this case, the current peak is substantially reduced to about one-fourth of the value for 0.4 V input. This can be semi-quantitatively explained by Equation 2.29 since the input transistors operate initially in weak inversion. The difference between two input voltage steps should be equal to $nU_T ln(I_1/I_2)$. The numerical value of $nU_T ln(I_1/I_2)$ is around 0.06-0.07. The difference of the input steps is 0.1 (0.4 minus 0.3). The discrepancy is due to two factors. One is the reduced effective input step as mentioned before. The other is that one of the input transistor moves out of weak inversion and operate in strong inversion when the current dramatically increases.

Summary

In this section we have presented a new class AB opamp suitable for low voltage operation. An experimental circuit of this class AB opamp has been fabricated. It demonstrates a superior large signal performance with comparable small signal characteristics. Due to its superior large signal performance, the core circuit can also serve as an input stage of a buffer amplifier. Since there is no positive feedback the new opamp is unconditionally stable. The design is straightforward and modular. The core circuit, (shown in bold lines in Figure 2.7), can also be used to replace the differential pair of a large number of opamp topologies. The resulting circuits would all operate as class AB amplifiers.

2.4   TRANSIENT BEHAVIOR OF CLASS AB OPAMPS

In this section, the transient behavior of one type of class AB opamp is studied. Two examples of this type of class AB opamp are shown in Figure 2.7 and Figure 3.6. Though differing in specific details, they both exhibit the same current versus input voltage relationship. It can be easily shown that the
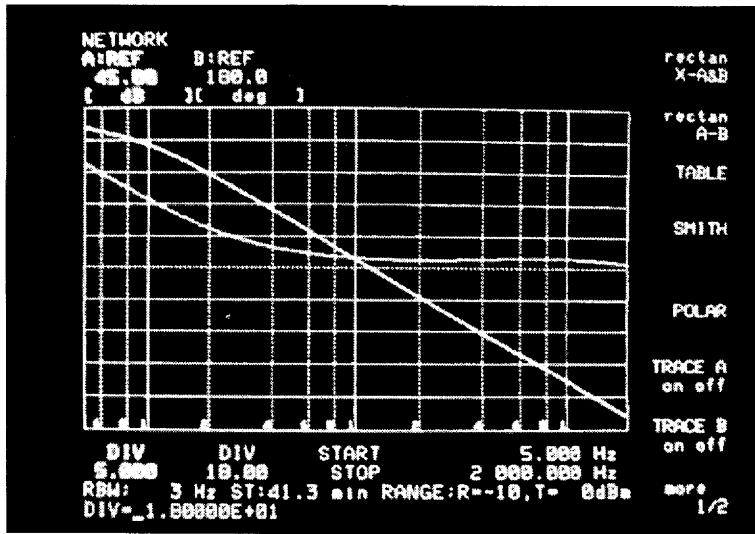
Figure 2.14.   Measured AC transfer function

currents flowing through the positive and the negative input transistors are

$$
\begin{aligned}
I^+ &= \tfrac{1}{2}\beta(V_{in}^+ - V_{in}^- + \Delta V)^2 \\
I^- &= \tfrac{1}{2}\beta(V_{in}^- - V_{in}^+ + \Delta V)^2
\end{aligned}
\tag{2.35}
$$

where ΔV is equal to $V_{gs} - V_T$ of the transistor. The net output current will take two different forms depending on the differential input magnitude $(V_{in}^+ - V_{in}^-)$. If $V_{in}^+ - V_{in}^-$ is larger than ΔV, one of two input transistors will be turned off, i.e., $I^- = 0$. The net output current will be

$$
\begin{aligned}
I_{out} &= I^+ - I^- \\
&= \tfrac{1}{2}\beta(V_{in}^+ - V_{in}^- + \Delta V)^2
\end{aligned}
\tag{2.36}
$$

The period in which only one input transistor conducts current is called the large signal period . On the other hand, if $V_{in}^+ - V_{in}^-$ is smaller than ΔV, both input transistors conduct current, i.e.,

$$
\begin{aligned}
I_{out} &= I_+ - I^- \\
&= 2\beta\Delta V(V_{in}^+ - V_{in}^-)
\end{aligned}
\tag{2.37}
$$

The period in which both transistors conduct current is called the small signal period . Both the large and the small signal periods are explained in detail in
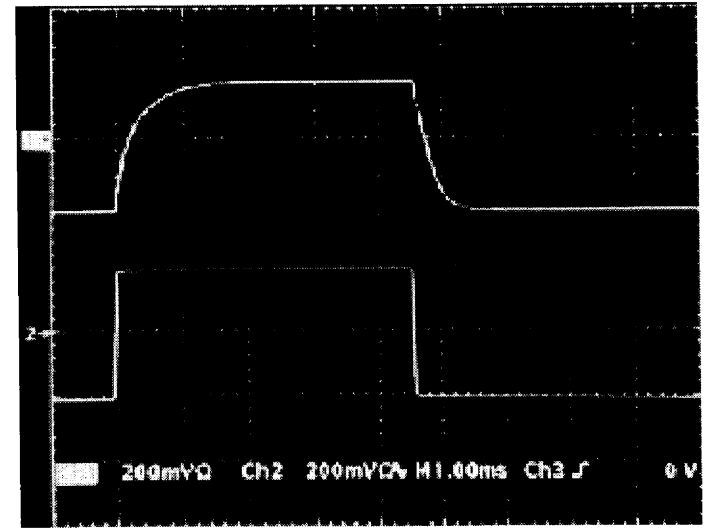
Figure 2.15.   Transient response of the opamp to a step input (0.4 V)

Chapter 3. Now we assume the opamp is configured in a unity gain (source follower) fashion and therefore the output voltage V_o is equal to V_{in}^-. The dynamic behavior of the output voltage can be described by Equation 2.38

$$
C_L \frac{dV_o}{dt} = I_{out}
\tag{2.38}
$$

The solution of the above different equation is different in the two periods as shown below.

Large signal period. In the large signal period, Equation 2.38 can be reduced to

$$
C_L \frac{dV_o}{dt} = \frac{1}{2}\beta(V^+ - V_o)^2
\tag{2.39}
$$

where V^+ is equal to $V_{in}^+ + \Delta V$. The solution to Equation 2.39 is then

$$
V_o(t) = \frac{\beta V_+^2}{2C_L} \frac{t}{1 + t/t_o}
\tag{2.40}
$$

where $t_o = 2C_L/\beta V_+$ and $V_o(0) = 0$ is assumed. We can calculate the duration of the large signal period based on the fact that the large signal period ends
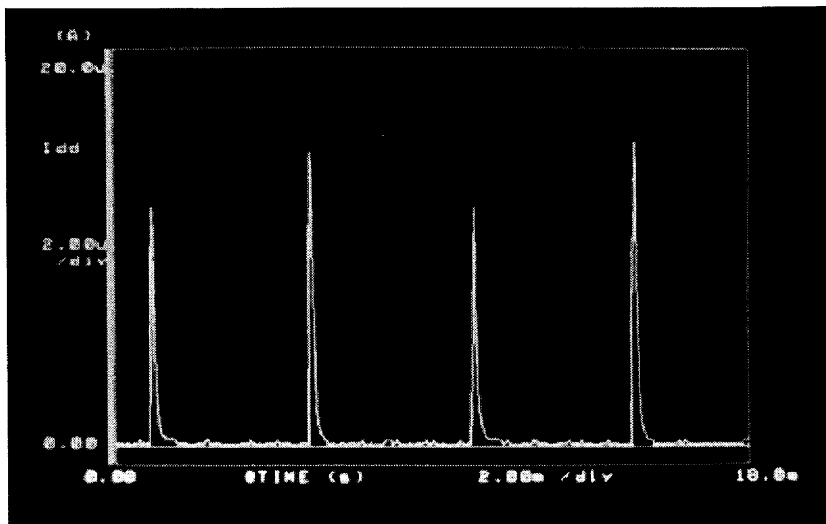
Figure 2.16.   Transient response of current supply for a step input (0.4 V)

Figure 2.17.   Transient response of current supply to a step input (0.3 V)

when the voltage difference between the positive and the negative input is equal to ΔV, i.e.,

$$V_{in}^+ - \frac{\beta V_+^2}{2C_L}\frac{t_{la}}{1 + t_{la}/t_o} = \Delta V \tag{2.41}$$

It can be easily shown that

$$t_{la} = \frac{V_{in}^+ - \Delta V}{2\Delta V}t_o \tag{2.42}$$

We can calculate an effective slew rate (SR_{eff}) for this type of class AB opamp. In accordance with the normal definition of slew rate, SR_{eff} is defined as the effective voltage difference $V_{in}^+ - \Delta V$ divided by the time t_{la}, i.e.,

$$\begin{aligned} SR_{eff} &= (V_{in}^+ - \Delta V)/t_{la} \\ &= \beta\Delta V(V_{in}^+ + \Delta V)/C_L \end{aligned} \tag{2.43}$$

However if a regular class A opamp is used instead, its slew rate would then become

$$\begin{aligned} SR &= 2I_{in+}/C_L \\ &= \beta(\Delta V)^2/C_L \end{aligned} \tag{2.44}$$

where I_{in+} stands for the quiescent current flowing through the positive input transistor. The factor 2 accounts for the fact that during the slewing period

twice of the input transistor current is used for charging or discharging the load capacitor C_L (assume the ratio of the current mirror is one).

The benefit of using a class AB opamp is seen by comparing the two slew rates for both class A and class AB opamps. The ratio of the two slew rates can be written in Equation 2.45

$$\frac{SR_{eff}}{SR} = 1 + \frac{V_{in}^+}{\Delta V} \tag{2.45}$$

The ratio has a typical value of 10 if we chose 2 V and 0.2 V for V_{in}^+ and ΔV.

Small signal period. In the small signal period, the dynamic of output voltage becomes

$$C_L\frac{dV_o}{dt} = 2\beta\Delta V(V_{in}^+ - V_o) \tag{2.46}$$

The solution for the above equation is

$$V_o(t) = V_{in}^+ - \Delta V e^{-\frac{2\beta\Delta V}{C_L}(t-t_{la})} \tag{2.47}$$

To achieve a given error percentage ϵ, the class AB opamp has to settle for a period of time t_{sm} which is

$$t_{sm} = \frac{C_L}{2\beta\Delta V} ln \frac{\Delta V}{\epsilon V_{ref}} \qquad (2.48)$$

It is our interest to calculate the ratio of the large and small signal period. The ratio measures to what degree the whole transient process is linear with respect to the input voltage. With the help of Equation 2.42 and Equation 2.48, the ratio boils down to

$$\frac{t_{sm}}{t_{la}} = \frac{1}{2}\frac{V_{in}^+ + \Delta V}{V_{in}^+ - \Delta V} ln \frac{\Delta V}{\epsilon V_{ref}} \qquad (2.49)$$

Suggested by Equation 2.49, the allocation of the time for the large and the small signal period is dependent on the magnitude of the input value. Therefore, the whole transient behavior can not be characterized as a linear settling one. We can use the linear settling assumption only if

- differential input is always smaller than ΔV or

- V_{in}^+ is much larger than ΔV.

In the case of second condition, Equation 2.49 boils down to

$$\frac{t_{sm}}{t_{la}} = \frac{1}{2} ln \frac{\Delta V}{\epsilon V_{ref}} \qquad (2.50)$$

For delta-sigma modulators, none of above two conditions is satisfied. Therefore, this type of class AB opamp should be avoided to implement high resolution and/or high linearity modulators.

One must remember that our result for the small signal period is based on a single-pole model for the opamp. More dedicated two-pole model can be used to yield fine structure of the above result. A useful but lengthy derivation can be found in [Shulman and Yang, 1994]. The advantage of our simplified model is not only to be able to examine the claim of the linear settling process but also to give a first cut calculation (Equation 2.49) of the allocation of time for each period. It is therefore convenient for circuit designers.

2.5 DYNAMIC OPAMPS: SLEWING, SETTLING AND POWER ISSUES

Background

Copeland and Rabaey first suggested a dynamic MOS amplifier in an inverter form [Copeland and Rabaey, 1979]. Later a family of dynamic amplifiers were

proposed and their performance was measured by Hosticka [Hosticka, 1980, Hosticka, 1981]. Also, a low power SC bandpass filter was described using dynamic opamps [Hosticka et al., 1982]. However, previous efforts have provided only a rudimentary understanding of the amplifier operation. In an effort to solve this problem, we provide a rigorous analysis of the settling and slewing behavior of dynamic opamps. We also compare dynamic opamps with traditional class A amplifiers. Dynamic opamps are particularly well suited for switched-capacitor circuits. The basic idea is that the amplifier is only required during the charge transfer period. For example, for the simple integrator shown in Figure 2.18, the charge is transferred from $C1$ to $C2$ and C_{load} during the early part of $\Phi1$. The amplifier needs to operate only during these periods. During this period the amplifier begins its operation with a large current (high speed) and rapidly ends up with a small current (high gain). Due to this inherent regulation of the bias current, dynamic amplifiers meet the two important requirements for switched-capacitors: fast and complete charge transfer.
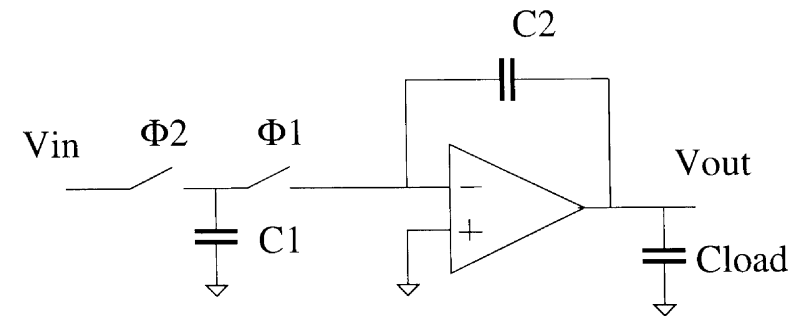
Figure 2.18. Switched-capacitor integrator

Analysis of dynamic amplifiers

Current characteristics. We begin our discussion with the bias current behavior of dynamic opamps. The bias current scheme suggested by Hosticka [Hosticka, 1980] is used and shown in Figure 2.19. The circuit operates in the following manner. During $\Phi2$ C_o is discharged and there is no current flowing through transistor M_4 and M_5. During $\Phi1$ the voltage at node 1 starts at V_{dd} and rapidly decreases as C_o charges up. Transistor M_1 and M_3 are the differential input pair of the amplifier. Transistor M_2 is not necessary for the basic operation of the bias circuit, however, it serves two important purposes. First, it provides a voltage drop between nodes 1 and 2 during $\Phi1$. If M_2 is not included then the initial gate voltage of M_4 and M_5 will be equal to the supply

voltage (V_{dd}). Therefore, the minimum voltage across M_5 before it goes out of the saturation region is equal to $V_{dd} - V_{Tn}$. This severely limits the minimum common-mode voltage of the amplifier. Second, the gate voltage and size of M_2 can be adjusted to tailor the bias current. Assuming transistor M2 is in
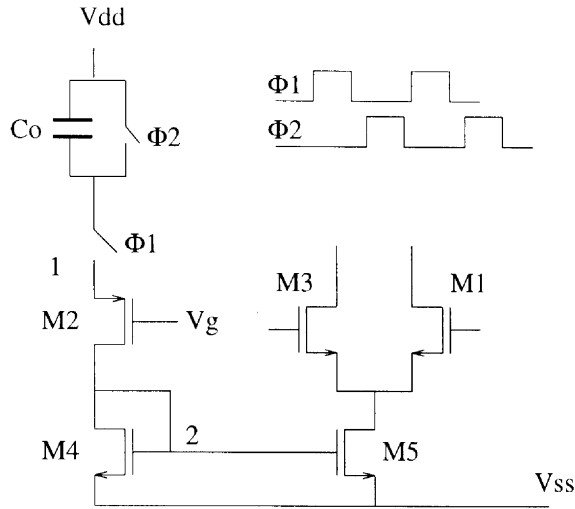
Figure 2.19.   Bias current scheme

the saturation region, one can easily derive the following equation for the bias current

$$I(t) = \frac{I_p}{(1 + t/t_o)^2},\qquad(2.51)$$

where $I_p = \frac{1}{2}k_p \frac{W_2}{L_2}\Delta V^2$, $t_o = C_o\Delta V/I_p$, $\Delta V = V_{DD} - V_g + V_{Tp}$. The current behavior can be totally described by two parameters: the peak current I_p and the time constant t_o. As long as transistor M_2 is in the saturation region, the size of M_4 has virtually no effect on the current behavior. One can ensure that M_2 remains in saturation by setting $V_g > V_{2max} + V_{Tp}$. V_{2max} can be made to be approximately equal to V_{Tn} by maintaining a large W/L ratio for M_4. Providing a large ratio for M_4 has the additional advantage that the common-mode input range for the opamp is maximized. Simulation results for two different W/L ratios of M4 are shown in Figure 2.20.

Slew rate and power consideration.   Slewing occurs when the differential input voltage is larger than the ΔV_d (I/g_m) of the differential pair transistors. During this period one of differential pair transistor (M_1 or M_3) is completely
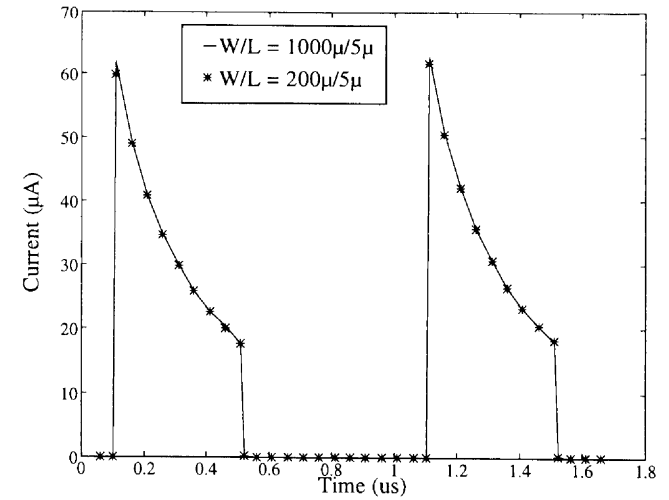
Figure 2.20.   Bias current behavior

shut off while the other one is completely on. The entire bias current (I_{ds5}) is used to charge or discharge the load capacitor. For simplicity, the single-stage opamp shown in Figure 2.26 is used for this analysis. The behavior is similar for other opamp circuits and only differs in the details. For example, for the two-stage Miller compensated opamp, during the slew period, the bias current charges and discharges the compensation capacitor rather than just the load capacitor. The final voltage V_f of dynamic opamps that will be reached at time t_d can be determined as follows

$$V_f(t_d) = \frac{1}{C_L}\int_0^{t_d}\frac{I_p}{(1 + t/t_o)^2}dt = \frac{I_p t_o}{C_L}\frac{t_d/t_o}{1 + t_d/t_o}.\qquad(2.52)$$

Combining Eq. 2.52 with the expression for I_p we have

$$t_d = \frac{\alpha C_L}{C_o - \alpha C_L}t_o,\qquad(2.53)$$

where $\alpha = V_f/\Delta V$. From the above expression, we can estimate the minimum value of Co. In order for the output to reach the final value before the end of $\Phi 1$, the condition $C_o > \alpha C_L \times (1 + kt_o/T_c)$ should hold. T_c is the clock period and k is a constant larger than 2. Using the above expressions, we can also define an effective slew rate (SR_d) for dynamic opamps $SR_d = V_f/t_d = \frac{C_o - \alpha C_L}{\alpha C_L t_o}V_f$. Using the same constraint for a class A opamp, the slewing period is equal to

T_c/k. Therefore, the slew-rate for a class A opamp is equal to $SR_A = V_f/t_A = kV_f/T_c$.

One of primary incentives to use a dynamic opamp is to save power. By appropriately regulating the bias current, the maximum power is consumed during the charge transfer period. Little or no power is consumed during the rest of the clock period. Therefore, the average power consumed is expected to be small. The average current flow can be calculated as follows

$$I_{av} = \frac{1}{T_c} \int_0^{\frac{T_c}{2}} \frac{I_p}{(1 + t/t_o)^2} dt = C_o \Delta V \frac{f_c f_o}{2f_c + f_o}, \qquad (2.54)$$

where $f_o = 1/t_o$ and $f_c = 1/T_c$. In the above expression, half duty cycle for the clock is assumed without any loss of generality. The power consumption is therefore $P_d = I_{av}V_{DD}$. For a class A opamp, the power consumption is given by $P_A = C_L V_{DD} SR_A$. We are now able to compare dynamic opamps with class A opamps. Under the same slew rate constraints, the power ratio can be expressed as

$$\frac{P_d}{P_A} = \frac{C_o f_c}{2f_c(C_o - \alpha C_L) + C_L SR/\Delta V}. \qquad (2.55)$$

This power ratio vs. clock frequency ($\alpha = 1$) is plotted in Figure 2.21. Dynamic
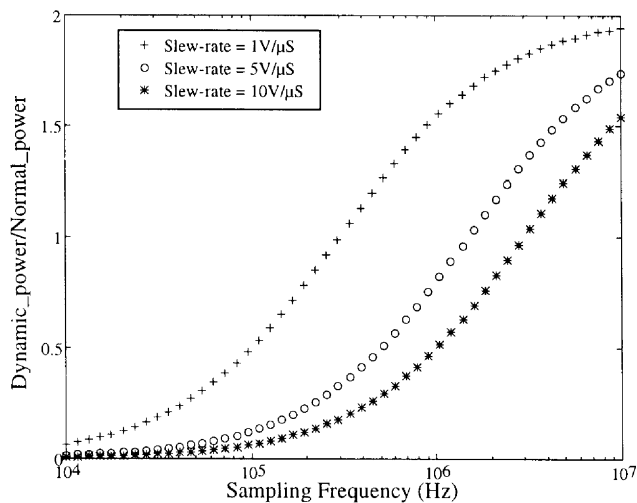
Figure 2.21.   Frequency dependence of power consumption

opamps consume less power than class A opamps at lower frequencies and become comparable at higher frequencies. Also, the larger the slew rate, the

higher is the savings. If we want the output to slew to the final value in a fixed portion of clock period, i.e., k is constant, the power ratio can be written as

$$\frac{P_d}{P_A} = \frac{C_o}{2C_o + \alpha(k-2)C_L}. \qquad (2.56)$$

This ratio is independent of the clock frequency. As long as $k > 2$, dynamic opamps consume less power than class A opamps for all frequencies. In the next section, a more detailed analysis containing the settling period also leads to a similar conclusion.

Settling behavior.   The closed loop voltage follower configurations shown in Figure 2.22 are used to derive the relationships for both the class A and the dynamic opamps. The total transient time is a very critical parameter in
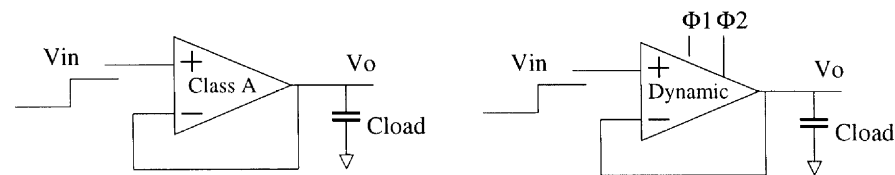
Figure 2.22.   Closed loop configuration

many applications, including switched-capacitor circuits and data converters. It consists of two separate periods, a slewing period and a settling period. The slewing period is determined by the available supply current and the input step. During the slewing period one of the differential pair transistors is completely off and so the amplifier is working in an open loop format. The simple small-signal model can no longer be used. As the output approaches the final value, the differential pair transistors enter their normal operating region and the circuit works in a closed loop form. The small-signal model is valid thereafter. There has been some previous efforts to analyze the transient behavior of class A amplifiers [Chuang, 1982, Lin and Nevin, 1986]. In these papers, a two-pole model has been used and both the frequency domain and time domain behavior have been studied. Analytical expressions for the total transient time were also derived.

In this section, the settling period for dynamic amplifiers in the unity gain frequency closed loop configuration shown in Figure 2.22 is studied first. Then analytical expressions for the total transient time are derived and compared to those for class A amplifiers. Due to the time-varying characteristics of the bias current the mathematical complexity of the two-pole small signal model makes it almost impossible to develop an analytical solution for the dynamic opamp.

A numerical solution is possible, however, it doesn't provide insight into the basic operation of the dynamic amplifier. Additionally, a two-pole model can be approximated by a single pole model when the second pole frequency is much higher than the unity gain frequency, i.e., large phase margin> 70°. In our analysis, the single-pole model is adopted. For a unity gain frequency configuration, the equation governing the output voltage for a step input can be written as

$$C_L \frac{dV_o(t)}{dt} + g_m(t)V_o(t) = g_m(t)V_{in} \qquad (2.57)$$

where $g_m(t) = \frac{g_{mo}}{1+(t+t_r)/t_o}$ is the transconductance of the input differential pair, t is the time after the input is applied, and t_r is the time interval between the rising edge of $\Phi 1$ and the moment when the input is applied. V_{in} is the unit step function. In the above expression, the g_{ds} of the output stage is neglected. Since $g_{ds}(t)/g_m(t) \propto \sqrt{I(t)}$ and since $I(t)$ decreases with time the effect of g_{ds} becomes more negligible as time progresses. An analytical solution for Eq. 2.57 is given by Eq. 2.58

$$V_o(t) = 1 - \frac{1}{(1 + t/(t_o + t_r))^k}, \qquad (2.58)$$

where $k = g_{mo}t_o/C_L$ and $g_{mo} = \sqrt{k_n W/LI_p}$. The comparison of this model with simulation results is shown in Figure 2.23. There is extremely good agreement between simulation results and the model.

One concern of dynamic opamps is that since the bias current is decreasing and becomes small towards the end of each $\Phi 1$, the settling period can be stretched [Laber and Gray, 1988]. This is true, however, the slewing period should be taken into account when considering the total transient time. For class A opamps, when the differential input is smaller than the certain threshold voltage (ΔV_d), the opamp undergoes settling only. On the other hand, when the differential input is larger than this threshold voltage, the opamp first slews and then when the difference between the input and output is less than ΔV_d it settles. This also holds true for dynamic opamps. Using a single-pole model the total transient time for a given input for a class A opamp can be written as

$$T_{total} = \begin{cases} -\tau ln\epsilon & \text{if } V_{in} < \Delta V_d \\ -\tau ln\frac{V_{in}}{\Delta V_d} + \frac{V_{in}-\Delta V_d}{SR_A} & \text{otherwise} \end{cases}$$

where V_{in} and SR_A are the differential input step and the slew rate of the class A opamp, respectively. Epsilon (ϵ) is the acceptable error percentage for the final value. A more rigorous yet similar solution using the two pole model can be found in [Chuang, 1982]. Likewise, for dynamic opamps the expression for
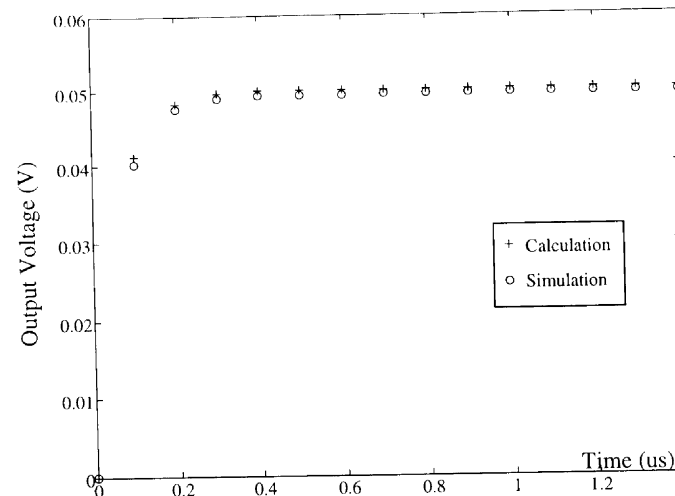
Figure 2.23.   Comparison of settling behavior

the total transient time is

$$T_{total} = \begin{cases} (\epsilon^{-\frac{1}{k}} - 1)t_o & \text{if } V_{in} < \Delta V_D(0) \\ T_s + (t_o + T_s)(\{\frac{\epsilon V_{in}}{\Delta V_D(T_s)}\}^{-\frac{1}{k}} - 1) & \text{otherwise} \end{cases}$$

where $\Delta V_D(0) = I_p/g_{mo}$ is the threshold voltage in the beginning of $\Phi 1$. T_s is the slewing time. Since the bias current is time-varying, so is the threshold voltage. $\Delta V_D(T_s) = \frac{\Delta V_D(0)}{1+T_s/t_o}$ is the threshold voltage at t is equal to T_s when the dynamic opamp starts to enter the settling period (small signal model is valid). The derivation of the pure settling part ($V_{in} < \Delta V_D(0)$) is straightforward from Eq. 2.58. For the slewing plus the settling part ($V_{in} \geq \Delta V_D(0)$), the slewing time can be found from the following equation

$$V_{in} - \frac{I_p t_o}{C_L} \frac{T_s/t_o}{1+T_s/t_o} = \frac{\Delta V_D(0)}{1+T_s/t_o}. \qquad (2.59)$$

To get this result, Eq. 2.52 is used with $t_d = T_s$. Figure 2.24 shows the total transient time vs. input voltage for both the class A and dynamic opamps under the same power consumption constraint. In this figure, one can notice that the total settling time for the dynamic opamp is always less than that for the class A opamp. In other words, for the same total transient time, dynamic opamps will consume less power. This can be understood as follows. When slewing takes place, due to the large initial supply current, the output
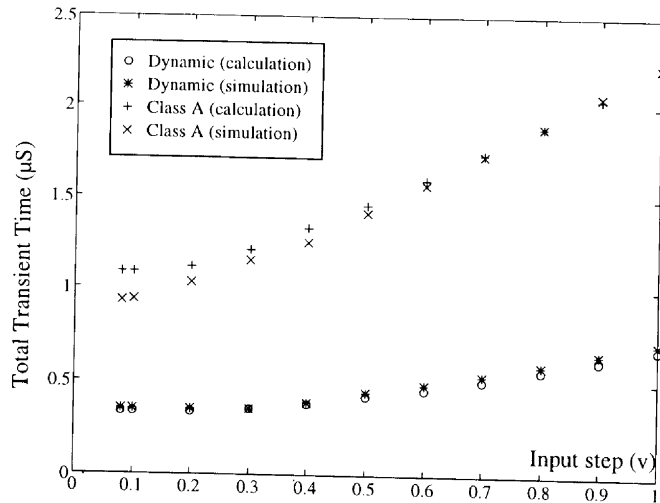
Figure 2.24.   Total transient time for different input steps

Figure 2.25.   Settling time for different input steps

voltage for a dynamic opamps increases more rapidly than that of a class A opamp. Consequently, a dynamic opamp starts settling much sooner than its counterpart. Therefore, the dynamic opamp will still have a large current to settle to its final value which results in smaller settling times. This is further illustrated in Figure 2.25. The settling period for different input steps is smaller for the dynamic opamp than that for the class A opamp. This is because the settling period of the dynamic opamp depends not only on the input step size, but also on the slewing period as illustrated by the total transient time expression. When the input step is larger, so is the slewing time T_s and, therefore, the available bias current becomes smaller. However, the threshold voltage $\Delta V_D(T_s)$ to enter the linear region becomes smaller too. This two opposite trends leads to a smaller variation of the settling time.

Design example

In this section, a design example is provided to emphasize the use of biasing techniques to generate high gain opamps. One method to increase the gain of a normal opamp is to use cascoding techniques. However, care must be taken with dynamic opamps due to the dynamically changing bias current. Traditional cascoding techniques prove to be problematic due to the large initial bias current. Alternatively, completely dynamic biased current mirrors may be used as done in [Castello and Gray, 1985a]. However, a simpler constant bias

low-voltage cascode [Babanezhad and Gregorian, 1987] can be used as shown in Figure 2.26. For this circuit the bias voltage V_{bn} and V_{bp} are kept constant. In general the bias voltages need to be selected such that transistors remain in the saturation region. For example, the bias voltage V_{bn} needs to be selected such that it meets the constraints given in Eq. 2.60

$$V_{Tn} + (m+1)\Delta V_3 < V_{bn} < 2V_{Tn} + \Delta V_3 \qquad (2.60)$$

where ΔV_3 is equal to $(V_{gs3} - V_{Tn})$ and is proportional to $\sqrt{I}$. Since in the dynamic case the current is time varying, so the selected range of V_{bn} also becomes time varying. When the bias current starts at the maximum value $I_{max} = I_p$, the upper bound and lower bound of the bias voltage range are V_{umax} and V_{lmax}, respectively. When the opamp enters the $\Phi 2$ period the bias current has reduced to a minimum value I_{min}. The corresponding upper bound and lower bounds becomes V_{umin} and V_{lmin}. Figure 2.26 shows these voltage bounds schematically. If there is an overlap between these two regions, then any value within this area can be used to bias the opamp safely. If there is no overlap then either a dynamically biased mirror can be used or a totally different current mirror may be used. In other words, the condition $V_{lmax} < V_{umin}$ must hold. This condition sets the peak current value for the bias current generator shown in Figure 2.19 and is given by $I_{max} = min\{k_n(\frac{W}{L})_3(\frac{V_{Tn}}{m+1})^2, k_p(\frac{W}{L})_{31}(\frac{V_{Tp}}{m+1})^2\}$.
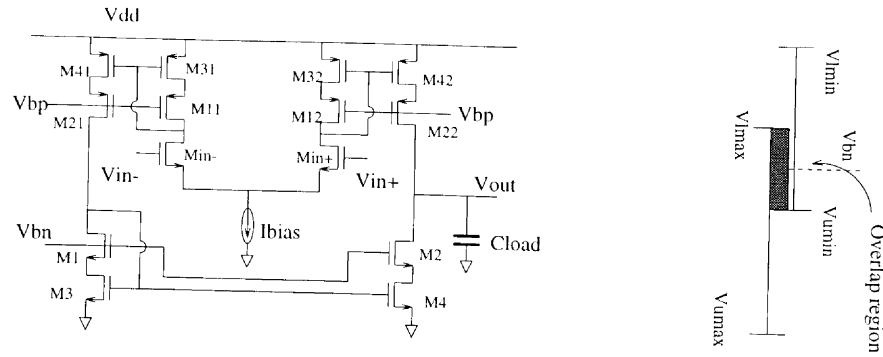
Figure 2.26.   Single-Stage OTA with bias scheme

Summary

In this section, analytical expressions are developed for, and the performance of dynamic amplifiers is compared with those of class A amplifiers. The relationships between the performance and the circuit parameters are derived. An analytical expression for the settling behavior for dynamic amplifiers is presented for the first time. By using this model, it is shown that under the same power condition, dynamic opamps settle to the final value quicker than class A opamps. Finally, a cascoded single stage dynamic opamp is presented.

2.6   CONCLUSIONS

The understanding of the transient behavior of the opamps is indispensable to the optimal design of modulators for oversampled converters. In this chapter, we have analyzed the transient process of three opamp types: class A opamps, class AB opamps and dynamic opamps.

An improved slew-rate model has been suggested for the two-stage Miller-Compensated opamps. This model is used to calculate the opamp's effective slew rate. A design example is given to validate the superiority of our method.

A better understanding of one class of class AB opamps is obtained through the rigorous analysis of its large signal and small signal period. An expression for an effective slew rate of the opamp is derived. Based on our derivations, the commonly used class AB opamps are not suitable for high resolution/high linearity delta-sigma modulators because the settling process is not really linear. Additionally as we will see in Chapter 5, the use of class AB opamps will result in additional nonlinearities through the power line. However, if the power budget is the primary concern rather than high resolution/high linearity, the use of class AB opamps can save sizable power as shown in Chapter 3.

The idea of dynamic opamps originates from the motivation to achieve both fast charge transfer and the large opamp gain simultaneously. We have completely analyzed their slewing and settling behavior. Again an effective slewing rate is given. We demonstrated that under the same power consumption, dynamic opamps settle to the final value quicker than their class A counterparts. This makes them suitable for low power low resolution/linearity applications. Unfortunately the transient nature of the supply current limits their use in high resolution/linearity delta-sigma converters.

3 OPTIMAL DESIGN OF OPAMPS FOR OVERSAMPLED MODULATORS

3.1 INTRODUCTION

Oversampled A/D converters are widely used in instrumentation, data acquisition, telecommunication, and consumer electronics. Advantages of oversampled A/D converters include a higher dynamic range and a larger signal-to-noise ratio than traditional architectures. Additionally, in these converters the requirement for precisely matched components is relaxed. In these converters the operational amplifier within the modulator is the most critical component. For instance finite gain, bandwidth and slew rate of the opamp cause an incomplete transfer of charge in the integrator which in turn causes nonlinearities. To show this effect, in Figure 3.1 we plot the error voltage, (the output voltage minus the input voltage), versus the input voltage for a first order delta-sigma converter. The gray curve shows the ideal behavior while the dark curve shows the effect of finite settling of the opamp. The sharp peaks in both curves are the result of tones [Candy and Benjamin, 1981]. Previous research [Medeiro and Perez-Verdu, 1994] has shown that some amount of harmonic distortion is inevitable. Additionally, it has been shown that the amount of distortion is input signal dependent. While a perfect opamp is not feasible, we can design
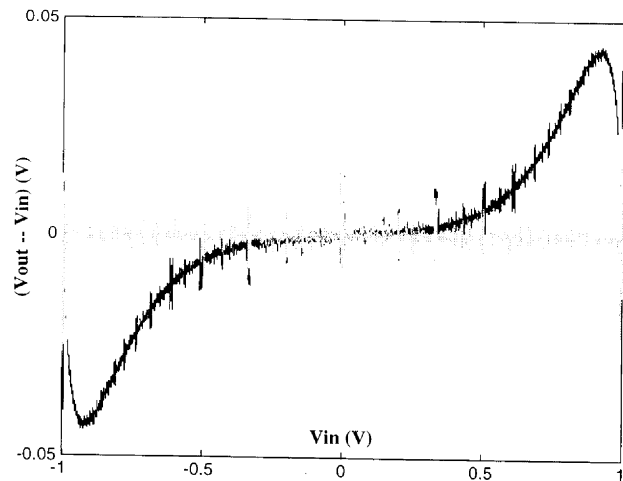
Figure 3.1.   Nonlinearity due to finite settling

an opamp to settle sufficiently for any given resolution. This accuracy in settling directly translates into a minimum bound on the power dissipated by the opamp. In [Castello and Gray, 1985b], Castello *et al.* addressed the issue of minimum power dissipation in a general SC filter for sine wave inputs. However, their method can not be extended to delta-sigma modulators directly due to the existence of the large feedback reference voltage in delta-sigma modulators. In [Degrauwe and Salchi, 1984], Degrauwe *et al.* developed an expression for the minimum transconductance for the opamp used in a micropower SC filter. However, in their paper the input signals are always assumed to be small such that there is no slewing. This is not true for opamps in delta-sigma modulators.

In this chapter, we address three issues related to the optimal design of oversampled converters: the theoretical minimum power dissipated by an ideal opamp; the best opamp topology in terms of power consumption and the optimal design strategy to achieve minimum power consumption for a class A opamp. This chapter extends the results presented in [Wang and Harjani, 1996a]. In Section 3.2 we classify some commonly used opamps for delta-sigma converters. In Section 3.3 we develop a general switched-capacitor (SC) integrator model that includes the large feedback signal inherent in delta-sigma modulators. In Section 3.4 and Section 3.5 we develop a model for the power consumed by the different opamp topologies classified in Section 3.2 and conduct a power comparison among them. In Section 3.6 we develop an optimal
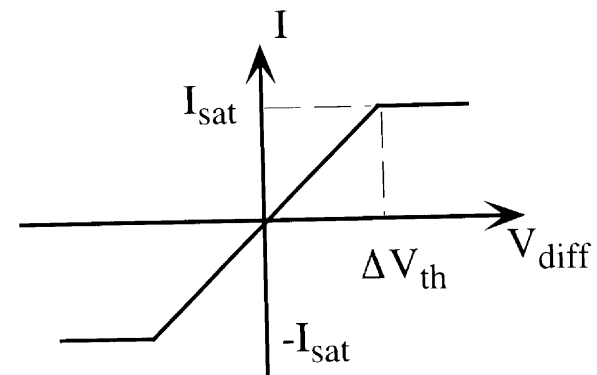
Figure 3.2.   Current characteristics of the class A opamp

design strategy for class A opamps. And finally in Section 3.7 we provide some conclusions.

3.2   OPAMP CLASSIFICATION

In order to provide a comprehensive comparison of power consumption, we first classify some commonly used opamp topologies in delta-sigma modulators and provide example circuits for them. Generally these opamps can be classified into either class A or class AB amplifiers. To avoid any possible confusion of terminology, we define a class A opamp as an opamp for which the available output current is limited and remains fixed even when a large differential input voltage is applied. This definition is graphically shown in Figure 3.2. In this figure $|I_{sat}|$ is the maximum output current flowing into and out of the load capacitor, and ΔV_{th} is the differential input voltage at which the output current saturates to its maximum value of $|I_{sat}|$. Examples of such amplifiers include the current gain (symmetrical) OTA [Milkovic, 1985] and the folded-cascode OTA [Ribner et al., 1985]. A fully differential current gain opamp is shown in Figure 3.3. For generality purposes the current mirror ratio is assumed to be $1 : B$. A fully differential folded-cascode opamp is shown in Figure 3.4. The current mirror ratios selected are optimal.

We define a Class AB opamp as an opamp for which the output current is not limited when a large differential voltage is applied. This definition is graphically shown in Figure 3.5. Traditionally class AB opamps [Castello and Gray, 1985a, Sansen et al., 1987, Wang and Harjani, 1996a, Degrauwe et al., 1982, Nagaraj, 1990, Kline et al., 1989, Hosticka, 1980, Hosticka, 1981] use a low and well-controlled quiescent current which is automatically increased when
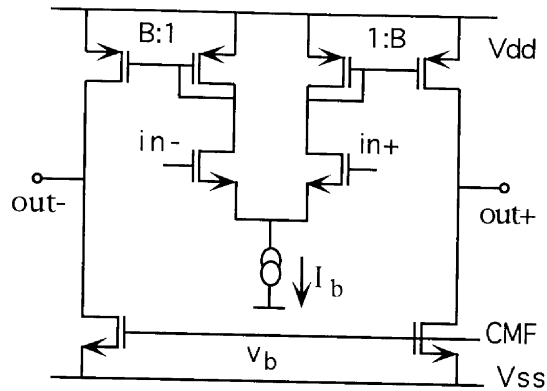
Figure 3.3.   Circuit schematic for the current gain opamp

Figure 3.5.   Current characteristics of the class AB opamp

Figure 3.4.   Circuit schematic for the folded-cascode opamp
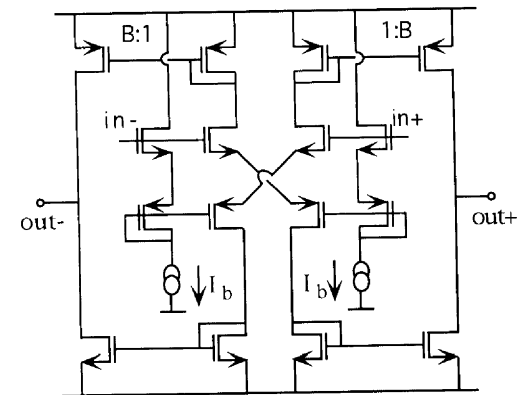
Figure 3.6.   Circuit schematic for the class AB opamp

a large differential input is applied. In Figure 3.6 we show the class AB opamp used by Castello[Castello and Gray, 1985a]. It is based on two pairs of source-coupled NMOS and PMOS transistors. The current mirror gain ratio between the input stage and the output stage is again assumed to be equal to $1 : B$. For both the fully differential opamps shown here the details of the common mode feedback circuitry are not included. Another opamp that is commonly referred to as a class A opamp is the Miller-compensated two-stage opamp. The circuit schematic for this opamp is shown in Figure 3.7. The characteristic output current vs. the differential input voltage is shown in Figure 3.8. As we can see, the output current has a limited value in one direction and an unlimited
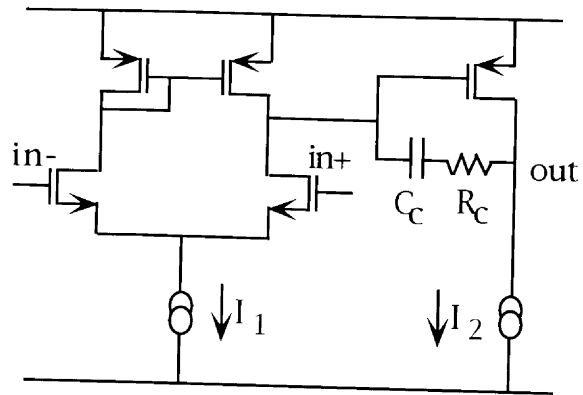
Figure 3.7.   Circuit schematic of the Miller-compensated two-stage opamp
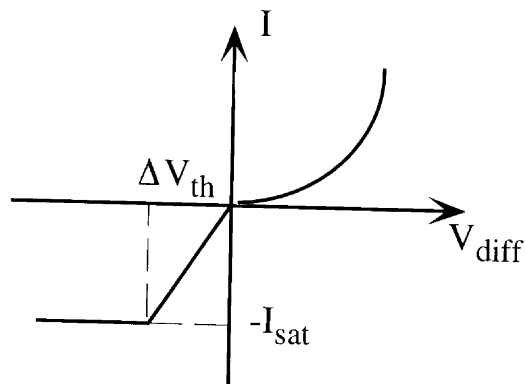
Figure 3.8.   Current characteristics for the Miller-compensated two-stage opamp

value in other direction. Because of the asymmetrical behavior of the output current, a Miller-compensated opamp does not directly fit into our definition of either a class A or a class AB opamp. However, since the limited output current direction determines the worst case slewing and settling behavior of the circuit we classify the Miller-compensated topology as a class A opamp.

3.3   A GENERAL SC-INTEGRATOR MODEL

The calculation of the power consumption for opamps used in delta-sigma modulator can not be made possible without a thorough appreciation of the switched-capacitor integrator in such modulators. A resolution requirement of

the overall converter imposes some limitation on the output voltage error of the integrator caused by finite slewing and finite settling of the opamp. To ensure that the slewing and settling is sufficient, a certain amount of power has to be dissipated. Therefore, the analysis of the power dissipation can be translated into the analysis of the dynamic behavior of the integrator.

In this section, the simple switched-capacitor integrator used in delta-sigma modulators is analyzed to establish differential equations governing the time-varying behavior. The integrator in Figure 3.9 is selected for the sake of simplicity. The results obtained can be extended to other more complex configurations without much effort. In a delta-sigma modulator feedback is generated by the sampling of the reference voltages[1]. For our example we shall assume a two phase non-overlapping clock scheme. During the first clock phase, Φ_1, both the input and one of the reference voltages, depending on the output of the comparator in the delta-sigma modulator, are sampled onto the input capacitor C_1 and the reference capacitor C_2 respectively (i.e., switch S_1 and S_3 or S_4 are closed). During Φ_2 the charge stored in these capacitors is then transferred to the integrating capacitor C_t (i.e., switch S_2 and S_5 are closed). For the Φ_1 clock phase the model is straightforward. For the Φ_2 clock phase the integrator can be modeled by two different equivalent circuits depending on the operational mode of the opamp. The two modes of operation are defined as large-signal mode and small-signal mode.

Large signal mode:.   When the voltage V_m at the negative input node of the opamp is larger than the threshold voltage ΔV_{th}, the opamp is said to be in large signal mode. Here, ΔV_{th} represents the linear region of function in the large signal mode. The time period for which V_m is larger than ΔV_{th} is termed as the large signal period. It is normally called the slewing period for class A opamps. During the large signal mode, one of the differential input transistors of the opamp is completely off. During this period the opamp is not operating as a negative feedback system. For this mode the output stage of the opamp can be represented by one current source ($I_2(t)$) and one current sink $I_1(t)$) whose values can be time-dependent. The simplified integrator schematic for this case is depicted in Figure 3.10. The activation of the switches S_2 and S_5 can be transformed into step inputs seen at the capacitor C_1 and C_2. In this model, V_1 is equal to the input voltage and V_2 is equal to either $+V_r$ or $-V_r$ depending on the output of the comparator, where $\pm V_r$ are the reference voltages. This model focuses on how node voltages and branch currents change with time without discussing the details of any particular opamp topology.

During the rising edge of V_1 and V_2 the amplifier cannot react instantaneously so the negative input of the opamp, V_m, also makes a step jump. The magnitude of the initial step is equal to
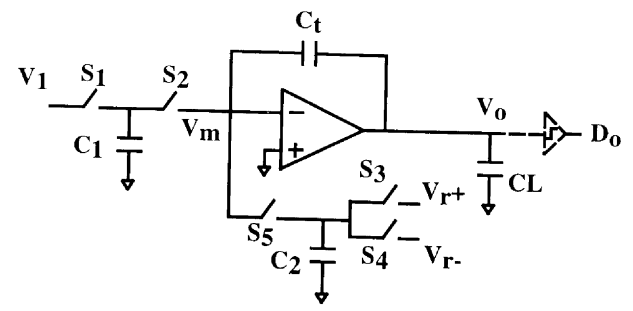
Figure 3.9.   SC integrator circuit in a delta-sigma converter
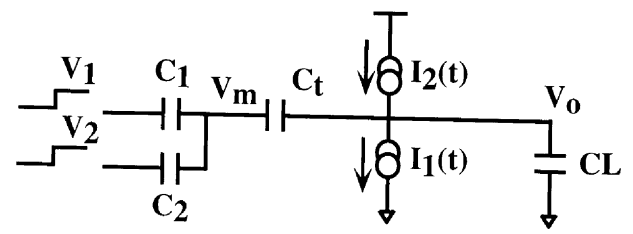
Figure 3.10.   Simplified large signal model for the SC integrator
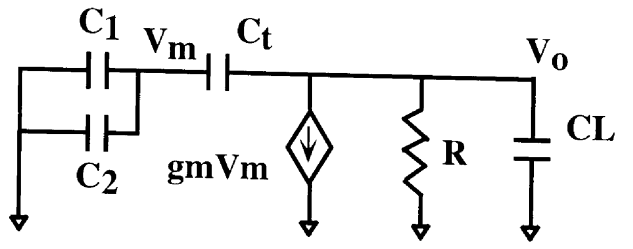
Figure 3.11.   Simplified small signal model for the SC integrator

$$V_{mi} = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2 + C_t C_L / C_t + C_L} \tag{3.1}$$

where V_2 is equal to $\pm V_r$ and is usually of the same magnitude as the supply voltage. For some combinations of V_1 and V_2, the opamp will experience a initial voltage jump that is larger than the threshold voltage. This will make the opamp operate first in the large signal mode and then in the small signal mode. From Kirchhoff's law of voltages and currents we can write the following set of equations

$$\begin{aligned}
I_1(t) - I_2(t) + C_L \frac{dV_o}{dt} &= C_t \frac{d(V_m - V_o)}{dt} \\
C_t \frac{d(V_m - V_o)}{dt} &= -(C_1 + C_2) \frac{dV_m}{dt}
\end{aligned} \tag{3.2}$$

The resulting differential solution for $V_m(t)$ is given by

$$\frac{dV_m}{dt} = -\frac{I_1(t) - I_2(t)}{C_{eff}} \tag{3.3}$$

where C_{eff} is $\left[((C_L + C_t)(C_t + C_1 + C_2) - C_t^2) \right] / C_t$. Equation 3.3 describes the voltage at the negative input of the opamp throughout the large signal period: from just after the initial voltage jump all the way to the beginning of settling. This equation provides the framework for the comparison of the various opamp topologies in the large signal period.

For a single ended class A opamp, for example in the case of the current gain opamp, either $I_1(t)$ or $I_2(t)$ is zero depending on the polarity of V_{mi}. For instance, let $I_2(t)$ be equal to zero. $I_1(t)$ now is equal to BI_b where B is the current mirror ratio and I_b is the tail current. For the fully differential version of the above mentioned class A opamp, neither $I_1(t)$ nor I_2 is zero. But their difference is equal to $BI_b/2$. This is the current that either charges or discharges one side of output. Due to its fully balanced nature, the rate of change of the differential output voltage is equivalent to that of a single ended opamp with an output current equal to BI_b. So the analysis for a single-ended opamp can be directly applied to its fully differential version without any change. In this case, V_m and V_o are now interpreted as the differential output and input voltage, respectively. This argument also applies to class AB opamps. The only difference being that for class AB opamps the current difference $I_1(t) - I_2(t)$ is a function of time.

Small signal mode: When the voltage V_m at the negative input node of the opamp is smaller than the threshold voltage ΔV_{th}, the opamp is said to function in the small signal mode. Accordingly, the time period in which the opamp operates in the small signal mode is defined as the small signal period. For this period the integrator can be modeled as shown in Figure 3.11. The current difference $I_1(t) - I_2(t)$ is now replaced by the differential input voltage

controlled current source Bg_mV_m, where g_m is the input transconductance, and is evaluated using the quiescent current for the input transistors. A finite output resistance R is added to model the effects of the finite gain of the opamp.

Using this model for the integrator, we can obtain the following new set of equations to describe the dynamic behavior of the voltages and currents,

$$
\begin{aligned}
Bg_mV_m + g_RV_o + C_L\frac{dV_o}{dt} &= C_t\frac{d(V_m-V_o)}{dt} \\
-C_t\frac{d(V_m-V_o)}{dt} &= (C_1+C_2)\frac{dV_m}{dt}
\end{aligned}
\tag{3.4}
$$

The resulting differential equations for $V_m(t)$ and $V_o(t)$ are given by

$$
\begin{aligned}
\frac{dV_m}{dt} &= -\frac{\hat{g}_mV_m}{C_{eff}} + \frac{\hat{g}_mV_{mf}}{C_{eff}} \\
\frac{dV_o}{dt} &= \frac{C_1+C_2+C_t}{C_t}\frac{dV_m}{dt}
\end{aligned}
\tag{3.5}
$$

The time-domain solutions for the above equations are

$$
\begin{aligned}
V_m(t) &= V_{mf} + \Delta V_{eff}e^{-\omega_{eff}t} \\
V_o(t) &= V_{of} + \tilde{C}\Delta V_{eff}e^{-\omega_{eff}t}
\end{aligned}
\tag{3.6}
$$

where C_{eff} is the effective capacitance defined before, $\hat{g}_m$ is the effective transconductance and V_{mf} is the final value of V_m as $t \to \infty$, respectively. Their expressions are given as follows.

$$
\begin{aligned}
\hat{g}_m &= Bg_m + \frac{C_1+C_2+C_t}{C_tR} \\
V_{mf} &= -\frac{C_1V_1+C_2V_2}{C_1+C_2+(1+A_o)C_t} \\
V_{of} &= -A_oV_{mf} \\
\omega_{eff} &= \frac{\hat{g}_m}{C_{eff}} \\
\tilde{C} &= \frac{C_1+C_2+C_t}{C_t} \\
\Delta V_{eff} &= \Delta V_{th} - V_{mf}
\end{aligned}
\tag{3.7}
$$

where $A_o = g_mR$ is the low frequency gain of the opamp. As A_o increases and approaches ∞, V_{mf} approaches zero and V_{of} approaches $-(C_1V_1 + C_2V_2)/C_t$ as expected. Note that during the small signal period the evolving errors at the integrator output node ($e_o(t)$) and the negative input node ($e_m(t)$) of the opamp can be related as follows

$$
\frac{e_o(t)}{e_m(t)} = \frac{V_o(t) - V_{of}}{V_m(t) - V_{mf}} = \tilde{C}
\tag{3.8}
$$

The above equation indicates that the two errors are linearly related by a constant factor. This result will be used in the next section. Also note that the resulting error due to the finite opamp gain is in the ballpark of $1/A_o$, and can

be made to be negligible when A_o is large. For clarity purposes the analysis in the rest of the paper will assume an infinite gain for the opamp. However, the effect due to finite gain can be added without too much effort.

So far we have established the time domain expressions for the negative input node voltage V_m, the integrator output voltage V_o and the relationship between their evolving errors for a general SC integrator. Using these equations, we can easily determine error voltages at these nodes at the end of the integrating phase (Φ_2). The error voltage carries the information of the supply current. Therefore, an estimate of the power consumption is made possible by analyzing the error voltage as discussed in the next section.

3.4   MODELS FOR POWER CONSUMPTION

In this section, we calculate the average power consumption for the opamp in a delta-sigma modulator. We focus on two typical input signals: DC inputs and sinusoidal inputs. The expression for the power consumption is developed for a DC input first and then extended for a sinusoidal input.

Let us define a new term: collective input set . It is the combination of the input signal and the reference voltage, and has only two different types: either the input signal plus the positive reference voltage $\{V_1, V_r\}$ or the input signal plus the negative reference voltage $\{V_1, -V_r\}$. The methodology we adopt here is to first compute the power consumption for the collective input sets, $P(V_1, V_r)$ and $P(V_1, -V_r)$, in one clock period. The overall power consumption is then computed according to the unique nature of the opamp. For example, the supply current is fixed in a class A opamp, so the overall power consumption must be equal to the larger value of the above two, i.e.,

$$
P_{overall} = max\{P(V_1, V_r), P(V_1, -V_r)\}
\tag{3.9}
$$

On the other hand, the supply current changes whenever the collective input set in a class AB opamp is altered. The overall power consumption is then the weighted-sum of $P(V_1, V_r)$ and $P(V_1, -V_r)$. The weight factor applied to each collective input set is nothing but the frequencies of occurrence of the collective set during normal conversion. Mathematically put,

$$
P_{overall} = f(V_1, V_r)P(V_1, V_r) + f(V_1, -V_r)P(V_1, -V_r)
\tag{3.10}
$$

where $f(V_1, V_r)$ and $f(V_1, -V_r)$ are the corresponding frequency of occurrence. In the rest of this section, we adopt this nomenclature for our calculations.

The average power consumed in one clock period

As mentioned in previous section, the clock period is assumed to have two distinct phases: an integrating phase and a sampling phase. The integrating

phase can be further partitioned into two periods: large signal period, T_{la}, and small signal period, T_{sm}. We now calculate the current dissipation during each period.

During the large signal period, the average output current, I_{out}, used to charge or discharge the output capacitor can be evaluated with the help of Equation 3.3 and is given by

$$\overline{I_{out}} = \frac{\int_0^{T_{la}} I_1(t)dt}{T_{la}} \tag{3.11}$$

$$= \frac{C_{eff}(V_{mi} - \Delta V_{th})}{T_{la}} \tag{3.12}$$

where V_{mi}, ΔV_{th} and T_{la} are the initial voltage jump at the negative input node of the opamp, the differential input threshold voltage and the length of the large signal period. The total average current dissipation during this period can be obtained from the average output current multiplied by a constant factor α which is opamp topology-dependent. The coefficient α accounts for the current dissipated by the rest of the circuit. The average total current I_{la} during the large signal period is then equal to $\alpha \overline{I_{out}}$. Note that the effective charge $C_{eff}(V_{mi} - \Delta V_{th})$ being transferred is independent of opamp topology. The different opamp topologies only impact the value of T_{la} and α. Normally, T_{la} for a class AB opamp is smaller than that for a class A opamp because of the availability of boosted current when a large differential input voltage is experienced.

For the small signal period the average current is evaluated in a somewhat different manner. With the help of Equation 3.5 and assuming an infinite gain, we have

$$\frac{dV_m}{dt} = -Bg_m\frac{V_m(t)}{C_{eff}} \tag{3.13}$$

Integrating the above equation gives

$$g_m = \frac{1}{BT_{sm}}C_{eff}ln\left(\frac{\Delta V_{th}}{v_m(T_{int})}\right)$$

$$= \frac{1}{BT_{sm}}C_{eff}ln\left(\frac{\hat{C}\Delta V_{th}}{e_o(T_{int})}\right) \tag{3.14}$$

where $V_m(T_{int})$ is the voltage at the negative opamp input node, and $e_o(T_{int})$ is the error voltage at the the output node of the opamp when the integrator finishes the integration. The relationship developed in Equation 3.8 was used to derive the expression in Equation 3.14. For weak inversion operation the transconductance of the differential pair is given by $g_m = I/nU_T$ [Degrauwe and Sansen, 1984], where I is the current flowing through either one of the

input transistors, n is the weak inversion slope factor and U_T is the thermal voltage. For weak inversion operation, Equation 3.14 can then be written as

$$\begin{aligned} I &= \frac{nU_T}{BT_{sm}}C_{eff}ln\left(\frac{\hat{C}\Delta V_{th}}{e_o(T_{int})}\right) \\ &= \frac{nU_T}{BT_{sm}}C_{eff}ln\left(\frac{2^N\hat{C}\Delta V_{th}}{V_{ref}}\right) \end{aligned} \tag{3.15}$$

where $e_o(T_{int}) = 2^{-N}V_{REF}$ is used for the error voltage at the end of the integrating period. N is related to the number of bits of resolution for the overall delta-sigma converter and V_{REF} is the magnitude of the reference voltage. For strong inversion operation the current becomes

$$I = \frac{\Delta V}{2BT_{sm}}C_{eff}ln\left(\frac{2^N\hat{C}\Delta V_{th}}{V_{ref}}\right) \tag{3.16}$$

where $g_m = 2I/\Delta V$ is used, ΔV is defined as $V_{gs} - V_T$ of the transistor and $\Delta V_{th} = \sqrt{2}\Delta V$. ΔV_{th} is the differential input threshold voltage. The total current dissipation $\overline{I}_{sm}$ during the small signal period is therefore the current in Equation 3.16 multiplied by another factor β. The coefficient β accounts for the current dissipated by the rest of the circuit. Either Equation 3.15 or Equation 3.16 can be used to calculate the power dissipated during the small signal period depending on the operating mode of the opamp.

The average current dissipated in one clock period is the weighted sum of the average current dissipation $\overline{I}_{sam}$ during the sampling phase, $\overline{I}_{la}$ during the large signal period, and $\overline{I}_{sm}$ during the small signal period, i.e.,

$$\overline{I} = \frac{\overline{I_{la}}T_{la} + \overline{I_{sm}}T_{sm} + \overline{I_{sam}}T_{sam}}{T} \tag{3.17}$$

We define an ideal opamp as an opamp with no current being dissipated in the sampling phase, i.e., $I_{sam} = 0$. Recall that the sampling phase is when the input is being sampled with switch S1 being closed in Figure 3.9. For a class A opamp, the total current supply is fixed and is the same for all time, therefore, $\overline{I}_{la} = \overline{I}_{sm} = \overline{I}_{sam}$. For a class AB opamp, the current dissipation in the large signal period is usually different from that in the small signal period, and the opamp consumes the same quiescent current in the small signal period as in the sampling phase, therefore, $\overline{I}_{la} \neq \overline{I}_{sm}, \overline{I}_{sm} = \overline{I}_{sam}$. Bearing this in mind, we can rewrite Equation 3.17 as

$$I = \begin{cases} (\alpha Q_1 + \beta Q_2)f_s & \text{ideal opamp} \\ (1+\gamma)(\alpha Q_1 + \beta Q_2)f_s & \text{class A opamp} \\ (\alpha Q_1 + (1+\gamma)\beta Q_2)f_s & \text{class AB opamp} \end{cases} \tag{3.18}$$

where Q_1 has the same expression for both weak inversion and strong inversion. It is equal to $C_{eff}(v_{mi} - \Delta V_{th})$. Q_2, on the other hand, has different expressions. It is equal to $2nU_T C_{eff}ln(2^N \Delta V/V_{REF})$ for weak inversion and $\Delta V C_{eff}ln(2^N \Delta V/V_{REF})$ for strong inversion. Here γ is defined as the ratio of the sampling phase and the integrating phase, $\gamma = T_{sam}/T_{int}$. The derivation for the above class AB opamp assumes zero large signal period which corresponds to infinite I_{la}. In principle, this is the most efficient way to consume power because now the entire integrating phase is devoted to the small signal period T_{sm}. The larger the settling period T_{sm}, the lower the current I_{sm} that is required to achieve the given resolution. Hereafter, whenever we refer to a class AB opamp, we are referring to this idealized condition. Please note that Q_1 is input voltage-dependent while Q_2 is input voltage-independent. In the following power analysis for different input signals, we will temporarily set aside the calculation for Q_2 as it is voltage independent and focus on Q_1. In the end, we will add the Q_2 term to our power estimation. The constant factors α and β in the power equation for different opamps are summarized in the Table 3.1. Note that any extra current consumed by the auxiliary circuitry such as the current subtractor in the adaptive opamp [Degrauwe et al., 1982] is assumed to be negligible.

Let us assume $C_1 = C_2$ for simplicity and x is the input signal after being normalized with respect to the reference voltage V_2. Therefore, the notation $P(V_1, \pm V_r)$ can be reduced to $P(x, \pm 1)$. The expression $Q_1 = C_{eff}(v_{mi} - \Delta V_{th})$ can be reduced to $C_1 V_1 + C_2 V_2$ if we neglect the load capacitance C_L and the constant factor $C_{eff}\Delta V_{th}$. By neglecting the Q_2 term, the minimum power consumption for the collective input set in one clock period can be calculated from Equation 3.18. It is summarized in Equation 3.19.

$$P(x, \pm 1) = \begin{cases} \alpha C_2 V_r V_{DD}|1 \mp x|f_s & \text{ideal opamp} \\ (1 + \gamma)\alpha C_2 V_r V_{DD}|1 \mp x|f_s & \text{class A opamp} \\ \alpha C_2 V_r V_{DD}|1 \mp x|f_s & \text{class AB opamp} \end{cases} \quad (3.19)$$

Please note that a class AB opamp has a similar expression as an ideal opamp when the Q_2 term is neglected. Equation 3.19 is the core expression for the power consumption calculations that follows.

Average power consumption for a DC input

Following our methodology outlined in the beginning of Section 4, the overall power consumption for a DC input can be easily obtained by using Equation 3.9 and Equation 3.10 and is shown here for the different opamp topologies.

Table 3.1.   Coefficients for various opamps

Opamp topology	α	β
Ideal	1	1
Current gain	$\frac{1+B}{B}$	$\frac{1+B}{B}$
Folded cascode	2	2
Castello	$\frac{1+B}{B}$	$\frac{1+B}{B}$
Adaptive	$\frac{1+B}{B}$	$\frac{1+B}{B}$

Class A opamp.   For a class A opamp, the power consumption for the two collective input sets is (see Equation 3.19)

$$P(x, \pm 1) = (1 + \gamma)\alpha C_2 V_r V_{DD}|1 \mp x|f_s \quad (3.20)$$

Since the supply current in a class A opamp is fixed, and opamp should be designed for the worst case to handle the largest charge transfer, the minimum power required takes the larger value of the above expression, i.e.,

$$P_A(x) = (1 + \gamma)\alpha C_2 V_r V_{DD}(1 + |x|)f_s \quad (3.21)$$

or $\hat{P}_A(x) = \alpha(1 + \gamma)(1 + |x|)$ in the unit of $C_1 V_r V_{DD} f_s$.

Ideal and Class AB opamp.   In this case, the average power consumption for the two collective input sets is (see Equation 3.19)

$$P(x, \pm 1) = \alpha C_2 V_r V_{DD}|1 \mp x|f_s \quad (3.22)$$

Both the ideal opamp and class AB can adaptively adjust their current to transfer charge. Therefore, the average power consumption can vary from $P(x, 1)$ to $P(x, -1)$ during different clock periods. According to Equation 3.10,

$$P_{AB} = f(x, 1)P(x, 1) + f(x, -1)P(x, -1) \quad (3.23)$$

where

$$\begin{aligned} f(x, 1) &= \frac{1+x}{2} \\ f(x, -1) &= \frac{1-x}{2} \end{aligned} \quad (3.24)$$

Plugging Equation 3.24 and Equation 3.22 into Equation 3.23, we have

$$P_{AB}(x) = \alpha C_1 V_r V_{DD} f_s(1 - x^2) \quad (3.25)$$

or $\hat{P}(x) = \alpha(1 - x^2)$. This equation indicates that the power consumption increases when the magnitude of the input decreases. This is somewhat counter intuitive. However, it can be understood as follows. If the magnitude of the input signal is close to the reference voltage $\pm V_r$, the digital output will be either "1" or "0" most of the time. Therefore, most of the time the net charge stored in the input capacitors (C_1 and C_2) is equal to $C_1 V_r (1 - |x|)$ in the sampling phase. Since x is close to one (one corresponds to the reference voltage), the current needed for this net charge transfer is small. On the other hand, if the input is close to zero, the digital output will have approximately equal number of "1"s or "0"s. The net charge being transferred from the input capacitors to the integrating capacitor becomes large resulting in a large amount of current.

Next, we consider the average power consumption for a sinusoidal input.

Average power consumption for a sinusoidal input

Using our earlier methodology, we extend the expression for the power consumption developed for a DC input to that for a sinusoidal input during signal conversion. Without loss of generality, we can assume a large oversampling ratio so that any sampled value of the sinusoidal signal can be treated as a quasi-static input. Assume that the input signal takes a sinusoidal form: $x = b + a\sin\omega t$, where b is the DC bias and a is the amplitude. Further $|b| \leq 1$, $0 \leq a \leq 1$ and $|b| + a \leq 1$ when normalized to V_r. The discussion is divided into two parts.

Class A opamp. Similar to the DC input case, class A opamps should be designed to handle the largest charge transfer. Therefore the normalized power consumption is obtained by replacing x in Equation 3.21 for the maximum amplitude of the sinusoidal signal $a + |b|$, i.e.,

$$\hat{P}_A = (1 + \gamma)\alpha(1 + a + |b|) \tag{3.26}$$

Ideal and Class AB opamps. For ideal and class AB opamps, the power consumption depends on the input signal magnitude. In this case, we obtain the average normalized power consumption by time-averaging the power consumption obtained in Equation 3.25 over one signal period. The normalized power consumption for both ideal and class AB opamps is then

$$\hat{P}_{AB} = \frac{1}{T} \int_0^T \left(1 - (b + a\sin\omega t)^2\right) dt \tag{3.27}$$

$$= \alpha\left(1 - a^2/2 - b^2\right)$$

So far we have obtained the expressions for the average power consumption for class A, ideal and class AB opamps used in a delta-sigma modulator for DC and sinusoidal inputs. It is our aim to find out what is the most optimal opamp topology in terms of power dissipation. In the next section, we compare the power dissipation for the various opamp topologies and select the best opamp choices for different applications.

3.5 COMPARISON OF POWER CONSUMPTION

For power comparison we now incorporate the Q_2 term into the formulas established in Section 3.4. We define an additional dimensionless quantity, $\eta = Q_2/C_1 V_r$. The comparison is made for DC inputs and sinusoidal inputs.

DC inputs

The normalized power consumption for a DC input is summarized in Table 3.2. A plot of the power consumption for the different opamp topologies is shown

Table 3.2.   Power consumption for DC inputs

Opamps	Normalized Power Consumption
Ideal	$\alpha(1 - x^2) + \beta\eta$
Class A	$(1 + \gamma)(\alpha(1 + x) + \beta\eta)$
Class AB	$\alpha(1 - x^2) + (1 + \gamma)\beta\eta$

in Figure 3.12. The inset PAB, PI and PA on the plot stands for the power consumption for a class AB, an ideal and a class A opamp. Care must be taken when interpreting these curves. For a class A opamp, the supply current is fixed after the design is completed. Therefore to accommodate a new input value, a new design and/or a new supply current is needed. The curve PA in Figure 3.12 simply maps out the relationship between the minimum power consumption and the maximum DC input. For example, a DC input of 0.6 requires a minimum power consumption of 5 units. An approach to minimize the supply current is illustrated in the next section. On the other hand, an ideal opamp and a class AB opamp can presumably adjust its tail current to handle the charge transfer during the large signal period. The supply current is designed only to meet the settling requirement during the small signal period. No new design is necessary when the DC input is changed. The curve PAB and PI depict the adaptability of the power consumption for different DC input signals.

By inspecting the plot, we conclude that a class A opamp consumes approximately the same power as a class AB opamp for a small magnitude DC input, but could consumes up to 6X the power of a class AB for a large magnitude signal. Our theoretical estimation agrees well with the results found in [Ritiniemi et al., 1994]. They estimated that a 4X power savings can be achieved by using a class AB opamp. A perfect class AB opamp consumes around 2X the power of an ideal one. The excess of power comes from the fact that a class AB opamp still consumes power during the sampling period while an ideal one does not. Real class AB opamps are likely to consume a little more power than shown here. Two factors have been neglected here. One, biasing overheads have been neglected and two, the large signal period is not exactly zero. However, the above analysis is indicative of the tradeoffs between the various classes while still being topology independent.
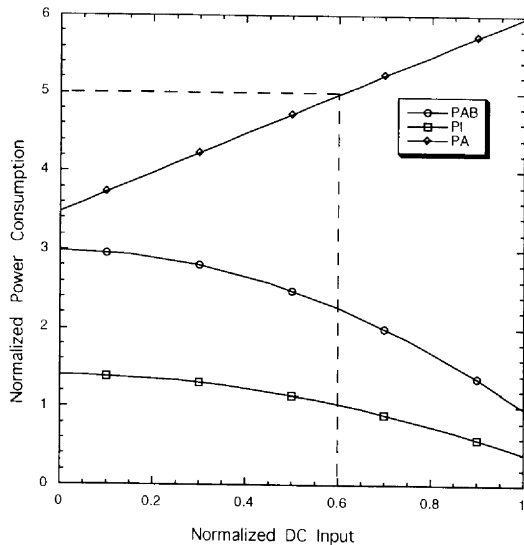
Figure 3.12.   Power comparison for DC inputs

Sinusoidal inputs

The normalized power consumption for a sinusoidal input is summarized in Table 3.3. The comparison between the opamp topologies is similar to DC inputs and is divided into two cases.

Table 3.3.   Power consumption for sinusoidal inputs

Opamps	Normalized Power Consumption
Ideal	$\alpha(1 - a^2/2 - b^2) + \beta\eta$
Class A	$(1 + \gamma)(\alpha(1 + a + |b|) + \beta\eta)$
Class AB	$\alpha(1 - a^2/2 - b^2) + (1 + \gamma)\beta\eta$

Zero DC bias.   The power consumption for sinusoidal inputs without a DC bias is shown in Figure 3.13. In this case, the power curves for class A, class
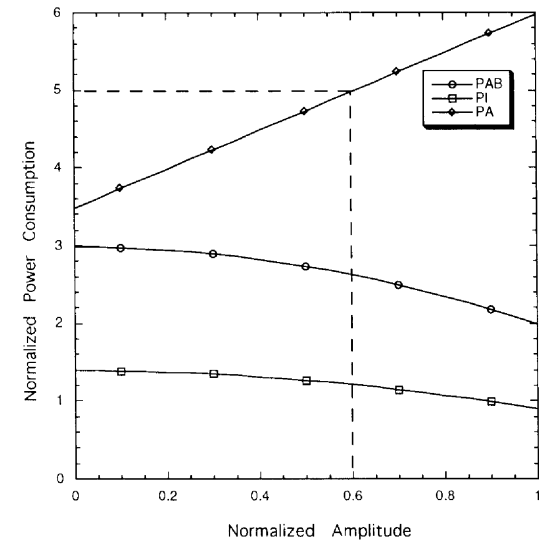
Figure 3.13.   Power comparison for sinusoidal inputs without DC bias

AB and ideal opamps are similar to those seen in Figure 3.12 except for some subtle differences. The curve PA remains the same. The difference between curve PAB in Figure 3.12 and Figure 3.13 lies in the large amplitude region where a class AB opamp consumes about two units of power in Figure 3.13 as opposed to one unit in Figure 3.12. This is because the larger of input signal, the lower the power consumed by a class AB opamp. Due to the oscillatory nature of a sinusoidal signal, its effective amplitude is reduced and therefore more power is consumed than would have been for a DC signal with the same amplitude.

DC offset. The power consumption for sinusoidal input with a DC bias offset is shown in Figure 3.14. We choose the DC bias voltage=0.5 (half the reference voltage) for illustration. The amplitude of the sinusoidal input is swept from zero to 0.5. Due to the existence of a non zero DC bias voltage, the power consumption for a class A opamp is large compared to an ideal or a class AB opamp even when the amplitude of the sinusoidal signal is close to zero. If the amplitude of the sinusoidal signal is around 0.1, then the minimum power that a class A opamp has to consume is 5 as illustrated in the figure. This is consistent with Figure 3.12 because the largest signal magnitude would be 0.6 (0.1 of signal amplitude plus 0.5 of DC bias). A class AB opamp consumes 2X the power of an ideal opamp just like in the case for DC inputs. The comparison
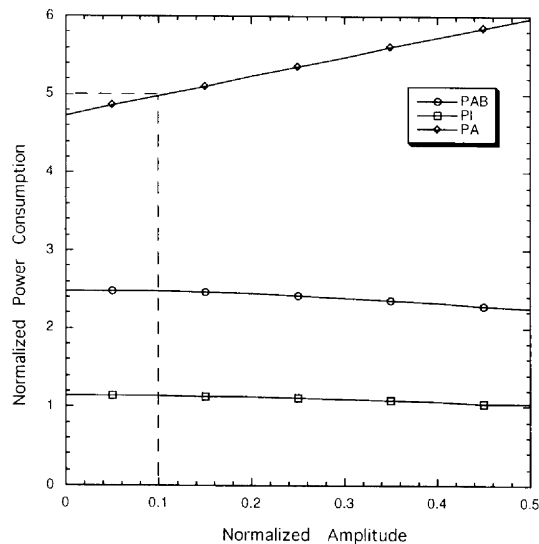
Figure 3.14.   Power comparison for sinusoidal input with DC bias

of the power consumption for the various opamp topologies in Section 5 can be summed up as follows.

- For DC inputs, class A opamps consume comparable power compared to class AB opamps for low level signals but consumes considerably larger amount of power (up to 6X) than class AB opamps for high level signals. The most efficient class AB opamp consumes about twice the power of an ideal opamp.

- For zero-offset sinusoidal inputs, the comparison is similar to DC inputs case. For DC-biased sinusoidal inputs, it is advantageous to use class AB

opamps even for a low level signal. However, the dynamic input range of the sinusoidal signal is limited due to the offset voltage.

If the power rather than the resolution is the primary objective in an oversampled A/D converter design such as might be found in biomedical applications, then the ideal choice is a class AB opamp. On the other hand, if high resolution and high linearity is the primary concern such as might be found in data acquisition, class A opamps are preferred over class AB opamps. This is because for class AB opamps the power consumption is input signal dependent. This can result in input signal dependent disturbance in the reference voltage which in turn causes nonlinearities [Ritiniemi et al., 1994].

3.6 DESIGN FOR OPTIMIZATION

The minimum power consumption for class A opamps was developed in the previous section. In this section, we attempt to answer the question as to how we design to approach this minimum. Since the supply current is the same for both the integration phase and the sampling phase, the problem can now be simplified as to how to partition the integration phase for slewing and settling so that the current is minimized.

The current minimization procedure is illustrated by a design example. The integrator in the delta-sigma modulator is designed using two different opamp topologies, a class A opamp and a class AB opamp. Both designs are generated for an 18-bit converter with a 250kHz clock rate. The reference voltage is selected to be 2.5V and input signal is 1V for a 5V power supply. The signal sampling capacitance is $5pF$, the feedback sampling capacitance is $5pF$ and the integrating and load capacitances are $10pF$ and $2pF$ respectively. For class A opamps, the slewing and settling periods are determined by the same fixed tail current. Therefore, $\overline{I_{la}}$ should be equal to $\overline{I_{sm}}$, i.e.,

$$\frac{\alpha Q_1}{T_{la}} = \frac{\beta Q_2}{T_{sm}} \qquad (T_{la} + T_{sm} = T/(\gamma + 1)) \qquad (3.28)$$

The problem simply boils down to minimizing the current $\overline{I_{sm}}$ ($\overline{I_{la}}$) given the constraint $T_{la} + T_{sm} = T/(\gamma + 1)$. It can be easily shown that the current dissipation is minimized when $T_{la} = Q_1 T/((\gamma + 1)(Q_1 + Q_2))$ and $I = \alpha(\gamma + 1)(Q_1 + Q_2)/T$. It is clear that the optimal slewing time T_{la} is solely determined by the ratio $Q_1/(Q_1 + Q_2)$. When the ratio Q_1/Q_2 increases, so does the slewing period. Following the analysis in the previous section, the ratio Q_1/Q_2 is in the range of $(v_{mi} - \Delta V_{th})/(2nU_T, \Delta V)ln(2^N \Delta V_{th}/V_{ref})$, where N is the number of bits of resolution. In Figure 3.15 four different U-shaped curves are plotted to show the optimal partition of the integration phase during each clock period. The U-shaped curve describes the total current needed vs. the fraction of time

used for slewing. For any given partition, the slewing current and the settling currents are calculated. The plotted current is the larger one of these two. As the slewing period increases, a smaller current is needed for the opamps to reach the final output value within the given slewing period. This is reflected by the curve segment left of the optimal point. One the other hand, as the slewing period increases, a smaller portion of the integration phase is left for settling. Therefore to achieve the given resolution in a shorter settling period, a larger current is needed. That is why the curve turns around and goes up when the partition ratio keeps increasing. The turning point corresponds to the optimal partition ratio. The optimal current can be calculated after we know the optimal partition ratio. As we can see, when the ΔV of the opamp is reduced towards weak inversion value, Q_1/Q_2 ratio increases. Therefore, the optimal partition point moves from Optimum Point 1 to Optimum Point 2. This leads to a conclusion that weak inversion operation gives the lowest power consumption as we expect. In fact the savings can be quite substantial, note the log scale on the Y-axis. For example for our design setting the ΔV of the differential pair to 0.3 volts rather than operating the opamp in weak inversion increases the power dissipation by 4X. Because Q_1/Q_2 in weak inversion is normally larger than one, the fraction of the clock period needed for slewing is larger than 0.5. For strong inversion operation, the fraction of the clock period used for slewing could be either larger than or smaller than one depending on the value of ΔV. The bold curve below shows the situation for a ideal class AB opamp. The duration of the large signal period of a class AB opamp is determined by the input voltage and not by the quiescent current. Therefore, there is no partitioning of time required. This curve assumes the optimal conditions, i.e., zero large signal period.

3.7   CONCLUSIONS

In this chapter we have addressed issues related to the optimal design of opamps for oversampled converters. We established a time-domain model for delta-sigma modulators that is independent of opamp topology. We focus on the dynamic behavior of the negative input of the opamp which ultimately determines the operation periods of the opamp. By introducing a new term *collective input set*, we propose a simple yet universal method to calculate the overall power consumption for the modulator. We discussed the best opamp topologies based on the power consumption for different applications. We put forward a design strategy to minimize the power consumption for class A opamps. The primary findings presented in this chapter can be summarized as follows.

■ A theoretical minimum power bound for an ideal opamp was developed.
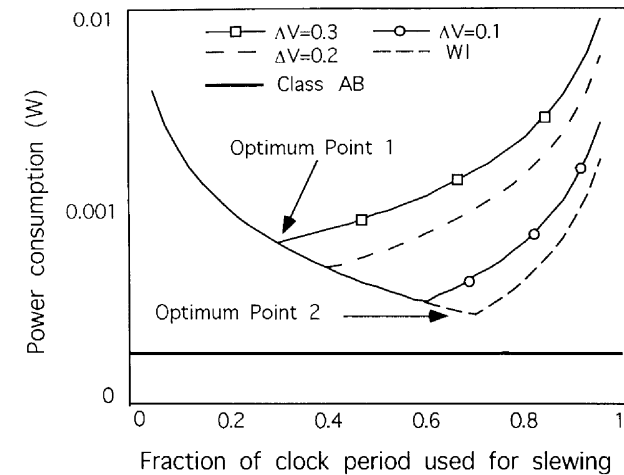
Figure 3.15.   Power optimization

■ Optimal class AB opamps consume about twice as much power as ideal opamps.

■ Class A opamps consume 1X to 6X the power for optimal class AB opamps. Savings for realistic class AB opamps are likely to be less.

■ Class A opamps are suitable for applications with high resolution/linearity requirements while class AB opamps are suitable for those with a restricted power budget.

■ Power minimization for class A opamps can be achieved by properly partitioning the integration phase for slewing and settling.

■ Operation in weak inversion leads to the lowest power consumption.

■ For weak inversion operation more than 50% of the integration phase should be devoted to slewing. For strong inversion operation a smaller fraction of the integration phase can be devoted to slewing.

These findings can be used as a guide to select the appropriate opamp topology and to achieve the minimum power consumption for class A opamps. The design technique shown here will be used in the design of a first order delta-sigma modulator as demonstrated in chapter 6.

Notes

1. The two reference voltages are usually generated from a single supply. The negative and positive value of V_r are generated by altering the clock phase. However, for simplicity here we shall assume two perfectly matched voltages

4   NONLINEAR SETTLING IN DELTA-SIGMA MODULATORS

4.1   INTRODUCTION

High linearity in data converters is an important feature for various applications such as instrumentation and data acquisition. However, a good handle on nonlinear effects is impaired by the lack of analytical models. This situation is worsened by the fact that nonlinearities from different origins contribute to the overall nonlinearity of the converter and it is difficult, if not impossible, to identify them individually during chip testing. Many authors circumvent this problem by either treating the nonlinear effect as a small perturbation to the ideal modulator or even as an additive white noise source. These methods do not establish a clear relationship between circuit parameters and overall nonlinearity. Therefore, they can not provide a quantitative guide for oversampled converters design.

In this chapter and the next chapter, we tackle the nonlinear problem from both the theoretical and the practical design point of view. In this chapter, we primarily focus on the nonlinear settling behavior of the modulators and we will discuss other nonlinear phenomena including voltage-dependent capacitor, nonlinear reference voltage and nonlinear DC gain in the next chapter. This
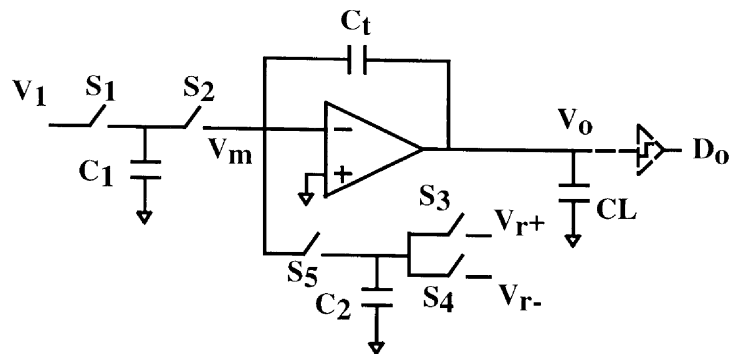
Figure 4.1.   Schematic of $\Delta\Sigma$ modulator

chapter is organized as follows. In Section 4.2 we establish a generic analytical framework to describe the nonlinear behavior in delta-sigma modulators. In Section 4.3, we apply the framework to the nonlinear settling error. We derive a dedicated analytical model to predict the characteristics of the nonlinear error: error shape, error height and height location. An experiment circuit was fabricated to corroborate the analytical model and the computer simulation. Finally we conclude this chapter in Section 4.4.

4.2 FRAMEWORK DEVELOPMENT

In this section, we develop a generic framework to describe quantitatively the nonlinear behavior in a delta-sigma modulator. In this framework we focus on how the nonlinear behavior in the modulator affects the overall linearity of the converter without discussing the concrete origin of each nonlinear effect. The generalization of our model is realized by using some phenomenologic parameters which can be determined once we know the nature of the underlying nonlinear source.

A simplified circuit diagram for a first order $\Delta\Sigma$ modulator is shown in Figure 4.1. A non-overlapping two phase clocking scheme is assumed. Let us denote Q^+ as the total charge transferred from the input capacitor C_1 and the reference capacitor C_2, to the integrating capacitor C_t during the integration period when the digital output from the comparator is "1". Likewise, let Q^- be the total charge transferred when the digital output is "0". Let P denote the probability that the digital output is equal to "1". In another words,

$$P = \frac{N^+}{N} = \frac{N^+}{N^+ + N^-} \tag{4.1}$$

where N^+ is the number of "1"s output, N^- is the number of "0"s output, and N is the number of clock periods for each conversion. The total charge transferred from the input and the reference capacitors to the integrating capacitor within the N clock periods can be written as

$$Q(N) = N^+ Q^+ + N^- Q^- \tag{4.2}$$

or in an alternative form

$$\frac{Q(N)}{N} = PQ^+ + (1 - P)Q^- \tag{4.3}$$

and therefore

$$P = \frac{Q^-}{Q^- - Q^+} + \frac{Q(N)}{N} \frac{1}{Q^- - Q^+} \tag{4.4}$$

The second term on the right hand side of the above equation is nothing but the quantization error and can be made to be arbitrarily small by increasing N. We shall therefore ignore it as we are primarily interested only in the nonlinear error. The above equation can therefore be reduced to

$$P = \frac{Q^-}{Q^- - Q^+} \tag{4.5}$$

Phenomenologically, we can always express Q^- and Q^+ in the following fashion

$$\begin{aligned} Q^+ &= (C_1 x - C_2 V_r)K^+ \\ Q^- &= (C_1 x + C_2 V_r)K^- \end{aligned} \tag{4.6}$$

where x is equal to V_1. The parameters, K^+ and K^-, measure any deviation from the ideal charge transfer. This deviation could be a result of nonlinear settling, capacitor nonlinearity or power supply disturbance, etc. For a perfect modulator, $K^+ = K^- = 1$. The mean or DC value of the digital output, $D(x)$, is equal to $2P - 1$. With the help of Equations 4.5 and 4.6, we can write

$$D(x) = \frac{C_1 x(K^+ + K^-) + C_2 V_r(K^- - K^+)}{C_2 V_r(K^+ + K^-) - C_1 x(K^+ - K^-)} \tag{4.7}$$

The mean value reduces to $\hat{D}(x) = C_1 x / C_2 V_r$ when the charge transfer is ideal as expected. The error $E(x)$ due to the nonlinearity is equal to $\hat{D}(x) - D(x)$, i.e.,

$$E(x) = \frac{(K^+ - K^-)(1 - \hat{x}^2)}{(K^- + K^+) - \hat{x}(K^+ - K^-)} \tag{4.8}$$

where $\hat{x} = C_1 x / C_2 V_r$ is the normalized input value. It is clear that it is the difference between the two coefficients (K^+ and K^-) that causes the nonlinear error. The specific expressions for K^+ and K^- will depend on the specific mechanism that causes the nonlinearity. The above equation serves as the framework for further investigation.

4.3 NONLINEAR SETTLING ERROR

Background

The nonlinear settling error in general switched capacitor circuits and $\Delta\Sigma$ modulators have been studied by several authors. In [Sansen et al., 1987], a thorough transient analysis including finite bandwidth and finite slew rate in switched capacitor filters was carried out by assuming linear feedback. However, their results cannot be directly applied here due to the highly nonlinear feedback inherent in the $\Delta\Sigma$ modulators. In [Hauser and Broderson, 1986, Yin et al., 1993], computer simulations and Z-domain analysis have been carried out to investigate the effect of finite bandwidth on the modulator performance assuming linear settling. However, because of the large feedback reference voltage used in $\Delta\Sigma$ modulators the opamps are forced to slew during the initial charge transfer transient. This slewing results in nonlinear settling. In [Williams and Wooley, 1994], the slew rate limitation was incorporated in their opamp settling response and the effect on SNR ratio was studied via computer simulations. In [Bishop et al., 1990], table-based simulations were used to study nonlinear settling. However, none of the above approaches provide analytical models for opamp induced nonlinearity. In [Medeiro and Perez-Verdu, 1994], the influence of opamp dynamics (slew rate and gain-bandwidth) and nonlinear DC gain on the behavior of a modulator has been analyzed and modeled. Unfortunately, their models were obtained by using power expansion and nonlinear curve fitting. The model provides little or no insight on how performance degradation can be related to circuit and system parameters. Traditionally, in order to avoid slew-limited distortion, large supply currents have been used resulting in increased power consumption.

In this section we apply the framework established in the previous section to the nonlinear settling problem in $\Delta\Sigma$ modulators. We develop an analytical model to relate the nonlinearity characteristics with circuit parameters. We also validate our model with measured data from fabricated ICs.

Parameter determination

The expressions for K^+ and K^- can be obtained by analyzing the dynamics of the integrator shown in Figure 4.1. The dynamics of the settling behavior of the integrator depends on the relative magnitude of the initial voltage jump at the negative input of the opamp, V_{mi} [Wang and Harjani, 1996b], and the threshold voltage of the differential input transistors, ΔV_{th}. If V_{mi} is larger than ΔV_{th}, the opamp has to go through a slewing period followed by a settling period. If V_{mi} is smaller than ΔV_{th}, the opamp will only experience pure settling. The change in the integrator output voltage, ΔV_o, at the end of the integrating

period, T, can be expressed as shown in Equation 4.9.

$$\Delta V_o(T) = \begin{cases} \frac{Q}{C_t} - \tilde{C}\frac{|Q|}{C_{eff}}sgn(Q)e^{-\omega T} \\ \frac{Q}{C_t} - \tilde{C}\Delta V_{th}sgn(Q)e^{-\omega(T-T_{slew})} \end{cases} \tag{4.9}$$

where $Q = C_1 x + C_2 V_2$; and x and V_2 are the input and feedback reference voltages, respectively. V_2 is equal to $\pm V_r$ depending on the digital output. $\tilde{C}$ is equal to $(C_1 + C_2 + C_t)/C_t$; ω is equal to $\hat{g}_m/C_{eff}$, where $\hat{g}_m$ is the effective input transconductance. T is the total time period for integration (slewing plus settling). T_{slew} is the slewing period and is equal to $(|Q| - C_{eff}\Delta V_{th})/I_s$, where I_s is the available output current during the slewing period and $sgn()$ is the signum function. Derivations for Equation 4.9 can be found in detail in Chapter 3. The first expression in Equation 4.9 corresponds to pure settling while the second one corresponds to slewing followed by settling. The above expression can be rewritten by factoring out the Q/C_t term.

$$\Delta V_o(T) = \begin{cases} \frac{Q}{C_t}(1 - \frac{\tilde{C}C_t}{C_{eff}}e^{-\omega T}) \\ \frac{Q}{C_t}(1 - \frac{\tilde{C}\Delta V_{th}C_t}{|Q|}e^{-\omega(T-T_{slew})}) \end{cases} \tag{4.10}$$

By comparing the above expression with Equation 4.6, we can obtain the general expression for K shown below.

$$K(x, V_2) = \begin{cases} 1 - \frac{\tilde{C}C_t}{C_{eff}}e^{-\omega T} \\ 1 - \frac{\tilde{C}\Delta V_{th}C_t}{|Q|}e^{-\omega(T-T_{slew})} \end{cases} \tag{4.11}$$

To be consistent with previous notations, we present the following equalities.

$$\begin{aligned} K^+(x) &= K(x, -V_r) \\ K^-(x) &= K(x, +V_r) \end{aligned} \tag{4.12}$$

The evaluation of $K(x)$ can be divided into two cases:

Pure linear settling. The first term on the right-hand side of Equation 4.11 corresponds to the pure settling situation. The initial voltage jump $|Q|/C_{eff}$ at the negative input node is always guaranteed to be smaller than the differential threshold voltage ΔV. The incomplete factor K is a constant independent of both the input signal and the reference voltage. Consequently, $K^+(x)$ is equal to $K^-(x)$. This implies, according to Equation 4.8, that there is no nonlinearity error if the settling process is completely linear. This has been pointed out by many authors backed by the simulation results. We provide a rigorous theoretical foundation for this assessment. In practical designs, the linear settling can not be approximated without very large power consumption or performance degradation. The opamp will usually experience both slewing and settling and is addressed next.

Slewing plus settling. The second term of Equation 4.11 corresponds to the slewing followed by settling situation. Several analytical characteristics are discussed here. It is very important to notice that $K(x, V_2)$ is only a function of the magnitude of the stored charge Q and is independent of the sign of this charge. This observation leads to the following characteristics.

$$
\begin{aligned}
K^+(-x) &= K^-(x) \\
K^-(-x) &= K^+(x) \\
K^+(0) &= K^-(0)
\end{aligned}
\tag{4.13}
$$

Plugging the above equation into Equation 4.8, we can obtain the analytical characteristics of the nonlinearity error $E(x)$.

$$
\begin{aligned}
E(-x) &= -E(x) \\
E(0) &= 0 \\
E(\pm 1) &= 0
\end{aligned}
\tag{4.14}
$$

The asymptotical behavior of the function $E(x)$ can be described as an odd symmetrical function with zeroes occurring at zero input, and the lower and upper limits of the input.

Analytical model

Pure settling only results in a gain error term which can easily be calibrated out. However, in general, for all practical situations the opamp in the modulator will experience both slewing and settling. We devote our analytical model to this situation. Since the error curve has odd symmetry, without loss of generality, we only develop the model for $x > 0$. Around the error peak it can be shown that $K^+(x)$ can be approximated by one. The resulting error from this assumption is negligible. The expression for $K^-(x)$ can be written as

$$
K^-(x) = 1 - \frac{\tilde{C}\Delta V_{th} C_t}{C_1 x + C_2 V_r} e^{-\omega(T - T_{slew})}
\tag{4.15}
$$

$$
= 1 - \frac{\alpha}{1 + \hat{x}} e^{\Omega(\hat{x})}
\tag{4.16}
$$

where

$$
\alpha = \tilde{C}\Delta V_{th} C_t / C_2 V_r
\tag{4.17}
$$

$$
\Omega(\hat{x}) = -\omega\left(T - \left|\frac{Q_{in} - Q_{th}}{I_s}\right|\right)
\tag{4.18}
$$

and $Q_{in} = C_2 V_r (1 + \hat{x})$, $Q_{th} = C_{eff}\Delta V_{th}$. Plugging the above expression into Equation 4.8, we can get

$$
E(\hat{x}) \approx \frac{\alpha(1 - \hat{x}) e^{\Omega(\hat{x})}}{2}
\tag{4.19}
$$

The peak error and location can be found by setting the first derivative of $E(x)$ to zero. The peak location turns out to be

$$
\hat{x}_o = 1 - \frac{C_{eff}}{C_2} \frac{1}{V_r} \frac{I_s}{g_m}
\tag{4.20}
$$

where $\omega = gm/C_{eff}$ has been used to derive the above expression. The expression can be further written as

$$
\hat{x}_o = \begin{cases} 1 - \frac{C_{eff}}{C_2} \frac{\Delta V_{gs}}{V_r} & \text{strong inversion} \\ 1 - \frac{C_{eff}}{C_2} \frac{2nU_T}{V_r} & \text{weak inversion} \end{cases}
$$

where ΔV_{gs} is equal to $V_{gs} - V_T$ of the input transistor. The error peak can be found to be

$$
E(\hat{x}_o) = \gamma e^{-\frac{T}{\tau}} e^{\left(\frac{2C_2/C_{eff}V_r - (\Delta V + \Delta V_{th})}{\Delta V}\right)}
\tag{4.21}
$$

where

$$
\gamma = \left(\frac{\Delta V \Delta V_{th}}{V_r^2}\right) \frac{(C_{eff} + C_t)C_{eff}}{C_2^2}
\tag{4.22}
$$

$$
\tau = \frac{1}{\omega}
\tag{4.23}
$$

τ stands for the time constant of the opamp. The equation is for strong inversion operation. Replacing ΔV_{gs} by $2nU_T$ will result in the expression for weak inversion operation. Equation 4.21 shows that the height of the nonlinearity error is exponentially proportional to $-T/\tau$, where T/τ is the total number of the time constants in the integration period. As will be shown later, this is a testable result which can be used to compare our model with experimental data. Additionally, it can be shown that the nonlinearity error in higher order $\Delta\Sigma$ modulators is dominated by the nonlinearity error in the first stage. Therefore, the analytical results developed here can be used to predict the opamp induced nonlinearity error for higher order converters as well.

By examining the expression of the error peak, we know that there exists a reference voltage V_r which yields a minimum error peak. Equating the derivative of $E(\hat{x}_o)$ with respect to V_r to zero will give us such minimum value, i.e.,

$$
V_{ro} = \frac{\Delta V C_{eff}}{C_2}
\tag{4.24}
$$

Figure 4.2 depicts the error peak dependence of the reference voltage for different input/reference capacitor ratios. The effective capacitance C_{eff} is kept as a constant (18pf) for both of the curves. Because the coefficient of V_r inside the
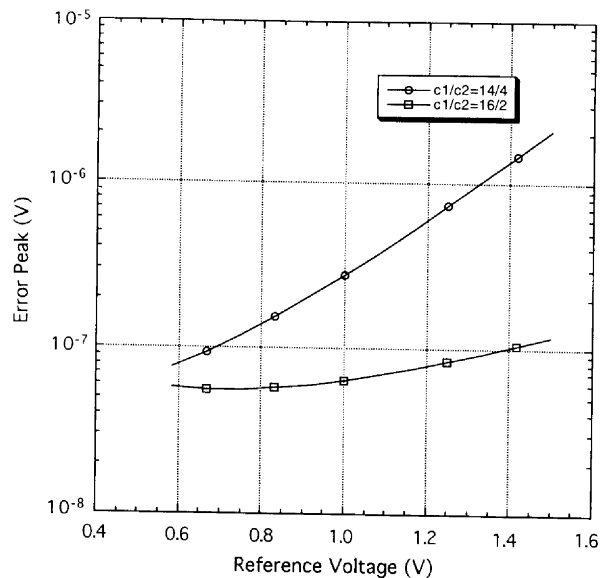
Figure 4.2.   Dependence of error peak on V_r

Figure 4.3.   Simulation vs. model

exponential is proportional to C_2, the error peak is a very sensitive function of the reference capacitance. For a fixed effective loading capacitance (C_{eff}) of an opamp, a larger value of C_1 tends to reduce the error peak. The additional benefits of using a smaller C_2 is that there is less variation of the error peak as opposed to larger variation for a larger C_2 when the reference voltage is changed.

Experimental results

Our model has been validated via difference equation simulations and via measured results from fabricated ICs. First, we present simulation results. In Figure 4.3 we plot the nonlinearity error (output-input) vs. the input for a 2nd order modulator. The gray curve shows the results from difference equation simulations using MATLAB and the dark curve with circles shows the results from our analytical model. As can be seen in the figure our analytical model and simulations results agree extremely well.

To further validate our results, a second order $\Delta\Sigma$ modulator was fabricated in a standard 0.8μm CMOS N-well process. The integrators in both the stages were autozeroed [Hurst and Levinson, 1989]. The settling behavior of the opamp is described by the number of settling time constants, T_{settle}/τ. In our design, the nominal value of this number for the first opamp is around 14 which falls into the fast regime described in [Williams and Wooley, 1994]. Since the length of the settling period T_{settle} is designed to be equal to half of the total integration period T, the total number of time constants T/τ is then equal to be 28. The input transistors are designed to operate in weak inversion. Therefore, the number of time constants is linearly proportional to the supply current. The modulator operates with a 5V supply voltage. A linear ramp from -80% to +80% of the input range is generated using a Wavetek 4808. The digital output is acquired via a National Instruments DIO-32F card.

According to Equation 4.21, if the supply current is reduced, so is the number of time constants. Therefore, the nonlinearity error is expected to increase exponentially. In our experiment, the supply current is set to six different settings of 0.25, 0.32, 0.40, 0.5, 0.65 and 1, where 1 corresponds to the nominal value. For each current setting, the nonlinearity error is measured. Figure 4.4 shows three sets of measured results. We use three curves to visualize how the nonlinearity error progresses when the supply current is reduced. These curves preserve the main features: odd symmetry around the mid-point of the input signal, occurrence of error peaks and near zero error at midpoint and both ends. As the input devices continue to operate in weak inversion, the location of the error peak is independent of the supply current and is located around 0.5 which agrees with theoretical predictions.
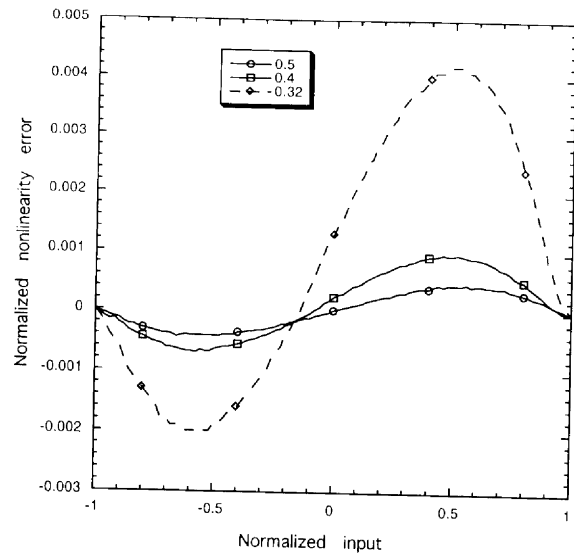
Figure 4.4. Measured nonlinearity error
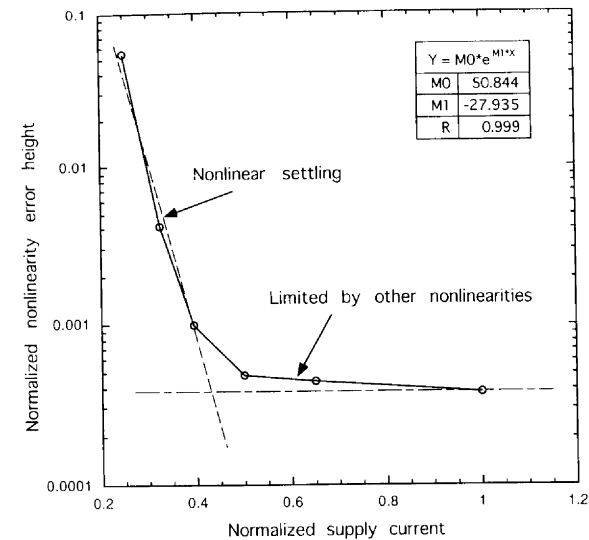
Figure 4.5. Current dependency of error height

As mentioned earlier, the height of the nonlinearity error is exponentially proportional to $-T/\tau$, the number of the total time constant. Therefore, for input devices in weak inversion, we expect to see a straight line in a semilog plot of error height vs. current. Figure 4.5 plots the maximum value of nonlinearity error vs. the supply current with the Y-axis being in log scale. As we can see the curve has two distinct regions. When the supply current is low ($\leq$ 0.5), the nonlinearity error increases exponentially with the reduced current. The inclined dashed line is the exponentially fitted curve. Since the X-axis represents the normalized supply current, the slope of the fitted line yields the number of the total time constant for the nominal supply current. The fitted slope is 27.935 which agrees very well with the design target of 28. In this region measurement fits the theory accurately. Please note that this extracted slope is independent of the total number of time constants for the second opamp. This observation justifies our assumption that the nonlinearity error is dominated by the nonlinear settling error from the first opamp. When the supply current increases, the nonlinearity error deviates from its exponential curve and starts to level off as shown by the horizontal dashed line. In another words, the nonlinearity error is limited by other nonlinear factors. One of the possible causes is capacitor nonlinearity due to the voltage dependence of the capacitor. A quick estimate can be carried out here. First-order voltage dependence is

canceled due to the fully differential structure. Only the second order term is considered here. When normalized, the capacitor nonlinearity error in the fully differential ADC must be of the form αV_r^2, where α is the second order coefficient and in the range of 1-10 ppm [Hester et al., 1990]. It has a ballpark value of 10^{-5} to 10^{-4} and is supply current-independent. This value agrees reasonably well with Figure 4.5. Figure 4.5 suggests that the nonlinearity error is usually limited by factors other than nonlinear settling for larger currents. The conventional wisdom in which we use a large supply current to limit the nonlinear settling distortion is not effective and this extra power is wasted. We can see from the figure that for our nominal design a 40 percent power reduction does not increase nonlinearity error.

4.4 CONCLUSIONS

In this chapter, we have established a mathematical framework to analyze the nonlinear behavior in $\Delta\Sigma$ modulators. The model utilizes only the device parameters, which allows designers to optimize the circuit performance. This model was confirmed using Matlab simulation. A second order $\Delta\Sigma$ modulator was fabricated to verify the theory prediction. The measurement data agree with the theory very well. Measurement results suggest that for higher currents nonlinearity is dominated by voltage-dependent capacitor nonlinearity. Using

our model a 40% reduction in power consumption did not result in increased nonlinearity.

In the next chapter, the established framework will be applied to other non-linear phenomena in the delta-sigma modulators. The individual nonlinear contribution to the overall nonlinearities will be examined.

5   OTHER NONLINEAR PHENOMENA IN DELTA-SIGMA MODULATORS

5.1   INTRODUCTION

The nonlinear settling behavior in delta-sigma modulators are discussed in Chapter 4. Based on the excellent agreement between the model and the measurement results for the nonlinear settling, we further apply our framework to other nonlinear phenomena in delta-sigma modulators. They include nonlinear capacitor error in Section 5.2 and nonlinear reference error in Section 5.3. In Section 5.4, we analyze the nonlinear DC gain-induced error. In Section 5.5 we use our experimentally-verified model to outline a design strategy to minimize power consumption. We leave some conclusions in Section 5.6.

5.2   NONLINEAR CAPACITOR ERROR

Monolithic capacitors play an important role in modern analog-to-digital converters. Examples can be found in oversampled A/D converters, algorithmic A/D converters and charge redistribution A/D converters. Besides capacitor value errors due to fabrication process variations, two other errors exist in a capacitor originating from its intrinsic physical nature. One is the dielectric
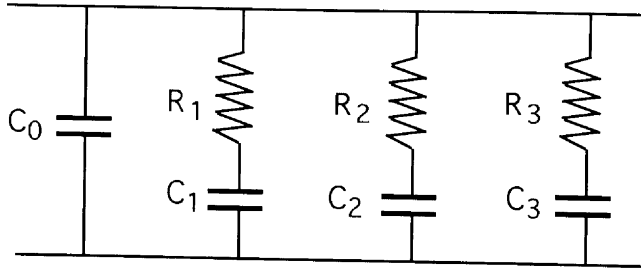
Figure 5.1.   Empirical model for dielectrical relaxation effect

relaxation in capacitors and the other is the voltage-dependence of the capacitance. In this section, we examine the impact of these two errors on the overall nonlinearity of the oversampled converters. We review the physical origin of the error upon which a simple model is established for each case. Each model is then utilized in the nonlinearity framework developed in Chapter 4 to calculate the corresponding nonlinearity error. Section 5.2 to Section 5.1 are devoted to the dielectric relaxation and Section 5.2 to Section 5.4 are devoted to voltage-dependent capacitance. A summary is provided in Section 5.1

Origin of the dielectric relaxation

The phenomenon of dielectric relaxation has been studied and explained by many researchers. The performance degradation of charge-distribution A/D converters due to this phenomenon has been studied in 1975 by [McCreary and Gray, 1975] and in 1990 by [Fattaruso et al., 1990]. It is our aim to investigate the impact of the dielectric relaxation on oversampled converters.

The basic principle of the dielectric relaxation phenomenon can be explained as follows. When a capacitor is charged to a input voltage, the dielectric material is polarized and the internal dipoles are formed. Because of the nature of the dipoles, they can not respond to the change of external electrical fields instantaneously. When the applied voltage is removed and two plates are shorted, some dipoles will not dissipate immediately. The undissipated dipoles will create image charges on the inside surface of the plate. When the two plates are disconnected, the image charge remains on the plate creating a recovery voltage. A simple empirical circuit suggested by [Dow, 1958] is shown in Figure 5.1. After a charging period, all the capacitor C_o to C_3 are charged to the input voltage. A quick shorting of the capacitor C_o will discharge C_o immediately and completely. However, capacitors C_1 to C_3 can not be discharged completely due to the finite RC time constants. During a float period, the residue

charge left on those capacitors will redistribute into C_o resulting in a recovering voltage. Since the model describes a linear system, the recovery voltage can be expressed as

$$V_r(t) = V_{in} \sum_{i=1}^{3} f_i(t, \tau_i) \qquad (5.1)$$

Where V_{in} is the initial applied voltage, and $\tau_i = R_i C_i$ is the time constant of the ith resistor. Equation 5.1 means that the recovery waveform is linear with respect to the applied voltage and symmetrical with respect to the voltage polarity. This should also hold for all capacitors regardless of gate materials. Extensive device measurements by [Fattaruso et al., 1990] have confirmed this empirical model.

Impact on the modulator

Let us first examine how dielectrical relaxation affects the performance of the switched-capacitor integrator shown in Figure 5.2. A two-phase non-overlapping clock scheme is assumed. During phase Φ_2 capacitor C_1 is charged to the input voltage V_1. During the succeeding non-overlapping period t_{non}, nothing happens to this capacitor. During phase Φ_1 capacitor C_1 is discharged and image charges are formed on the inside surface of both the plates. The succeeding non-overlapping period serves as a float period and a recovery voltage αV_1 is built. Therefore, a residue charge $\alpha C_1 V_1$ is created and stored on the input capacitor, where α is a constant determined by the dielectrical material and the length of the float period. During phase Φ_2 on the next cycle, the net charge transferred to the capacitor C_2 is $(1 - \alpha)C_1 V_1$ instead of $C_1 V_1$ for an ideal capacitor. This is equivalent to an ideal integrator with a different input capacitor size $(1 - \alpha)C_1$. When the integrator is used in the delta-sigma modulator, the dielectrical relaxation will only create a gain error which can be easily calibrated out. Additionally since the actual size of the integrating capacitor C_2 is not important, the impact on C_2 due to the dielectrical relaxation will not make any difference on the overall linearity performance. The same argument holds true for a noninverting SC integrator. Therefore, we conclude that the dielectrical relaxation of the capacitor does not contribute to the overall nonlinearities of the delta-sigma converters.

Origin of voltage-dependence of capacitors

The capacitor nonlinearity originates from voltage-dependent capacitance . The capacitor-voltage (CV) relationship has been studied extensively and some of derivations are cumbersome. For pedagogical purposes, we illustrate this CV behavior by using a simplified model illustrated in [Gregorian and Temes, 1986].
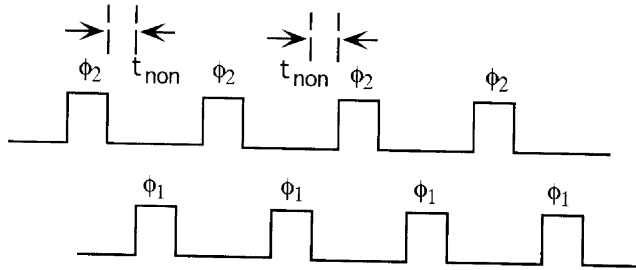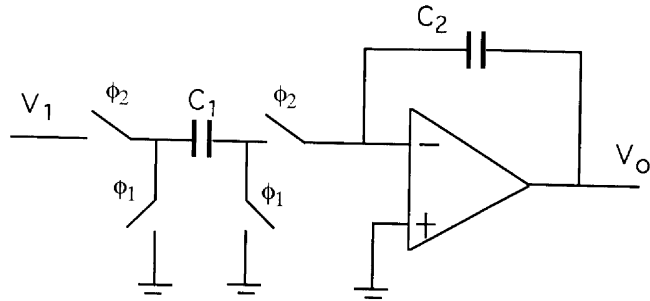
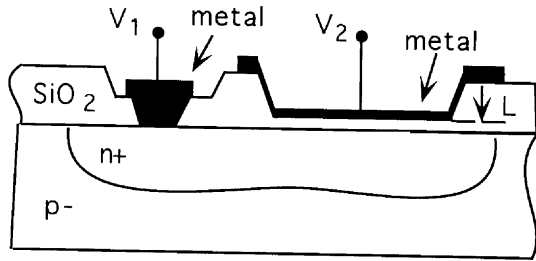**Figure 5.2.**   An inverting SC integrator

Figure 5.3.   MOS capacitor with positively-biased voltage

Depending on the material that forms the plate, there are mainly three types of MOS capacitor: Metal-or Poly -over-Diffusion structure, Poly-over-Poly structure and Metal-over-Poly structure. We use Metal-over-Diffusion type as an example. As shown in Figure 5.3, the heavily doped n^+ region serves as the bottom plate of the capacitor. The top plate is formed by growing a layer of metal on SiO_2. Thin film SiO_2 also serves as as insulator. When the voltage of the top plate V_2 is larger than the voltage of the bottom plate V_1, the bottom
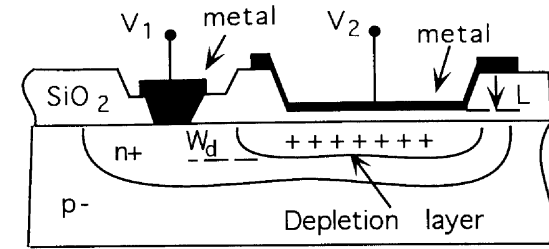
Figure 5.4.   MOS capacitor with negatively-biased voltage

plate should be negatively-charged and the negative charge is supplied by the abundant n^+ layer. On the other hand, if V_2 is smaller than V_1, the bottom plate should be positively-charged. This is possible only if a depletion layer in n^+-region is created (Figure 5.4). The effective capacitance seen between two plates is now regarded as the series connection of two capacitors: one is the intrinsic capacitance C_i contributed by the gate oxide, the other is the induced depletion layer capacitance C_d. Since the depletion length is dependent on the applied voltage, so too is the total effective capacitance. It can be shown that

$$C_{eff} = \frac{C_i + C_d}{C_i C_d}$$

$$= C_i \left(1 + \frac{2K_{ox}^2 \epsilon_o (V_1 - V_2)}{q N_D K_s l^2} \right)^{-0.5}$$

(5.2)

where N_D is the uniform n^+-doping density, and K_s and K_{ox} are the relative permittivity of Si and SiO_2, respectively. As shown in the above equation, C_{eff} decreases with increasing $V_1 - V_2$. This is true until strong inversion occurs on the silicon surface. In the vicinity of C_i, the voltage coefficient of capacitor C_{eff} is defined as

$$\alpha_1 = \frac{1}{C_{eff}} \frac{dC_{eff}}{dV}$$

(5.3)

Plugging Equation 5.2 into Equation5.3, we have

$$\alpha_1 = -\frac{2K_{ox}^2 \epsilon_o}{q N_D K_s l^2}$$

(5.4)

A typical value for α_1 is around 10-100 ppm. For metal-over-polysilicon and poly-over-poly capacitor, the voltage coefficient values are in the same range as for metal-over-diffusion. The second order voltage coefficient can also be derived by taking the second derivative of Equation 5.2.

Nonlinear capacitor induced error

In this sub-section, we discuss the overall nonlinearity of the modulator contributed by the nonlinear capacitor. In general, the voltage dependence of a capacitor can be written as

$$C = C_o(1 + \alpha_1 V + \alpha_2 V^2) \tag{5.5}$$

where α_1 and α_2 are the first order and second order coefficients. Typical values for them are 10-100 ppm and 1-10 ppm, respectively. V is the voltage across the capacitor. When the conventional fully differential circuits are employed, the first order voltage dependence (linear dependence) will be reduced by the common mode rejection ratio, which is around 40dB or a 100 times reduction in magnitude. This allows us to ignore the linear dependence of capacitance on the applied voltage. The total charge stored in the input and the reference capacitors can now be written as

$$
\begin{aligned}
Q^+ &= C_1 x + C_1\alpha_2 x^3 - (C_2 V_r + C_2\alpha_2 V_r^3) \\
Q^- &= C_1 x + C_1\alpha_2 x^3 + (C_2 V_r + C_2\alpha_2 V_r^3)
\end{aligned} \tag{5.6}
$$

Therefore, the corresponding K factors are

$$K^+ = 1 + \eta \frac{\hat{x}^3 - \gamma}{\hat{x} - 1} \tag{5.7}$$

$$K^- = 1 + \eta \frac{\hat{x}^3 + \gamma}{\hat{x} + 1} \tag{5.8}$$

where

$$\eta = \alpha_2 \left(\frac{C_2 V_r}{C_1} \right)^2 \tag{5.9}$$

$$\gamma = \left(\frac{C_1}{C_2} \right)^2 \tag{5.10}$$

Please note that the above K factors preserve asymmetry $K^+(-\hat{x}) = K^-(\hat{x})$. This indicates that the error function $E(\hat{x})$ should also exhibit the asymmetry. Plugging these two expressions into Equation 4.8 yields

$$E(\hat{x}) = \eta \hat{x} (\gamma - \hat{x}^2) \tag{5.11}$$

Equation 5.11 indicates that in general the nonlinearity in the delta-sigma modulators from nonlinear capacitors is quadratically proportional to the reference voltage. Therefore, we should use a lower reference voltage whenever

Table 5.1.   Ratio of the nonlinearitiy for two different reference voltages

Chip #	T_1	T_2	T_3	F_1	F_2	F_3	S_1	S_2	S_3	S_4
Ratio	5.26	5.01	5.6	3.83	3.06	4.28	4.11	5.51	2.84	4.63

possible to minimize nonlinear capacitor effects. Table 5.1 summarizes the ratio of measured nonlinearity peaks for two different reference voltages $V_r = 2.5$ and $V_r = 1.25$. The measurements are done for ten different chips with the same design but different reference voltages. According to Equation 5.11, when the reference voltage is doubled, the nonlinearity error should increase 4X. The mean of the ratios from the measured data is 4.414 with only 10 % deviation from the ideal value of 4. This confirms our theory very well.

Summary

In this section we devoted our discussion to the overall nonlinearity due to the nonlinear capacitor. Two main error sources were investigated. We find that one of the error sources, dielectric relaxation, does not contribute to the overall nonlinearity rather it only introduces a gain factor which can be calibrated out. On the other hand, voltage-dependent capacitors are responsible for the overall nonlinearity and it has a square law dependence on the reference voltage. If the primary concern is the high linearity, then a lower reference voltage is recommended.

5.3   NONLINEAR REFERENCE VOLTAGE ERROR

Nonlinear behavior in delta-sigma modulators can be also due to imperfect reference voltages. This problem has been mentioned by authors in [Eynde and Sansen, 1993] and [Ritiniemi et al., 1994]. In [Eynde and Sansen, 1993], the unsettled reference voltage has been modeled by a nonideal charge transfer, i.e.,

$$Q = \begin{cases} (1 - \epsilon^+)C_1(V_r - V_{in}) & \text{if } D = 1 \\ (1 - \epsilon^-)C_1(-V_r - V_{in}) & \text{if } D = -1 \end{cases} \tag{5.12}$$

where D stands for the digital output of the comparator. ϵ^+ and ϵ^- are the percentage of the charge transfer error during the integrator period for the corresponding digital output. It can be easily shown that the above expression is a special case of our framework, where $K^+ = 1 - \epsilon^+$ and $K^- = 1 - \epsilon^-$. However, this model does not correctly describe the charge transfer error due to an unsettled reference voltage. The reason is that this model implicitly assumes that the input voltage has the same percentage finite settling error as

the reference voltage. This usually is not true. Additionally the above model does not provide any insights as to how the unsettled reference voltages are practically induced.

In fact many mechanisms can cause the reference voltage not to settle to its final value. Among them, the finite inductance and the finite capacitance associated with the reference line and the use of class AB opamps are some of the most primary mechanisms. In this section, we apply our framework established in Chapter 4 to these two scenarios and examine their roles on the overall nonlinearity of the delta-sigma modulator.

Sampling-induced reference error

Because the reference voltage is associated with the finite inductance and capacitance, the sampling on such reference voltage normally introduces ringing. As a matter of fact, such ringing can often account for the deadband seen in higher order delta-sigma modulators. In order to make the problem tractable, we make the following assumptions:

- The reference voltage is only disturbed during the sampling period.

- The ringing of the reference voltage repeats itself in every sampling period.

- The reference voltage is restored to its stable value at the end of every integration period.

The second assumption guarantees that the positive reference voltage has the same ringing shape when it is sampled, as does the negative reference voltage. The third assumption guarantees that the ringing curve has the same initial value for all sampling periods. Together these two assumptions imply that the settling error at the end of the sampling period is a constant and dependent on neither any previous error nor the input signal. Generally, the settling error for the positive and the negative voltage could differ from each other. According to our framework, the nonlinearity $E(x)$ can be obtained once we find the value of K factor (K^+ and K^-). This is straightforward after we develop the expression of the charge transfer as follows

$$
\begin{aligned}
Q^+ &= C_1 x - C_2 V_r (1 - \epsilon^+) \\
&= (C_1 x - C_2 V_r)(1 + \frac{\epsilon^+}{\hat{x}-1})
\end{aligned}
\tag{5.13}
$$

and

$$
\begin{aligned}
Q^- &= C_1 x + C_2 V_r (1 - \epsilon^-) \\
&= (C_1 x + C_2 V_r)(1 - \frac{\epsilon^-}{\hat{x}+1})
\end{aligned}
\tag{5.14}
$$

By definition, we have the expression for K factor as follows

$$
\begin{aligned}
K^+ &= 1 + \frac{\epsilon^+}{\hat{x}-1} \\
K^- &= 1 - \frac{\epsilon^-}{\hat{x}+1}
\end{aligned}
\tag{5.15}
$$

Consequently the nonlinearity due to sampling-induced unsettled reference voltage can be obtained through Equation 4.8

$$
E(x) \approx \frac{(\epsilon^- - \epsilon^+) - (\epsilon^- + \epsilon^+)\hat{x}}{2}
\tag{5.16}
$$

Equation 5.16 indicates that the nonlinearity error is a linear function of input signal plus a constant factor. This linear error can be treated as a gain error which can be easily calibrated out. This is different from the nonlinearity caused by the nonlinear settling and the nonlinear capacitor. The main reason is that the unsettled reference error (ϵ^+ or ϵ^-) is a constant and it contributes directly to the incomplete transfer of charge. The transfer incompleteness is therefore independent of the input signal unlike the case in the nonlinear settling and the nonlinear capacitor where the incomplete charge transfer is dependent on the input signal. Therefore, a sampling induced reference voltage error does not contribute to the overall nonlinearity of the delta-sigma modulator.

Class AB opamp-induced reference error

The use of class AB opamps could also introduce additional nonlinearity errors. As we have already shown in Figure 2.16 and Figure 2.17 that a spike in supply current is inevitable when the opamp experiences a step input signal. What is worse is that the height of such a spike is strongly dependent on the magnitude of the input signal. Because of the finite inductance and the finite capacitance of the power line, a supply current spike will result in a supply voltage ringing. If we assume that the reference voltage is generated from the same power supply, the ringing on the power supply is also reflected on the reference voltage. Unlike the sampling-induced unsettled reference voltage, class AB opamp-induced error is dependent on the input signal. In order to the model this effect, we make the following assumptions

- The power supply ringing can be modeled by a linear differential equation.

- The reference voltage linearly follows the power supply ringing.

- The reference voltage is restored to its stable value at the end of the integration period.

Together these assumptions imply that at the end of the sampling period, the deviation of reference voltage from its stable value is linearly proportional

to the height of the current spike. These assumptions also implies that the reference voltage ringing is memoryless. Practically these assumptions are never completely true. Nevertheless, as we will see soon nonlinearities do occur even under these idealized conditions. Please note that the voltage spike height is only a function of the absolute value of charge stored $|Q|$ inside the input and reference capacitors. Mathematically the dynamic behavior of the reference voltage in the sampling period can be written as

$$V_r(t) = V_r + \alpha f_1(|Q|) f_2(t) \tag{5.17}$$

According to assumption 1, since the differential equation that describes the ringing is linear, the spike height $f_1(|Q|)$ can be separated from the time function $f_2(t)$ and factored out as a coefficient. At the end of the sampling period, $f_2(t)$ takes a definite value and can be absorbed into the constant α. We further assume that function $f_1(|Q|)$ takes the following form

$$
\begin{aligned}
f_1(|Q|) &= f_1(|C_1 x \pm C_2 V_r|) \\
&= \alpha_1 |C_1 x \pm C_2 V_r| + \alpha_2 |C_1 x \pm C_2 V_r|^2
\end{aligned}
\tag{5.18}
$$

The justification of this approximation is based on the fact that ideally the height of the current spike is quadratically dependent on the differential input signal for a class AB opamp (see Equation 2.36). Adopting the previous notation ϵ, we can write

$$
\begin{aligned}
\epsilon^+ &= \alpha_1 C_2 V_r (1 - \hat{x}) + \alpha_2 (C_2 V_r)^2 (1 - \hat{x})^2 \\
\epsilon^- &= \alpha_1 C_2 V_r (1 + \hat{x}) + \alpha_2 (C_2 V_r)^2 (1 + \hat{x})^2
\end{aligned}
\tag{5.19}
$$

Plugging the above expression into Equation 5.16, we have

$$E(x) = \alpha_2 (C_2 V_r)^2 \hat{x} (1 - \hat{x}^2) \tag{5.20}$$

Equation 5.20 exhibits the same asymptotical characteristics as nonlinear settling, i.e., the nonlinear error is an odd symmetrical function with zeroes occurring at zero input, and the lower and upper limits of the input. Equation 5.20 also indicates that the nonlinear error is quadratically proportional to the reference voltage. Therefore, whenever it is possible, a lower reference voltage is favored when a class AB opamp is used in the modulator.

Summary

To summarize this section, we have examined the impact of the nonideal reference voltage on the overall nonlinearity of delta-sigma modulators. Two different origins of such nonidealities were identified and are incorporated into

our framework. We found that if the imperfection of the reference voltage is caused by sampling and independent of the input signal, it does not contribute to the overall nonlinearities. On the other hand, if the imperfection has a strong dependence on the input signal like from the use of a class AB opamp, its contribution to the overall nonlinearities is inevitable. Further, if we can assume that the error is linearly and quadratically proportional to the input signal (Equation 5.19), the resulting nonlinearity shape resembles that resulting from the nonlinear settling.

5.4 NONLINEAR DC GAIN ERROR

Another important source of nonlinearity error comes from the nonlinear DC gain. The origin of this nonlinearity is reviewed first and the equivalence of two commonly used expression is established. Because the effect of the DC gain nonlinearity on the overall performance of delta-sigma converters is analytically intractable, we analyze the harmonic distortion in a SC integrator due to such nonlinearities.

Origin of the DC nonlinearity

Many factors contribute to the DC nonlinearity of the opamp. Essentially, the DC characteristics such as DC gain and DC transfer function are derived from the small signal model of the opamp. This small signal model is mathematically a linearized approximation of the real circuit. A second order fourier expansion of the current-voltage relation of the differential input pair will reveal the nonlinear nature of the DC gain. In order to elaborate this point, let us look at the operation of a different input pair of a typical opamp shown in Figure 5.5.

If we neglect the channel length modulation and apply the square law of the current-voltage relationship, we have the following equations

$$
\begin{aligned}
I^+ &= \tfrac{1}{2}\beta(V_{in+} - V_s - V_T)^2 \\
I^- &= \tfrac{1}{2}\beta(V_{in-} - V_s - V_T)^2 \\
I &= I^+ + I^-
\end{aligned}
\tag{5.21}
$$

where V_T is the threshold voltage of the transistor, and β is equal to kW/L. The difference $I^+ - I^-$ can be easily found as

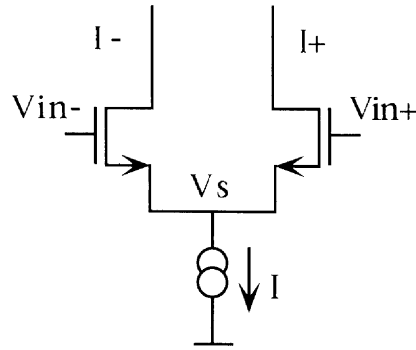$$I^+ - I^- = V\sqrt{I\beta}\sqrt{1 - \beta V^2/(8I)} \tag{5.22}$$

Figure 5.5.   Differential input pair of a typical opamp

where V is equal to $V_{in+} - V_{in-}$. By definition, the DC gain is equal to the output voltage change divided by the input voltage change, i.e.,

$$
\begin{aligned}
A &= (I^+ - I^-)R/V \\
&= \sqrt{I\beta}R\sqrt{1 - \beta V^2/(8I)} \\
&= A_o\sqrt{1 - \beta V^2/(8I)}
\end{aligned}
\tag{5.23}
$$

where R is the output resistance and is assumed a constant, and A_o is the linear DC gain. As we can see immediately, the real DC gain is a function of the input differential voltage, which results in nonlinearity. If the input voltage is small, Equation 5.23 can be further simplified to

$$
\begin{aligned}
A &= A_o\sqrt{1 - \beta V^2/(4I)} \\
&\approx A_o(1 - \beta V^2/(8I))
\end{aligned}
\tag{5.24}
$$

The DC gain of the opamp is an even function of input differential voltage when other effects are neglected. Clearly, a large current improve the linearity.

Equivalent expression for DC gain nonlinearity

Opamp DC gain nonlinearity is usually expressed in two different ways in literature. In [Medeiro and Perez-Verdu, 1994], this nonlinearity is expressed by the output voltage dependence of the DC gain, i.e.,

$$
A = A_o(1 + \gamma_1 V_o + \gamma_2 V_o^2)
\tag{5.25}
$$

where A_o is the DC gain when the output voltage V_o is zero; γ_1 and γ_2 are first order and second order coefficients, respectively. In [Lee and Meyer, 1985],

the nonlinearity is expressed by the higher order dependence of the output voltage on the input voltage, i.e., a nonlinear transfer function between the input voltage and the output voltage.

$$
V_o = \alpha_1 V_i + \alpha_2 V_i^2 + \alpha_3 V_i^3
\tag{5.26}
$$

It is well known that it is advantageous to utilize a fully differential opamp so that even order harmonic can be suppressed by the common mode rejection ratio (CMRR). Therefore, we ignore the second order and only consider the third order term $\alpha_3 V_i^3$. The Equation 5.26 is now reduced to

$$
V_o = \alpha_1 V_i + \alpha_3 V_i^3
\tag{5.27}
$$

Using numerical iteration technique, we can obtain an approximate solution for Equation 5.27 as shown in Equation 5.28.

$$
\begin{aligned}
V_i &= (V_o - \alpha_3 V_i^3)/\alpha_1 \\
&\approx (V_o - \alpha_3/\alpha_1^3 V_o^3)/\alpha_1 \\
&= V_o(1 - \alpha_3/\alpha_1^3 V_o^2)/\alpha_1
\end{aligned}
\tag{5.28}
$$

By definition, the DC gain can be written as V_o/V_i, i.e.,

$$
\begin{aligned}
A &= \alpha_1/(1 - \alpha_3/\alpha_1^3) \\
&\approx A_o(1 + \alpha_3/\alpha_1^3 V_o^2)
\end{aligned}
\tag{5.29}
$$

where $A_o = \alpha_1$ is used. We can see that it is the nonlinearity in the DC transfer function that causes the dependence of DC gain on the output voltage of the opamp, and Equation 5.29 is equivalent to Equation 5.27, i.e.,

$$
V_o = \alpha_1 V_i + \alpha_3 V_i^3 \iff A = A_o(1 + \gamma_2 V_o^2)
\tag{5.30}
$$

The corresponding coefficients are related by

$$
\begin{aligned}
A_o &= \alpha_1 \\
\gamma_2 &= \alpha_3/\alpha_1^3
\end{aligned}
\tag{5.31}
$$

Harmonic distortion induced by nonlinear DC gain

The harmonic distortion of the integrator caused by the nonlinear DC gain can be analyzed via charge conservation in a switched-capacitor system. A non-inverting integrator is shown in Figure 5.6. At the end of nth integration, $t = t_n$, the voltage at the negative input of the opamp has a nonzero voltage, $-V_o(t_n)/A(t_n)$, i.e., the virtual ground of the negative input node is no longer valid because of the finite DC gain. The charge transferred out of the input
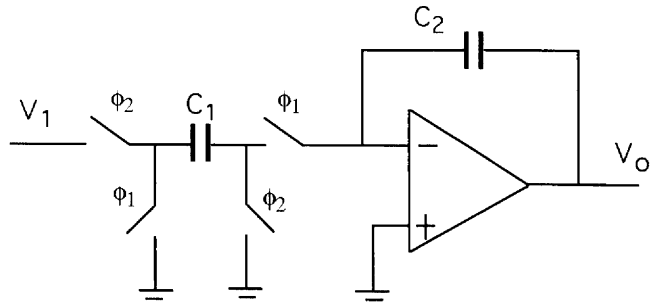
Figure 5.6.   A two phase non-inverting SC integrator

capacitor C_1 is the difference between $Q_i(t_{n-1})$ and $Q_i(t_n)$, the stored charge on capacitor C_1 at time $t = t_{n-1}$ and $t = t_n$, respectively. In another words,

$$
\begin{aligned}
\Delta Q_i(t_n) &= Q_i(t_{n-1}) - Q_i(t_n) \\
&= C_1 V_i - C_1 V_o(t_n)/A(t_n)
\end{aligned}
\tag{5.32}
$$

On the other hand, the charge stored on the capacitor C_t at $t = t_n$ and $t = t_{n-1}$ can be written as

$$
\begin{aligned}
Q_o(t_n) &= C_t(V_o(t_n) + V_o(t_n)/A(t_n)) \\
Q_o(t_{n-1}) &= C_t(V_o(t_{n-1}) + V_o(t_{n-1})/A(t_{n-1}))
\end{aligned}
\tag{5.33}
$$

Charge conservation requires that

$$
\Delta Q_i(t_n) = Q_o(t_n) - Q_o(t_{n-1})
\tag{5.34}
$$

i.e.,

$$
\begin{aligned}
C_1 V_i(t_{n-1}) - C_1 V_o(t_n)/A(t_n) = \\
C_t[V_o(t_n)(1 + 1/A(t_n) - V_o(t_{n-1})(1 + 1/A(t_{n-1}))]
\end{aligned}
\tag{5.35}
$$

The above equation indicates that the dependence of the DC gain on the output voltage will result in harmonic distortion (HD) . One technique to evaluate the harmonic distortion coefficients is described in [Lee and Meyer, 1985]. The basic idea is to assume a perfect input and output sinusoidal signal with fundamental frequency ω. Substituting them into the above equation will result in a sinusoidal component with higher order harmonics. The corresponding harmonic coefficients can therefore be obtained. The drawback of this technique involves some tedious trigonometrical manipulation. We here present an improved and systematic approach to obtain HD coefficients.

The approach we use here is first to transform Equation 5.35 into its continuous time counterpart. The difference equation is transformed into a differential equation [Gregorian and Temes, 1986], i.e.,

$$
V(t_n) - V(t_{n-1}) \Longleftrightarrow T\frac{dV(t)}{dt}
\tag{5.36}
$$

where $T = t_n - t_{n-1}$ is the clock period. Equation 5.35 becomes

$$
C_t T \frac{d}{dt}(V_o(t) + V_o(t)/A(t)) = C_1(V_i(t) - V_o(t)/A(t))
\tag{5.37}
$$

where $A(t) = A_o(1 + \gamma V_o^2(t))$. Since γ is small, $V_o(t)/A(t)$ can be approximated by $V_o(t)(1 - \gamma V_o^2(t))/A_o$. Equation 5.37 is further transformed into

$$
C_t T \frac{d}{dt}[V_o(t)(1 + 1/A_o) - \gamma V_o^3(t)/A_o] = C_1[V_i(t) - V_o(t)(1 - \gamma V_o^2(t)/A_o]
\tag{5.38}
$$

This equation describe the dynamic nonlinear behavior of the integrator with DC gain nonlinearity. When a input takes the signal following form

$$
V_i(t) = V_{in} cos(\omega t)
\tag{5.39}
$$

then the output signal can be written as

$$
V_o(t) = \sum_k V_k cos(k\omega t + \phi_k)
\tag{5.40}
$$

By definition, the kth order harmonic distortion HD_k is equal to V_k/V_1. The value of V_k can be found with the help of the Volterra Series theory [Schetzen, 1980]:

$$
\begin{aligned}
V_k &= \frac{1}{2^{k-1}}\frac{|\eta_k|}{|\eta_1|}V_{in}^k \\
\phi_k &= arg(\eta_k)
\end{aligned}
\tag{5.41}
$$

where η_k is the coefficient appearing in Equation 5.42,

$$
V_o(t) = \sum_k \eta_k e^{jk\omega t}
\tag{5.42}
$$

where $V_o(t)$ is the output signal when a hypothetical input signal $V_i = e^{j\omega t}$ is applied to the integrator. In our case, we are primarily interested in the first three harmonics and assume that higher order harmonics are negligibly small. Equation 5.42 can now be simplified to Equation 5.43

$$
V_o(t) = \eta_1 e^{j\omega t} + \eta_2 e^{j2\omega t} + \eta_3 e^{j3\omega t}
\tag{5.43}
$$

Plugging the above equation and $V_i = e^{j\omega t}$ into Equation 5.38 results in a simple algebra equation. Equating the coefficients for $e^{j\omega t}$, $e^{j2\omega}$ and $e^{j3\omega}$ on both side yields

$$
\begin{aligned}
2\pi(1 + 1/A_o)j\eta_1 &= \frac{C_1}{C_t}(1 - \eta_1/A_o) \\
2\pi(1 + 1/A_o)2j\eta_2 &= -\frac{C_1}{C_t}\eta_2/A_o \\
6\pi j[(1 + 1/A_o)\eta_3 - \gamma\eta_1^3/A_o] &= -\frac{C_1}{C_t}(\eta_3 - \gamma\eta_1^3)/A_o
\end{aligned}
\tag{5.44}
$$

The solutions for η_1, η_2 and η_3 are

$$
\begin{aligned}
\eta_1 &\approx \frac{1}{2\pi}\frac{C_1}{jC_t} \\
\eta_2 &= 0 \\
\eta_3 &\approx \frac{6\pi j + C_1/C_t}{6\pi j A_o}\gamma\eta_1^3
\end{aligned}
\tag{5.45}
$$

The corresponding HD coefficients are therefore

$$
\begin{aligned}
HD_2 &= 0 \\
HD_3 &= \frac{\gamma}{16\pi^2 A_o}(\frac{C_1}{C_t})^2 V_{in}^2
\end{aligned}
\tag{5.46}
$$

where $C_1/C_t < 6\pi$ is assumed in the derivation of the expression of HD_3. As expected, the second order harmonic coefficient is zero. The third order harmonic distortion is linearly proportional to the second order coefficient in the DC gain expression and inversely proportional to DC gain shown in Equation 5.30. The third order HD is also quadratically proportional to the magnitude of the input signal. The above calculation of the harmonic distortion is based on a noninverting two-phase SC integrator. Similar results are expected for an inverting SC integrator.

Summary

This section deals with the nonlinear DC gain error. It is shown that a large DC gain is essential to minimize the DC gain nonlinearity. The harmonic distortion of a SC integrator due to nonlinear gain is analyzed using a revised computation technique. By using the fully differential circuit, the second order harmonic distortion becomes negligibly small and only the third order harmonic distortion prevails. We find that, if permitted, a smaller value of input capacitor size compared to the integrating capacitor is helpful to reduce the 3rd order harmonic distortion.

5.5 POWER SAVING STRATEGIES

With the increased interest in low voltage and low power A/D converters design, comes the innovative design techniques. The new design techniques have

been reported for both digital and analog components. There are also some reports on new topologies for delta-sigma A/D converters. However, we believe that there is still room to reduce power consumption of existing topologies by optimally designing their building blocks, particularly the opamps.

In Chapter 3, we estimated the power consumption for commonly used opamps for delta-sigma modulators and suggested a design methodology to achieve optimal design for a given accuracy requirement. In this section we extend the previous analysis to take nonlinearities into consideration.

As we can notice on Figure 4.5, there are two distinct regions of nonlinearities, one of which is characterized by nonlinear settling (region I) and another by other nonlinear mechanisms (region II). The power-saving strategies differ in these two regions.

Strategy I

Although settling requirements are greatly relaxed provided the settling process is linear, linear settling is normally not realizable in practice. A conservative approach to achieve high resolution and high linearity is to design the integrator such that settling error is less than half LSB. Intuitively, some power is wasted to ensure such stringent settling requirement. As we will see in this section, this intuition is justified and a design methodology is suggested to save power.

The starting point of our analysis is to recognize that the error height in Figure 4.3 rather than the each settling error must be less than the LSB. According to Equation 3.6, the error voltage at the output of the integrator when the integration is finished is

$$
\begin{aligned}
e_o(T) &= V_o - V_{of} \\
&= \tilde{C}\Delta V_{th}exp\left(-\frac{T - T_{slew}}{\tau_{old}}\right) \\
&= \tilde{C}\Delta V_{th}exp\left(-\frac{(1-m)T}{\tau_{old}}\right)
\end{aligned}
\tag{5.47}
$$

where ΔV_{th} is the threshold voltage for the differential input pair, m is the fraction of the time used for slewing, and τ_{old} is the time constant of the opamp. Conventionally, the error voltage is set to be equal to half of LSB which gives

$$
n_{old} = \frac{T}{\tau_{old}} = \frac{1}{1 - m}ln(2^{N+1}\tilde{C}\frac{\Delta V_{th}}{V_r})
\tag{5.48}
$$

where N is the number of bits of resolution. The left hand side of the equation stands for the total number of time constant in one integration period, T.

Under the new model, the largest error occurs at $\hat{x} = \hat{x}_o$ and the magnitude is $E(\hat{x}_o)$. Keeping in mind that this error is a normalized with respect to the reference voltage. The actual error is $C_2 V_r/C_1 E(\hat{x}_o)$. Equating $C_2 V_r/C_1 E(\hat{x}_o)$

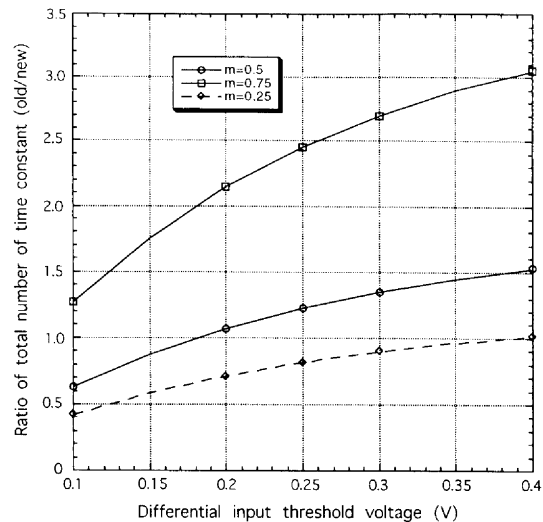**Figure 5.7.**   Time constant ratio versus ΔV

with $V_r/2^{N+1}$ yields

$$\frac{T}{\tau_{new}} = ln\left(2^{N+1}\frac{C_{eff}(C_{eff}+C_t)}{C_1 C_2}\frac{\Delta V \Delta V_{th}}{V_r^2}\right) + \frac{2C_2/C_{eff}V_r - (\Delta V + \Delta V_{th})}{\Delta V}$$

(5.49)

The larger the time constant, the larger the power consumption. Therefore, the ratio of the total time constants n_{old}/n_{new} reflects the relative power consumption for the same modulation designed by the old and the new philosophy respectively, where n_{new} is equal to T/τ_{new}. The ratio n_{old}/n_{new} being larger than one implies that the new design consumes less power. In order to study the impact of different circuit parameters on the ratio of total time constant, several graphs are plotted next.

Time constant ratio vs. ΔV. The ratio of T/τ_{old} and T/τ_{new} vs. ΔV is plotted in Figure 5.7 for three different values of m, where m is the fraction of the integration period devoted to slewing. The number of bits of resolution is chosen as 14. This plot shows that for a typical value of $m = 0.5$, the old design method results in almost the same power as the new design method when the opamp is design on the edge of strong inversion $\Delta V = 0.2$. When the threshold voltage increases, the new design method is favored to save power.
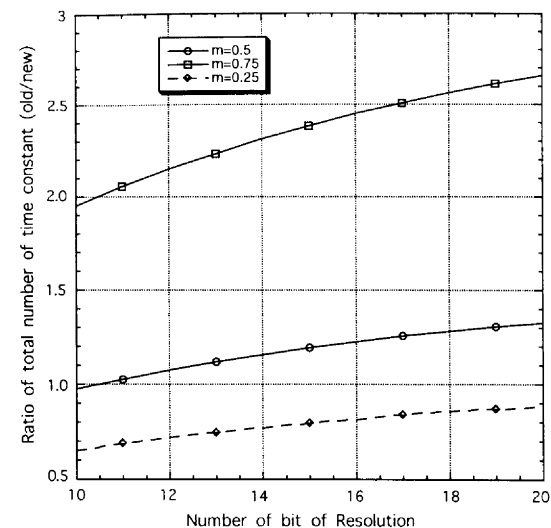
Figure 5.8.   Time constant ratio versus resolution

Time constant ratio vs. N. The time constant ratio vs. resolution is plotted in Figure 5.8. Again for a typical value of $m = 0.5$, the new design method is favored for the resolution requirement is larger than 10 bits. The saving can be as big as 30% for a 20 bit resolution application. The main reason is that the old design uses more stringent settling requirement for each clock period while the new design considers only the overall nonlinearity. Under the new design, during each individual clock period the integrator does not need to to settle to 20 bit, which in turn greatly reduces the current requirement.

Time constant ratio vs. capacitor ratio. The time constant ratio vs. capacitor ratio is plotted in Figure 5.9 with a fixed value of $C_1 + C_2$. For a typical value of $m = 0.5$, the new design is favored. The larger the capacitor ratio, the more power the new design saves. The reason can be found from Equation 5.49 and Equation 5.48. Under the old design philosophy, the power consumption is directly tied to the settling requirement of the output voltage which in turn is tied to the total load capacitance. When the sum of capacitor C_1 and C_2 is fixed, so is the total time constant and the power consumption no matter how the ratio C_1/C_2 changes as reflected in Equation 5.48. On the other hand, under the new design philosophy, the power consumption changes with the ratio C_1/C_2. As indicated in Equation 5.49, n_{new} is linearly proportional to C_2 inside the second right-hand side term, but only logarithmically proportional
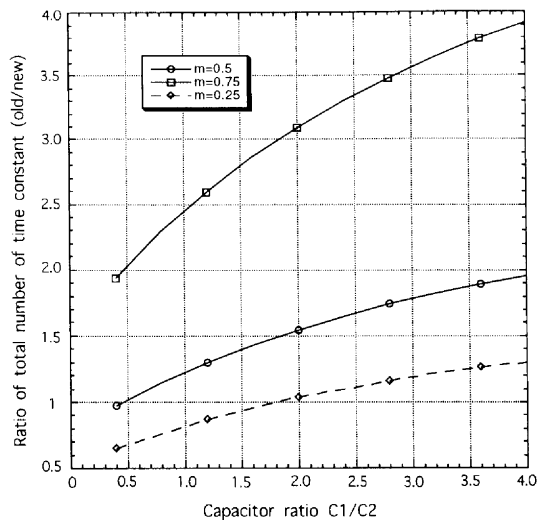
Figure 5.9.   Time constant ratio versus capacitor ratio

to $1/(C_1 C_2)$ inside the first right-hand side term. The overall effect is that the new time constant is monotonically decreasing when the ratio C_1/C_2 increases. Consequently, the ratio of the total time constant increases as C_1/C_2 increases. Based on the above argument, Equation 5.49 implies that under the new design philosophy, for a given total load capacitance requirement, a smaller value of the reference capacitor C_2 is favored to save power.

Strategy II

Since the nonlinearity is limited by mechanisms other than nonlinear settling in Region II, running more than certain amount of current will not improve the linearity at all. This is because nonlinearities such as nonlinear capacitor and the unsettled reference voltage are independent of current. In this case the strategy is first to estimate the nonlinear error from those current-independent sources and find the maximum value (E_{max}) among them. The minimum current can be obtained by equating the nonlinear settling error with E_{max}. Graphically this is equivalent to find the corner current from Figure 4.5, i.e.,

$$E(\hat{x}_o) = E_{max} \qquad (5.50)$$

This leads to

$$\frac{T}{\tau} = ln\left(\frac{C_{eff}(C_{eff} + C_t)}{C_2^2} \frac{\Delta V \Delta V_{th}}{V_r^2 E_{max}} \right) + \frac{2C_2/C_{eff}V_r - (\Delta V + \Delta V_{th})}{\Delta V} \qquad (5.51)$$

Given the value of T, the whole integration period, we can calculate the time constant τ and therefore the current consumption. An example will be given in Chapter 6 to demonstrate the design strategy.

5.6   CONCLUSIONS

In this chapter, the framework developed in Chapter 4 to calculate nonlinearity in delta-sigma modulators is further extended to other phenomena including nonlinear capacitor, nonlinear reference voltage and nonlinear DC gain. The main findings are as follows. Based on these findings and the theoretical model, we outline a design strategy to minimize the power consumption of the modulator.

- Dielectric relaxation has no impact on the linearity performance of the delta-sigma modulators.

- The nonlinear capacitor error due to the voltage-dependent capacitance is quadratically proportional to the reference voltage.

- Sampling induced reference variation will not contribute to the overall nonlinearity. A small value for the reference voltage is preferred.

- The use of class AB opamps will cause nonlinearity even under the simplified condition. A small value for the reference voltage is preferred.

- Nonlinear DC gain will cause harmonic distortion in the SC integrator used in the modulator.

- Two power saving plans are outlined depending the magnitude of the nonlinearity.

    Our analytical model only utilize the parameters from both integrators and transistors. Compared to conventional practice where either empirical parameters or curve fitting has been used, our methodology not only makes better predictions but also provides a convenient means to guide the design.

6 CIRCUIT IMPLEMENTATION OF DELTA-SIGMA MODULATORS

6.1 INTRODUCTION

In this chapter, we discuss the implementation details of delta-sigma modulators. Our primary target applications are data acquisition and low frequency instrumentation. Therefore, the extremely high linearity is our top design priority. A complete second order delta-sigma modulator has been fabricated and the nonlinearity results were reported in Chapter 4. However, copyright issues prevent us from discussing the implementation details. As an integral part of our research, instead, we examine the design issues for a first order delta-sigma modulator. This chapter is arranged as follows. Section 6.2 outlines the overall structure for a first order delta-sigma modulator and its timing diagram. Section 6.3 discusses the design of the integrator. The need for auto-zeroing technique is addressed and the principle of one implementation is explained. Section 6.4 is devoted to the design of the opamp. The optimal design principle and design strategy developed in the previous chapters are applied here to determine the supply current and device sizes. The fully differential implementation of the integrator requires a common mode feedback (CMFB) circuitry to stabilize the common mode output voltage of the fully differential opamp. The
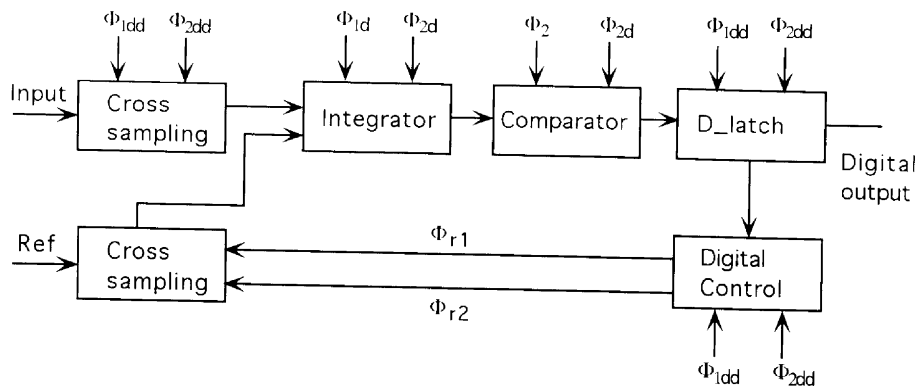
Figure 6.1.   A system overview of a first order delta-sigma modulator

design of a switched-capacitor realization of the CMFB circuitry is discussed. Section 6.5 discusses the comparator design. Section 6.6 briefly describes the digital circuitry for the feedback control in the modulator and the two-phase nonoverlapping clock generation. Section 6.7 shows the measured results. Finally we provide some conclusions in Section 6.8.

6.2   SYSTEM OVERVIEW

In this section, the system level diagram of a first order delta-sigma modulator is presented. The building block designs are discussed in detail in the following sections. The whole system is implemented using fully differential circuit, and a two-phase nonoverlapping clocking scheme is employed. The overall block diagram is shown in Figure 6.1 A first order delta-sigma modulator consists of four main building blocks: the fully differential integrator, the comparator, the D-latch and the digital control circuitry. The switch control signals that are associated with each building block are also shown in Figure 6.1. The cross sampling block is actually the sampling stage (input stage) of the integrator. We deliberately separate them out from the integrator in order to emphasize the nature of the sampling, which will be explained in detail in Section 6.3. The letter "d" and "dd" that appear in the subscript of clocking signals Φ_1 and Φ_2 stand for delayed versions of the corresponding phases. For example, the clocking signal Φ_{1d} stands for the delayed version of Φ_1, and Φ_{1dd} the delayed version of Φ_{1d}. The timing diagram for all the phases are depicted in Figure 6.2. Text that appears to the left of the each phase shows which building block is controlled by that signal. A brief description for each phase

is as follows. The comparator stays in the reset period during Φ_2 and starts the comparison at its falling edge. The digital outcome of the comparator is valid through the whole interval between the falling edge of current Φ_2 and the rising edge of the next Φ_2. A pull-up positive feedback circuit is added to accelerate the comparison and is controlled by Φ_{2d}. The details are explained in Section 6.5. The integrator complete the integration during Φ_{2d}. To eliminate the possibility of making a false comparison, the comparator starts making a decision slightly before the end of Φ_{2d}. After completing the integration phase, the integrator enters the auto-zero phase during Φ_{1d}. The D-latch reads in the comparator output during Φ_{1dd} and latches the value until the rising edge of the next Φ_{1dd} before being updated. Therefore, the D-latch provides a valid digital output for a complete period. Two switching signals Φ_{r1} and Φ_{r2} for the reference voltages are generated during this period, and are aligned with the cross sampling phases Φ_{1dd} and Φ_{2dd} for the input voltages. Ideally, phases Φ_{1d} and Φ_{1dd} should be made the same without any relative delay. Practically the delay is necessary to minimize signal dependent charge injection from the cross sampling switches.

The design details for the integrator, the opamp, the comparator and the digital circuitry are discussed in the following sections.

6.3   INTEGRATOR DESIGN

The integrator makes up the most important component in a delta-sigma modulator. For a higher order ($n \geq 2$) delta-sigma modulator, the noise and the distortion coming from the first integrator will have larger impact on the overall modulator performance than that from other integrators. For example, the nonlinearity from the nonlinear settling in the first order dominates the overall nonlinearity error in a second order delta-sigma modulator, as shown in Section 4.4. Generally the above assessment can be put into more vigorous form through Z-domain analysis. A linearized Z-domain digram of a second order delta-sigma modulator is shown in Figure 6.3. The imperfection from each integrator is treated as an additive noise seen at the output of that integrator. The Z-domain expression for the digital output can be written as

$$Y(Z) = Z^{-1}X(Z) + E_1(Z)(1-Z^{-1}) + E_2(Z)(1-Z^{-1})^2 + E(Z)(1-Z^{-1})^2 \quad (6.1)$$

where $E_1(Z)$ and $E_2(Z)$ are imperfection from first and second integrator respectively. $E(Z)$ is the quantization noise. Clearly the imperfection from the second integrator is suppressed by a second order highpass filter as opposed to a first order highpass filter for the first integrator. Therefore, imperfections from the first integrator have much larger impact on the measured signal than the second integrator. This is also true for the higher order modulators.
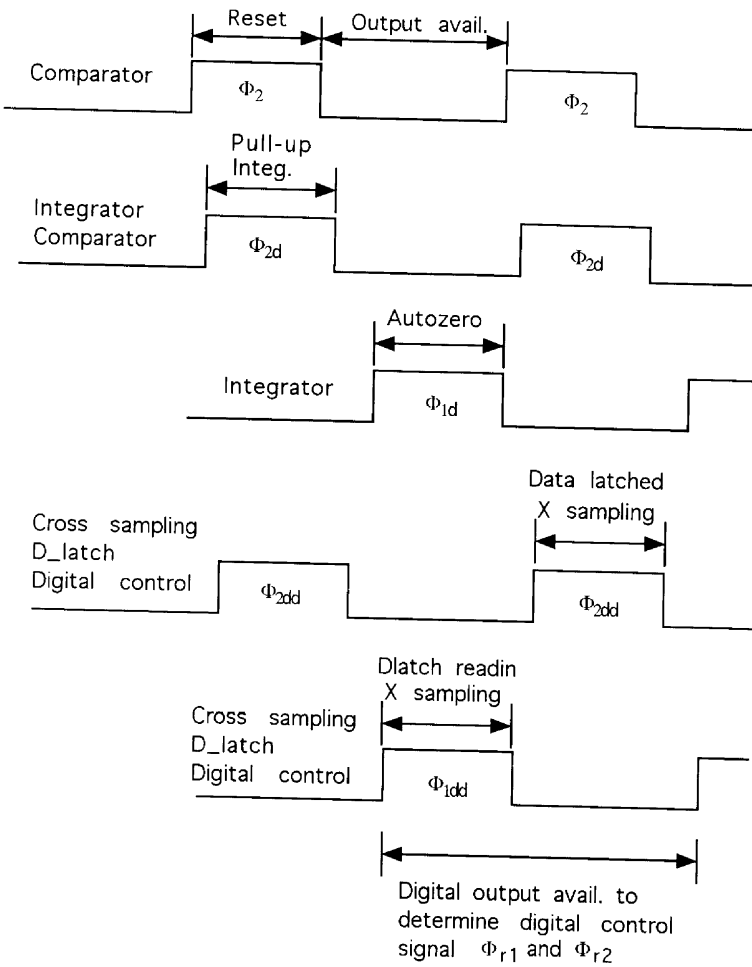
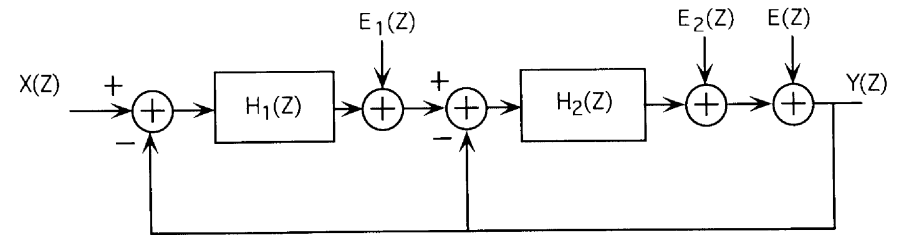**Figure 6.2.**   Control signal timing diagram

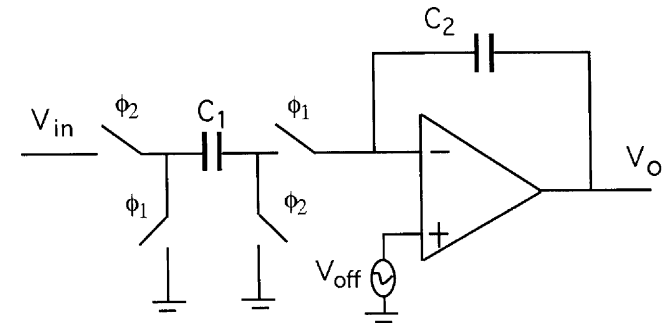**Figure 6.3.**   Z-domain schematic of a second order $\Delta\Sigma$ modulator

Figure 6.4.   A noninverting SC integrator without autozeroing

An important nonideal effect in a switched-capacitor (SC) integrator is the DC offset voltage and flicker noise . For near DC applications such as data acquisition and sensor instrumentation, flick noise becomes a severe problem. Techniques have been developed to alleviate these problems. The two main techniques are chopper stabilization and auto-zeroing. We only focus on the auto-zero technique here. Figure 6.4 shows a noninverting SC integrator with parasitic insensitive configuration. The overall DC offset and flicker noise are taken into account as an offset voltage V_{off} at the positive input of the opamp. The Z-domain equation of the integrator can be written as

$$V_o(Z) = \frac{C_1}{C_2} \frac{V_{in}(Z)Z^{-1}}{1 - Z^{-1}} + \frac{C_1}{C_2} \frac{V_{off}(Z)}{1 - Z^{-1}} \tag{6.2}$$

The first term on the right hand side of Equation 6.2 corresponds to the ideal integrator with no offset voltage. The second term is the error term. The problem for this circuit comes from the fact that the plate of capacitor C_1 that is connected to the negative input of the opamp during Φ_1 sees two different voltage: analog ground during phase Φ_1 and the offset voltage during Φ_2.
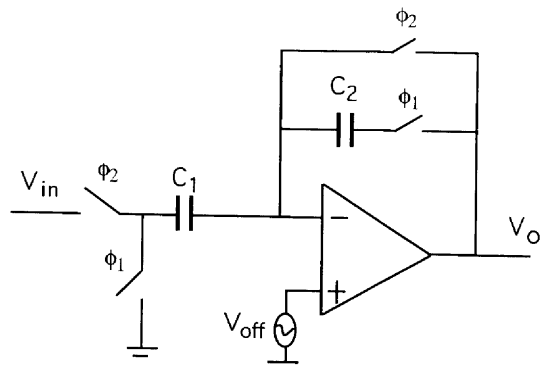
Figure 6.5.   A noninverting SC integrator with autozeroing

The difference between these two voltages is being accumulated through the integrator and eventually forces V_o to hit the rail. The idea behind the simple auto-zero technique is never to disconnect the top plate of capacitor C_1 from the negative input of the opamp as shown in Figure 6.5. The switched path between the negative input and the output of the opamp is needed to charge the input capacitor C_1 during Φ_2. The Z domain equation of the auto-zeroed integrator is then

$$V_o(Z) = \frac{C_1}{C_2}\frac{V_{in}(Z)Z^{-1}}{1 - Z^{-1}} + \frac{C_1}{C_2}\frac{V_{off}(Z)(1 - Z^{-1/2})}{1 - Z^{-1}} \qquad (6.3)$$

The term $1 - Z^{-1/2}$ in Equation 6.3 serves as a high pass function, and any low frequency component of the offset voltage will be substantially suppressed. Therefore, the DC offset voltage will vanish and the $1/f$ flicker noise in the low frequency region will be reduced. One drawback of this circuit is that due to existence of the switched path between the input and the output of the opamp, the output voltage has to swing back from its value during Φ_1 to V_{off} during Φ_2 in a timely fashion. This imposes a stringent requirement on the slew rate of the opamp. Once we understand that the role of the switched path is to charge the input capacitor, we can modify the current configuration to avoid this problem. The idea is to create a different route to discharge the input capacitor. One technique to implement this is shown in Figure 6.6 and is called gain-squared auto-zero. The principle of the circuit can be understood as follows. During Φ_1, the charge stored in the input capacitor C_1 is transferred to the integrating capacitor C_2, i.e., capacitor C_1 is discharged. Meanwhile, the capacitor C_4 and C_3 are precharged. During the following Φ_2, capacitor C_1 is charged to
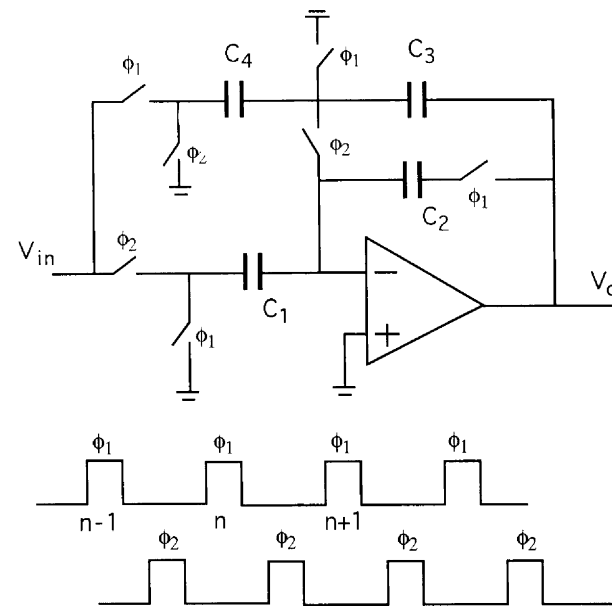
Figure 6.6.   A noninverting SC integrator with modified autozeroing

the input voltage. A charge equal to C_1V_{in} is stored on the bottom plate of capacitor C_1 (left side). Because of the charge conservation, the same amount of charge has to be moved out of the top plate of capacitor C_1. In Figure 6.5, this charge is routed to the opamp. In Figure 6.6, this charge is routed to the capacitor C_4 to neutralize the charge previously stored there. It is essential that capacitor C_4 be the same size as capacitor C_1. Otherwise, the extra charge will be redistributed to capacitor C_3 resulting in a disturbance of the output voltage V_o. This defeats our purpose. The actual size of capacitor C_3 is not important because it only serves as a holding capacitor during Φ_2. Normally a small value is chosen to minimize the total load capacitance. An additional advantage of using this configuration is that the DC gain of the opamp in the integrator transfer function is squared. Let us provide a brief derivation for this statement. We assume that the opamp has a finite but linear DC gain. In another words, the magnitude of the offset seen at the negative input of the opamp is equal to the output voltage of the opamp divided by a constant DC gain A. Let us denote $\Phi_1(n-1)$ as the instance of the end of the $(n-1)th$ phase Φ_1 and $\Phi_2(n-1)$ the end of immediate following phase Φ_2. In order to derive the transfer function of the integrator, we have to find the relationship

between the output voltage $V_o[\Phi_2(n-1)]$ and $V_o[\Phi_1(n-1)]$. At $\Phi_1(n-1)$ the charge on the top plate of capacitor C_1, C_3 and C_4 are

$$
\begin{aligned}
Q_{C_1}[\Phi_1(n-1)] &= -C_1 V_o[\Phi_1(n-1)]/A \\
Q_{C_4}[\Phi_1(n-1)] &= -C_1 V_{in}[\Phi_1(n-1)] \\
Q_{C_3}[\Phi_1(n-1)] &= -C_3 V_o[\Phi_1(n-1)]
\end{aligned}
\tag{6.4}
$$

At $\Phi_2(n-1)$, the respective charge on each capacitor becomes

$$
\begin{aligned}
Q_{C_1}[\Phi_2(n-1)] &= -C_1\{V_o[\Phi_2(n-1)]/A + V_{in}[\Phi_2(n-1)]\} \\
Q_{C_4}[\Phi_2(n-1)] &= -C_1 V_o[\Phi_2(n-1)]/A \\
Q_{C_3}[\Phi_2(n-1)] &= -C_3\{V_o[\Phi_2(n-1)]/A + V_o[\Phi_2(n-1)]\}
\end{aligned}
\tag{6.5}
$$

where $C_4 = C_1$ is used. Since one plate of capacitor C_2 is floating, the charge stored on C_2 will not change. Therefore, during the interval from $\Phi_1(n-1)$ to $\Phi_2(n-1)$, the total charge stored on the three capacitors C_1, C_2 and C_4 should be conserved, i.e.,

$$
Q_{c_1} + Q_{c_2} + Q_{c_4}|_{\Phi_1(n-1)} = Q_{c_1} + Q_{c_2} + Q_{c_4}|_{\Phi_2(n-1)}
\tag{6.6}
$$

Plugging Equation 6.4 and Equation 6.5 into Equation 6.6, we have

$$
\alpha V_o[\Phi_1(n-1)] + C_1 V_{in}[\Phi_1(n-1)] = \beta V_o[\Phi_2(n-1)] + C_1 V_{in}[\Phi_2(n-1)]
\tag{6.7}
$$

where

$$
\begin{aligned}
\alpha &= \frac{C_1 + AC_3}{A} \\
\beta &= \frac{2C_1 + C_3 + AC_3}{A}
\end{aligned}
\tag{6.8}
$$

If we further assume that the input signal dose not change value during phase Φ_2, we then have

$$
V_o[\Phi_2(n-1)] = \frac{\alpha}{\beta} V_o[\Phi_1(n-1)]
\tag{6.9}
$$

Equation 6.9 describes the relationship of the output voltage V_o during phase Φ_1 and phase Φ_2. If the opamp is ideal and the DC gain is infinite, Equation 6.9 indicates that the output voltage in the end of the integration phase Φ_1 should be equal to that in the end of the sampling phase Φ_2. With the help of Equation 6.9, we can now calculate the transfer function of the integrator. From the charge conversation, the difference between charge stored in the capacitor C_1

during $\Phi_2(n-1)$ and $\Phi_1(n)$ will be equal to the change of charge stored on the integrating capacitor C_2. Mathematically put, we have

$$
\begin{aligned}
&C_2(1 + \frac{1}{A})(V_o[\Phi_1(n)] - V_o[\Phi_1(n-1)]) = \\
&C_1(V_{in}[\Phi_2(n-1)] + \frac{V_o[\Phi_2(n-1)]}{A} - \frac{V_o[\Phi_1(n)]}{A})
\end{aligned}
\tag{6.10}
$$

Transforming Equation 6.10 into a Z-domain expression, we obtain

$$
\frac{V_o(Z)}{V_{in}(Z)} = \frac{C_1 A Z^{-1}}{(A+1)C_2(1 - Z^{-1}) + C_1(1 - \frac{\alpha}{\beta})}
\tag{6.11}
$$

Equation 6.9 is used to derive above equation. We are primarily interested in the DC behavior of the transfer function expressed by Equation 6.11. It can be easily shown that at DC the transfer function becomes

$$
\frac{V_o(Z)}{V_{in}(Z)}\Big|_{Z=1} = \frac{C_3 A^2}{C_1 + C_3}
\tag{6.12}
$$

Equation 6.12 indicates that when this autozeroed integrator is used in the delta-sigma modulator, the quantization error left around DC is proportional to $1/A^2$ as opposed to $1/A$ in the non-autozeroed or simple auto-zeroed integrator. Thus the performance degradation due to the finite DC gain is greatly reduced.

The fully differential version of Figure 6.6 is shown in Figure 6.7. In the actual implementation, the sizes for capacitor C_1 and C_2 are chosen to be the same and are equal to $2pF$. The size of the integrating capacitor is chosen to be $4pf$, and the holding capacitor C_h is equal to $1pf$. The clock signals Φ_{1dd} and Φ_{2dd} are generated by delaying Φ_{1d} and Φ_{2d}. Since the switches that are associated with the integrator capacitor C_t (controlled by phase Φ_{2d}) connect only to the virtual ground, they only exhibit signal independent charge injection. However, the switches in the cross sampling lattice contribute signal dependent charge injection. The arrangement of the switching signals ensures that these charges can not be injected into the integrating capacitor C_t due to the open path[Choi et al., 1983]. The signal independent charge injected into C_t is a common mode signal and is further suppressed by the fully differential implementation of the modulator.

In this section, we stressed the importance of the careful design of the first integrator while the design requirements for the second and/or higher integrators can be relaxed. The principle of the simple and gain-squared auto-zero techniques to reduce the sensitivity of the finite gain and flicker noise is also explained. The next design step is the implementation of the opamp inside the integrator which is discussed in the next section.
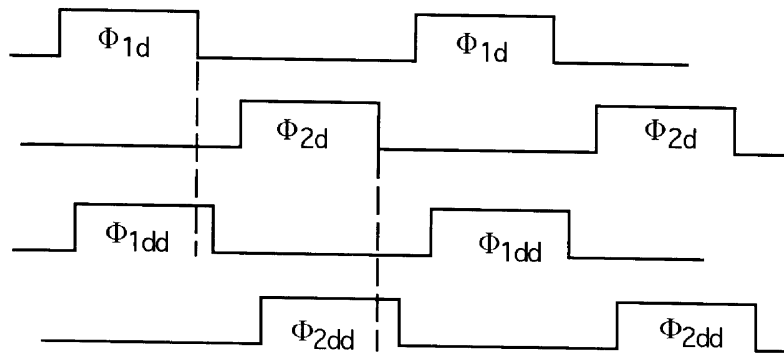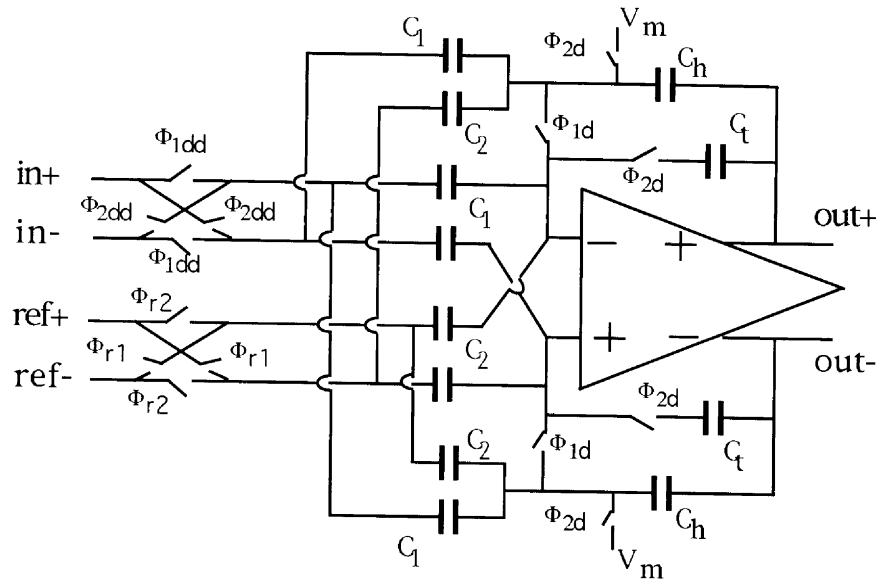
Figure 6.7.   A fully differential SC integrator with gain-squared autozeroing
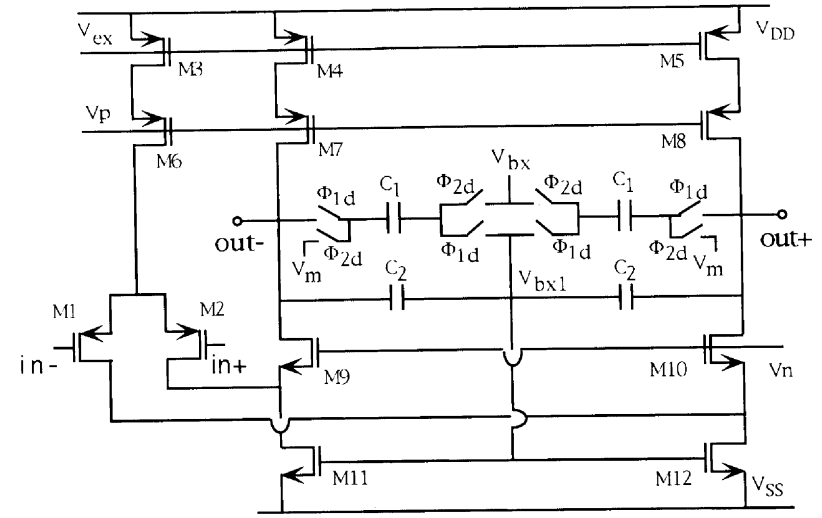
Figure 6.8.   The folded-cascode opamp used in the modulator

6.4   OPAMP DESIGN

As we mentioned in Chapter 3, opamps remain the most critical component in the modulator. According to the results we presented there, class A opamps are the best choice for high resolution/high linearity delta-sigma modulators. Commonly used class A opamps include folded cascode opamp, current gain opamp and Miller-compensated opamp. The criteria to select the optimal design is good power-speed performance, high low-frequency open loop gain and low distortion when a large signal is applied. Based on this criteria, a folded-cascode opamp is chosen [Rebeschini, 1989]. The circuit schematic is shown in Figure 6.8 and its bias circuit is shown in Figure 6.9. The circuit is fully differential and cascode transistors M_7 to M_{10} are employed to increase the output impedance. Since the modulator is designed for data acquisition, the flicker noise from the differential input pair is of concern. Therefore, PMOS input transistors are chosen to reduce such noise. The supply current and the device sizes are determined based on our design strategy explained in the previous chapter. The four capacitors, with values C_1 and C_2, and their associated switches form the capacitive common mode feedback (CMFB) circuit. The operation principle will be explained in detail.

Supply current and device sizes.   Since high linearity is our primary concern, and the nonlinear errors described in Chapter 5 are our dominate error
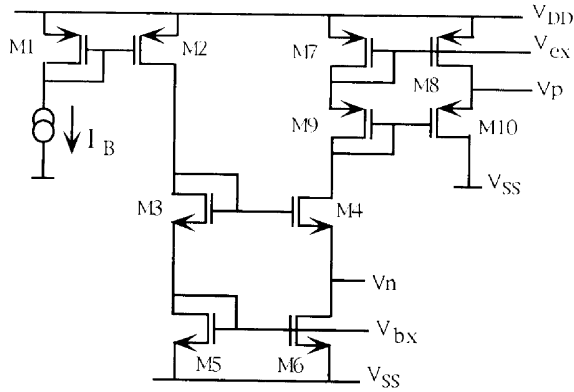
Figure 6.9. The bias circuit for the folded-cascode opamp

sources, we will adopt the design strategy II suggested in that chapter. Let us first repeat the main design equation as follows.

$$\frac{T}{\tau} = ln\left(\frac{C_{eff}(C_{eff} + C_t)}{C_2^2}\frac{\Delta V \Delta V_{th}}{V_r^2 E_{max}}\right) + \frac{2C_2/C_{eff}V_r - (\Delta V + \Delta V_{th})}{\Delta V} \quad (6.13)$$

where T is the total time period for integration phase, and normally is equal to half of the sampling period if a two-phase non-overlapping clocking scheme is used. τ is the time constant of the opamp. C_{eff} is equal to sum of the input and the reference capacitor. C_2 is the reference capacitor and C_t is the integrating capacitor. V_r is the reference voltage and is chosen to be $2V$. ΔV_{th} is the threshold voltage for the differential input pair. ΔV is equal to $V_{gs} - V_T$ of the transistors and is to be designed around $0.2V$. E_{max} is the maximum normalized nonlinear errors. The exact value for E_{max} is not important and can vary by 2X-4X since the E_{max} term appears only in the log expression, i.e., the number of total time constants is a very slow function of the term E_{max}. We assume that it is equal to 2^{-M}, where the value of M is given below. In our application, we assume $C_1 = C_2$ and $C_t = 2C_1$. Plugging in numerical values, we can obtain the following equation

$$\frac{T}{\tau} \approx (M - 3)ln2 + 7.6 \quad (6.14)$$

If the relationship among C_1, C_2 and C_t differs from what is mentioned above, Equation 6.14 will not vary a lot. The value of M is usually in the vicinity of 13 to 14. Under the conventional design paradigm, the error left at the opamp

output after the integration period must be less than half LSB (least significant bit), i.e.,

$$\hat{C}\Delta V e^{-T_S/\tau} \leq \frac{V_r}{2^{N+1}} \quad (6.15)$$

where T_S is the time used for settling and its optimal value is around half the integration period (see Chapter 3). The variable N is the number of bits of resolution. Equation 6.15 can be rewritten as Equation 6.16

$$\frac{T}{\tau} = ln(2^{N+1}\hat{C}\frac{\Delta V_{th}}{V_r}) \quad (6.16)$$

Plugging the numerical values, we have

$$\frac{T}{\tau} \approx 2(N - 1)ln2 \quad (6.17)$$

where N is normally considered as the number of bit of resolution of the underlying converter. In weak inversion operation, the current dissipation is linearly proportional to the number of time constant. Let us compare the power consumption of the opamp designed by the old and the new strategy assuming $N = 16$ and $M = 13$. The ratio of the power consumption is equal to the ratio of the number of the time constant, i.e.,

$$\frac{(M - 3)ln2 + 7.6}{2(N - 1)ln2} = \frac{14.5}{20.7} = 0.7 \quad (6.18)$$

Equation 6.18 suggests that under the new design strategy, as much as 30% power consumption can be saved. This calculation agrees very well with the measured results shown in Figure 4.5.

After finding out the number of time constants from Equation 6.14, we can calculate the transconductance g_m of the differential input pair using the relationship $g_m = C_{eff}/\tau$, and the result is shown in Equation 6.19

$$\begin{aligned} g_m &= 14.5C_{eff}/T \\ &= 29C_{eff}f \end{aligned} \quad (6.19)$$

where $T = 2/f$ is used. The factor of 2 accounts for the fact that T is the integration period and is equal to half the sampling period if a two phase clock is assumed. In our application, f, the sampling frequency, is equal to $200KHz$ and C_{eff}, the effective load capacitance, is equal to $10pF$. Therefore, a magnitude of 58μ is obtained for the input transconductance g_m. The required current and the device size of the differential input pair can be obtained through the following equations (assume strong inversion operation)

$$\begin{aligned} \Delta V &= \sqrt{\frac{2I}{kW/L}} \\ g_m &= \sqrt{2IkW/L} \end{aligned} \quad (6.20)$$

where $\Delta V = V_{gm} - V_T$ and is chosen to be around 0.2. Solving Equation 6.20, we have $I = 5.8\mu A$ and $W/L \approx 6$. After the current conducting through the input transistor is available, the device sizes of all other transistors can be computed. After a couple of iterations, the device sizes are finalized and are summarized in Table 6.1 for the opamp core circuit and in Table 6.2 for the bias circuitry.

Table 6.1.   Device sizes for the opamp core circuit

	M_1	M_2	M_3	M_4	M_5	M_6
W	$180\mu m$	$180\mu m$	$272\mu m$	$136\mu m$	$136\mu m$	$136\mu m$
L	$20\mu m$	$20\mu m$	$16\mu m$	$16\mu m$	$16\mu m$	$8\mu m$
	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}
W	$48\mu m$	$48\mu m$	$20\mu m$	$20\mu m$	$192\mu m$	$192\mu m$
L	$8\mu m$	$8\mu m$	$20\mu m$	$20\mu m$	$40\mu m$	$40\mu m$

Design of the common mode feedback circuit.   The design of a fully differential opamp requires a common mode feedback circuit. Many circuit topologies[Haspeslagh and Sansen, 1988, Duque-Carrillo, 1993] have been used in literatures. A capacitive common feedback circuit is shown in Figure 6.10. In order to explain the basic operation, we omit the NMOS cascode transistors and replace the top PMOS transistors by ideal current sources. This is valid because we are only concerned with the common mode operation of the circuit. The understanding of the circuit operation can be made as follows. During Φ_{2d} two capacitor C_1 are precharged to $C_1(V_{bx} - V_m)$, where V_m is a preset voltage which the common mode output voltage is expected to be and normally is chosen to be the midpoint of the rail-rail power supply. During Φ_{1d}, the common plate of two

Table 6.2.   Device sizes for the bias circuit

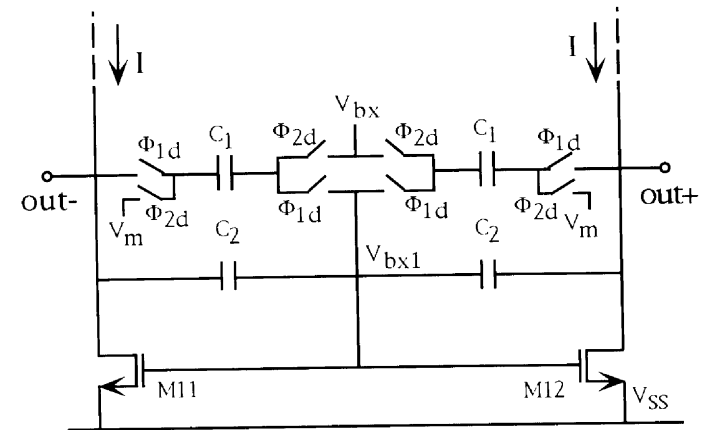|	M_1	M_2	M_3	M_4	M_5
W	$10\mu m$	$10\mu m$	$3\mu m$	$24\mu m$	$24\mu m$
L	$20\mu m$	$20\mu m$	$40\mu m$	$40\mu m$	$40\mu m$
	M_6	M_7	M_8	M_9	M_{10}
W	$24\mu m$	$34\mu m$	$17\mu m$	$9\mu m$	$28\mu m$
L	$40\mu m$	$16\mu m$	$16\mu m$	$16\mu m$	$8\mu m$

Figure 6.10.   A capacitive common mode feedback circuit

capacitors C_1 are connected to V_{bx1}. If the common mode of the output voltage changes, this forces V_{bx1} to move in the same direction through the coupling of capacitor C_1. Because of the negative feedback nature of the transistors M_{11} and M_{12}, the change of gate voltage V_{bx1} induces the opposite movement of the drain voltages which are in this case V_{out+} and V_{out-}. The stabilization of the common mode voltage is therefore achieved. Mathematically put, during the precharge phase Φ_{2d}, the charge stored on the two capacitors C_1 and the two capacitors C_2 are

$$\begin{aligned} Q_{c1}^{2d} &= 2C_1(V_{bx} - V_m) \\ Q_{c2}^{2d} &= 2C_2(V_{bx1}^{2d} - V_{cm}^{2d}) \end{aligned} \qquad (6.21)$$

where V_{cm}^{2d} is the common mode (CM) of the output voltage during Φ_{2d} and is equal to half of the sum of voltage V_{out+} and V_{out-}. When Φ_{1d} is high, the stored charges become

$$\begin{aligned} Q_{c1}^{1d} &= 2C_1(V_{bx1}^{1d} - V_{cm}^{1d}) \\ Q_{c2}^{1d} &= 2C_2(V_{bx1}^{1d} - V_{cm}^{1d}) \end{aligned} \qquad (6.22)$$

The principle of charge conservation requires that $Q_{c1}^{2d} + Q_{c2}^{2d}$ be equal to $Q_{c1}^{1d} + Q_{c2}^{1d}$. After some simple algebraic manipulation, we obtain

$$V_{bx1}^{1d} - V_{cm}^{1d} = \frac{C_1(V_{bx} - V_m)}{C_1 + C_2} + \frac{C_2(V_{bx1}^{2d} - V_{cm}^{2d})}{C_1 + C_2} \qquad (6.23)$$

The right hand side of Equation 6.23 is evaluated during Φ_{2d} and is fixed during Φ_{1d}. Therefore, Equation 6.23 indicates that the gate voltage V_{bx1} moves in the

same direction as V_{cm}^{1d}, the CM of the output voltage which in turn is stabilized through the negative feedback mechanism. Ideally, the common mode output voltage should be kept the same during both two phases and be equal to V_m. Practically this will not happen as shown in Equation 6.24

$$V_{cm}^{1d} = \frac{C_1 V_m}{C_1 + C_2} + \frac{C_2 V_{cm}^{2d}}{C_1 + C_2} \qquad (6.24)$$

The approximation $V_{bx1}^{1d} \approx V_{bx1}^{2d} \approx V_{bx}$ is made to derive the above expression from Equation 6.23. The difference between V_{cm}^{2d} and V_{cm}^{1d} can be shown to be equal to

$$V_{cm}^{1d} - V_{cm}^{2d} = \frac{C_1}{C_1 + C_2}(V_m - V_{cm}^{2d}) \qquad (6.25)$$

If V_{cm}^{2d} is equal to V_m for any integration period, then V_{cm}^{1d} will be equal to V_m in the following auto-zero period On the other hand, as long as V_{cm}^{2d} differs from the preset voltage V_m, so does V_{cm}^{1d}. More than that, the difference between V_{cm}^{2d} and V_{cm}^{1d} is always nonzero. A larger value of C_2 is helpful in minimizing this difference. However, to avoid overloading the integrator, the choice of capacitor C_2 is usually a design compromise.

6.5   COMPARATOR DESIGN

The comparator in a delta-sigma modulator serves as a one bit quantizer and generates a stream of digital outputs. In the linearized delta-sigma model, an ideal comparator is replaced by an additive white noise source. The intrinsic offset voltage and device noise of a practical comparator can be treated as an additive noise superimposed on the quantization white noise. The comparator hysteresis can also be modeled as additive white noise [Boser and Wooley, 1988]. Therefore, all the nonidealities of the comparator experiences the same noise-shaping as the quantization noise. This means that the nonidealities of the comparator within the signal bandwidth are reduced. This renders the design of comparator as a comparatively easy task.

Figure 6.11 shows a regenerative comparator used in our design. The comparator offers benefits of high speed, low power and small area. Many variations of this comparator have been used in literature. The circuit is fully differential with inputs V_{in+} and V_{in-}. The outputs V_{cout+} and V_{cout-} need to be buffered which will be shown later. Transistors M_1 to M_4 form the input stage resembling the input stage of a symmetrical OTA (operational transconductance amplifier). Transistor M_5 to M_{12} serve as an output stage, where transistors M_{10} to M_{12} form a pull-down positive feedback latch while transistors M_6, M_8 and M_9 form a pull-up positive feedback latch. The clock signal Φ_d to transistor M_7 is the slightly -delayed version of the clock signal Φ. The reason
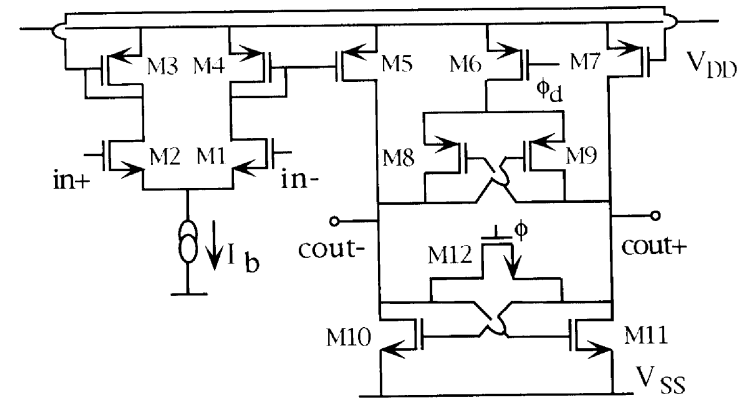
Figure 6.11.   Circuit schematic for the regenerative comparator

for delay is that the pull-down latch makes the decision first on which direction each output voltage should regenerate, and then the pull-up latch helps to accelerate the outcome. The comparator will function well even without the pull-up feedback latch. However, the comparator speed will increase if the pull-up latch is enabled. The basic principle of operation can be understood as follows with the help of Figure 6.12 and Figure 6.13. During the reset phase where Φ is high, both of the output voltage V_{cout+} and V_{cout-} are reset to the same value. Suppose the positive input voltage V_{in+} is larger than the negative input voltage V_{in-}. Transistor M_7 will conduct more current than transistor M_5. However, since both the gate voltage and the drain voltage of transistors M_{10} and M_{11} are the same, they should conduct the same amount of current. The gate voltage is determined by Equation 6.26

$$I_b = \frac{1}{2}K\frac{W}{L}(V_1 - V_T)^2 \qquad (6.26)$$

where $V_1 = V_2$ and V_T is the threshold voltage of the transistor. From Figure 6.12, we can see that the differential current mirrored from the differential input pair is redistributed in such way that the same amount of current flows through transistors M_{10} and M_{11}. When Φ goes low (transistor M_{12} is open), the comparator enters the comparison phase. Both transistors M_{10} and M_{11} experience a step current input with opposite polarity. For instance, just before Φ goes low, let transistor M_7 conducts $I_b + \Delta$ of current while transistor M_{11} conducts I_b. After Φ goes low, all the current conducted by M_7 has to go through M_{11}. Therefore, transistor M_{11} experiences a current step jump with a magnitude of Δ. This will force the drain voltage of transistor M_{11} to increase.
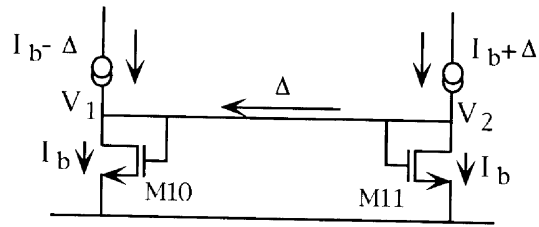
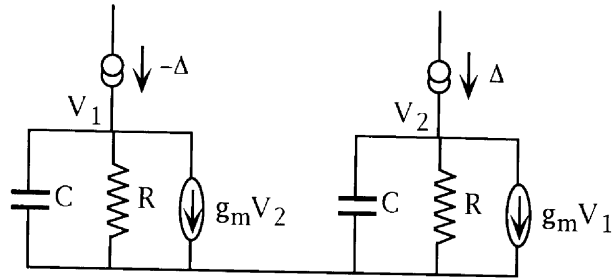**Figure 6.12.**   Circuit schematic for the comparator during the reset phase

Figure 6.13.   Circuit schematic for the comparator during the comparison phase

Similarly, the drain voltage of transistor M_{10} will be forced to decrease. Because of the positive feedback mechanism, both drain voltages will accelerate towards the opposite rail voltages. The outputs are then interpreted as a logic zero or one representing the results of the comparison. A quantitative analysis of the operation can be made as follows. Figure 6.13 shows the small signal model when Φ goes low. The equations describing the small signal model in S-domain can be established as

$$
\begin{aligned}
g_o V_1(S) + g_m V_2 + CSV_1(S) &= -\frac{\Delta}{S} \\
g_o V_2(S) + g_m V_1 + CSV_2(S) &= \frac{\Delta}{S}
\end{aligned}
\tag{6.27}
$$

The solutions of the above equations are

$$
V_1(t) = \frac{\Delta}{g_m - g_o}(1 - e^{t/\tau})
\tag{6.28}
$$

$$
V_2(t) = \frac{\Delta}{g_m - g_o}(e^{t/\tau} - 1)
\tag{6.29}
$$

where τ is the equal to the time constant RC of the transistor, and g_o is the reciprocal of the drain-to-source resistance R. The above equations indicate
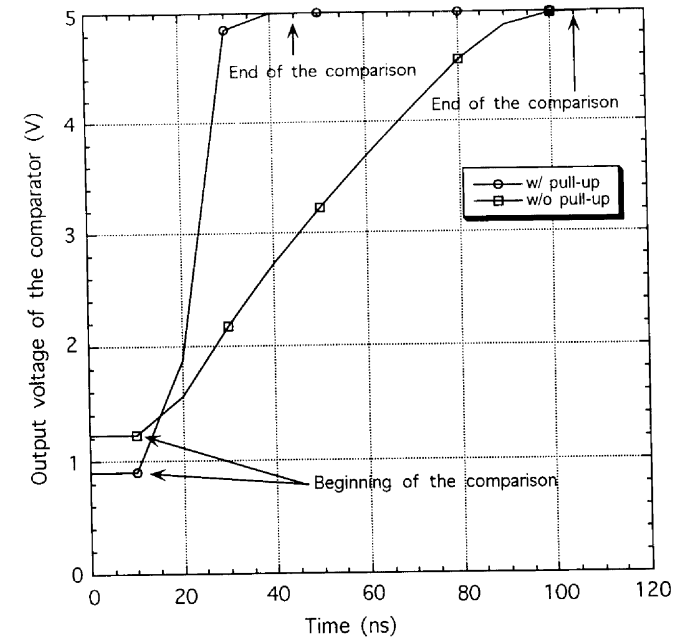
Figure 6.14.   Comparator with and without pull-up circuitry

that a simple small signal model can reveal the exponential nature of the positive feedback mechanism, though the small signal model no longer holds after a couple of time constant. The speed of this comparator can be greatly increased if the pull-up positive feedback is enabled. Figure 6.14 shows the behavior of the output voltage of the comparator after the comparison is engaged for a $0.1V$ differential input voltage. The quiescent tail current for the comparator with and without the pull-up circuit are around 50 nA and 2.5μ A, respectively. As we can see, even though the comparator with the pull-up circuit consumes 50 times less current than the comparator without the pull-up circuit, it reaches its decision 3 times faster than its counterpart.

As mentioned before, a buffer inverter is needed for the comparator output. In the delta-sigma modulator, the comparator is followed by a D-latch. If the output is not buffered, the output voltage will take a non-logic value determined by Equation 6.26. This non-logic value (neither V_{DD} nor V_{SS}) will cause the D-latch to consume static power during the reset phase. To circumvent this problem, a simple clocked inverter is needed as shown in Figure 6.15. During the comparison phase, both buffers serve as two inverters. During the reset phase,
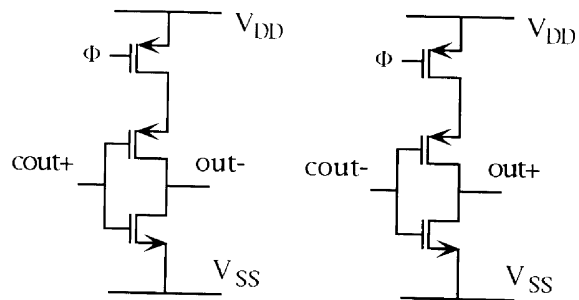
Figure 6.15.   A buffer circuit for the comparator output

the clocked transistor in the inverter turns off. Both of the buffer output V_{out+} and V_{out-} become logic low. Therefore, there is no static power consumed in the succeeding D-latch. The device sizes for all transistors in the comparator is summarized in Table 6.3.

Table 6.3.   Device sizes for the comparator

	M_1	M_2	M_3	M_4	M_5	M_6
W	100μm	100μm	8μm	8μm	16μm	4μm
L	4μm	4μm	24μm	24μm	24μm	10μm
	M_7	M_8	M_9	M_{10}	M_{11}	M_{12}
W	16μm	4μm	4μm	4μm	4μm	4μm
L	24μm	4μm	4μm	10μm	10μm	4μm

6.6   DIGITAL CONTROL AND CLOCK

The two-phase nonoverlapping clock generation circuitry is straightforward in a delta-sigma modulator and is essentially the same as the circuitry used in a switched-capacitor filter. The circuit is shown in Figure 6.16. The circuit is constructed such that not only phases Φ_1 and Φ_2 are nonoverlapping but also their complementary phases are nonoverlapping too. The delaying of these two phases can be achieved by passing them through an even number of inverters. The digital control circuit is depicted in Figure 6.17. It generates the switching signals Φ_{r1} and Φ_{r2} to control the cross sampling of the differential reference voltage.
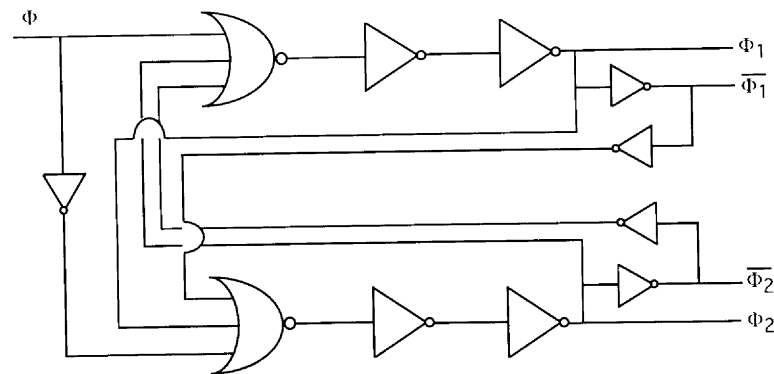
Figure 6.16.   Circuit schematic for the two-phase nonoverlapping clock generation
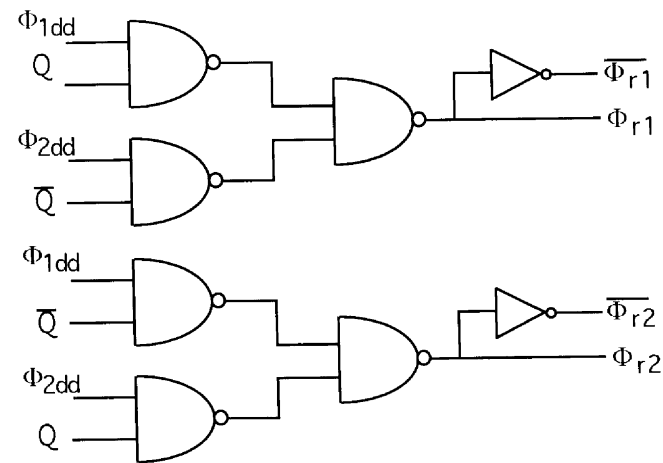
Figure 6.17.   Circuit schematic for the digital feedback control circuit

6.7   EXPERIMENTAL RESULTS

Two first order delta-sigma modulator implementations of Figure 6.1 have been integrated in a $2\mu m$ CMOS technology. The whole chip operates from a 5V power supply. A microphotograph of the chip is shown in Figure 6.18. The whole chip includes one modulator with a class A folded cascode opamp and the other with a class AB folded cascode opamp. As to the class AB folded cascode opamp, an additional circuitry is added to the class A version to boost the output current when a large input signal is encountered. The rest of the circuit in the modulator is kept the same.

The purpose of this implementation is to demonstrate the principle of the first order delta sigma modulator. For an arbitrary DC input, the average of the digital output approaches the input. However, if the DC input is an integer divisor of the quantization level, then theoretically the average of the digital output should be equal to the input exactly. In the test setup, the one bit digital output from the modulator was transmitted to a Tektronix digitizing oscilloscope for the different input DC values. The MATLAB simulations and the measurement data are shown for each input value respectively. It is well known that for a first order delta-sigma modulator, the analog input can be calculated from its digital output plus an error term as shown below.

$$X = \frac{C_1(N^+ - N^-)}{C_2(N^+ + N^-)} + \frac{C_t(V_{of} - V_{oi})}{C_2(N^+ + N^-)} \tag{6.30}$$

where C_1, C_2 and C_t are the input capacitor, reference feedback capacitor and integrating capacitor respectively. The voltage V_{of} and V_{oi} are the final and initial voltage at the output of the integrator when the conversion starts and ends. The number N^+ and N^- are the number of "1"s and "0"s in one conversion period. In our design, C_1 is chosen to be equal to C_2. The second term on the right hand side of Equation 6.30 makes up the conversion error term and it is highly correlated to the input. However, if the input DC signal takes an integer decimal value, the modulator output exhibits a periodic pattern and the error term vanishes. The input value can be obtained by simply calculating the ratio of the difference and sum of N^+ and N^- in one pattern period. For example, in Figure 6.21 and Figure 6.22, there are nine "ones" and seven "zeros" in one pattern period. The input value is then evaluated as

$$X = \frac{9 - 7}{9 + 7} = \frac{1}{8} \tag{6.31}$$

The modulator outputs have been recorded for the input DC signal equal to zero, one-eighth, one-quarter and three quarter of the reference voltage in Figure 6.19, Figure 6.21, Figure 6.23 and Figure 6.25. As we can see, excellent

agreement exists between chip measurements and their corresponding MATLAB simulations.

6.8   CONCLUSIONS

The design of a first order delta-sigma modulator in $2\mu m$ CMOS technology has been described in this chapter. After the system overview, the design considerations for each building block are discussed in detail. The experimental siderations for each building block are discussed in detail. The experimental delta-sigma modulator has been realized using switched-capacitor circuits and employs a nonoverlapping two phase clock. We have chosen a fully differential architecture to provide a larger signal swing, immunity to noise, power supply rejection, common mode signal rejection and suppression of nonlinearities from capacitors and the opamp. A folded-cascode opamp is chosen to provide good power-speed performance. A regenerative comparator without offset compensation is chosen to serve as the one-bit quantizer of the modulator.

The performance of the modulator is assessed by a comparison between MATLAB simulation and measurement data. A periodic pattern in the output is expected to occur for an input being equal to an integer divisor of quantization level. This pattern has been observed experimentally and agrees well with the theoretical evaluation (Matlab simulation). This validates our design considerations.
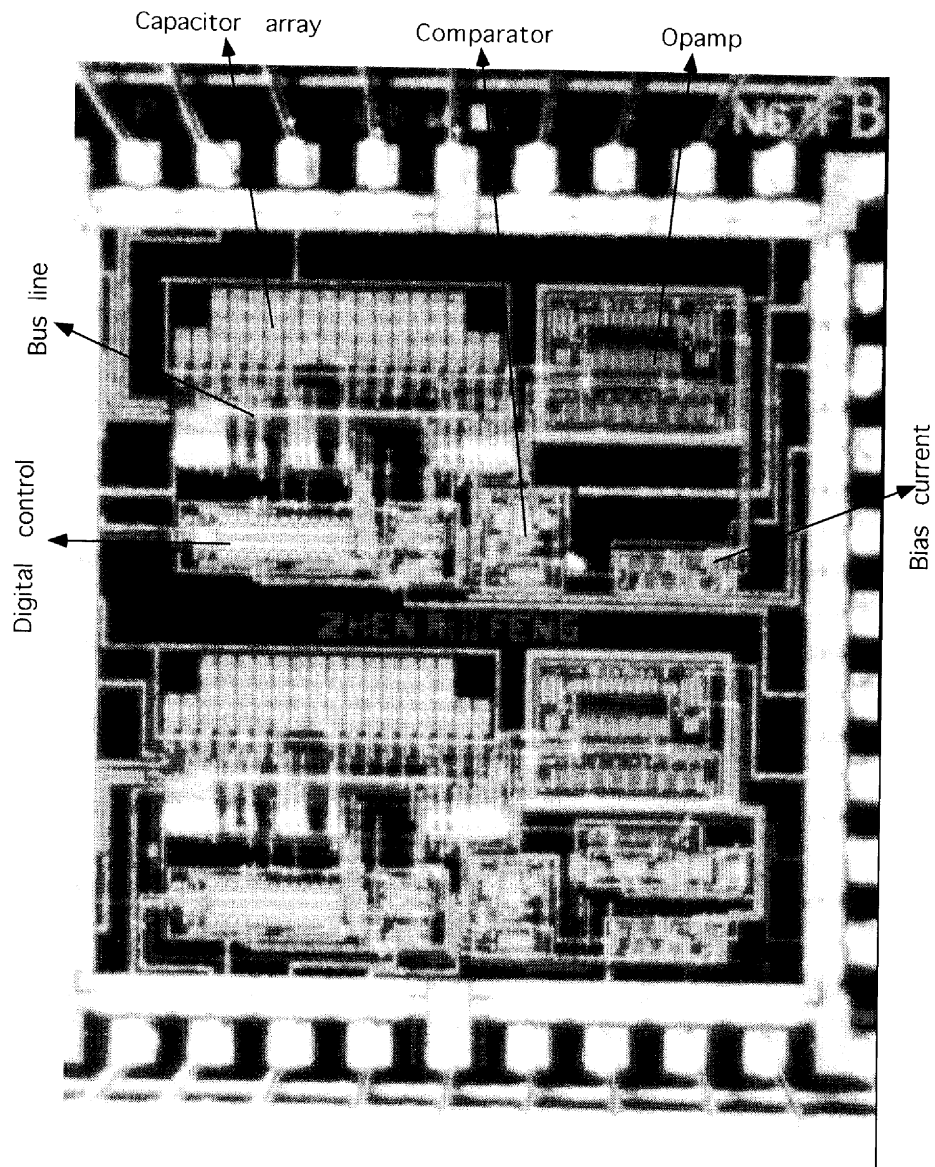
Figure 6.18.   Microphotograph of a two channel first order $\Delta\Sigma$ modulator
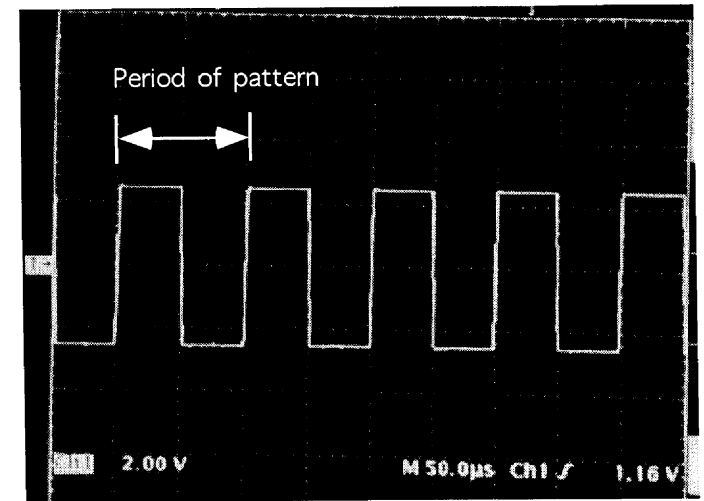
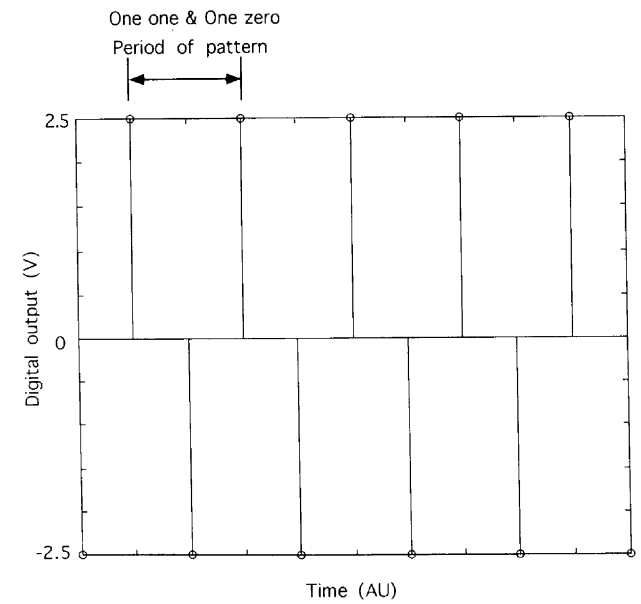**Figure 6.19.**   Modulator output for the analog input with zero magnitude

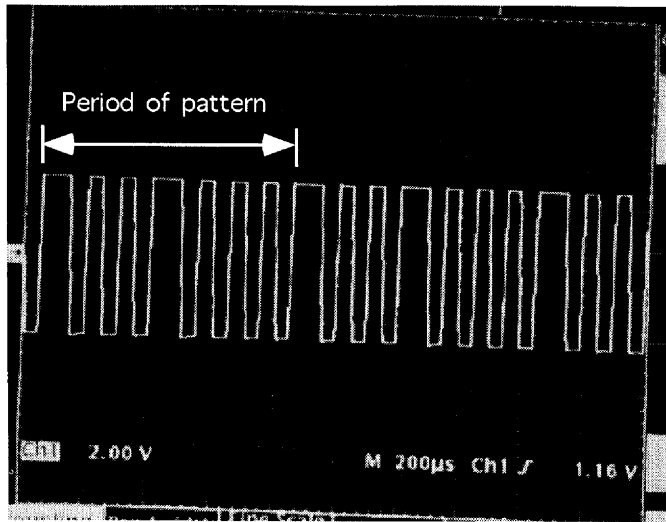**Figure 6.20.**   Matlab simulation for the modulator output

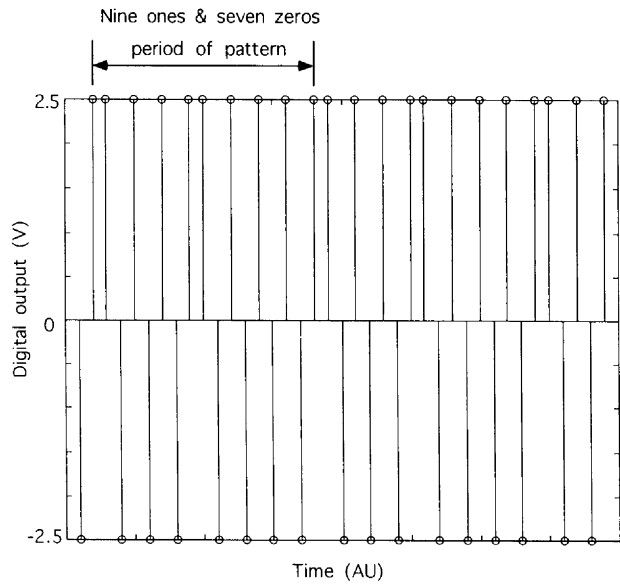**Figure 6.21.**   Modulator output for the analog input with 1/8 reference voltage

Figure 6.23.   Modulator output for the analog input with 1/4 reference voltage
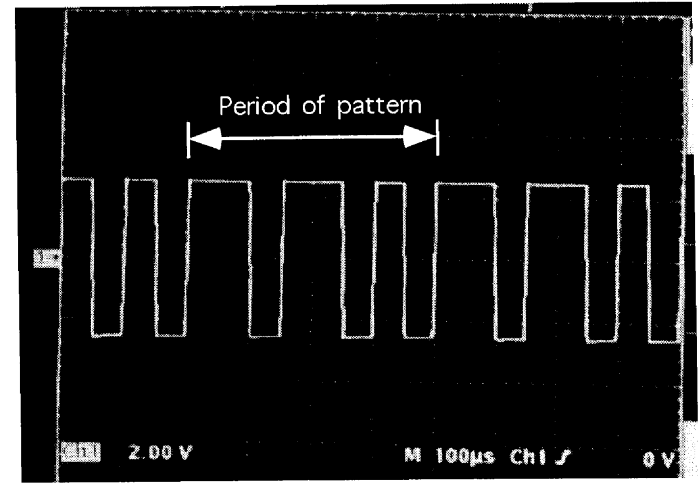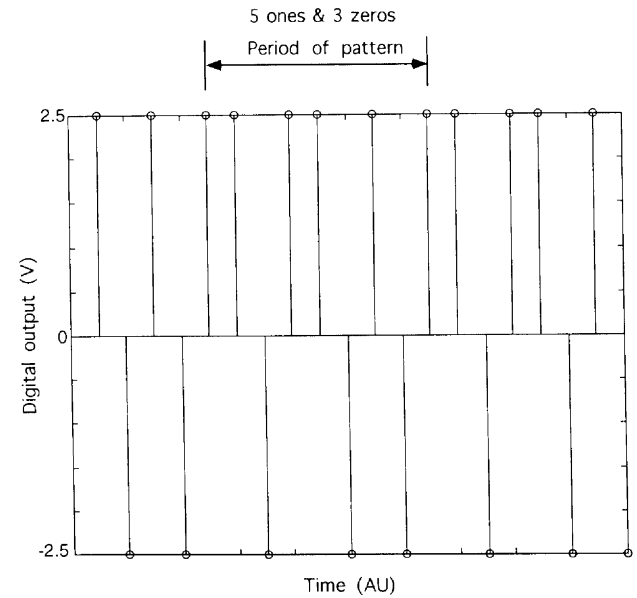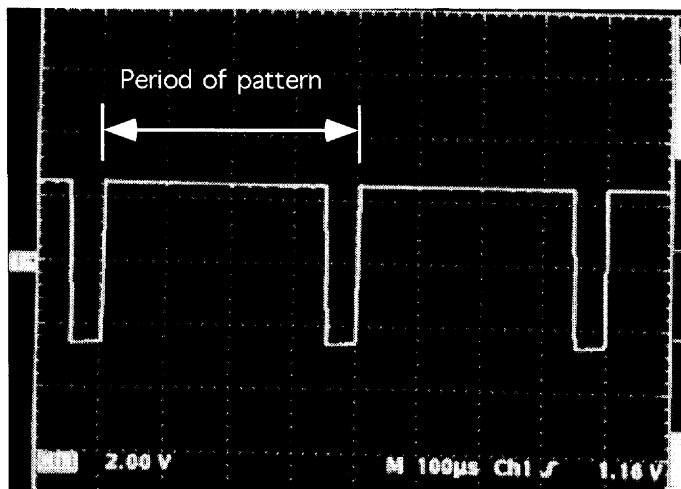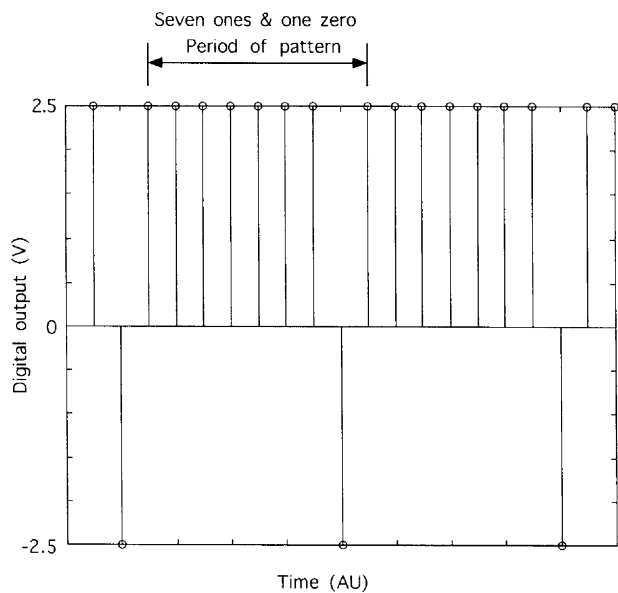

Figure 6.22.   Matlab simulation for the modulator output

Figure 6.24.   Matlab simulation for the modulator output

Figure 6.25.   Modulator output for the analog input with 3/4 reference voltage

Figure 6.26.   Matlab simulation for the modulator output

7   CONCLUSIONS

In this book we have presented a methodology for the optimal design of modulators for oversampled converters. The optimization is made possible by carefully examining two important aspects of the modulator: power consumption and nonlinearity. Experimental chips have been fabricated to validate both the nonlinear analysis and the principle of the new class AB opamp. The validity of our power analysis has been verified by experimental work done by other researchers. This chapter summarizes the main contributions of our work and some closing remarks.

7.1   CONTRIBUTION

The scientific contribution of this work can be summarized as follows:

- Power analysis
  A power analysis framework is developed to calculate and compare the power consumption for various opamp topologies used in modulators for oversampled converters. The method is general and is applicable to all topologies.

- Nonlinearity analysis
  A nonlinearity analysis framework is developed to accommodate a wide range of nonlinear effects that occur in modulators.

- Design strategy
  Two design strategies for the modulator utilizing class A opamps are proposed. The first one is suitable for the design without nonlinearity consideration. By choosing the proper strategy, substantial power saving can be realized when implementing highly linear delta-sigma modulators.

- Verification
  The nonlinear settling in the nonlinearity analysis is experimentally verified via a careful selected and well-controlled design.

- Circuit design
  A novel class AB opamp is proposed and experimentally validated.

7.2 CONCLUSIONS

In this work we have shown that the optimal design of modulators for oversampled converters can be realized on three counts: opamp selection, nonlinearity understanding and design strategy. The choice in each count is application specific depending on whether it is for high resolution, high linearity or medium resolution/linearity but low power application. For the opamp selection, a decision must be made between class A and class AB opamps. The class AB opamps consume less power at the cost of the larger nonlinearity. For the nonlinearity analysis, an estimate of the magnitude of the nonlinear errors in two different regions should be made prior to the design because it directly affects the choice of the design strategy. In fact, these three areas interact with each other and a careful examination of them in an integrated way will result in considerable power reduction. Measurement results from fabricated ICs confirm that as much as 40 % power reduction is possible before there is any noticeable increase in the delta-sigma converter nonlinearity error.

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