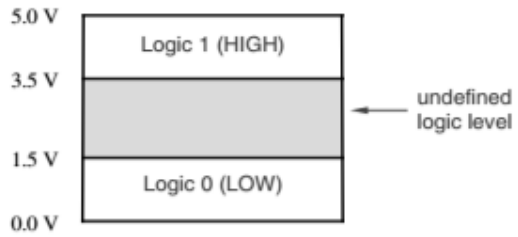
Electrónica III

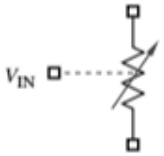
Curso 2021

Estructura y Comportamiento de los Circuitos Digitales

ITBA

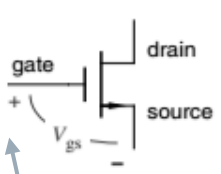
CMOS vs TTL





Podemos pensar al transistor MOS como una resistencia controlada por tensión
En un circuito digital el transistor MOS trabaja solo en dos modos:

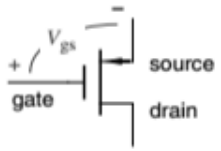
Corte : R = 1 MOhm
Saturación: R = 10 Ohm



Voltage-controlled resistance:
increase V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \geq 0$

Circuit symbol for
an n-channel MOS
(NMOS) transistor.

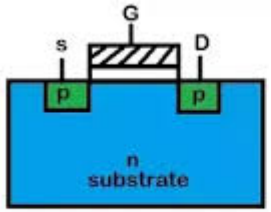


Voltage-controlled resistance:
decrease V_{gs} ==> decrease R_{ds}

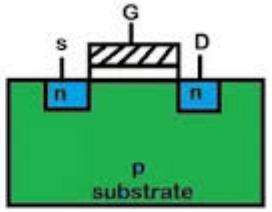
Note: normally, $V_{gs} \leq 0$

Circuit symbol for a
p-channel MOS
(PMOS) transistor.

I gate = I Leakage



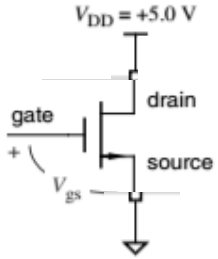
pmos



nmos

Tensión entre gate - source : $V_{gs} = V_g - V_s$

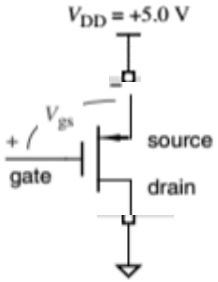
Resistencia entre drain y source: R_{ds}



Si $V_g > V_s$, o sea $V_g - V_s = V_{gs} \geq 0$ => R_{ds} disminuye su valor

Si $V_g = V_s$: $V_{gs} = 0$ => $R_{ds} \approx 10$ MΩ

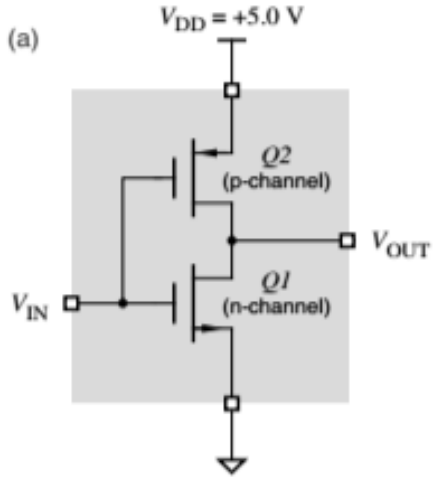
Si $V_g > V_s$: $V_{gs} = V_{DD} = 5$ Volt => $R_{ds} \approx 10$ Ω



Si $V_g < V_s$, o sea $V_g - V_s = V_{gs} \leq 0$ => R_{ds} disminuye su valor

Si $V_g = V_s$: $V_{gs} = 0$ => $R_{ds} \approx 10$ MΩ

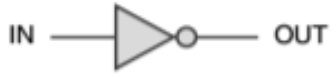
Si $V_g < V_s$: $V_{gs} = V_{DD} = -5$ Volt => $R_{ds} \approx 10$ Ω

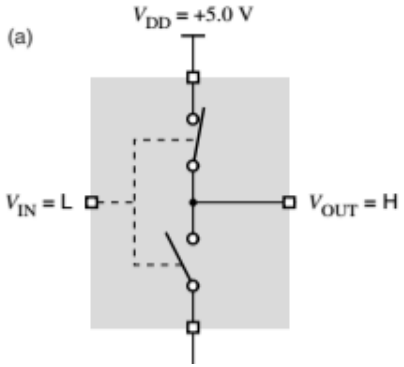


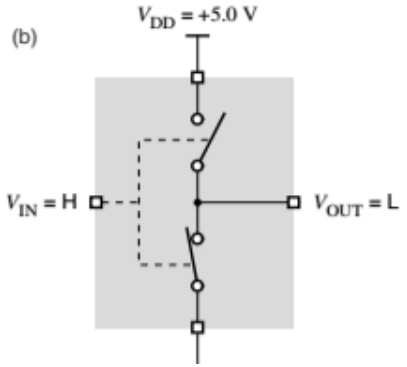
(b)

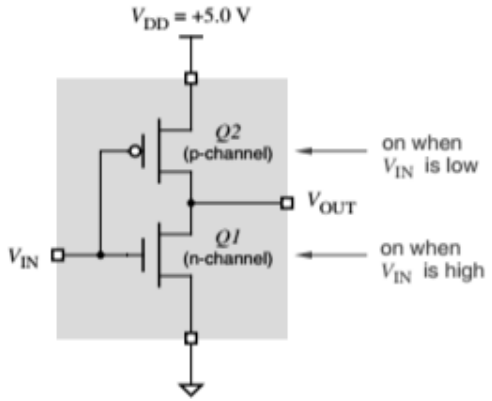
V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

(c)

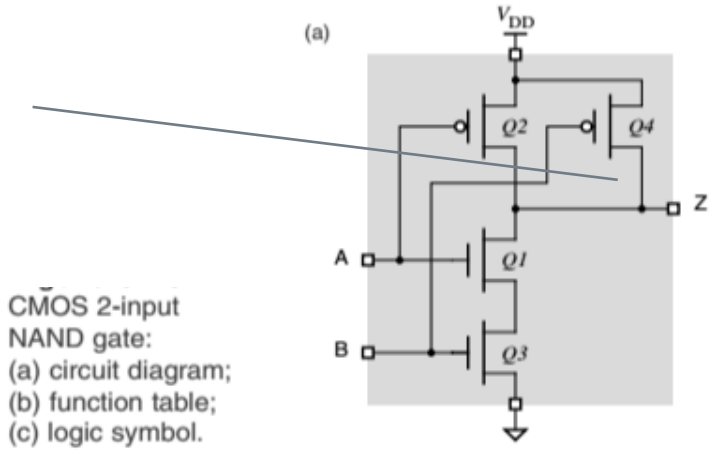








Una compuerta NAND o NOR de k entradas, usa k transistores Canal n y k transistores Canal p

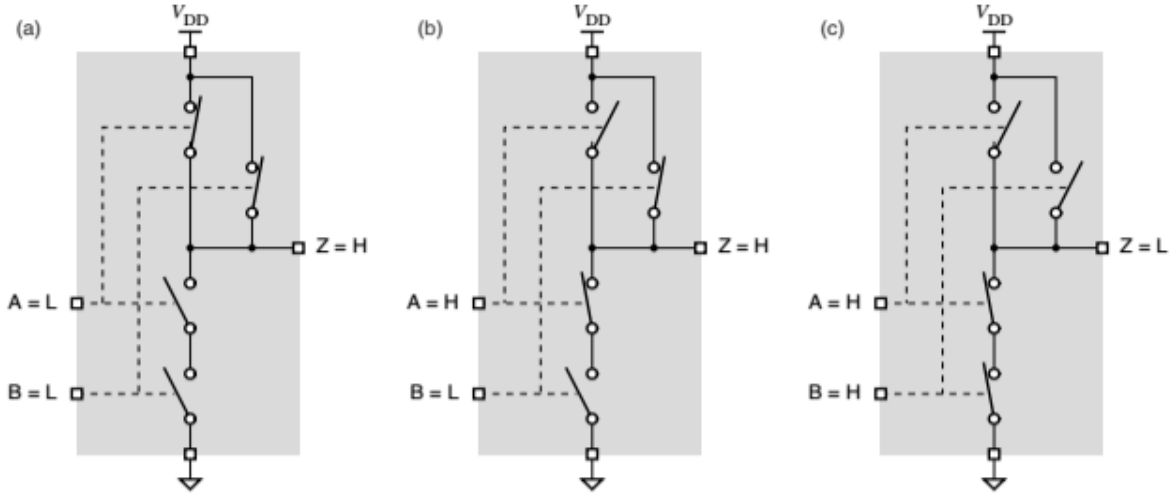


(b)

A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

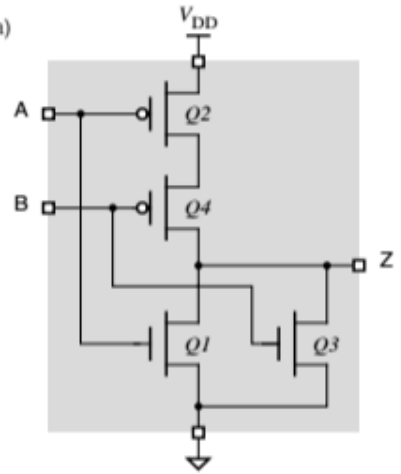
(c)

CMOS 2-input NAND gate: (a) circuit diagram; (b) function table; (c) logic symbol.



Switch model for CMOS 2-input NAND gate: (a) both inputs LOW; (b) one input HIGH; (c) both inputs HIGH.

(a)



(b)

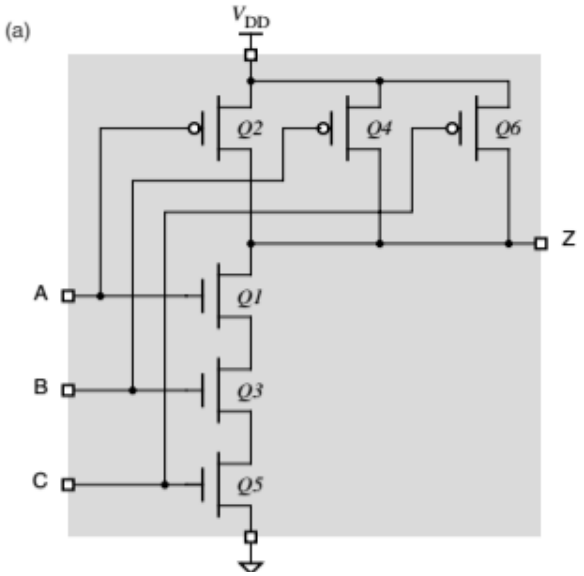
A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)

CMOS 2-input NOR gate:
(a) circuit diagram;
(b) function table;
(c) logic symbol.

Fan In: Número de Entradas de una Compuerta

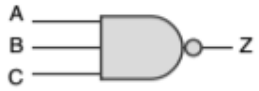
(a)



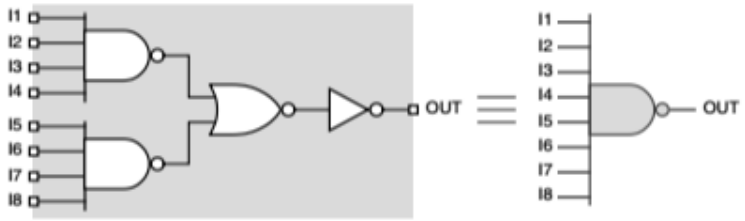
(b)

A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	L	off	on	off	on	off	on	H
L	L	H	off	on	off	on	on	off	H
L	H	L	off	on	on	off	off	on	H
L	H	H	off	on	on	off	on	off	H
H	L	L	on	off	off	on	off	on	H
H	L	H	on	off	off	on	on	off	H
H	H	L	on	off	on	off	off	on	H
H	H	H	on	off	on	off	on	off	L

(c)



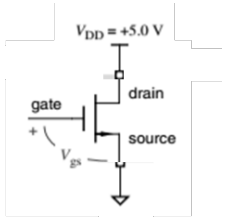
CMOS 3-input NAND gate: (a) circuit diagram; (b) function table; (c) logic symbol.

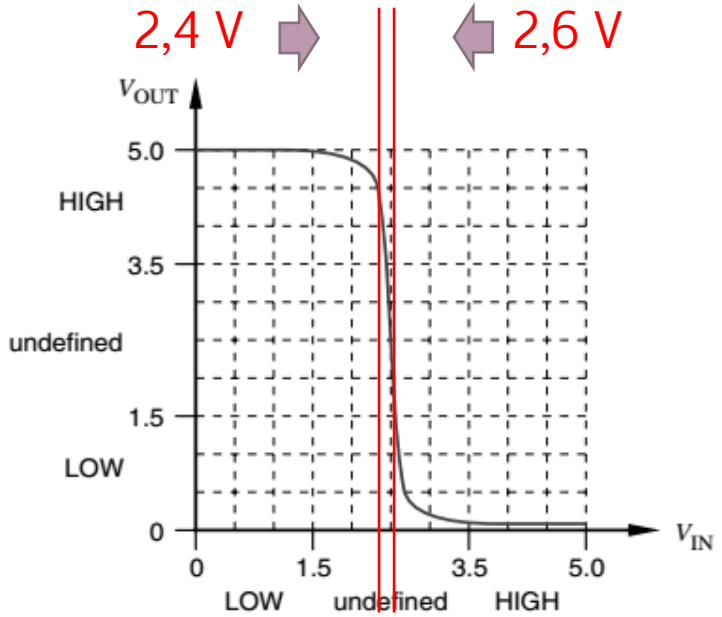


Logic diagram equivalent to the internal structure of an 8-input CMOS NAND gate.

Comportamiento Estático

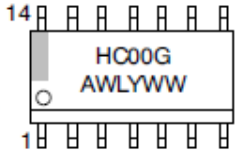
ITBA



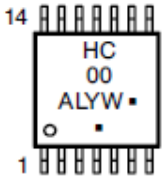


5,0 V	*3,3 V*			*5,0 V*	*3,3 V*
NMH = 1,4 V	0,9 V	Vcc – 0,1 V →	V_{CC}		
			V_{OHmin}	4,9 V	3,2 V
			HIGH		
			High-state DC noise margin ←		
			V_{IHmin}	3,5 V	2,3 V
		$0.7\ V_{CC}$			
			ABNORMAL		
			V_{ILmax}	1,5 V	1 V
NML = 1,4 V	0,9 V	$0.3\ V_{CC}$			
			LOW		
			Low-state DC noise margin ←		
		GND + 0,1 V →	V_{OLmax}	0,1 V	0,1 V
		0			

SOIC-14
D SUFFIX
CASE 751A

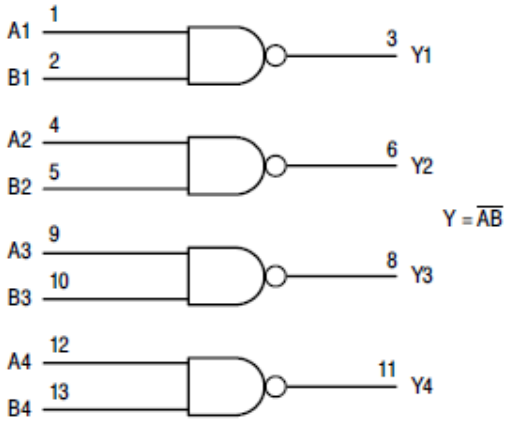


TSSOP-14
DT SUFFIX
CASE 948G



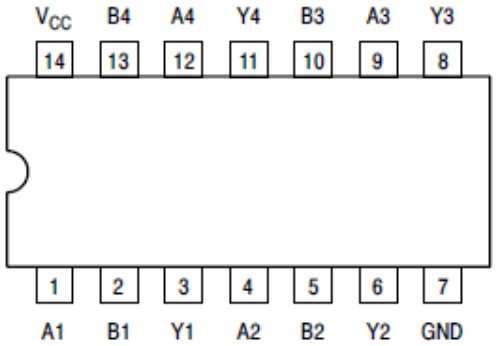
74HC00

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

Pinout: 14-Lead Packages (Top View)



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 s SOIC or TSSOP Package	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

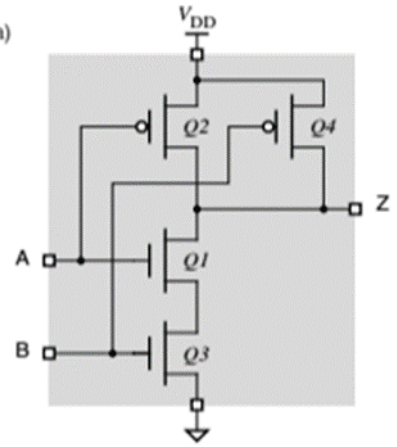
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		− 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

6.2 ESD Ratings

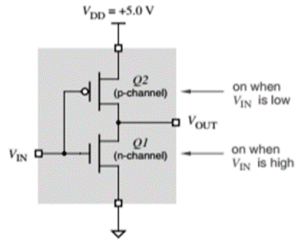
			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

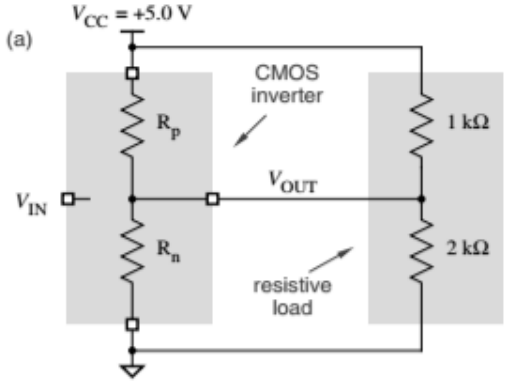
(a)

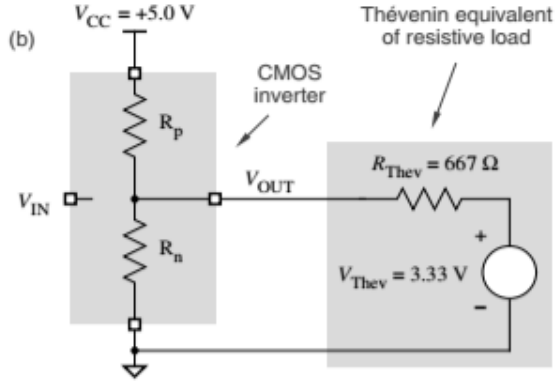


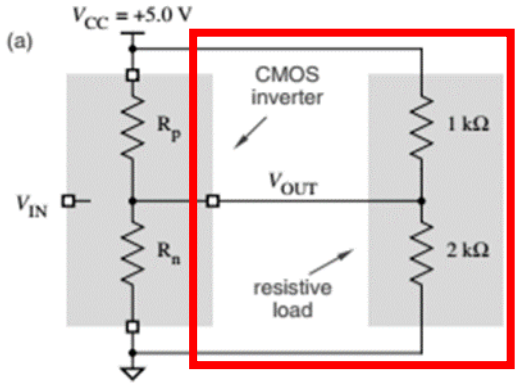
DC CHARACTERISTICS (Voltages Referenced to GND)

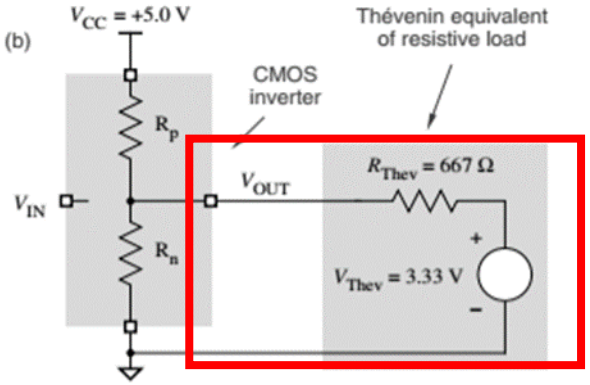
Symbol	Parameter	Condition	V_{CC} (V)	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1V or V_{CC} -0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1V or V_{CC} - 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4mA$ $\|I_{out}\| \leq 4.0mA$ $\|I_{out}\| \leq 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4mA$ $\|I_{out}\| \leq 4.0mA$ $\|I_{out}\| \leq 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	6.0	2.0	20	40	μA



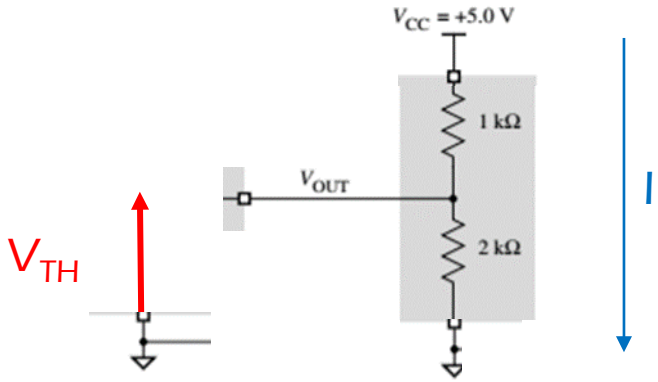


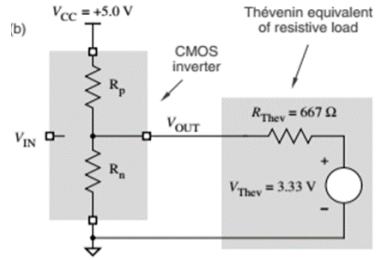






Como calculamos el circuito equivalente de Thevenin?



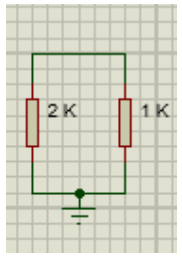


$$5V - I \times 1K\Omega - I \times 2\ K\Omega = 0$$

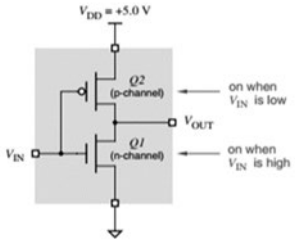
$$I = \frac{5\ V}{1\ K\Omega + 2\ K\Omega} = 1{,}67\ mA$$

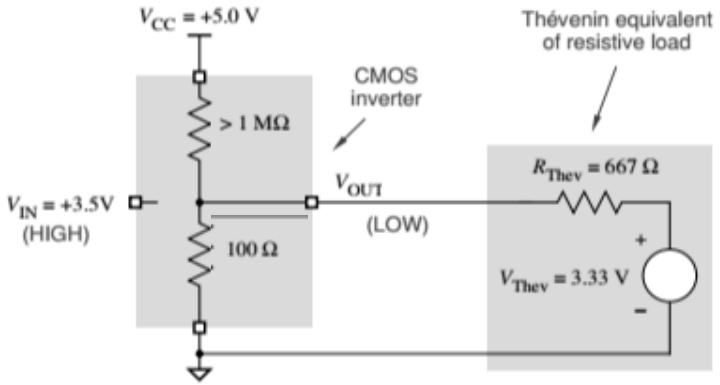
$$V_{TH} = 1{,}67\ mA \times 2\ K\Omega = 3{,}33\ V$$

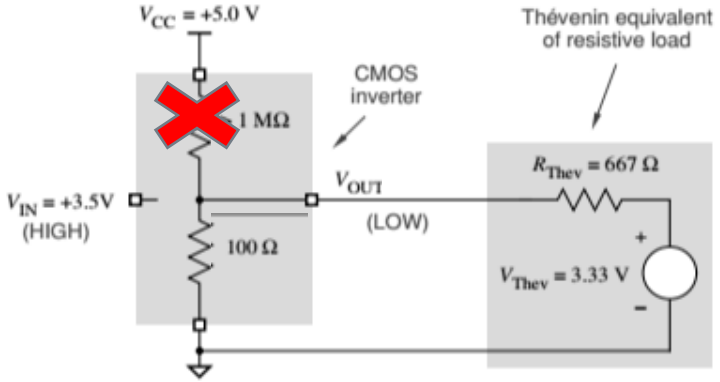
RV_{TH}



$$R_{TH} = \frac{2K\Omega\ x\ 1K\Omega}{1\ K\Omega + 2\ K\Omega} = 667\ \Omega$$







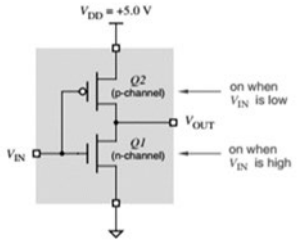
V_{OUT} = 3,33 V x (100 / (100 + 667)) = 0,43 V

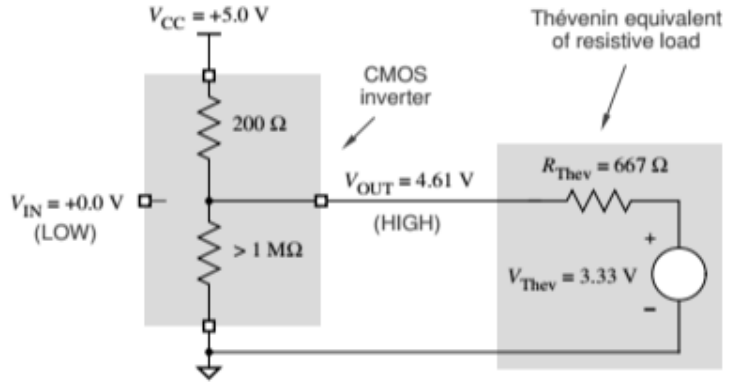
3,33 V – I x 667 Ω - I x 100 Ω = 0

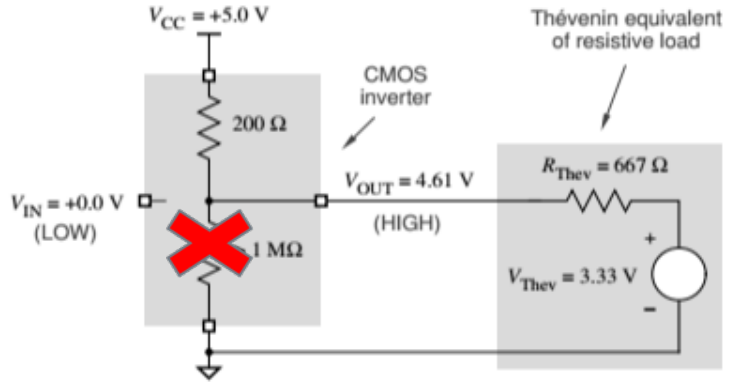
I = 3,33 V / (667 + 100) = 4,34 mA

Vout = 4,34 mA x 100 Ω = 0,43 V

V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \leq$ 20μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \leq$ 2.4mA	3.0	0.26	0.33	0.40	
		$\lvert I_{out}\rvert \leq$ 4.0mA	4.5	0.26	0.33	0.40	
		$\lvert I_{out}\rvert \leq$ 5.2mA	6.0	0.26	0.33	0.40	





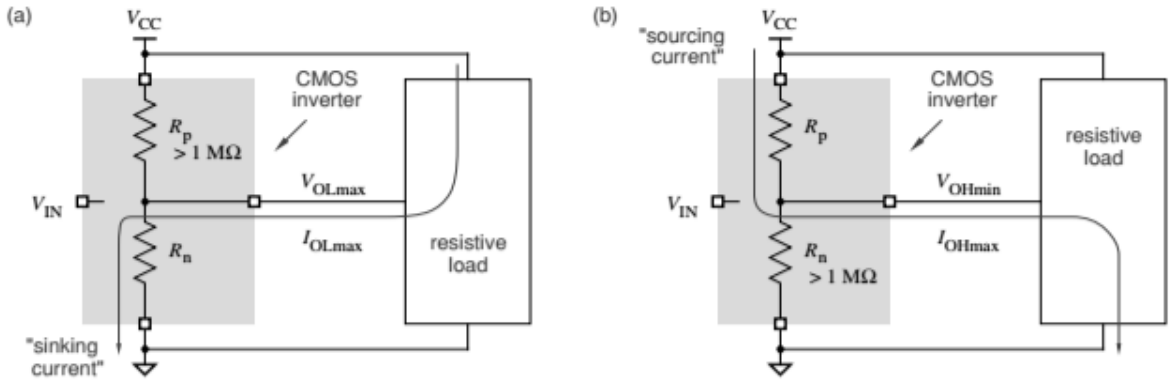


5 V – I x 200 Ω - I x 667 – 3,33 V = 0

I = 1,92 mA

Vout = 5 V – 200 Ω x 1,92 mA = 4,61 V

V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \leq 20\mu A$		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL}	$\lvert I_{out}\rvert \leq 2.4mA$	3.0	2.48	2.34	2.20	
			$\lvert I_{out}\rvert \leq 4.0mA$	4.5	3.98	3.84	3.70	
			$\lvert I_{out}\rvert \leq 5.2mA$	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level	V_{in} = V_{IH} or V_{IL}		2.0	0.1	0.1	0.1	V



$$R_{p(on)} \approx \frac{V_{DD} - V_{OHminT}}{|I_{OHmaxT}|}$$

$$R_{n(on)} \approx \frac{V_{OLmaxT}}{I_{OLmaxT}}$$

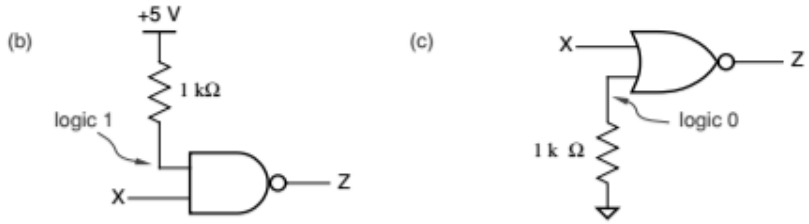
DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	Guaranteed Limit -55 to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1V or V_{CC} -0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1V or V_{CC} - 0.1V $\|I_{out}\| \leq 20\mu A$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} =V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4mA$ $\|I_{out}\| \leq 4.0mA$ $\|I_{out}\| \leq 5.2mA$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20\mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4mA$ $\|I_{out}\| \leq 4.0mA$ $\|I_{out}\| \leq 5.2mA$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0µA	6.0	2.0	20	40	µA

Fanout = Iout / Iin = 20 uA / 1 uA = 20

Fanout = Iout / Iin = 4.0 mA / 1 uA = 4000

Conexión de Pines no utilizados



6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	