Paralleling power MOSFETs in high current applications

Effect of MOSFET parameter mismatch on current and power dissipation imbalance

About this document

Scope and purpose

Due to continuously growing need for higher power in low voltage applications which are typically supplied with less than 200 V DC, MOSFETs with the lowest possible conduction resistance $R_{DS(on)}$ are in high demand. In many applications, a single MOSFET is not sufficient to carry the necessary current, which poses a demand for paralleling of MOSFETs in order to reduce the conduction losses as well as reducing the operating temperature and improving the efficiency of a power converter.

With a need for paralleling of MOSFETs in a power converter, the design engineer is faced with a topic of uneven current sharing and imbalance of power dissipation between paralleled MOSFETs due to fact that they are not perfectly synchronized during the turn-on and turn-off processes.

This application note highlights the MOSFET parameters which are playing an important role in current sharing and quantifies the additional power loss incurring in a MOSFET which carries more current due to current sharing imbalance.

Intended audience

Power electronics design engineers who are paralleling MOSFETs and need to quantify the margin which is required for a non-ideal case of current sharing between them.

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1 Introduction

When several MOSFETs are connected in parallel in order to increase the overall system current capability, it is often assumed that the current is equally distributed or equally shared between the paralleled devices. However, there are several characteristics of the PCB layout and several MOSFET parameters that influence this distribution and cause imbalance to the current sharing whenever the parameters are not perfectly matched, or if the layout is not perfectly symmetrical. Investigation of the layout effects on current sharing is out of scope of this paper, but other literature is available addressing also this topic [1], [2].

Imbalance to the current sharing means that some devices will conduct higher than average currents, resulting in higher than average power dissipation and consequently higher maximum component temperature with regard to the temperatures resulting from estimates that assume perfect current sharing and equal component power dissipation.

The increased power dissipation and the excess component temperatures will limit the maximum system performance, hence demand for certain amount of oversizing. In other words – additional MOSFETs need to be added in parallel, in order for the system to meet specific requirements.

The resulting distribution of average power dissipation between the paralleled MOSFETs depend on the current distribution, but is also affected by the nature of the output load current and on the switching modulation being applied.

In motor drives applications a sinusoidal output current is the ouput of each half bridge and the resulting power dissipation differs from DC applications. SVM and SPWM are the typical modulation methods of driving the sinusoidal output currents.

This paper aims to explain how to size the system considering not only “typical” (i.e. ideal) performance, but also realistic circumstances caused by inevitable component parameter variation.

2 Circuit description

The circuit used for this research, is a half bridge topology with MOSFETs connected in parallel. Initially, the current sharing is examined for 2 MOSFETs in parallel as shown in **Figure 1**. The final results are then also shown for the system with 4 MOSFETs and 6 MOSFETs in parallel.

The performance of the half bridge in **Figure 1** is simulated for a continuous PWM (*f = 10 kHz* and *D.C. = 50 percent*), while driving a constant load current I_L. The load current is swept up to 100 A per MOSFET.

The simulation model includes parasitic inductances and resistances of all the interconnections (not shown in the simplified schematic) of a PCB layout optimized for symmetrical current sharing, therefore the model exhibits an idealized symmetry of the PCB layout. Thus, all current imbalance in the simulation is caused by the mismatch of the MOSFET parameters, or in other words, with identical MOSFET parameter settings, the resulting switching waveforms are perfectly symmetrical or equal at all the MOSFETs.

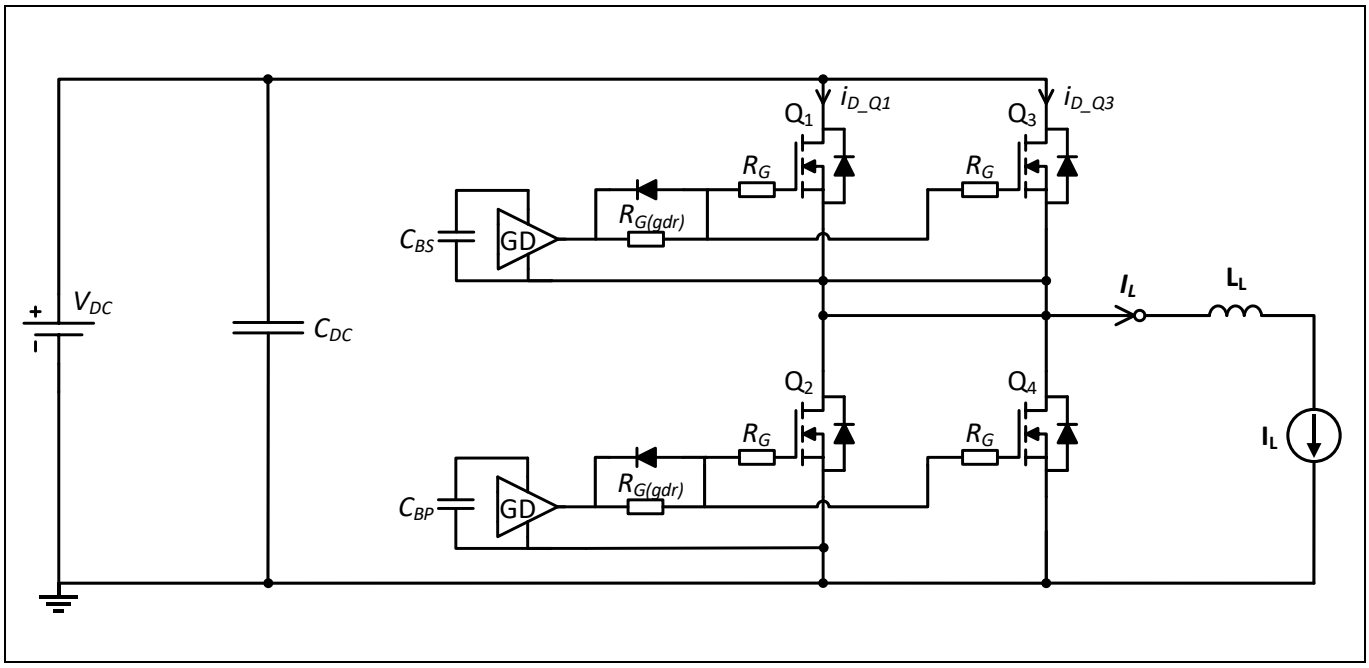

Figure 1 Simplified half bridge schematic

The circuit parameters are shown in **Table 1**.

Table 1 Circuit parameters: 2 MOSFETs in parallel

Parameter	Symbol	Value
Gate resistor – gate driver side	$R_{G(gdr)}$	12 Ω
Gate resistor – MOSFET side	R_G	22 Ω
DC bus capacitance	C_{DC}	1.65 mF
DC bus supply voltage	V_{DC}	48 V
Gate driver supply voltage	V_G	15 V
MOSFET case temperature	T_C	25 °C

Circuit description

The circuit using 2 MOSFETs in parallel is used initially to demonstrate the current imbalance and to explain the extraction of relevant data. The process is then repeated with 4 and with 6 MOSFETs connected in parallel, in order to compare the effects with regard to system size (extent of paralleling).

When paralleling higher number of MOSFETs, certain circuit parameters have to be adjusted in order to maintain the same condition with regards to a single MOSFET in the parallel chain. Simply put, in a perfectly balanced setup, the load at each MOSFET needs to be the same regardless of the system size.

This implies that if the load current condition is swept up to 200 A (100 A per MOSFET) for the 2-in-parallel model, it needs to reach 400 A for the 4-in-parallel model. The load current condition as given in the result charts is therefore normalized by per number of MOSFETs. The normalized load current is defined by the following equation:

$$I_{L\_p.NQ} = \frac{I_L}{N_Q}$$

Where:

- I_L → Absolute value of load current
- N_Q → Number of MOSFETs connected in parallel

For example, if the normalized value of load current is 100 A, the actual load current is different depending on the setup that is represented:

- 2 MOSFETs in parallel:
  $I_{L\_p.NQ}$ = 100 A → I_L = 200 A
- 4 MOSFETs in parallel
  $I_{L\_p.NQ}$ = 100 A → I_L = 400 A
- 6 MOSFETs in parallel
  $I_{L\_p.NQ}$ = 100 A → I_L = 600 A

In order to maintain the same condition on the bus voltage (assuming relatively high supply source inductance), the DC bus capacitance has to be increased. The gate driving circuit also has to be adjusted, as well as some parasitic parameters. The adjustments are visible when comparing **Table 1**, **Table 2** and **0**.

Table 2 Circuit parameters: 4 MOSFETs in parallel

Parameter	Symbol	Value
Gate resistor – gate driver side	$R_{G(gdr)}$	6 Ω
Gate resistor – MOSFET side	R_G	22 Ω
DC bus capacitance	C_{DC}	3.3 mF
DC bus supply voltage	V_{DC}	48 V
Gate driver supply voltage	V_G	15 V
MOSFET case temperature	T_C	25 °C

Table 3 Circuit parameters: 6 MOSFETs in parallel

Parameter	Symbol	Value
Gate resistor – gate driver side	$R_{G(gdr)}$	4 Ω
Gate resistor – MOSFET side	R_G	22 Ω
DC bus capacitance	C_{DC}	4.95 mF
DC bus supply voltage	V_{DC}	48 V
Gate driver supply voltage	V_G	15 V
MOSFET case temperature	T_C	25 °C

With regards to results, naming of MOSFETs uses odd numbers for high side MOSFETs and even numbers for low side MOSFETs. The conditions are selected in a way that MOSFET Q_1 represents the outlier with the harshest condition, making it the primary D.U.T. (device under test).

3 Current sharing parameters

There are several parameters that influence how current is distributed among the paralleled devices in a switching application like the half bridge. The overview in **Table 4** compares the effects of the most significant parameters to current sharing. The conclusions are drawn from a preliminary investigation comparatively evaluating the parameter influence to current imbalance. Additional literature, which also considers layout is listed in references [1].

The “imbalance behavior” column in **Table 4** describes the qualitative effect of a particular parameter mismatch to power dissipation. It describes how power dissipation at the corresponding MOSFET is affected, when the value of the parameter in question is reduced at this MOSFET (opposite behavior applies when the value is increased). The “comparison” column compares the mismatch quantitatively.

Table 4 Parameters most significant to current sharing

Parameter		Imbalance behavior: effect of parameter value reduction to the corresponding MOSFET	Comparison
Total gate resistance	$R_{G(tot)}$	**Increase** of power dissipation at turn ON **Decrease** of power dissipation at turn OFF	Imbalance caused by 1 percent resistance tolerance is small compared to other influences compared here Internal $R_{G(int)}$ mismatch dominates at lower external R_G (< 10 Ω), in this condition datasheet $R_{G(int)}$ value range causes medium imbalance
Gate - source capacitance	C_{GS}	**Increase** of power dissipation at turn ON **Decrease** of power dissipation at turn OFF	Datasheet value range causes medium to high imbalance
Gate - drain capacitance	C_{GD}	**Increase** of power dissipation at turn ON **Decrease** of power dissipation at turn OFF	Datasheet value range has less effect compared to R_G and C_{GS}
Gate threshold voltage	$V_{GS(th)}$	**Increase** of power dissipation at turn ON **Increase** of power dissipation at turn OFF	Datasheet value range causes high imbalance

In addition to the above mentioned effects, R_G and also g_{fs} values have a noticeable effect on current sharing in combination with the listed parameters from **Table 4**. With R_G - faster switching (smaller R_G) generally means better current sharing, whereas with g_{fs}, higher values tend to increase the imbalance.

In conclusion, the effects of the parameters are similar – faster switching of an individual MOSFET results in an increase of overall power dissipation to the faster MOSFET at turn ON, and decrease of power dissipation at turn OFF. The main difference with the $V_{GS(th)}$ parameter, is in the early turn ON and a delayed turn OFF which results in power dissipation increase for both transitions at the same component (see current waveforms in Chapter 5).

Current sharing parameters

Furthermore, increased power dissipation at the MOSFET with the lowest $V_{GS(th)}$, causing additional increase in junction temperature T_J will result in a further decrease of $V_{GS(th)}$ of the corresponding MOSFET, consequently increasing the imbalance.

The research of this application note focuses on $V_{GS(th)}$ as it was identified as the most critical for current sharing.

Note: *The conclusions of this application note refer to current sharing in particular!*
Meaning for example: the effect of gate loop inductance (L_G), is considered negligible for current sharing – this does not mean that L_G is insignificant for other switching phenomenons like causing oscillations, etc…

4 $V_{GS(th)}$ conditions

The gate threshold voltage [$V_{GS(th)}$] parameter in the datasheet states the minimum and maximum guaranteed value as well as the typical value that can be expected for the device.

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=154 µA

Figure 2 $V_{GS(th)}$ range according to datasheet parameters

The analysis of productive parts reveals that the $V_{GS(th)}$ value rage in **Figure 3** is much smaller than limits stated in the datasheet. Each lot can contain several hundreds or thousands of parts depending on the chip size and wafer size used.

This $V_{GS(th)}$ spread (minimum to maximum) between individual MOSFETs varies between technology generations, voltage classes and most importantly between manufacturers. It has been identified as one of the most distinguishing features of Infineon MOSFETs. Offering a very low variation of $V_{GS(th)}$ makes Infineon MOSFETs a perfect fit for applications requiring MOSFET paralleling.

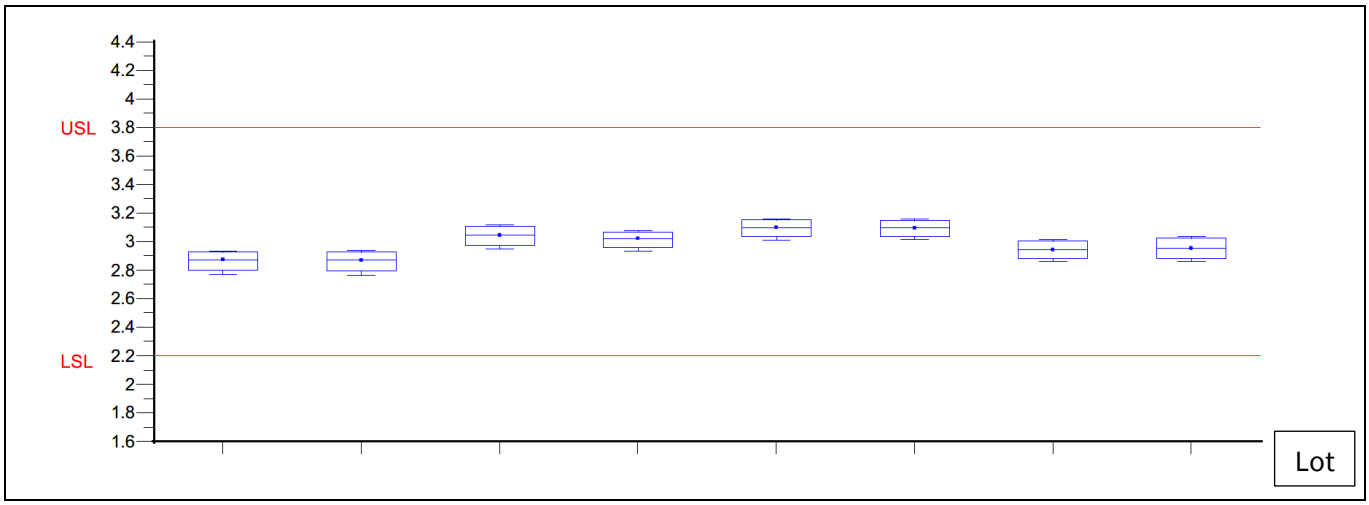

Figure 3 Example box plots of $V_{GS(th)}$ spread of multiple lots: 2.75 V to 3.15 V = 0.4 V

The examples in the following chapters quantify the current imbalance and power dissipation imbalance in a system where paralleled MOSFETs are attributed a combination of $V_{GS(th)}$ distribution, which would result in the least favorable outcome for one of the MOSFETs.

Compared to a perfectly balanced system the two additional examples consider the extreme values of the following ranges:

- worst hypothetical combination according to datasheet specification – minimum and maximum values: $\Delta V_{GS(th)}$ = 1.6 V
- worst probable combination arising from the range of an example lot: $\Delta V_{GS(th)}$ = 0.5 V

5 Imbalance caused by unmatched $V_{GS(th)}$

Chapter 2 describes the circuit used for the purpose of evaluating the effects of current imbalance. The circuit is perfectly symmetrical, which results in a perfectly distributed current between the parallel branches given that the MOSFET parameters are perfectly matched. The example of switching with perfectly matched MOSFETs or perfectly distributed current is shown in **Figure 4**. This case will serve as reference to compare with the cases of switching with mismatched parameters / imbalanced distribution of current.

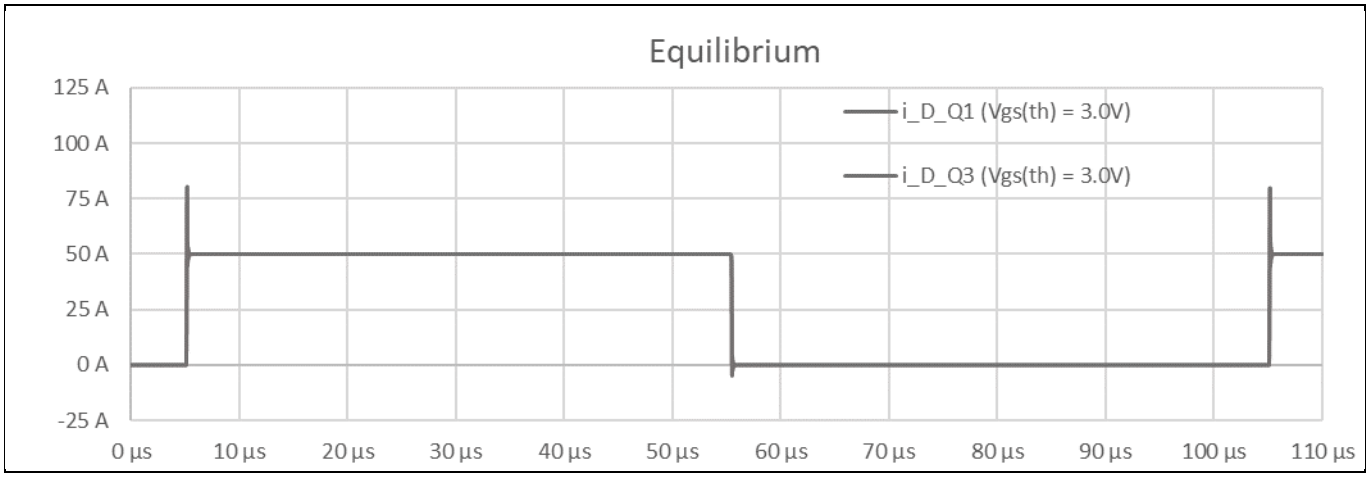

Figure 4 Simultaneous switching of two perfectly balanced paralleled MOSFETs – i.e. Equilibrium

The red and blue plots in **Figure 5** represent the same circuit, except in this case there is a big difference between the $V_{GS(th)}$ values of the high side MOSFETs. What we consider the worst case scenario is when $V_{GS(th)}$ of one MOSFET assumes the maximum value given by the datasheet, and the second one the minimum datasheet value.

$V_{GS(th)\_Q1}$ = 2.2 V

$V_{GS(th)\_Q3}$ = 3.8 V

When the gate driver starts charging both gates simultaneously, the one with the lower threshold voltage will start to turn on earlier, thus reaching a considerable I_D before the other MOSFET begins to conduct. The extent of this effect depends on the difference between the two threshold voltage values.

Note: The MOSFET with smaller $V_{GS(th)}$ will consequently conduct higher current during both turn ON and turn OFF switches.

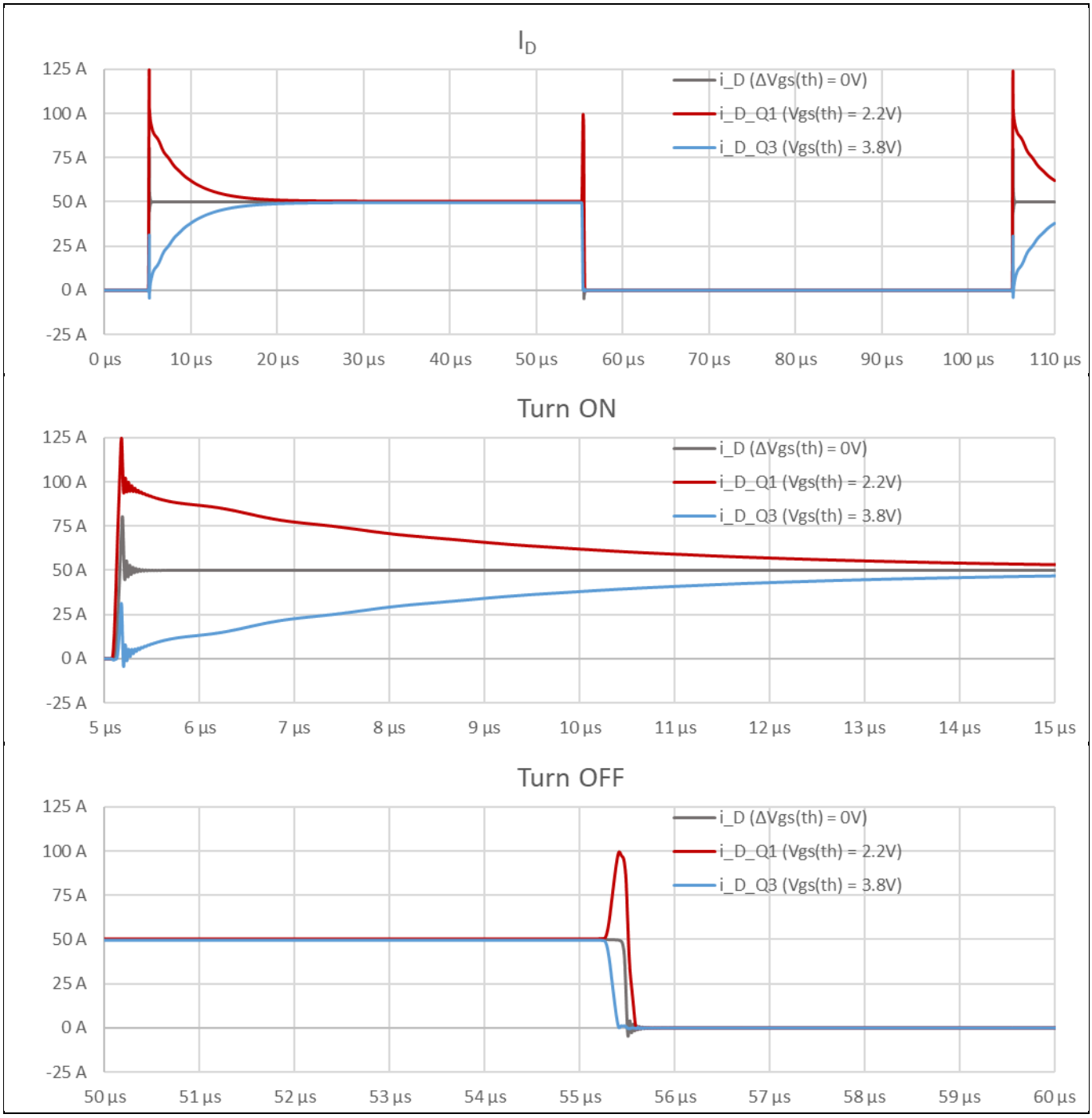

Figure 5 **Switching of two paralleled MOSFETs with highest possible difference in $V_{GS(th)}$ – Worst case mismatch according to datasheet parameters**

Another example of parallel switching with unmatched threshold voltages is shown in **Figure 6**. In this case the difference is smaller. It represents the biggest possible mismatch arising from the spread of $V_{GS(th)}$ values from a sample lot, as explained in Chapter 4.

$V_{GS(th)\_Q1}$ = 2.8 V

$V_{GS(th)\_Q3}$ = 3.3 V

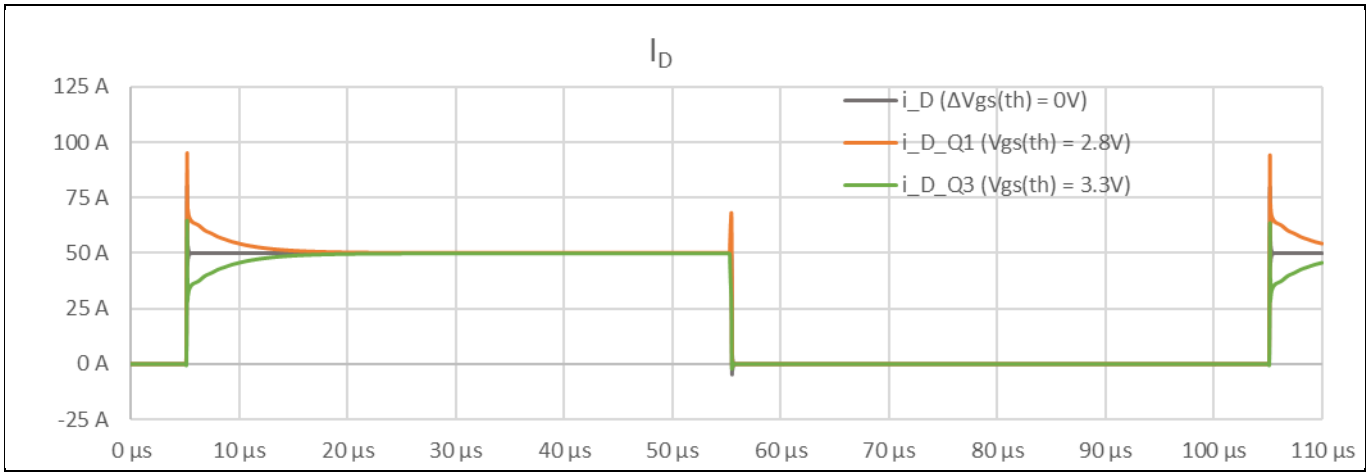

Figure 6 Switching of two paralleled MOSFETs with 0.5 V difference in $V_{GS(th)}$ – Worst case mismatch according to sample lot data

When designing the system, the current limiting values of the MOSFET need to be considered, however the overall average power loss could just as likely represent the limiting factor with regard to the maximum MOSFET junction temperature.

The dissipated energy can be broken down into three parts:

- E_{ON} – Turn-on switching loss energy – energy dissipated at a single turn-on transition
- E_{OFF} – Turn-off switching loss energy – energy dissipated at a single turn-off transition
- E_{CND} – Conduction loss energy – energy dissipated during MOSFET conduction within one PWM cycle
- T_{CND} – Time of conduction – the time interval used to measure conduction energy

Conduction is considered to begin after turn-on process is completed – meaning when v_{GS} is above miller plateau (often defined at a certain level above miller plateau). v_{DS} voltage and thus power dissipation in this interval is linearly proportional to the MOSFET drain current i_D:

$$v_{DS} = R_{DS(on)} \cdot i_D$$

Conduction losses therefore depend on $R_{DS(on)}$ and i_D alone. So if i_D was to settle immediately after the switch, the conduction losses should be the same for both MOSFETs. But, as it can be observed from **Figure 5** and **Figure 6**, the difference in the drain currents persists for a considerable time after the switch, even if $R_{DS(on)}$ of both parallel MOSFETs is the same. This unbalance is maintained by the parasitic inductances surrounding the MOSFET ($L_{D\text{-}HS}$ = 3 nH, $L_{S\text{-}HS}$ = 1 nH, $L_{D\text{-}LS}$ = 1 nH, $L_{S\text{-}LS}$ = 3 nH). In this case in the range of 10 µs.

Higher current flowing through a MOSFET will cause higher losses both during switching as well as during conduction. This means higher parasitic inductances will also cause more dissipation imbalance arising from conduction losses.

Table 5 lists the losses obtained from the simulation for this particular working point ($I_{L\_p.NQ}$ = 50 A). The losses are equal for both MOSFETs when the $V_{GS(th)}$ values are perfectly matched (Equilibrium).

Table 5 Energy dissipation at each MOSFET in one PWM cycle (100 µs)

	Equilibrium		$\Delta V_{GS(th)}$ = 0.5 V		$\Delta V_{GS(th)}$ = 1.6 V	
	Q_1	Q_3	Q_1	Q_3	Q_1	Q_3
E_{ON} [µJ]	63.19	63.19	87.94	44.32	140.27	15.11
E_{OFF} [µJ]	173.01	173.01	257.61	96.59	463.61	18.58
E_{CND} [µJ] (at T_{CND} = 49us)	199.95	199.95	206.35	194.06	219.10	184.73
E_{PWM_Cycle} [µJ]	436.15	436.15	551.9	334.97	822.98	218.42

Considering the given operating point (f_{PWM}, *D.C.*) these loses can be used to calculate average power dissipation at each MOSFET.

$$P_{CND\_avg} = \frac{T_{CND}(o.p.)}{T_{CND}} E_{CND} \cdot f_{PWM}$$

$$P_{SW\_avg} = E_{SW} \cdot f_{PWM}$$

Where

$$E_{SW} = E_{ON} + E_{OFF}$$

and:

T_{CND}(o.p.) – time of conduction valid for an alternative operating point

Table 6 Average power dissipation at each MOSFET at fPWM = 10 kHz; D.C. = 50 percent

	Equilibrium		$\Delta V_{GS(th)}$ = 0.5 V		$\Delta V_{GS(th)}$ = 1.6 V	
	Q_1	Q_3	Q_1	Q_3	Q_1	Q_3
P_{ON_avg} [W]	0.63	0.63	0.87	0.44	1.40	0.15
P_{OFF_avg} [W]	1.73	1.73	2.57	0.96	4.63	0.18
P_{CND_avg} [W]	1.99	1.99	2.06	1.94	2.19	1.84
P_{avg} [W]	4.35	4.35	5.5	3.34	8.22	2.17

Unmatched $V_{GS(th)}$ therefore causes increase of losses in the MOSFET with lower $V_{GS(th)}$ (Q_1), with regard to the perfectly balanced system (Equilibium). There is a considerable increase in both switching losses, and a slight increase of conduction losses arising from $V_{GS(th)}$ mismatch.

From **Table 6** we can observe that with a $V_{GS(th)}$ difference of **0.5 V** (± 0.25 V) we have an **additional 26 percent** more power dissipation on the MOSFET with lower $V_{GS(th)}$ and **additional 88 percent** higher power dissipation if we assume the worst case scenario of **$\Delta V_{GS(th)}$ = 1.6 V (± 0.8 V)**, according to datasheet parameters.

The MOSFET with higher $V_{GS(th)}$ (Q_2) on the other hand exhibits a decrease of losses vs. the Equilibrium. The significant values that have to be considered for system design, are the the ones with increased dissipation, since these result in the above average temperature of the affected (hottest) MOSFET. This temperature will consequently represent a limiting factor for output current of the half-bridge.

6 Increase of losses at the MOSFET with lowest $V_{GS(th)}$

Note: The results from this point on, focus on the power dissipation of the MOSFET with increased losses due to the imbalance – i.e. »hottest MOSFET«, since this MOSFET will represent the limiting factor of the system output current

Note: The results in this chapter do not account for the temperature dependency of $V_{GS(th)}$. Considering the $V_{GS(th)}$ temperature dependency is described in Chapter 7.

Repeating the simulation from Chapter 5 at various load currents, provides the extended data showing how the maximum imbalance power losses are increased with current at various $\Delta V_{GS(th)}$ at the hottest MOSFET. The following charts show the average power loss at the hottest MOSFET, for the given operating point:

- f_{PWM} = 10 kHz
- D.C. = 50 percent

The losses have been broken down to show the contribution of switching losses and conduction losses separately.

- $P_{Q1(SW\_avg)}$ – average switching losses at MOSFET Q_1
- $P_{Q1(CND\_avg)}$ – average conduction losses at MOSFET Q_1
- $P_{Q1(avg)}$ – overall average losses at MOSFET Q_1 (sum of conduction and switching losses)

The same analysis can be performed for higher number of paralleled MOSFETs – shown in subchapters 6.2 and 6.3.

When paralleling more than two MOSFETs, the harshest condition of $V_{GS(th)}$ mismatch for a given range of $V_{GS(th)}$, values, is the lowest $V_{GS(th)}$ at the hottest MOSFET, and highest $V_{GS(th)}$ at all the other paralleled devices.

Note: For easier comparison, the load current in the following charts is given as normalized load current that represents load current divided by number of MOSFETs. Details explained in Chapter 2. This means the maximum current shown in the charts for 2 paralleled MOSFETs $I_{L\_p.NQ}$ = 100 A, represents the condition of the load current of I_L = 200 A, while the maximum current of $I_{L\_p.NQ}$ = 100 A in the charts for 4 paralleled MOSFETs, represents the output load current of I_L = 400 A.

6.1 2 MOSFETs in parallel

Figure 7 shows the losses per MOSFET for the “hottest MOSFET” i.e. the MOSFETs with highest dissipation (in this case Q1). **Table 7** shows the combinations of $V_{GS(th)}$ values used in the simulations.

All the charts include the example with no imbalance in the circuit for reference ($\Delta V_{GS(th)}$ = 0 V).

Table 7 $V_{GS(th)}$ values

MOSFET	Equilibrium $\Delta V_{GS(th)}$ = 0 V	Production trend $\Delta V_{GS(th)}$ = 0.5 V	Datasheet range $\Delta V_{GS(th)}$ = 1.6 V
Q_1	3.0 V	2.8 V	2.2 V
Q_3	3.0 V	3.3 V	3.8 V

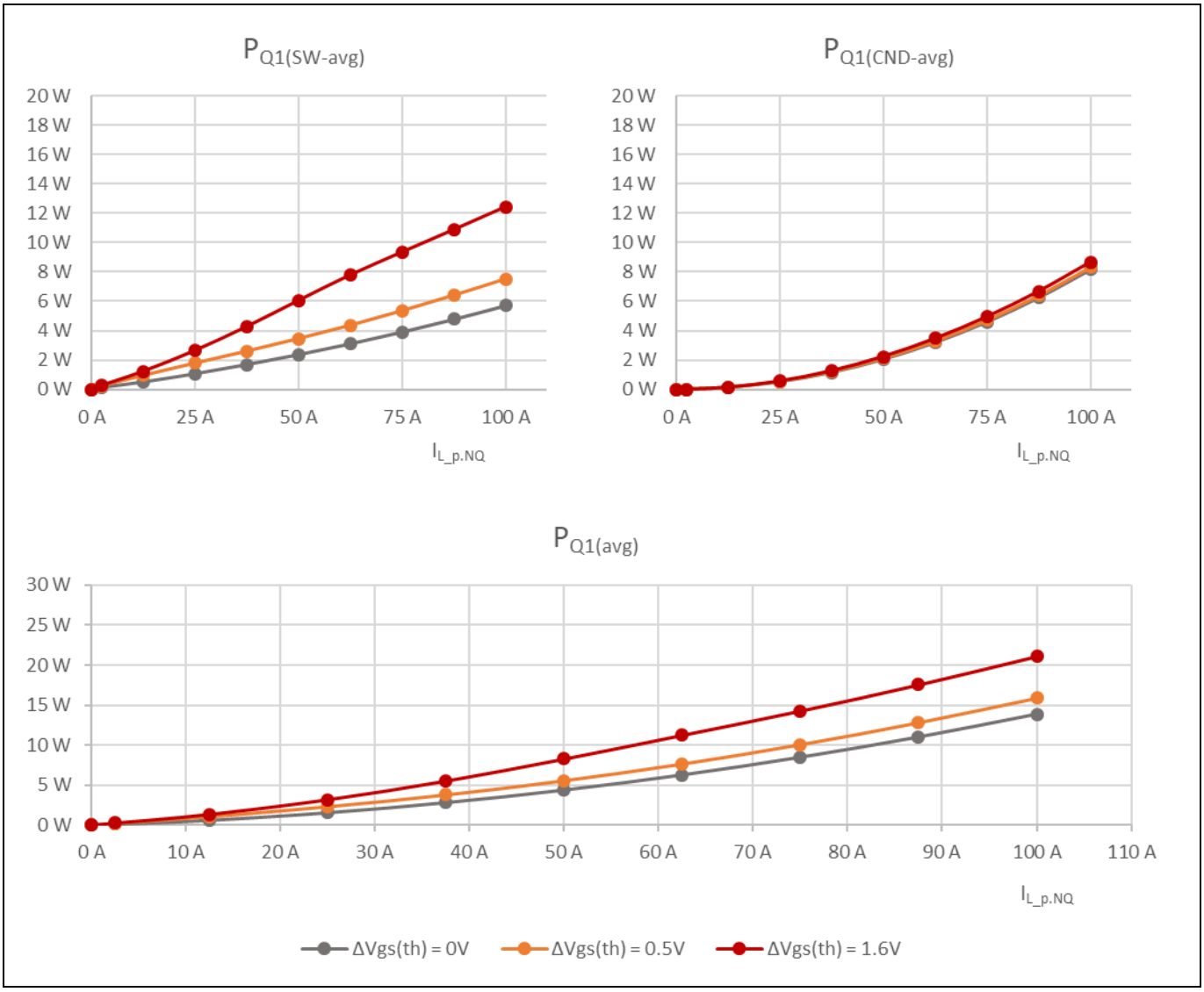

Figure 7 Average power dissipation at the hottest MOSFET at f_{PWM} = 10 kHz; D.C. = 50 percent

What is clearly visible upon examining the graphs above is that:

- the increase of power loss arising from the imbalanced system is attributed primarily to switching losses
- in a balanced system at $I_{L\_p.NQ}$ > 50 A, the switching loss is **smaller** than conduction loss
- in an imbalanced system at $I_{L\_p.NQ}$ > 50 A, the switching loss is **larger** than conduction loss

Comparing the imbalance to equilibrium reference:

In the case of maximum $\Delta V_{GS(th)}$, the overall losses at the hottest MOSFET are increased by:

- 104 percent at $I_{L\_p.NQ}$ = 25 A
- 88 percent at $I_{L\_p.NQ}$ = 50 A
- 52 percent at $I_{L\_p.NQ}$ = 100 A

With the value of $\Delta V_{GS(th)}$ = 0.5 V, the increase of losses for the hottest MOSFET is considerably smaller. The overall losses are increased by:

- 48 percent at $I_{L\_p.NQ}$ = 25 A
- 26 percent at $I_{L\_p.NQ}$ = 50 A
- 14 percent at $I_{L\_p.NQ}$ = 100 A

6.2 4 MOSFETs in parallel

As mentioned earlier, when the analysis is conducted for larger numbers of paralleled MOSFETs, the worst condition for a given $\Delta V_{GS(th)}$ is examined, meaning the “hottest MOSFET“ exhibits the lowest $V_{GS(th)}$, and the remaining MOSFETs connected in parallel will have the highest (same) $V_{GS(th)}$. The combinations in question are shown in **Table 8**.

Table 8 $V_{GS(th)}$ values

MOSFET	Equilibrium $\Delta V_{GS(th)}$ = 0 V	Production trend $\Delta V_{GS(th)}$ = 0.5 V	Datasheet range $\Delta V_{GS(th)}$ = 1.6 V
Q_1	3.0 V	2.8 V	2.2 V
Q_3, Q_5, Q_7	3.0 V	3.3 V	3.8 V

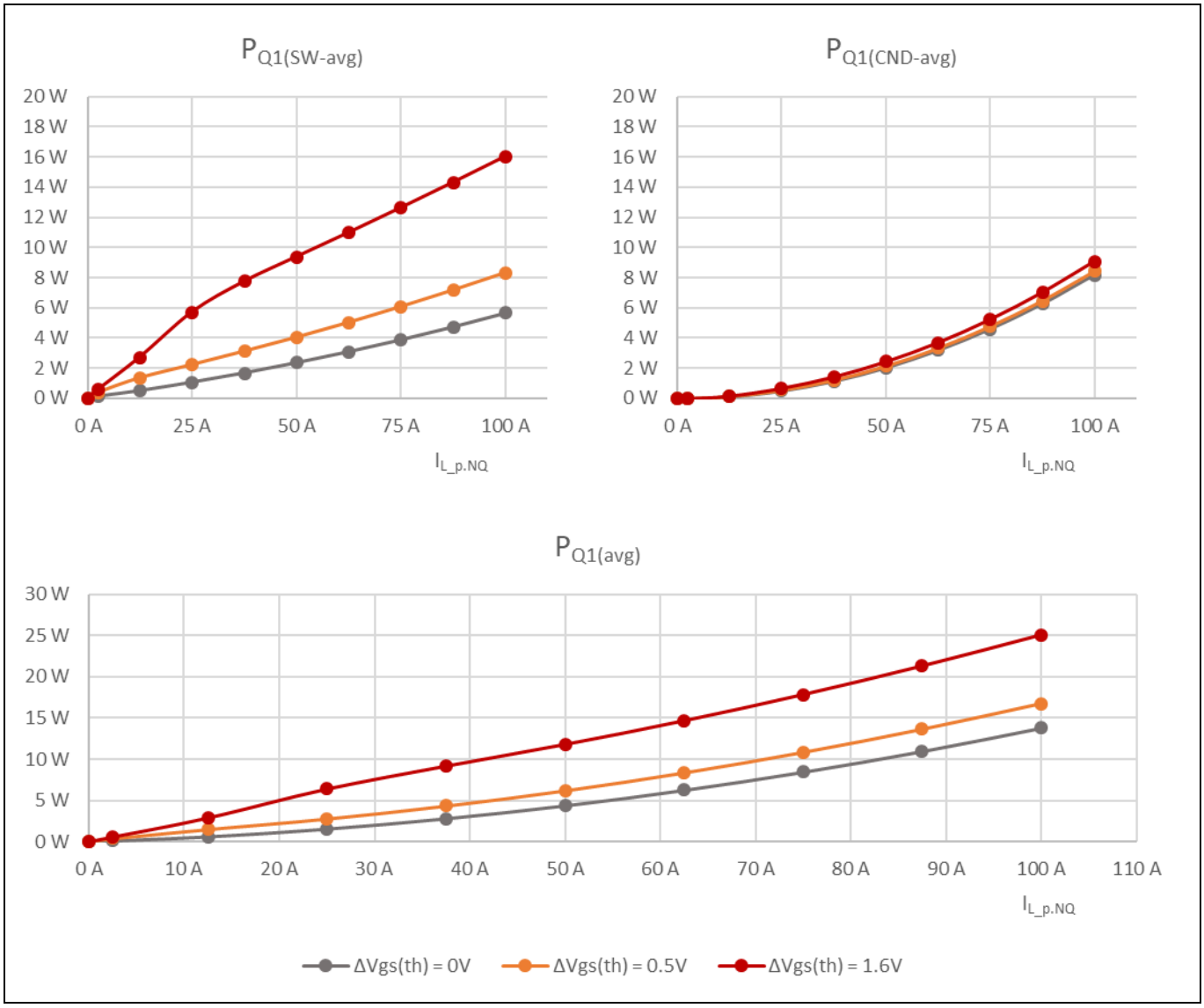

Figure 8 Average power dissipation at the hottest MOSFET at f_{PWM} = 10 kHz; D.C. = 50 percent

Similar conclusions can be drawn as in the previous example. Conduction loss contribution to the overall losses, though slightly increased, is still negligible.

The switching losses in this case are increased considerably comparing to the 2-in-parallel system.

Comparing the imbalance to equilibrium reference:

At $\Delta V_{GS(th)}$ = 1.6 V, the overall losses at the hottest MOSFET are increased by:

- 308 percent at $I_{L\_p.NQ}$ = 25 A
- 169 percent at $I_{L\_p.NQ}$ = 50 A
- 81 percent at $I_{L\_p.NQ}$ = 100 A

Increase of losses at the MOSFET with lowest VGS(th)

At $\Delta V_{GS(th)}$ = 0.5 V, the overall losses at the hottest MOSFET are increased by:

- 77 percent at $I_{L\_p.NQ}$ = 25 A
- 41 percent at $I_{L\_p.NQ}$ = 50 A
- 21 percent at $I_{L\_p.NQ}$ = 100 A

6.3 6 MOSFETs in parallel

Example of using 6 MOSFETs in parallel. The combinations in question are shown in **Table 9**.

Table 9 $V_{GS(th)}$ values

	Equilibrium $\Delta V_{GS(th)}$ = 0 V	**Production trend $\Delta V_{GS(th)}$ = 0.5 V**	**Datasheet range $\Delta V_{GS(th)}$ = 1.6 V**
Q_1	3.0 V	2.8 V	2.2 V
Q_3, Q_5, Q_7, Q_9, Q_{11}	3.0 V	3.3 V	3.8 V

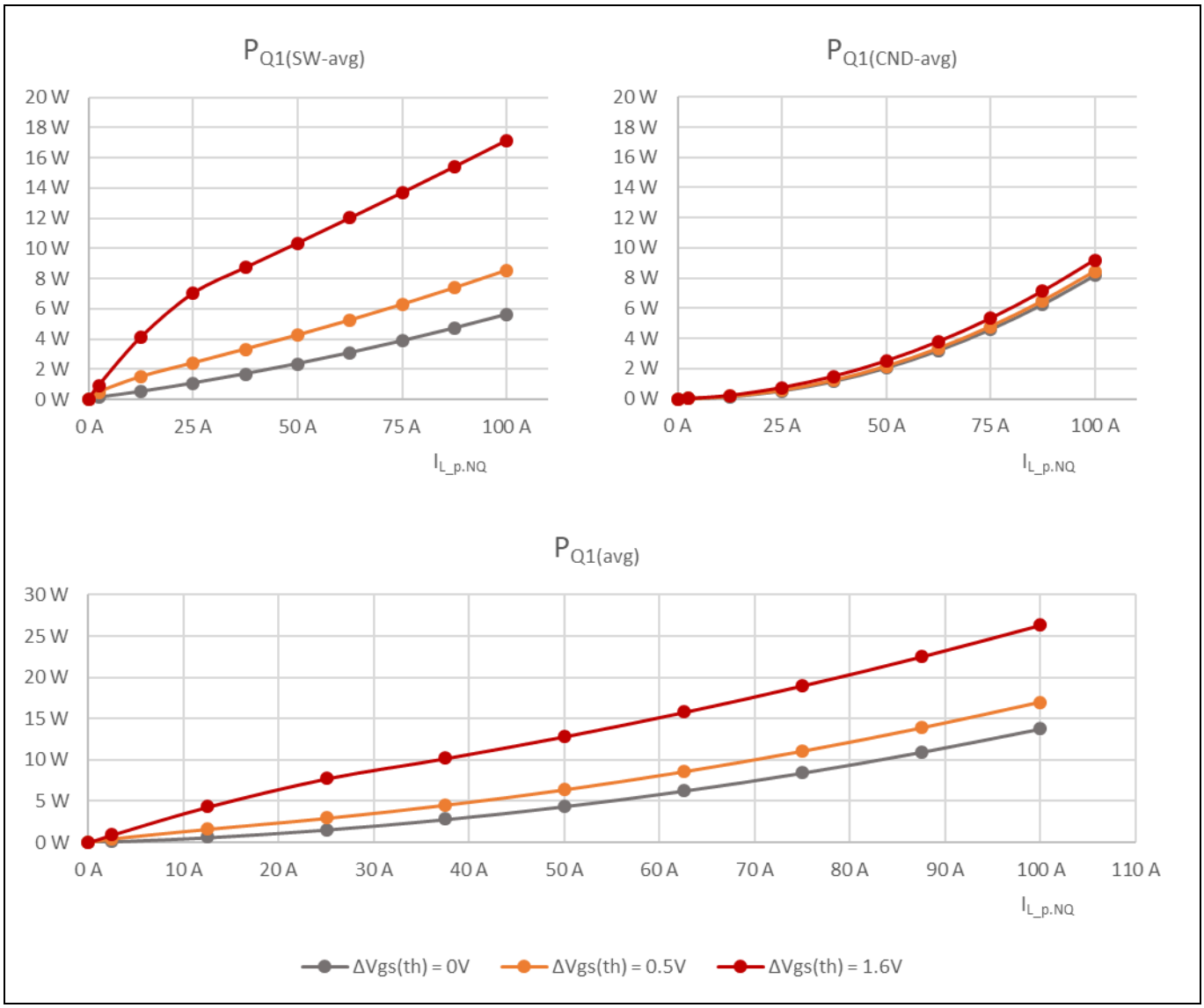

Figure 9 Average power dissipation at the overloaded MOSFET at f_{PWM} = 10 kHz; D.C. = 50 percent

Increase of losses at the MOSFET with lowest VGS(th)

While the increase of losses at the hottest MOSFET is even greater when paralleling 6 MOSFETs. The relative increase compared to 4 MOSFETs is not as big when comparing 4 MOSFETs versus 2 MOSFETs in parallel.

Comparing the imbalance to equilibrium reference:

At $\Delta V_{GS(th)}$ = 1.6 V, the overall losses at the hottest MOSFET are increased by:

- 396 percent at $I_{L\_p.NQ}$ = 25 A
- 193 percent at $I_{L\_p.NQ}$ = 50 A
- 91 percent at $I_{L\_p.NQ}$ = 100 A

At $\Delta V_{GS(th)}$ = 0.5 V, the losses at the hottest MOSFET are increased by:

- 90 percent at $I_{L\_p.NQ}$ = 25 A
- 46 percent at $I_{L\_p.NQ}$ = 50 A
- 23 percent at $I_{L\_p.NQ}$ = 100 A

6.4 Increase of worst case losses in relation to number of MOSFETs in parallel

One conclusion that can be drawn from the previous examples is that the stress on the hottest MOSFET is worse with higher number of paralleled MOSFETs. The charts in **Figure 10** show the increase of losses with regards to the number of paralleled MOSFETs at several load currents. Again the three $\Delta V_{GS(th)}$ are considered, including the reference with no imbalance.

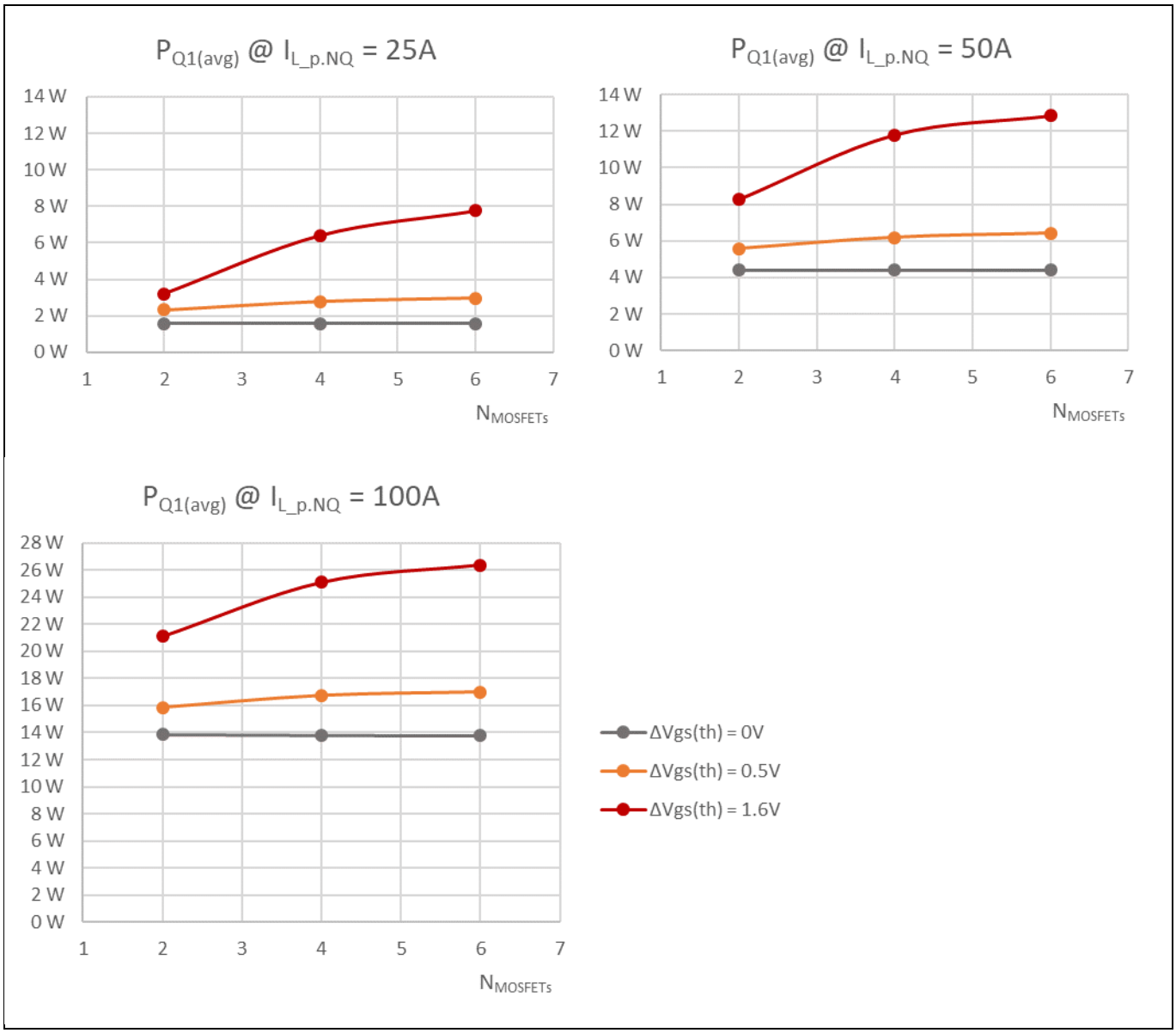

Figure 10 Increase of worst case losses in relation to number of MOSFETs in parallel

Though hard to quantify – the charts in **Figure 10** indicate the increase of stress to the hottest MOSFET with regard to the number of MOSFETs being paralleled. There is a steep increase of the imbalance with 2 MOSFETs in parallel, and further relatively high increase when using 4 MOSFETs, especially for visible in the worst case scenario. However further increasing the number of MOSFETs leads to less additional increase.

What can be seen from the charts, is the benefit arising from the tighter $V_{GS(th)}$ spread. Even when paralleling 6 MOSFETs with $\Delta V_{GS(th)}$ = 0.5 V, the dissipation imbalance is more favorable than when paralleling just 2 MOSFETs with $\Delta V_{GS(th)}$ = 1.6 V.

7 Example of temperature increase considering thermal characteristics

If the thermal characteristics of the system are considered, the data of power dissipation can be used to calculate the temperature of an individual MOSFET. Assuming a simplified thermal resistance of MOSFET (junction to heatsink) of R_{thJH} = 1.5 K/W, and a steady homogenous temperature of the heatsink itself, the MOSFET junction temperature T_j correlates to the MOSFET power dissipation according to the formula below:

$$T_j = P_{avg} \cdot R_{thJH} + T_{hs}$$

The temperatures of the hottest MOSFET are plotted in **Figure 11**, and apply to the example for the heatsink temperature of T_{hs} = 80 °C.

Conditions in summary:

- f_{PWM} = 10 kHz
- D.C. = 50 percent
- R_{thJH} = 1.5 K/W
- T_{hs} = 80 °C

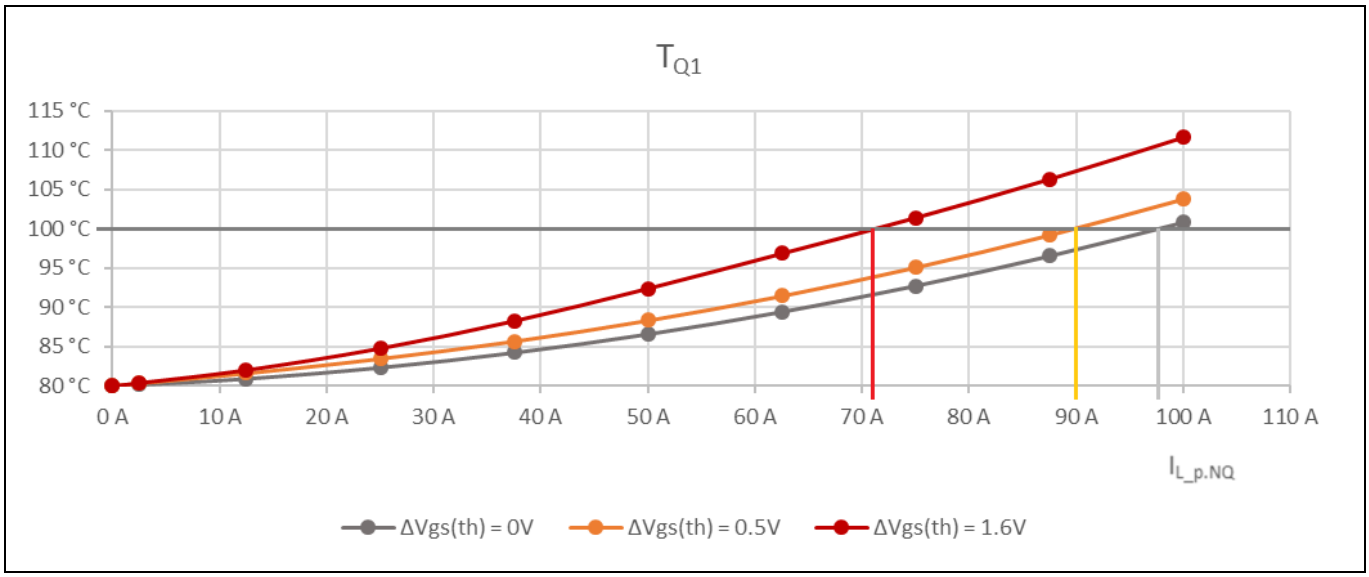

Figure 11 Temperature of the hottest MOSFET vs. output current – 2 MOSFETs in parallel

The way to make use of the above graph is by observing the output current at a particular device temperature, where the graph refers to the hottest MOSFET. The reference again will be the perfectly balanced system that is represented by the gray curve in **Figure 11**. In this case all the paralleled MOSFETs will have the same temperature.

If for example the system requirements allow for the maximum $T_{j(max)}$ = 100°C (as marked in **Figure 11**), then the output current will be limited accordingly:

- at $\Delta V_{GS(th)}$ = 0 V → $I_{L(max)\_p.NQ}$ = 98 A
- at $\Delta V_{GS(th)}$ = 0.5 V → $I_{L(max)\_p.NQ}$ = 90 A
- at $\Delta V_{GS(th)}$ = 1.6 V → $I_{L(max)\_p.NQ}$ = 71 A

Repeating the same exercise for systems with 4 or 6 MOSFETs in parallel, the results are shown in **Figure 12** and **Figure 13**.

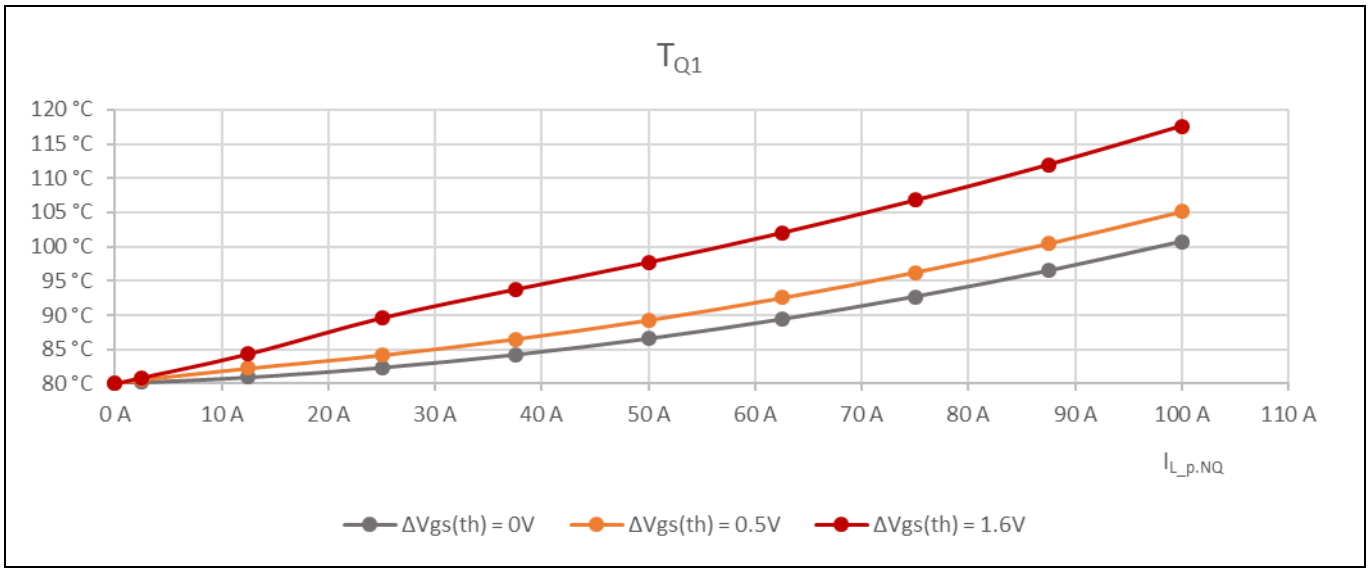

Figure 12 Temperature of the hottest MOSFET vs. output current – 4 MOSFETs in parallel

4 MOSFETs in parallel:

- at $\Delta V_{GS(th)}$ = 0 V → $I_{L(max)\_p.NQ}$ = 98 A
- at $\Delta V_{GS(th)}$ = 0.5 V → $I_{L(max)\_p.NQ}$ = 86 A
- at $\Delta V_{GS(th)}$ = 1.6 V → $I_{L(max)\_p.NQ}$ = 57 A

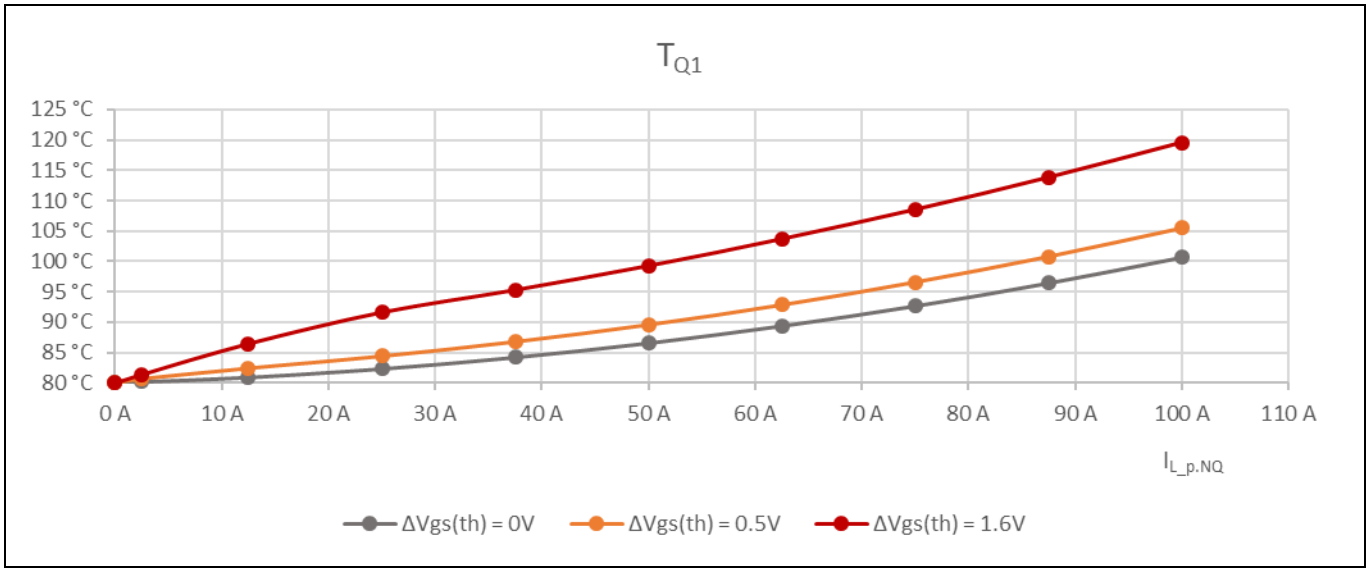

Figure 13 Temperature of the hottest MOSFET vs. output current – 6 MOSFETs in parallel

6 MOSFETs in parallel:

- at $\Delta V_{GS(th)}$ = 0 V → $I_{L(max)\_p.NQ}$ = 98 A
- at $\Delta V_{GS(th)}$ = 0.5 V → $I_{L(max)\_p.NQ}$ = 85 A
- at $\Delta V_{GS(th)}$ = 1.6 V → $I_{L(max)\_p.NQ}$ = 52 A

Improving result accuracy

A simplification that was assumed in the previous exercise is a constant $V_{GS(th)}$ with respect to the MOSFET temperature. The results are valid as a direct correlation to absolute values of $V_{GS(th)}$.

In a more realistic scenario, the initial $V_{GS(th)}$ values would represent measured values at a given temperature (e.g., 25°C) at which the devices would be characterized. With increased temperature comes a considerable reduction in $V_{GS(th)}$, and since the MOSFET with the lowest $V_{GS(th)}$ is also the hottest, the imbalance will increase the $\Delta V_{GS(th)}$ between the paralleled MOSFETs even further.

The temperature dependency of $V_{GS(th)}$ is shown in **Figure 14**.

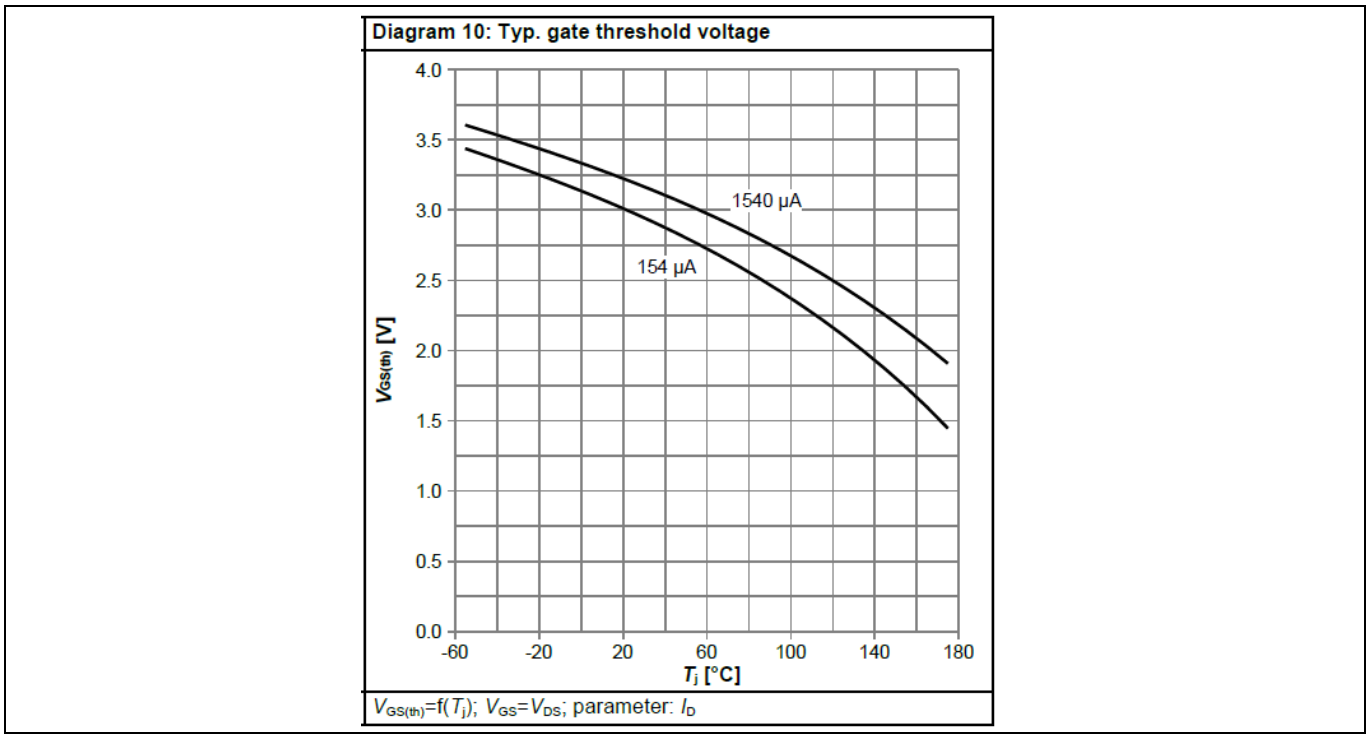

Figure 14 $V_{GS(th)}$ characteristic of an OptiMOS™ 5 family MOSFETs according to datasheet

In order to improve the prediction of the output current limit, the newly obtained temperatures, can be used to repeat the simulation at any particular operating point of interest, using resultant $V_{GS(th)}$ values determined by the T_j of the initial simulation (also considering the T_j of the cooler MOSFETs). The characteristic decrease of $V_{GS(th)}$ (T_j) obtained from the graph in **Figure 14**, should be deducted from the initial $V_{GS(th)}$ values that were assumed in the first simulation iteration (typically values of characterization at 25°C).

The repeated simulation, conducted using the updated $V_{GS(th)}$ values, will produce a second iteration result, where a further increase of the imbalance is to be expected compared to the initial results. The errors of the second iteration will be reduced, although if required the procedure can be iteratively repeated.

The MOSFET model used in the simulations was a level 1 (L1) model which assumes a constant junction temperature. Alternatively the level 3 (L3) simulation model could be used but with a lot of L_S might cause convergence issues.

8 AC output load current

In applications such as motor drives the half bridge (typically 3 phases) is used to generate an AC power signal that generates positive or negative torque in an electric motor.

The output load current in this case is a sine wave of a given amplitude (see **Table 10** for parameter overview):

$$i_{Load}(t) = I_m * \sin(\omega_m * t + \varphi)$$

$$\omega_m = 2 * \pi * f_{el}$$

$$PF = \cos(\varphi)$$

Applying different control algorythms – e.g. space vector modulation (SVM), or sinusoidaly weighted pulse width modulation (SPWM), can also affect the overall power loss. Comparison between various control algorhithms is beyond the scope of this paper. What is essential – when comparison is made between effects of MOSFET characteristics, it is necessary to compare those results at same control algorhithms and identical conditions.

The switching modulation scheme applied in this investigation is SPWM with conditions and settings as defined in **Table 10**. Theese SPWM conditions are used in the following examples.

Table 10 Load and SPWM parameters and conditions

	Description	Value
I_m	Amplitude of the load current (sweep)	0 A → 100 A (per MOSFET)
f_{el}	Electrical frequency of the load / motor (Frequency of modulating wave)	100 Hz
φ	Phase shift of the load sine wave with regard to the modulating waveform of the control	0
PF	Power factor	1
M	Modulation index of PWM (“amplitude” of PWM D.C.)	0.8
f_{PWM}	Carrier frequency	10 kHz
DT	Dead time applied to the PWM waveforms	1 µs

In contrast to the DC example, where a single PWM cycle, at the given load condition, supply voltage and D.C. of PWM, is enough to provide sufficient data to calculate average MOSFET power dissipation, in AC, every switching instance is conducted at a different output current condition. Additionally calculating the conduction losses needs to consider the pulse width of each cycle which is changing according to the modulation scheme.

An example is shown in Figure 15 where one cycle of the load current sine wave is plotted against corresponding drain current of the HS switch (I_{D_HS}). The I_{D_HS} is shown separately for the positive and the negative part. The PWM frequency in the demonstrated example is relatively slow in order to better demonstrate the principle.

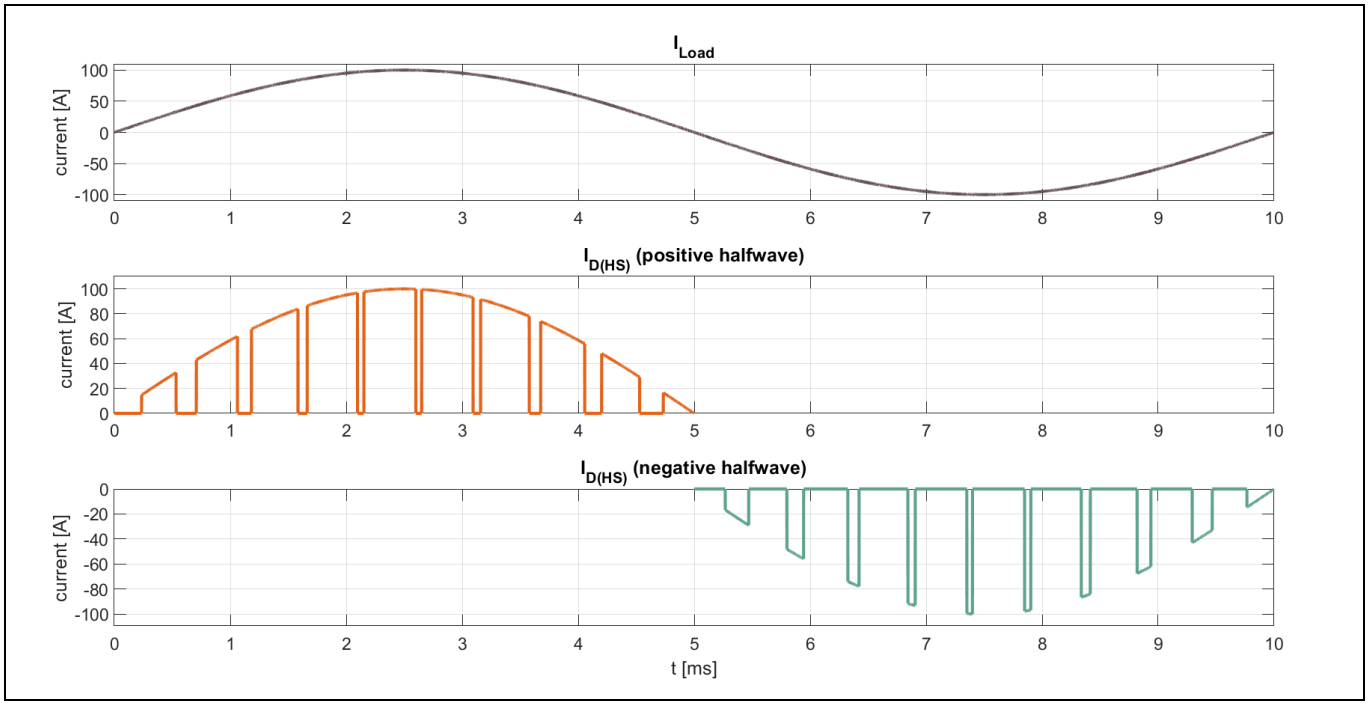

Figure 15 Load current sine waves plotted against drain current of the HS switch

In order to calculate the MOSFET losses for the full sine period, in addition to the forward conduction contributions considered in previous chapters for the forward conducting MOSFET, the energy dissipated during the negative halfwave needs to be obtained. In full, MOSFET loss contributions, differentiated by their characteristics, are broken down in to the following categories of instantaneous losses:

- E_{on} – MOSFET switching loss at turn ON
- E_{off} – MOSFET switching loss at turn OFF
- P_{cnd} – conduction loss of the open MOSFET channel in forward conduction
- P_D – conduction loss of the body diode
- E_{Doff} – reverse recovery loss of the body diode

To calculate the MOSFET loss averaged across the sine cycle, each of these contributions need to be evaluated for the condition at which they occur. Meaning for example - E_{on} has to be obtained for every value of I_{Load} corresponding to the instance of turn ON as defined by the PWM. Similar for the other contributions.

Tabulating the loss contributions for a limited number of operating points across a range of I_{Load} can simplify obtaining values by means of interpolation. Thus loss calculations at various PWM conditions can be made relatively quickly based on the so called loss lookup table which is obtained from a repetition of more complex simulation or even measurements with limited number of operating points.

The following graphs show average MOSFET losses in relation to current imbalance similar to the previous chapters, however in this case with sinewave i_{Load}, and applied SPWM with conditions as defined in **Table 10**. The amplitude of the load current (I_m) is swept and the result is average power dissipated in a MOSFET plotted against I_m.

AC output load current

Average power refers to the averaging across the sine wave cycle. The total average losses ($P_{tot(avg)}$) are again broken down into switching and conduction loss.

- $P_{Q1(SW\_avg)}$ – average switching losses at MOSFET Q_1
- $P_{Q1(CND\_avg)}$ – average conduction losses at MOSFET Q_1
- $P_{Q1(tot\_avg)}$ – total average losses at MOSFET Q_1 (sum of $P_{Q1(CND\_avg)}$ and $P_{Q1(SW\_avg)}$)

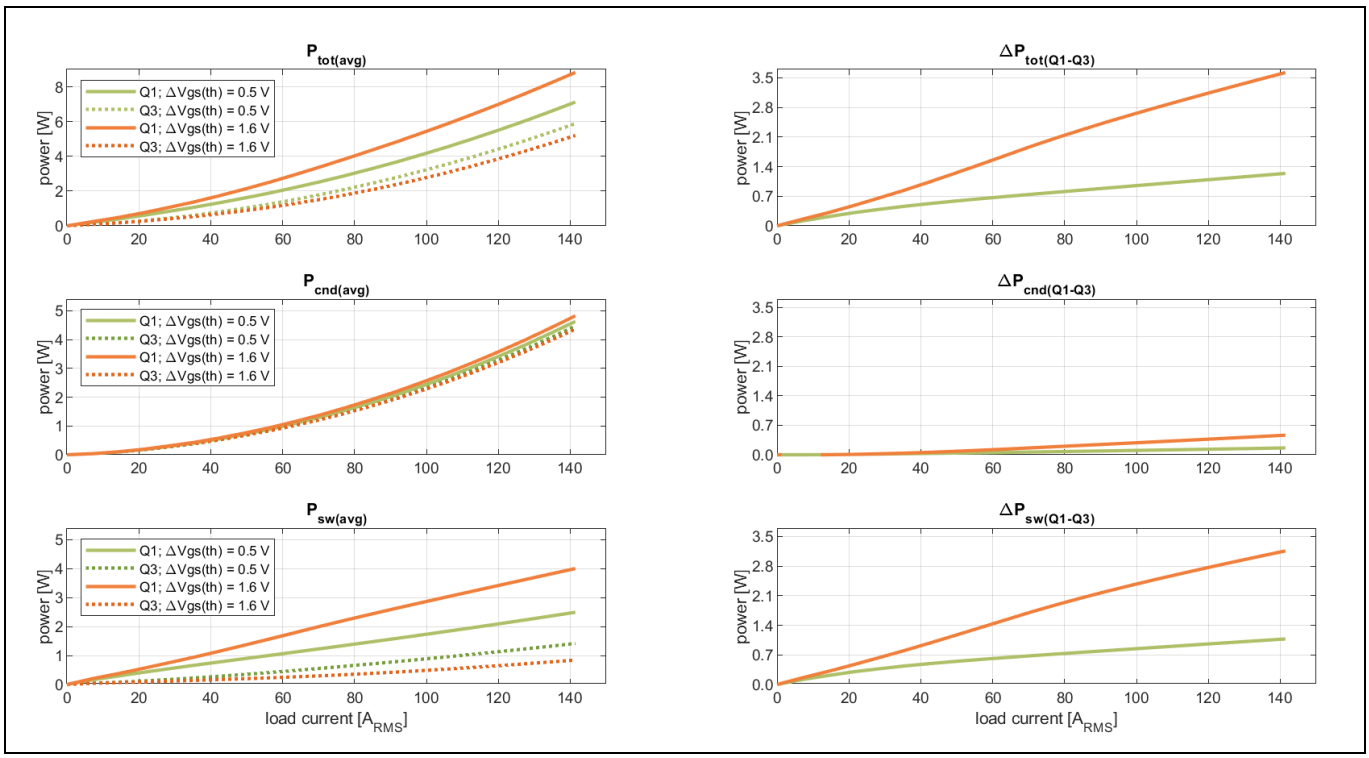

Figure 16 Average power dissipation at MOSFETs Q_1 and Q_3 (2 MOSFETs in parallel)

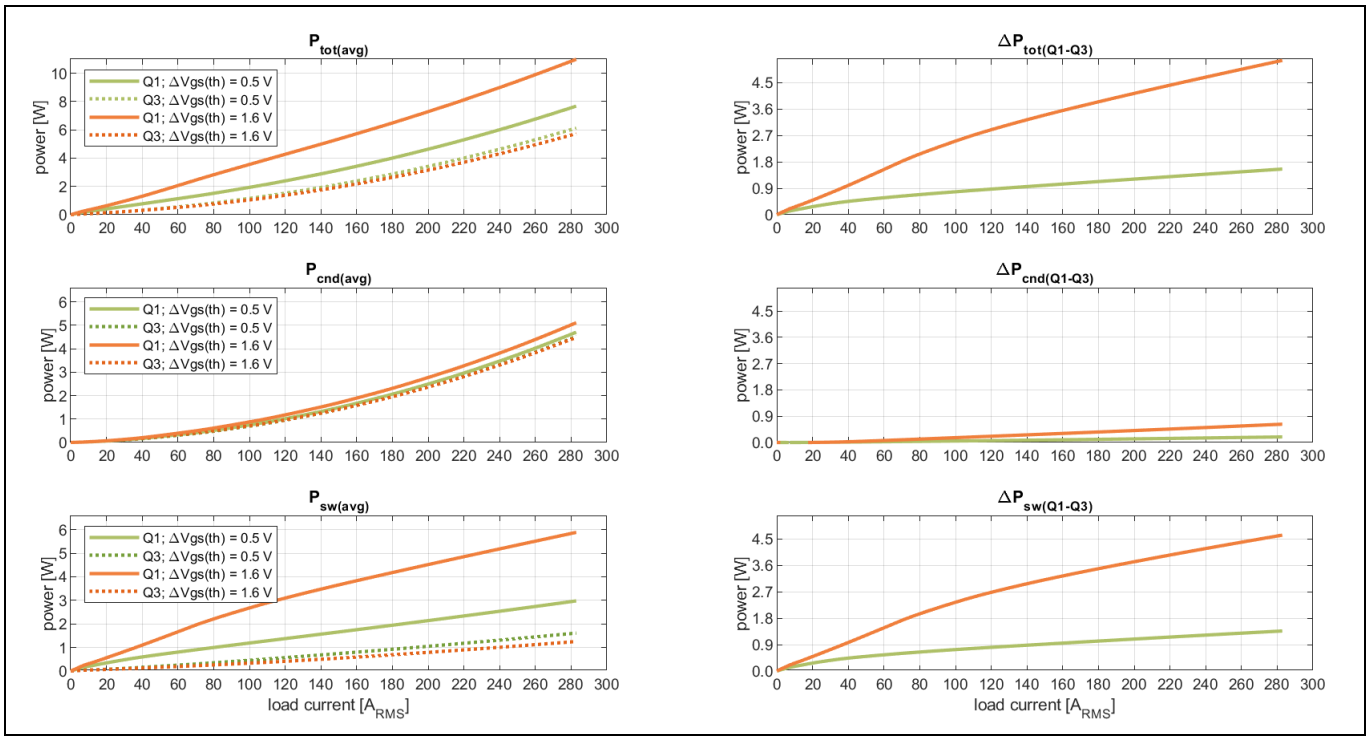

Figure 17 Average power dissipation at MOSFETs Q_1 and Q_3 (4 MOSFETs in parallel)

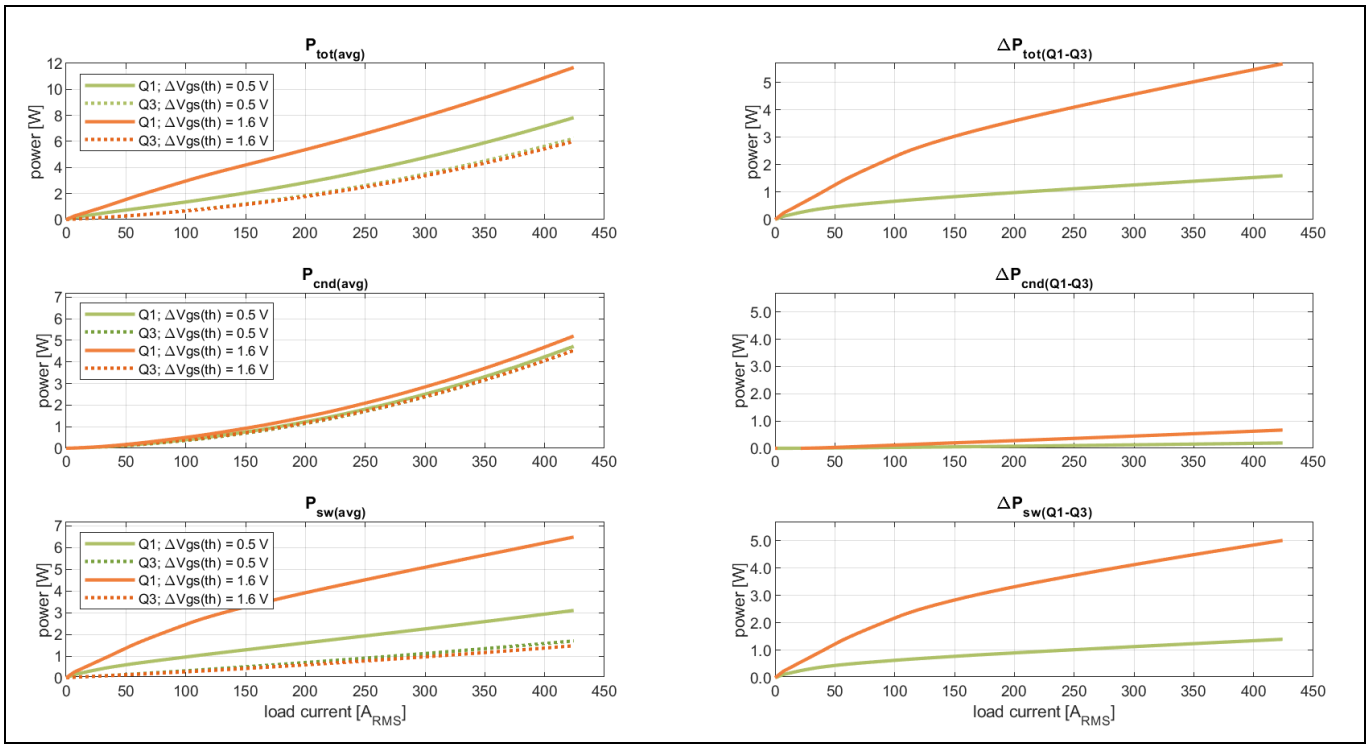

Figure 18 Average power dissipation at MOSFETs Q_1 and Q_3 (6 MOSFETs in parallel)

Comparing the results to the DC case in chapter 6, the effects of current imbalance are the same qualitatively. However, quantitatively the dissipation imbalances are smaller when using sine output current, due to differences in load current and modulation scheme. The comparisons of power dissipations at Q_1 between DC and AC load current, are shown in **Table 11** and **Table 12** for $\Delta V_{GS(th)}$ = 0.5 V and $\Delta V_{GS(th)}$ = 1.6 V respectively.

Table 11 DC vs. AC comparison of worst case dissipation @ $\Delta V_{GS(th)}$ = 0.5 V

	$I_{L\_p.NQ}$ (DC)		$I_{L\_p.NQ}$ (AC – RMS)	
	35 A	**70 A**	**35 A RMS**	**70 A RMS**
P (Q_1) – 2 parallel MOSFETs	3.5 W	9.1 W	2.5 W	7.0 W
P (Q_1) – 4 parallel MOSFETs	4.0 W	9.8 W	2.9 W	7.6 W
P (Q_1) – 6 parallel MOSFETs	4.2 W	10.0 W	3.0 W	7.7 W

Table 12 DC vs. AC comparison of worst case dissipation @ $\Delta V_{GS(th)}$ = 1.6 V

	$I_{L\_p.NQ}$ (DC)		$I_{L\_p.NQ}$ (AC – RMS)	
	35 A	**70 A**	**35 A RMS**	**70 A RMS**
P (Q_1) – 2 parallel MOSFETs	5.0 W	13.0 W	3.4 W	8.7 W
P (Q_1) – 4 parallel MOSFETs	8.6 W	16.5 W	5.0 W	10.9 W
P (Q_1) – 6 parallel MOSFETs	9.7 W	17.7 W	5.6 W	11.5 W

9 Conclusion

The focus of this paper is the phenomenon of current sharing – i.e. current distribution between MOSFETs connected in parallel in a half-bridge switching topology. The simulations were performed on an example of a buck converter operating in continuous switching operating point at constant duty cycle (D.C.) and a DC output load current (I_L), as well as SPWM modulation with sinusoidal output current waveforms. Similar analysis can be performed utilizing various modulation techniques like trapezoidal or SVM.

The effects of layout asymmetries were not the scope of this research, nevertheless the quantity of the parasitic inductance – though symmetrical – does affect the extent of conduction loss imbalance, since higher inductance will cause a slower settling of I_D imbalance after turn-on. Reader can find more on layout effects in reference literature [1], [2].

The goal was to define practical means for quantifying imbalances in current sharing, to explain the procedure of the analysis, and to quantify the imbalance arising from $V_{GS(th)}$ parameter mismatch. Mismatch of $V_{GS(th)}$ is considered the most important among the parameters affecting current imbalance, since it causes increase of switching loss at the same MOSFET at both, turn ON and turn OFF.

Since establishing worst case conditions in bench tests is just as unlikely as establishing perfect conditions (requires hand picking specific set of values), bench tests tend to give more favorable results than simulated worst case analysis. Different MOSFETs will therefore have different failure rates in the field if the system is not over-engineered. A worst case analysis ensures that the margins of the design are kept at an optimum.

In order to present the effects of an individual parameter, the layout has been idealized to the point of making it perfectly symmetrical, despite the parasitic inductances and resistances are included in this analysis and represent realistic values that correspond to an actual circuit. Typical switching conditions were also considered in the simulation model, so that the results are representative to the MOSFET being used in a real half-bridge circuit.

The investigation compared the power dissipation imbalance for different magnitude of $V_{GS(th)}$ mismatch:

- worst case mismatch based on datasheet limiting values
- worst probable mismatch according to an example lot parameter distribution

In effect, the imbalance results in a reduction of overall output current capacity. Compared to the idealized scenario with perfect sharing, the extent of the current capacity reduction can be as much as 50 percent (when paralleling six or more MOSFETs, assuming the $V_{GS(th)}$ mismatch is at its worst datasheet values).

The higher the number of MOSFETs being paralleled, the harsher the condition to the MOSFET with the lowest $V_{GS(th)}$, though there is no simple linear correlation between power dissipation increase vs. number of MOSFETs being paralleled.

Reducing the $V_{GS(th)}$ mismatch, can mitigate the problem of current imbalance, meaning less system over-engineering is needed in the design. The reduced $V_{GS(th)}$ mismatch, considered in this application, shows considerable improvement in performance compared to the datasheet parameter example. Managing the current imbalance can result in system size reduction consequently keeping down the overall cost.

The state-of-the-art Infineon MOSFETs utilize advanced production processes, resulting in high quality MOSFETs that exhibit tight spread of parameters, making them very well suited for parallel operation.

References

[1] App note: AN_1803_PL11_1804_092613
Paralleling MOSFETs in high-current LV drive applications
https://www.infineon.com/dgdl/Infineon-ApplicationNote_MOSFET_Paralleling_MOSFETs_in_high-current_LV_drive_applications-AN-v01_00-EN.pdf?fileId=5546d46262b31d2e0162f284b7583d1b

[2] App note: Paralleling of power MOSFETs for higher power output
https://www.infineon.com/dgdl/para.pdf?fileId=5546d462533600a401535744b4583f79

Revision history

Document version	Date of release	Description of changes
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V 1.1	14-05-2021	Added chapter on AC output load current

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