8.10 A 5V-to-150V Input-Parallel Output-Series Hybrid DC-DC Boost Converter Achieving 76.4mW/mg Power Density and 80% Peak Efficiency

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Ultrahigh voltage conversion ratio (VCR) DC-DC boost converters are essential for biomedical, optics, sensing and diagnostics applications. For realizing an ultrahigh VCR, the conventional boost converter would result in a large duty ratio D, a large inductor current I_L and thus a significantly degradation on power efficiency, and its VCR is limited by the parasitic resistors. Figure 8.10.1 top shows the recently reported hybrid boost converters. The multilevel boost converter (MLBC) has a single inductor at the input, and has the feature of input-series-output-series. Therefore, multilevel boost converters considerably improve the VCR and reduce the device voltage stress with the flying capacitors. However, the MLBC topologies still suffer from the problems of low efficiency and low power density caused by the large I_L. Another topology with multipath boost converters (MPBC) has the feature of input-parallel-output-parallel. The MPBC can effectively reduce the I_L of each branch by connecting parallel input inductors. But the output-parallel structure does not improve the VCR nor reduce the device voltage stress. To address the above issues, this work presents a hybrid input-parallel output-series high power density ultrahigh-VCR step-up DC-DC converter for electrostatic and piezoelectric actuators used for small-scale flyweight devices. This converter is very challenging due to the low V_{IN} (<5V), high V_{OUT} (>100V), high output power (>200mW) and high power density (volume<10mm^3 and weight<100mg). We use both mW/mm^3 and mW/mg for the power density units to emphasize the importance of the size and weight for flying robots.

Figure 8.10.1 bottom shows the proposed converter consists of a 5-stage series-parallel switched-capacitor (SP-SC), an inductor-based boost converter, a parallel-to-series (P2S) interface circuit and a N-stage Cockcroft-Walton (CW) voltage multiplier (VM). The SC circuit and the inductor are connected in parallel at the input to reduce the current flowing through the inductor, thereby reducing the size and the loss of the inductor. In the meanwhile, in the Bipolar-CMOS-DMOS (BCD) process, the V_{DS} of NLDMOS is usually scalable (for example, 5V/10V/16V/24V/36V/…), while the voltage rating of the integrated capacitors has less choices (only 5V/12V/70V MIM or MOM capacitors). Therefore, the SP-SC, which need low-voltage capacitors and high-voltage MOSFETs, is used to reduce the size of the SC converter. The parallel-to-series interface circuit converts the parallel connection at the input into a series connection to the output by adjusting the operation time of the SC converter and the boost converter. And the post-N-stage CW voltage multiplier further improves the VCR while reducing the voltage stresses on its components (V_{CAP}=V_{DIO_STRESS}=2V_{OUT}/N). Overall, the VCR of proposed converter is VCR_{Total}=VCR_{VM}×(VCR_{SPSC}+VCR_L) and the efficiency is evaluated by $\eta_{Total}=\eta_{VM}\times(k_{SPSC}\times\eta_{SPSC}+k_L\times\eta_L)$, where $k_{SPSC}=P_{IN,SPSC}/P_{IN,Total}$, and $k_L=P_{IN,L}/P_{IN,Total}$.

Figure 8.10.2 illustrates the operation principle, capacitor voltage and inductor current balance issues. There are two phases depending on whether the capacitors discharge or the inductor demagnetizes. During phase 1, the capacitors of the SP-SC are series-connected to be charged by V_{IN}. And the inductor demagnetizes to charge the flying capacitor C_{F2} with C_{F1} and to charge C_{F4} with C_{F3}. The voltages of C_{F2} and C_{F4} reach V_L+V_{CF1} and V_L+V_{CF3} respectively. In phase 2, the inductor magnetizes and the capacitors of the SP-SC are parallel-connected to charge C_{F1} to V_{SPSC} and to charge C_{F3} to V_{SPSC}+V_{CF2}. Meanwhile, the SP-SC capacitors charge the C_O to V_{SPSC}+V_{CF2}+V_{CF4}.

The parallel connection at the input will cause unbalanced inductor current distribution, and the series connection at the output will cause unbalanced capacitor voltage stresses. The proposed converter sets the current flowing through the inductor by adjusting the output voltage of the boost and the SP-SC. When the number N_{VM} of VM stages is odd (two-branch matched case), the two branches of the inductor and the SP-SC charge the same number of the VM flying capacitors (for N_{VM}=3, inductor node IN_D charges C_{F2} and C_{OUT}, SP-SC node IN_C charges C_{F1} and C_{F3}). In this case, the total input power remains unchanged but is distributed to the SP-SC and inductor parts in proportion to their output voltages, as shown in Fig. 8.10.2 (bottom right). When the number of voltage multiplier stages is even (two-branch unmatched situation), the two branches of the inductor and the SP-SC charge the different number of the capacitors (for N_{VM}=2, inductor node IN_D charges C_{F2}, SP-SC node IN_C charges the C_{F1} and C_{OUT}). The difference of the two situations is that in unmatched situation, the total output power changes. This suggests that we can set the current flowing through the inductor by adjusting the number of VM stages with V_{OUT} unchanged, so as to optimize the efficiency or the power density. Meanwhile, the adjustable parameters ($k_{V,L}$ and $k_{V,C}$) are different in matched and unmatched situations. However, regardless of matched or unmatched conditions, the voltage stresses of the VM capacitors are fixed ($V_{STRESS\text{-}CF1}$=V_{INC}, $V_{STRESS\text{-}CF2/3/...}$=$V_{INC}$+$V_{IND}$, $V_{STRESS\text{-}CO}$= V_{OUT}).

Figure 8.10.3 shows the circuit implementation, start-up mechanism and capacitor-free bootstrap circuit. The proposed converter is modulated by pulse-frequency feedback control loop. The SP-SC circuit uses an all-NMOS power stage. The middle switches for the parallel operation are all 5V NMOS, while the voltage stress of the top and bottom switches increase step by step as the number of stages increases (5V/10V/16V/20V/24V NLDMOS used, respectively). The switches of the boost converter and P2S interface circuit are 36V LDMOS. In order to obtain higher output power, the capacitors of the SP-SC and voltage multiplier are off-chip. As shown in Fig. 8.10.3 (bottom right), the middle switches (S_{Mx}) of the SP-SC are driven by C_{SPx} through voltage-borrowing because the source of S_{Mx} is connected to the bottom plate of C_{SPx}. And the top switches (S_{Tx}) need to be driven by V_{DDH} (10V). The V_{DDH} can be obtained by another proposed interleaved converter from the node V_{CT1} without using any additional components and bootstrap capacitors. The interleaved converter can achieve the self-starting without requiring additional start-up circuit design. In the start-up process (Fig. 8.10.3, bottom left), the drive signal stimulated by the clock (CLK) could turn on the bottom switches (S_{Bx}), and the V_{DD} will charge the capacitors of the SP-SC to 4.3V (V_{DD}–V_F) with the help of the body diode of the top switches (S_{Tx}). Then the C_{SPx} charges the gate of S_{Mx} to normally turn on or turn off. When S_{Mx} are turn-on, the nodes V_{CT1} and V_{DDH} will be charged to 10V and 9.3V (V_{CT1}–V_F) separately, thus the entire converter will enter steady-state by the start-up process.

The proposed hybrid input-parallel output-series boost converter is fabricated in a 0.18μm BCD process. Figure 8.10.4 (top left) shows the measured steady-state waveforms under different frequencies with VCR of 30. The converter realizes V_{OUT}=150V and P_{OUT} =900mW with V_{IN}=5V, f_{SW}=2.5MHz and L=2.2μH with 4-stage voltage multiplier. The output ripple at V_{OUT} is 4V (2.67% of V_{OUT}) and the output voltages of the SP-SC and boost converter are 24V and 40V, respectively. Figure 8.10.4 (top right) gives the measured switching node waveforms verifying the voltage stress of 5V across all capacitors of the SP-SC, and 55V across all capacitors of the VM. Figure 8.10.4 (bottom) shows the key node waveforms of the three phases during the start-up process, which are CLK on, V_{DD} on and V_{DDH} on. The circuit realizes self-starting and is consistent with the previous discussion.

Figure 8.10.5 shows the peak efficiency, maximum output power and V_{OUT} plots. The converter realizes maximum output power P_{OUT} =1200mW with V_{OUT}=150V and V_{IN}=5V using a 4-stage VM, and maximum P_{OUT} =1380mW with the same parameters and a 5-stage VM. Figure 8.10.5 (top right) shows that the output voltage in open-loop of the proposed converter decreases with increasing frequency. Theoretically, there is no limit for the maximum V_{OUT} of the proposed converter by increasing the number of VM stages. We observed V_{OUT}=280V with 6 VM stages, and V_{OUT} would keep going up with more VM stages. When the output voltage is not regulated, the proposed converter can achieve a maximum power output of 1.61W at V_{OUT}=100V and V_{IN}=5V with a 4-stage voltage multiplier, as shown in Fig. 8.10.5 (bottom left). And the proposed converter can achieve a maximum efficiency of 80% at V_{OUT}=109V and P_{OUT}=950mW.

Figure 8.10.6 provides performance comparisons between the proposed converter and state-of-the-art designs [1–6]. The proposed converter can greatly increase the VCR and reduce the voltage stress of components by the input-parallel output-series structure, thereby significantly reducing the size and weight of the components (the L is reduced by >50× down to 2.2μH and no need for C_{bypass}). The proposed converter achieves 2.6× higher volumetric power density and 3.9× higher gravimetric power density. And the presented design has the highest switching frequency and peak power efficiency. Figure 8.10.7 shows a die micrograph and component breakdown. Total die area is 2.24mm^2.

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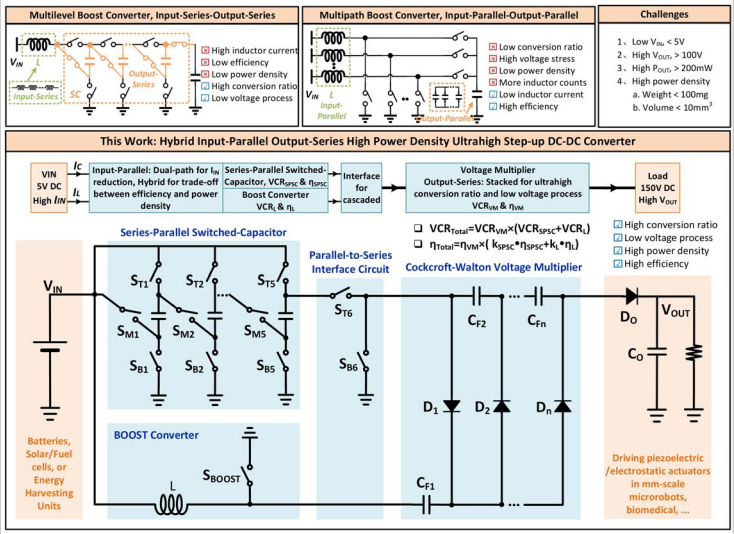


Figure 8.10.1: Proposed Input-Parallel Output-Series Hybrid DC-DC Boost Converter.

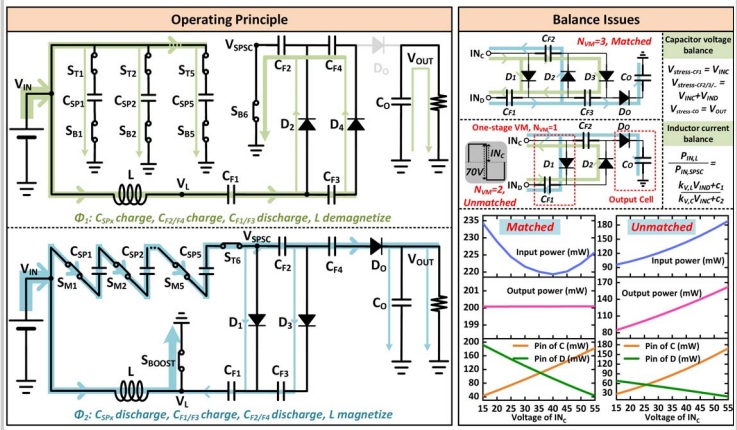


Figure 8.10.2: Operation principle, capacitor voltage and inductor current balance issues.

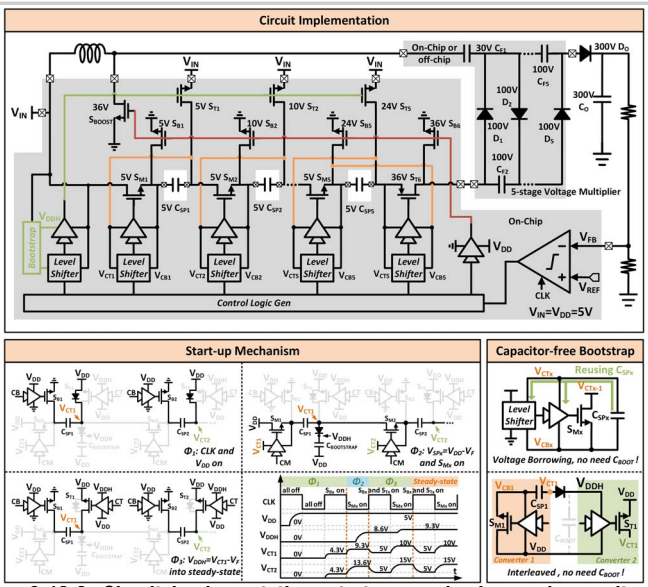


Figure 8.10.3: Circuit implementation, start-up mechanism and capacitor-free bootstrap circuit.

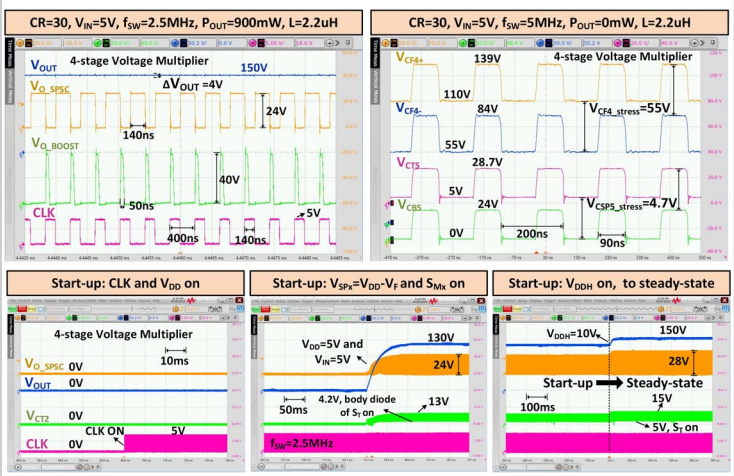


Figure 8.10.4: Measured start-up, steady-state and voltage stress of capacitors waveforms.

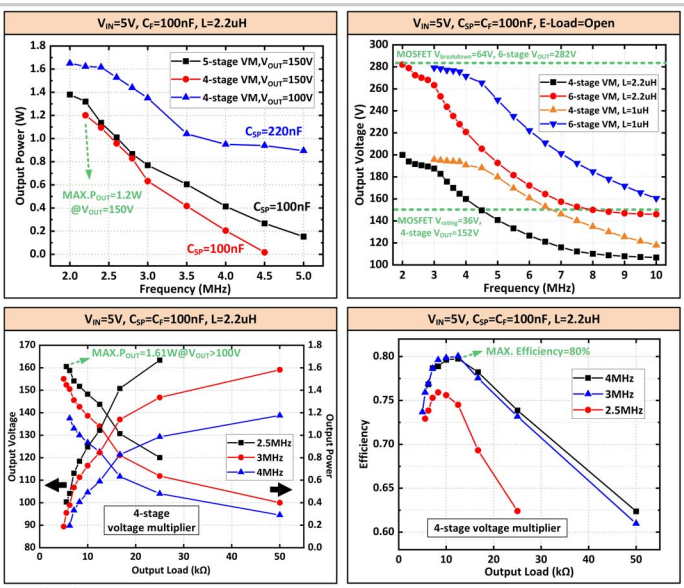
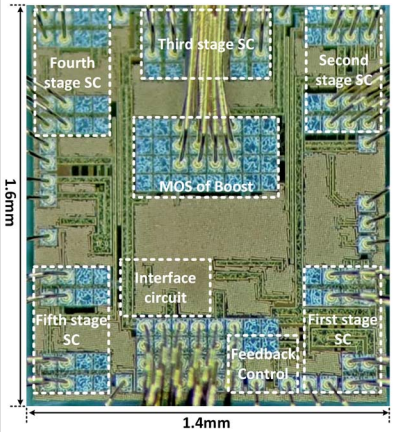


Figure 8.10.5: Measured maximum output power, output voltage compared to rated and breakdown limits and power efficiency.

	TPE'18 [1]	ADI LT8365 [2]	TI TPS61390 [3]	ECCE'19 [4]	ISSCC'21 [5]	ISSCC'23 [6]	This Work
Topology	Boost-Flyback	Boost and Voltage Multiplier	Boost	DC-AC-DC	Switched Capacitor	Single Chip Switched-Capacitor with Boost	Hybrid Input-Parallel-Output-Series
Process (nm)	800nm BCD	NA	NA	Discrete	1μm SOI BCD	180nm SOI BCD	**180nm BCD**
Die Area (mm²)	2.6mm×2.4mm	5mm×4mm	3mm×3mm	NA	4mm×1.46mm	1.5mm×1.14mm	**1.6mm×1.4mm**
Process V_{MAX} (V)	300	150	85	NA	20	32	**36**
V_{IN} (V)	3.7	9-30	2.5-5.5	3.7	16 - 20	3.7	**5**
V_{OUT} (V)	100-300	-250/250	85	2700	$V_{OUT,PP}$ -300	$V_{OUT,PP}$ -300	**150**
VCR	81	28	34	730	15	81	**30**
$F_{SW,MAX}$ (kHz)	150	100-500	700	0.04	1	>30	**2500**
Feedback control	PFM	PSM	PWM	NA	Digital		**PFM**
Passive components	6.2μH, 300μH	10μH, 1206 C_F×4	4.7uH	2.9μH, 351μH, 4.7μF C_{Bypass}, 0603 C_{Couple}×10, 0201 C_F×109	0402 C_F×16	100μH, 27μF C_{Bypass}, 0402 C_F ×16	**2.2μH, 01005 C_{SP}×5, 0402 C_F×4**
Weight[2] (mg)	40	200	NA	178.6	49.6	76	**15.7**
Volume[2] (mm³)	12.5	71.2	383	35.5	9.4	15	**4.7**
Power Density[2] mW/mg	9.8	12.5	NA	0.9	8.1	19.7	**76.4**
Power Density[2] mW/mm³	31	35	0.78	4.6	42.6	100	**255**
P_{OUT} (mW)	390	10mA	300	162	400	1500	**1200**
Peak Efficiency	72%	75%	62%	34%	NA[1]	NA[1]	**80%**

(1) Design was characterized with capacitor load; therefore, reactive power and efficiency are reported (different from other designs)
(2) Metrics are based on passive component weight & volume only

Figure 8.10.6: Performance comparison with the state-of-the-art designs.



V_{IN}=5V, V_{OUT}=150V with 4-stage voltage multiplier			
Process	0.18um BCD		
Off-chip Devices	Flying Cap×5 (01005, 0.1/0.22μF, 5V)	0.4mm×0.2mm ×0.2mm×5	0.08mg×5
	Flying Cap×4 (0402, 0.1μF, 100V)	1mm×0.5mm× 0.5mm×4	1.2mg×4
	PFL1609-222 (2.2μH, 400mΩ)	1.8mm×0.95m m×1.07mm	6mg
	BAS16L Diode ×4 (100V, 0402C)	1mm×0.5mm× 0.6mm×4	0.83mg×4
	BAS521 (300V, SOD523)	0.8mm×1.3mm ×0.6mm	1.2mg
	Total	4.7mm^3	15.72mg
Die Area	Total Area	2.24mm^2	
	Used Area	1.2mm^2	

Figure 8.10.7: Annotated die micrograph and implementation breakdown.

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