ENTC
Electronic and Telecommunication Engineering

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Department of Electronic and Telecommunication Engineering

University of Moratuwa, Sri Lanka

This is to certify that

K. A. W. T. Kodithuwakku

has participated in the 64-hour short course on

SystemVerilog for ASIC/FPGA Design & Verification

conducted by the Department of Electronic & Telecommunication Engineering,

University of Moratuwa, Sri Lanka

For online verification

Course Coordinator

Head
Dept. of Electronic & Telecommunication Engineering

30 April 2023

Short Course Outline

This short course is on SystemVerilog for ASIC/FPGA Design & Verification.

The following were covered:

- Introduction to HDLs
- Design & Verification of 9 example designs:
  - 1-bit adder
  - N-bit adder: parametrization
  - Combinational ALU: Verification with classes
  - Counter
  - Functions, look up tables & decoders
  - FIR filter: retiming
  - Parallel to serial converter: AXI-Stream, randomized verification
  - UART receiver & transmitter
  - Matrix vector multiplier: advanced parameterization, transactional testbenches
- Bus protocols with AXI Stream
- Converting any module to AXI Stream
- Assembling a full system: UART + AXIS + Matrix vector multiplier
- ASIC flow: synthesis, place & route using Synopsys Design Compiler & IC Compiler
- SystemVerilog best practices to write clean & readable design code
- CI/CD: automated verification with GitHub actions
- Implementing a full system on FPGA; sending inputs, receiving outputs, comparing with expected outputs using Python
- Tips for advanced projects

Assignments: completion of at least three out of the following four assignments required to be eligible for the course completion certificate

- AXI stream accumulator
- Cleaning up SystemVerilog code following best practices
- ASIC synthesis, place & route of a full system using Synopsys tools
- FPGA implementation and testing of a full system

Dates: 12th February 2023 to 23rd April 2023 (17 sessions)
6:00 p.m. – 10:30 p.m. on Saturdays and 9:00 a.m. – 11:00 a.m. on Sundays

Venue: Online lectures & office hours, physical lab session for FPGA implementation