

# And gate

project\_and - [C:/sv course ass/maxpool\_Ass2/project\_and/project\_and.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator

- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

ELABORATED DESIGN - xc7z010clg400-1 (active)

Elaborated Design is out-of-date. Constraints were modified. details Reload

Sources

- Design Sources (1)
  - test\_and (test\_and.sv)
- Constraints (1)
  - constrs\_1 (1)
    - Zybo-Master.xdc
- Simulation Sources (1)
  - Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

Zybo-Master.xdc

Enabled

General Properties

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

- ☐ Open Implemented Design
- ☐ View Reports
- ☒ Open Hardware Manager
- ☐ Generate Memory Configuration File
- ☐ Don't show this dialog again

OK Cancel

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	synth_design Complete!								1	0	0.00	0	0	4/23/23, 10:07 AM	00:00:20	Vivado Synthesis Default
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	0.809		0	1	0.00	0	0	4/23/23, 10:08 AM	00:00:42	Vivado Implementation Default

Source File: Zybo-Master.xdc

Type here to search

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project\_and - [C:/sv course ass/maxpool\_Ass2/project\_and/project\_and.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access

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HARDWARE MANAGER - localhost/xilinx\_tcf/Diogenet/210279545026A

There are no debug cores. Program device Refresh device

Hardware

Name	Status
localhost (1)	Connect
xilinx_tcf/Diogenet/210279545026A	Open
arm_dap_0 (0)	N/A
xc7z010_1 (1)	Not programmed

Properties

Select an object to see properties

test\_and.sv

C:/sv course ass/maxpool\_Ass2/project\_and/project\_and/srcs/sources\_1/new/test\_and.sv

```
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21
22
23 module test_and(
24     input logic a,b,
25     output logic out
26 );
27
28     assign out = a&b;
```

Tcl Console

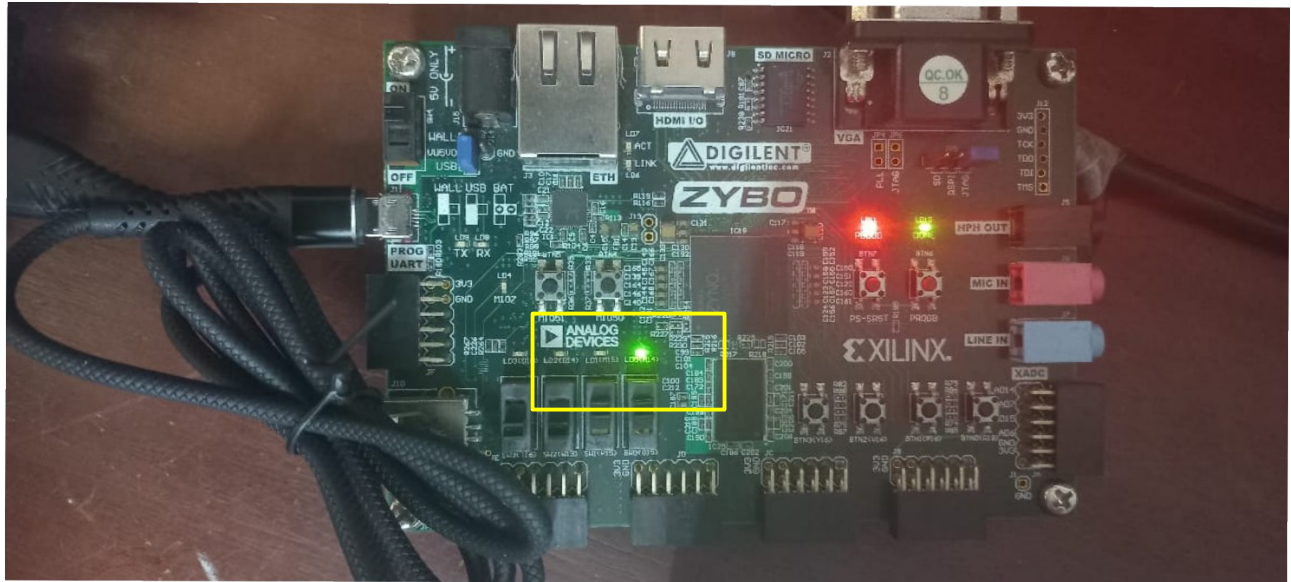
```
current_hw_device [get_hw_devices xc7z010_1]
refresh_hw_device -update_hw_probes false [lindex [get_hw_devices xc7z010_1] 0]
INFO: [Labtools 27-1435] Device xc7z010 (JTAG device index = 1) is not programmed (DONE status = 0).
```

Type a Tcl command here

Type here to search

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Showing the input high on the FPGA only when the both a and b pins are high in



**step-by-step process for running RTL code on a Zybo board using Vivado:**

1. Open Vivado and create a new project by clicking on "File" -> "New Project". Follow the prompts to select the project name, location, and target device. In this case, select the Zybo board as the target device.
2. Add your RTL code to the project by clicking on "File" -> "Add Sources". Select your RTL code files and add them to the project.
3. Create a new block design by clicking on "Create Block Design" under "Flow Navigator". Name the block design and add the Zybo board as a part.
4. Add your RTL code to the block design by clicking on "Add IP" in the block design diagram. Select "Add or create design sources" and add your RTL code files to the block design.
5. Generate the HDL wrapper by clicking on "Generate Output Products" in the block design diagram. Select "Generate RTL Sources" and "Create HDL Wrapper".
6. Generate the bitstream by clicking on "Generate Bitstream" under "Flow Navigator". Wait for the bitstream generation to complete.
7. Launch the hardware manager by clicking on "Open Hardware Manager" under "Flow Navigator". Connect the Zybo board to your computer using a USB cable.
8. In the hardware manager, click on "Open Target" and select the Zybo board. Then, click on "Program Device" and select the bitstream file you generated in step 6.
9. Click "Program" to program the bitstream onto the Zybo board. Wait for the programming to complete.

# Counter module

project\_counter - [C:/sv course ass/maxpool\_Ass2/project\_counter/project\_counter.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access Ready

Flow Navigator PROJECT MANAGER - project\_counter

- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

Sources

- Design Sources (2)
  - counter\_wrapper (counter\_wrapper.sv) (2)
    - Counter\_1: counter (counter.sv)
    - Divider\_1: xil\_defaultlib.divider
  - test\_counter (test\_counter.sv)

Hierarchy Libraries Compile Order

Source File Properties

Counter.xdc

Enabled

Location: C:/systemverilog-master/systemverilog-master/rtl/counter\_wrapper.sv

Type: XDC

General Properties

Project Summary counter\_wrapper.sv counter.sv Counter.xdc

C:/systemverilog-master/systemverilog-master/rtl/counter\_wrapper.sv

```
1 module counter_wrapper(  
2     input logic board_clk, rst, incr,  
3     output logic [3:0] count_reg  
4 );  
5  
6     wire clk;  
7  
8     counter #(.WIDTH(4)) Counter_1 (.*);  
9     divider #(.FREQ(1)) Divider_1 (.*) // FREQ set to 1 Hz  
10  
11 endmodule  
12
```

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)

1:0 Insert SystemVerilog

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project\_counter - [C:/sv course ass/maxpool\_Ass2/project\_counter/project\_counter.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access Synthesis and Implementation Out-of-date details

Flow Navigator PROJECT MANAGER - project\_counter

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG

Sources

- Design Sources (2)
  - counter\_wrapper (counter\_wrapper.sv) (2)
    - Counter\_1: counter (counter.sv)
    - Divider\_1: divider (divider.sv)
  - test\_counter (test\_counter.sv)

Hierarchy Libraries Compile Order

Source File Properties

counter\_wrapper.sv

Enabled

Location: C:/systemverilog-master/systemverilog-master/rtl/counter\_wrapper.sv

Type: SystemVerilog

General Properties

Project Summary counter\_wrapper.sv counter.sv Counter.xdc

C:/systemverilog-master/systemverilog-master/rtl/counter\_wrapper.sv

```
1 module counter_wrapper(  
2     input logic board_clk, rst, incr,  
3     output logic [3:0] count_reg  
4 );  
5  
6     wire clk;  
7  
8     counter #(.WIDTH(4)) Counter_1 (.*);  
9     divider #(.FREQ(1)) Divider_1 (.*) // FREQ set to 1 Hz  
10  
11 endmodule  
12
```

Tcl Console Messages Log Reports Design Runs

```
Run output will be captured here: C:/sv course ass/maxpool_Ass2/project_counter/project_counter.runs/synth_1/runme.log  
[Sun Apr 23 10:40:18 2023] Launched impl_1...  
Run output will be captured here: C:/sv course ass/maxpool_Ass2/project_counter/project_counter.runs/impl_1/runme.log  
add_files -norecurse C:/systemverilog-master/systemverilog-master/rtl/divider.sv  
update_compile_order -fileset sources_1
```

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## mvm\_uart\_system

A matrix-vector multiplier is an operation that takes a matrix and a vector as inputs, and produces a vector as output. The output vector is obtained by multiplying each row of the matrix by the corresponding element of the input vector, and then summing the results.

UART+AXIS streams are also used on the final system of mvm\_uart\_system.

project\_mvm - [C:/sv course ass/maxpool\_Ass2/project\_mvm/project\_mvm.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Flow Navigator PROJECT MANAGER - project\_mvm

PROJECT MANAGER

- Settings
  - Add Sources
  - Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
    - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
    - Open Implemented Design
- PROGRAM AND DEBUG

Sources

- Design Sources (1)
  - fpga\_module (fpga\_module.sv) (1)
- Constraints
- Simulation Sources (1)
- Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

fpga\_module.sv

Enabled

Location: C:/sv course ass/maxpool\_Ass2/proj

Type: SystemVerilog

General Properties

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy
synth_1		Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)

Source File: fpga\_module.sv

23:0 Insert SystemVerilog

Type here to search

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## utilization reports of synthesis

project\_mvm - [C:/sv course ass/maxpool\_Ass2/project\_mvm/project\_mvm.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access Implementation Complete

Flow Navigator SYNTHESIZED DESIGN - xc7z010clg400-1 (active)

Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Set Up Debug
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic

IMPLEMENTATION

- Run Implementation
- Open Implemented Design
  - Constraints Wizard

Sources

- Netlist
  - fpga\_module
    - Nets (9)
    - Leaf Cells (5)
      - mvm\_uart\_system\_0 (mvm\_uart\_system)

Source File Properties

fpga\_module.sv

General Properties

Tcl Console Messages Log Reports Design Runs Utilization Timing

Hierarchy

Name	Slice LUTs (17600)	Slice Registers (35200)	Bonded IOB (100)	BUFCTRL (32)
fpga_module	5271	3373	4	1
mvm_uart_system_0 (mvm_uart_system)	5271	3373	0	0

utilization\_1

Type here to search

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project\_mvm - [C:/sv course ass/maxpool\_Ass2/project\_mvm/project\_mvm.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access

Implementation Complete ✓

Default Layout

Flow Navigator

- Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS**
  - Run Synthesis
  - Open Synthesized Design**
    - Constraints Wizard
    - Edit Timing Constraints
    - Set Up Debug
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
    - Constraints Wizard

SOURCES Netlist x

- fpga\_module
  - Nets (9)
  - Leaf Cells (5)
  - mvm\_uart\_system\_0 (mvm\_uart\_system)

Source File Properties

fpga\_module.sv

General Properties

Project Summary x Device x fpga\_module.sv x

utilization\_1

Tcl Console Messages Log Reports Design Runs Utilization x Timing

Hierarchy

Name	Slice LUTs (17600)	Slice Registers (35200)	Bonded IOB (100)	BUFGCTRL (32)
fpga_module	5271	3373	4	1
mvm_uart_system_0 (mvm_uart_system)	5271	3373	0	0

Windows Taskbar: 90°F Mostly sunny 12:17 PM 4/23/2023

project\_mvm - [C:/sv course ass/maxpool\_Ass2/project\_mvm/project\_mvm.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access

Implementation Complete ✓

Default Layout

Flow Navigator

- Open Elaborated Design
- SYNTHESIS**
  - Run Synthesis
  - Open Synthesized Design**
    - Constraints Wizard
    - Edit Timing Constraints
    - Set Up Debug
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- IMPLEMENTATION**
  - Run Implementation
  - Open Implemented Design**
    - Constraints Wizard
    - Edit Timing Constraints
    - Report Timing Summary
    - Report Clock Networks

SOURCES Netlist x

- fpga\_module
  - Nets (9)
  - Leaf Cells (5)
  - mvm\_uart\_system\_0 (mvm\_uart\_system)

Source File Properties

Select an object to see properties

Project Summary x Device x fpga\_module.sv x

Timing

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Check Timing (11159)

User Ignored Paths

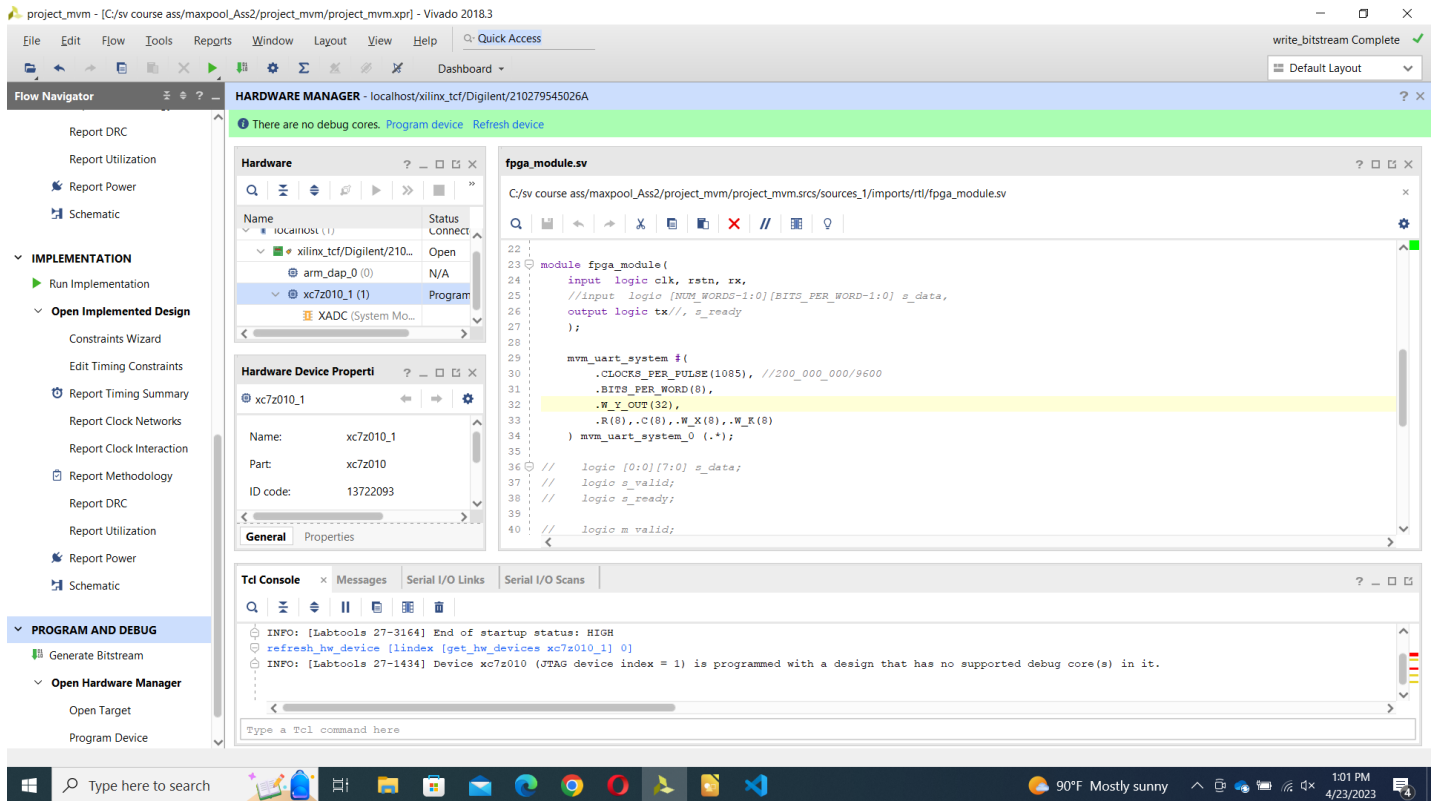
Unconstrained Paths

Timing Summary - impl\_1 (saved)

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): NA	Worst Hold Slack (WHS): NA	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA	Total Hold Slack (THS): NA	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA	Number of Failing Endpoints: NA	Number of Failing Endpoints: NA
Total Number of Endpoints: NA	Total Number of Endpoints: NA	Total Number of Endpoints: NA

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## Successfully upload the code to the zybo fpga given in the lab



## Some of the Final resultss of the mvm\_uart system

