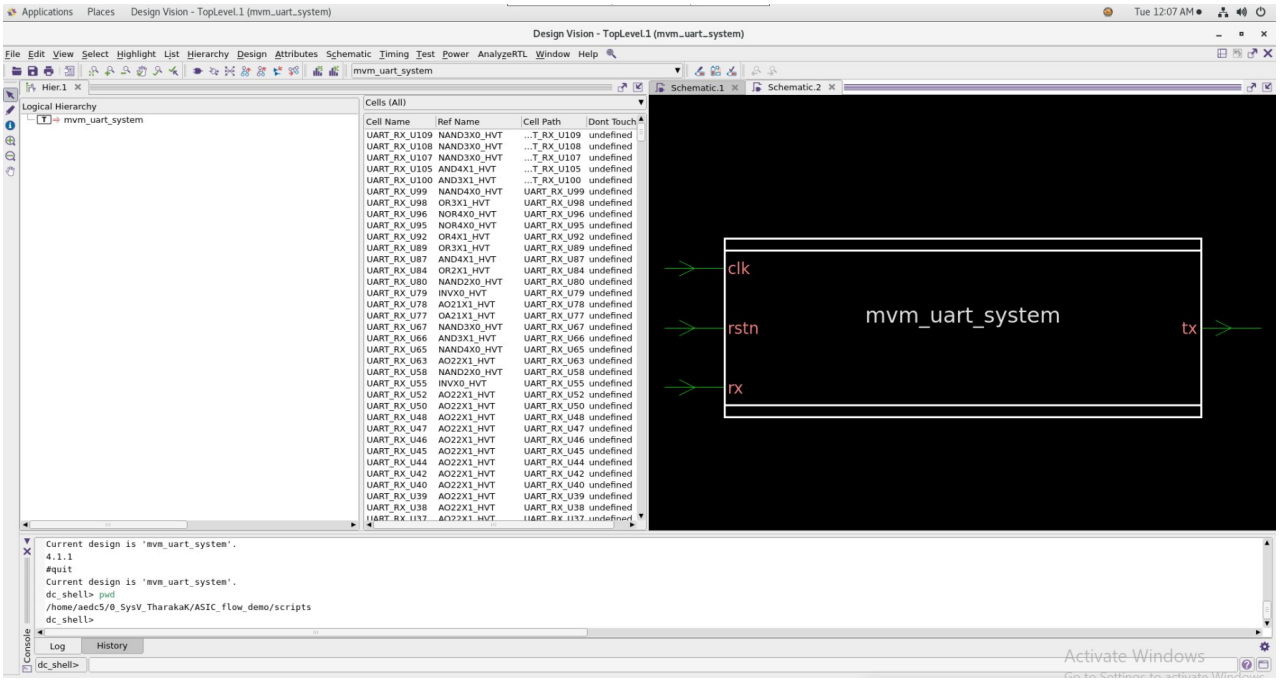
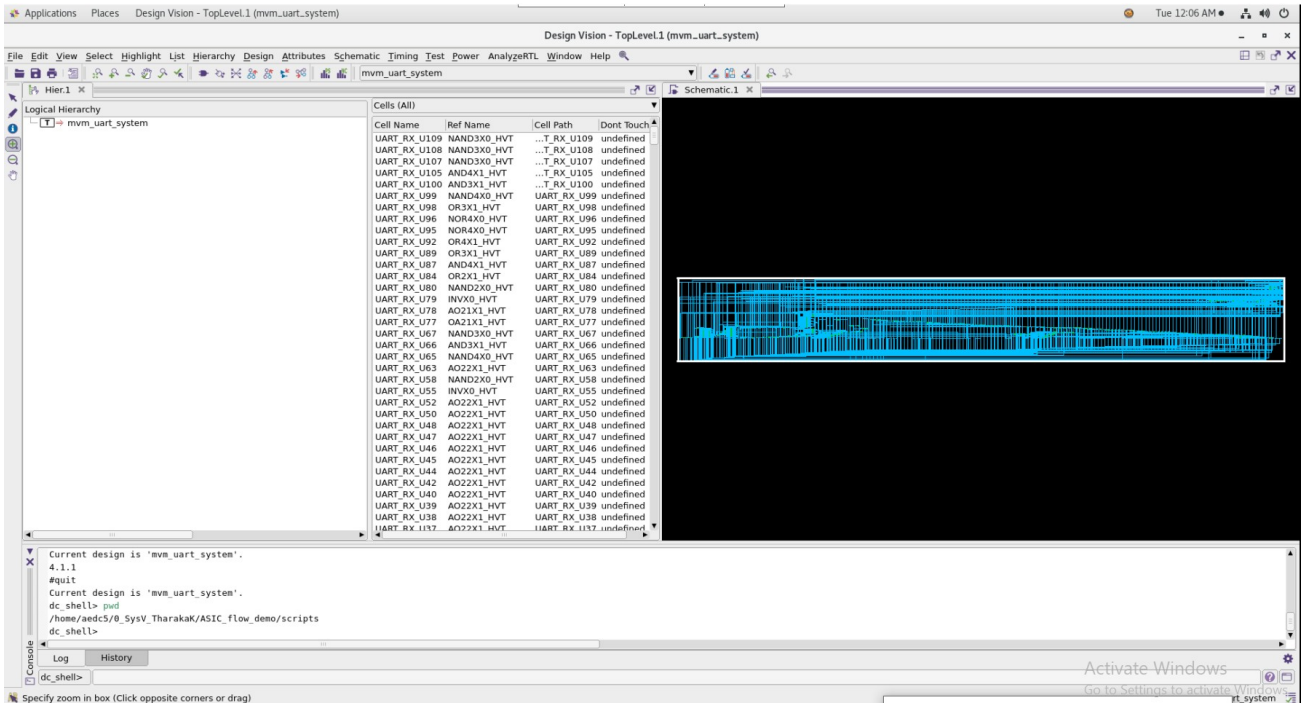
Assignment 03

Tharaka Kodithuwakku
ENTC20
200102603536

Named used on the folder : 0_SysV_TharakaK



The synthesized RTL design schematic visualized in Design Vision of DC



The reports contain information

Area_Report

Total area = 4816.39 um^2

Open | mvm_uart_system_area.rpt | ~/0_SysV_TharakaK/ASIC_flow_demo/report | Save

```
****************************************
Report : area
Design : mvm_uart_system
Version: T-2022.03-SP5-1
Date   : Mon Apr 17 23:58:59 2023
****************************************

Library(s) Used:

    saed32hvt_ss0p7v125c (File: /home/aedc5/libs/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_nldm/
saed32hvt_ss0p7v125c.db)

Number of ports:                          4
Number of nets:                        1068
Number of cells:                        923
Number of combinational cells:          612
Number of sequential cells:             310
Number of macros/black boxes:             0
Number of buf/inv:                      119
Number of references:                    51

Combinational area:               1728.941639
Buf/Inv area:                      394.177350
Noncombinational area:            2163.527918
Macro/Black Box area:                0.000000
Net Interconnect area:             923.917724

Total cell area:                  3892.469557
Total area:                       4816.387281
1
```

Plain Text | Tab Width: 8 | Ln 1, Col 1 | INS

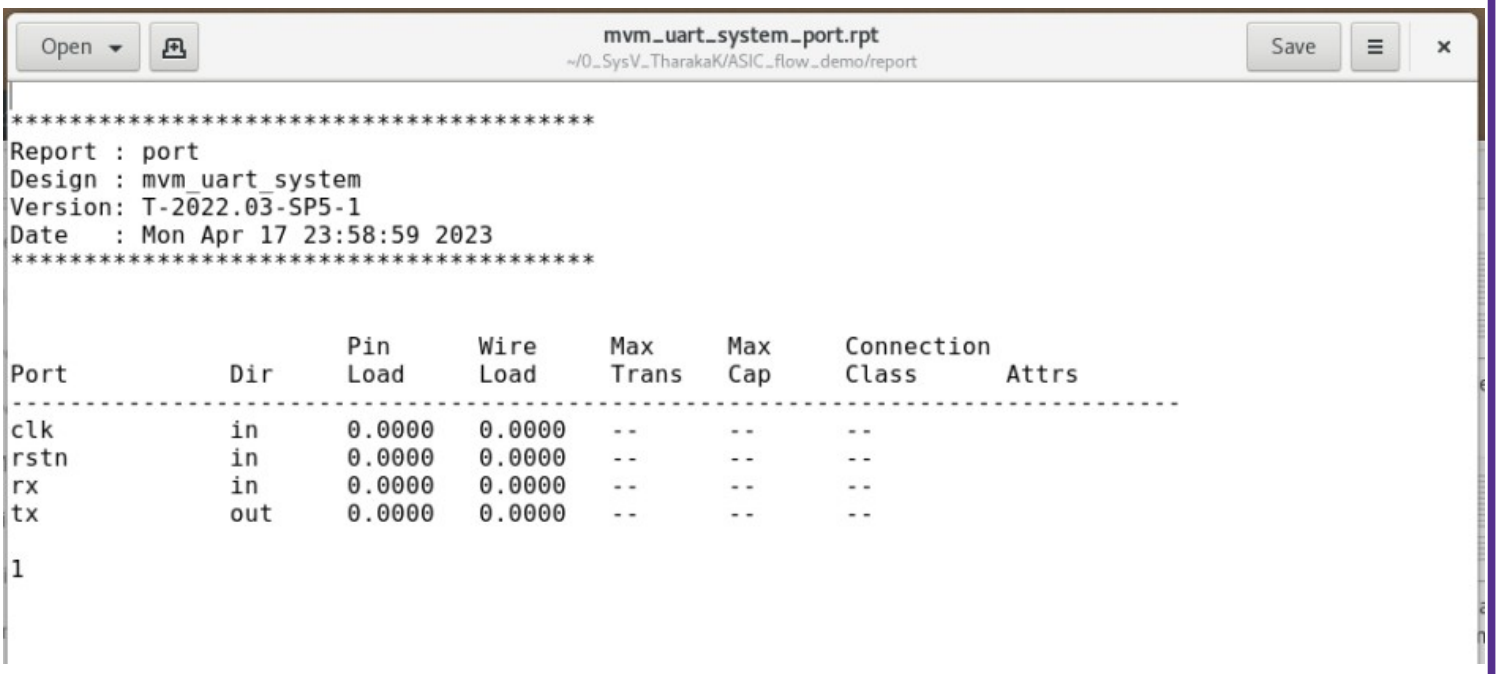
Area Reference Report

```
------------------------------------------------------------------------
Total 51 references                                   3892.469557
```

Cell Report

```
                                                                  7.116032  n
UART_TX_state_reg_24_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
UART_TX_state_reg_25_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
UART_TX_state_reg_26_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
UART_TX_state_reg_27_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
UART_TX_state_reg_28_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
UART_TX_state_reg_29_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
UART_TX_state_reg_30_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
UART_TX_state_reg_31_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                                  7.116032  n
--------------------------------------------------------------------------------
Total 922 cells                                                   3892.469557
1
```

Port Report




```
****************************************
Report : port
Design : mvm_uart_system
Version: T-2022.03-SP5-1
Date   : Mon Apr 17 23:58:59 2023
****************************************


                    Pin      Wire     Max      Max      Connection
Port          Dir   Load     Load     Trans    Cap      Class      Attrs
--------------------------------------------------------------------------------
clk           in    0.0000   0.0000   --       --       --
rstn          in    0.0000   0.0000   --       --       --
rx            in    0.0000   0.0000   --       --       --
tx            out   0.0000   0.0000   --       --       --

1
```

Power Report

Open ▾ | mvm_uart_system_power.rpt — ~/0_SysV_TharakaK/ASIC_flow_demo/report | Save

```
Operating Conditions: ss0p7v125c   Library: saed32hvt_ss0p7v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
mvm_uart_system        8000              saed32hvt_ss0p7v125c


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   1.4768 mW   (98%)
  Net Switching Power  =  25.1597 uW    (2%)
                         ---------
Total Dynamic Power    =   1.5020 mW  (100%)

Cell Leakage Power     =  26.4171 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
---------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network  1.4512e+03           0.0000              0.0000         1.4512e+03  (  94.95%)  i
register           3.1416           0.6379          1.1574e+07            15.3546  (   1.00%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational     22.5152          24.5218          1.4844e+07            61.8805  (   4.05%)
---------------------------------------------------------------------------------------------------
Total          1.4768e+03 uW       25.1597 uW       2.6417e+07 pW      1.5284e+03 uW
1
```

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Time Report

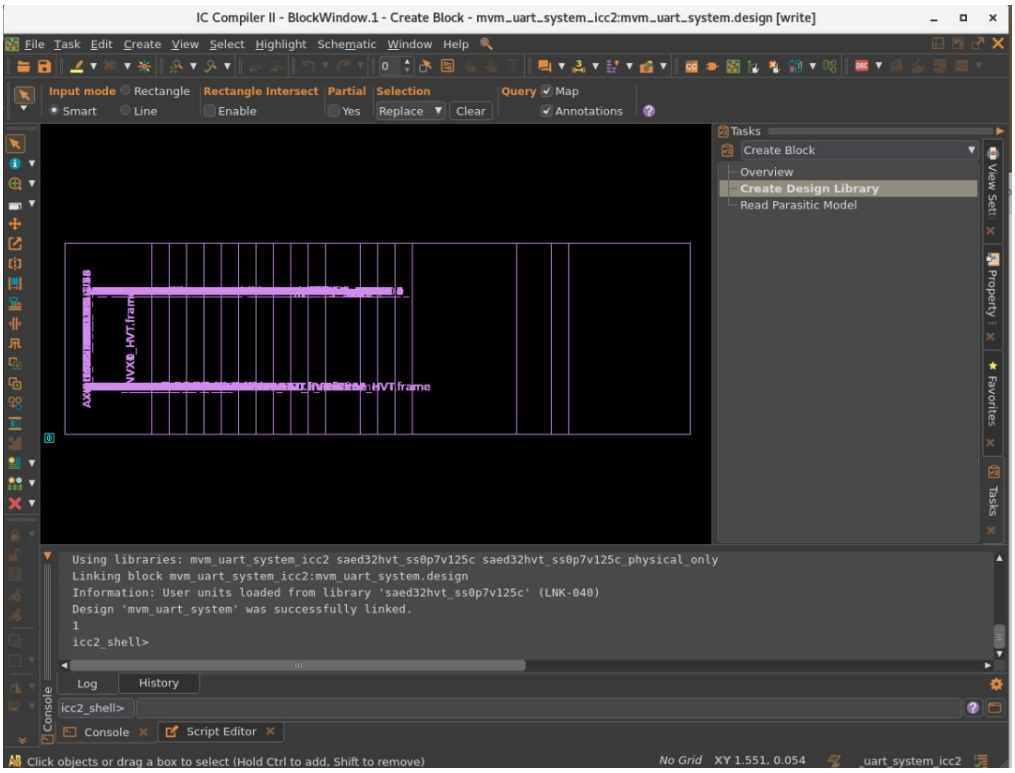
Negative slack timing violation
All looks almost similar

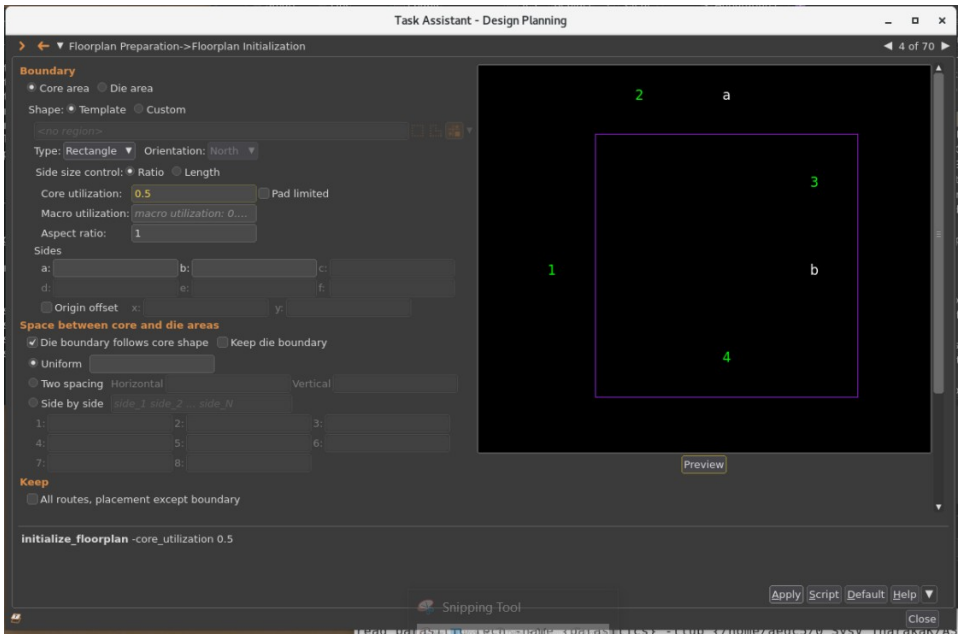
Applications Places Text Editor

Open

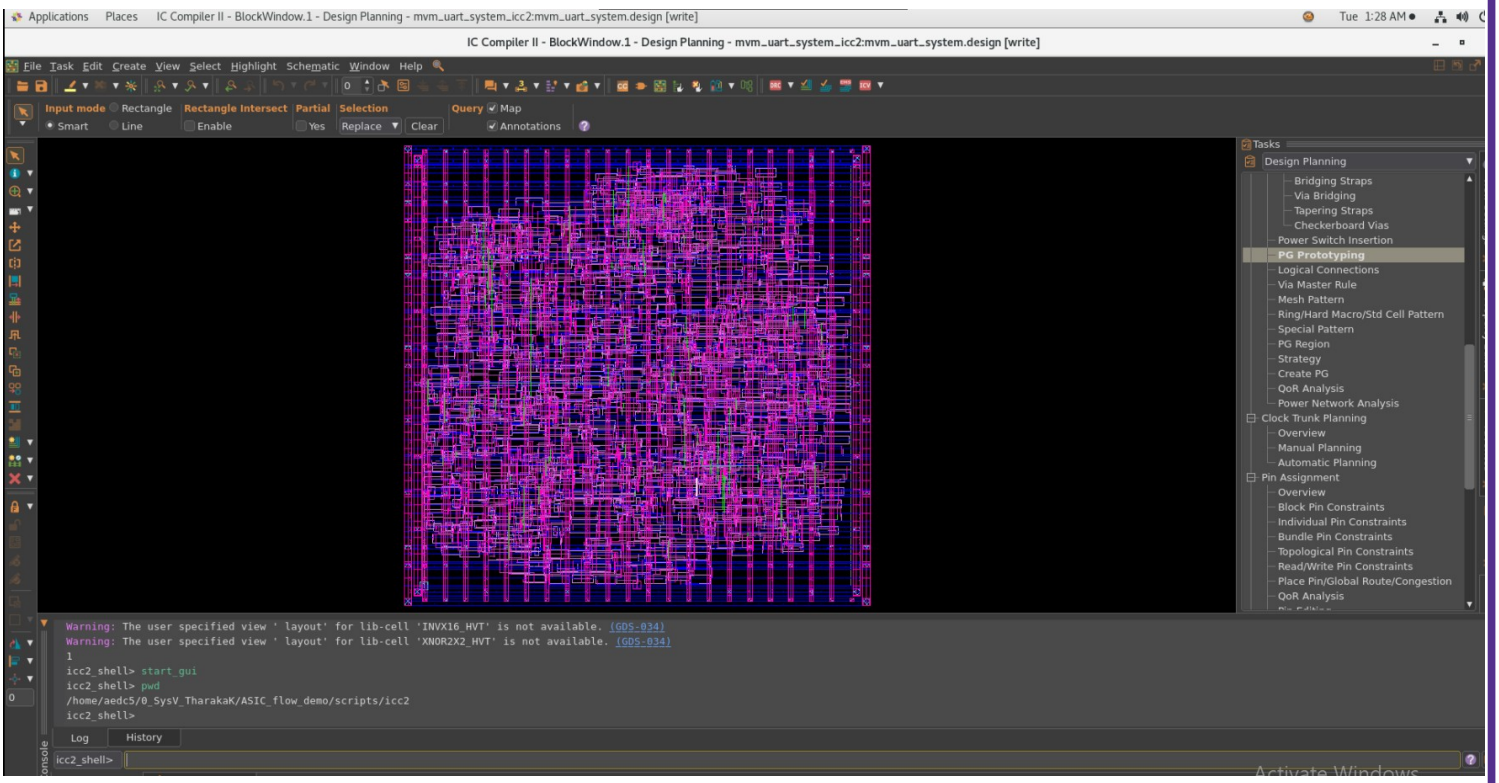
mvm_uart_system_timing.rpt
~/0_SysV_TharakaK/ASIC_flow_demo/report

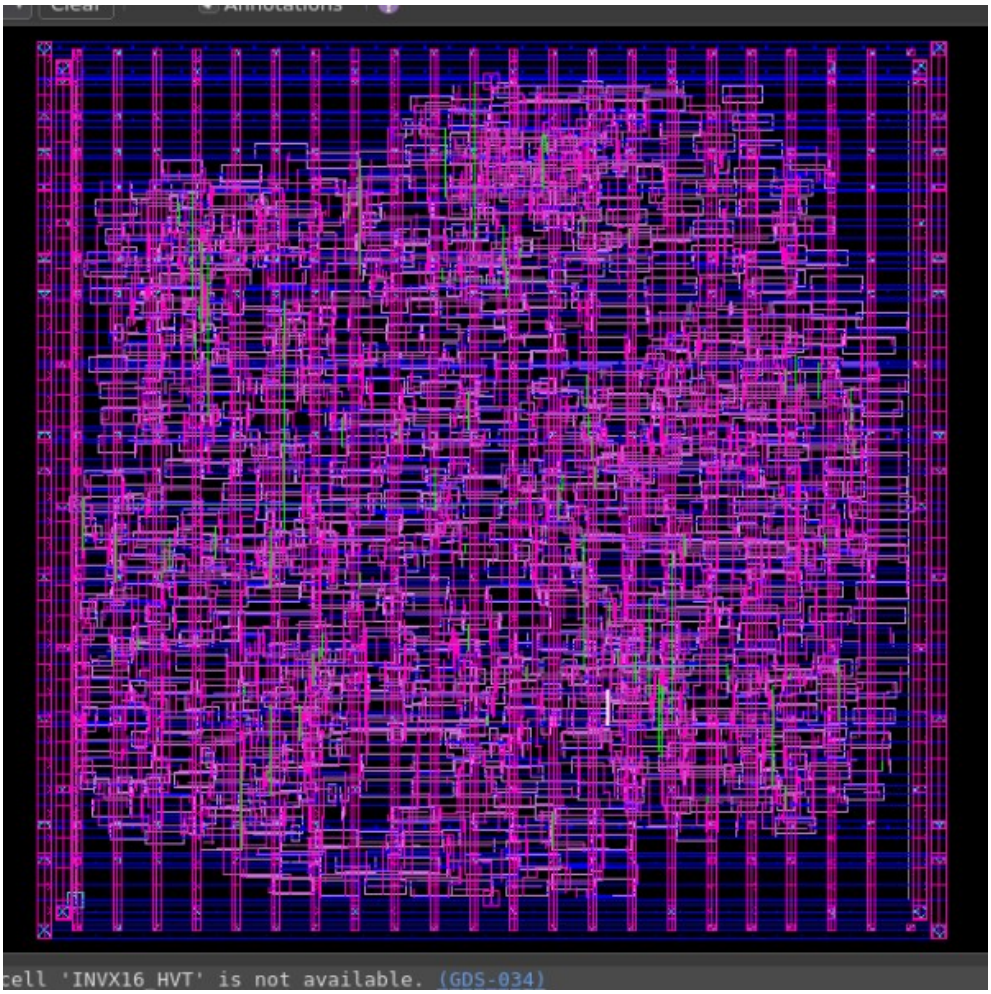
```
slack (VIOLATED)                                                                -3.678


Startpoint: UART_TX_state_reg_30_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: UART_TX_m_packets_reg_11_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
mvm_uart_system    8000                  saed32hvt_ss0p7v125c

Point                                   Fanout       Cap     Trans      Incr       Path
-------------------------------------------------------------------------------------------
clock clk (rise edge)                                                   0.000      0.000
clock network delay (ideal)                                             0.000      0.000
UART_TX_state_reg_30_/CLK (DFFARX1_HVT)                         0.000   0.000      0.000 r
UART_TX_state_reg_30_/QN (DFFARX1_HVT)                          0.172   0.508      0.508 r
n107 (net)                               1        0.486                 0.000      0.508 r
U122/Y (NAND4X0_HVT)                                            0.307   0.420      0.929 f
UART_TX_n219 (net)                       1        0.481                 0.000      0.929 f
U150/Y (NOR4X1_HVT)                                             0.113   0.781      1.709 r
UART_TX_n215 (net)                       3        1.293                 0.000      1.709 r
U30/Y (AND4X1_HVT)                                              0.305   0.576      2.286 r
m_ready (net)                           11        5.239                 0.000      2.286 r
U136/Y (AO21X2_HVT)                                             0.319   0.747      3.032 r
n114 (net)                              19        8.915                 0.000      3.032 r
U86/Y (AO22X1_HVT)                                              0.264   0.531      3.563 r
UART_TX_n3 (net)                        11        4.813                 0.000      3.563 r
UART_TX_U242/Y (AO221X1_HVT)                                    0.183   0.479      4.042 r
UART_TX_n440 (net)                       1        0.619                 0.000      4.042 r
UART_TX_m_packets_reg_11_/D (DFFASX1_HVT)                       0.183   0.000      4.042 r
data arrival time                                                                  4.042

clock clk (rise edge)                                                   0.700      0.700
clock network delay (ideal)                                             0.000      0.700
UART_TX_m_packets_reg_11_/CLK (DFFASX1_HVT)                             0.000      0.700 r
library setup time                                                     -0.336      0.364
data required time                                                                 0.364
-------------------------------------------------------------------------------------------
data required time                                                                 0.364
data arrival time                                                                 -4.042
-------------------------------------------------------------------------------------------
slack (VIOLATED)                                                                  -3.678
```


IC Compiler II - BlockWindow.1 - Create Block - mvm_uart_system_icc2:mvm_uart_system.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Input mode Rectangle Smart Line
Rectangle Intersect Enable
Partial Yes
Selection Replace Clear
Query Map Annotations
Tasks
Create Block
Overview
Create Design Library
Read Parasitic Model
Using libraries: mvm_uart_system_icc2 saed32hvt_ss0p7v125c saed32hvt_ss0p7v125c_physical_only
Linking block mvm_uart_system_icc2:mvm_uart_system.design
Information: User units loaded from library 'saed32hvt_ss0p7v125c' (LNK-040)
Design 'mvm_uart_system' was successfully linked.
1
icc2_shell>
Log History
icc2_shell>
Console Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY 1.551, 0.054


Task Assistant - Design Planning
Floorplan Preparation->Floorplan Initialization
4 of 70
Boundary
Core area Die area
Shape: Template Custom
Type: Rectangle Orientation: North
Side size control: Ratio Length
Core utilization: 0.5 Pad limited
Macro utilization:
Aspect ratio: 1
Sides
Origin offset
Space between core and die areas
Die boundary follows core shape Keep die boundary
Uniform
Two spacing Horizontal Vertical
Side by side
Keep
All routes, placement except boundary
initialize_floorplan -core_utilization 0.5
Preview
Apply Script Default Help
Close

The completed PnR layout visualized inside ICC2





The final exported GDSII file visualized using kLayout