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Low power and high speed 8x8 bit multiplier using non-clocked Pass Transistor Logic

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Abstract: In this paper we have analyzed an 8-bit multiplier circuit using non clocked pass gate families with help of carry save multiplier (CSA) technique. The multiplier cell of the adder is designed by using pass transistors (*n*-transistors), *p*-transistors used as cross-coupled devices. The adder cell is designed by using multiplexing control input techniques. A combination of *n*- and *p*-transistors used on the mirror logic and inverters of full adder circuit. These multipliers are useful in the portable battery operated multimedia devices for energy efficient. The 8 bit multiplier circuit has been simulated using microwind3 VLSI layout CAD tool. We have analyzed the power dissipation, propagation delay, PDP and EPI (energy per instruction) and compared our results with other pass transistor logics as well as published results. From the simulated results it was found that the power dissipation and propagation delay are low in our designed non-clocked pass transistor logics. Our multiplier circuit shows a power dissipation improvement of 97.6% from Amir *et.al* and 46.30%, 23.24% and 0.15% from Rizwan *et.al*. Our multipliers gives better propagation delay compared to Rizwan *et.al* that are89.56%, 88.39% and 88.31%

[Keywords: 8 bit multiplier, multiplexing control input techniques, power dissipation, propagation delay, VLSI CAD tools and Energy Per Instruction.]

1. Introduction

Multiplication is an important fundamental function in arithmetic logic operation. Since, multiplication dominates the execution time of most DSP algorithms; therefore high-speed multiplier is much desired [1]. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. With an ever-increasing quest for greater computing power on battery-operated mobile devices, design emphasis has shifted from optimizing conventional delay time area size to minimizing power dissipation while still maintaining the high performance [2]. The low power and high speed VLSI can be implemented with different logic style. The three important considerations for VLSI design is power area and delay. There are many proposed logics (or) low power dissipation and high speed and each logic style has its own advantages in terms of speed and power [3-4].

Pass-transistor logic is reported as another alternative logic that can enhance circuit performance [4]. Since can propagate signals using both the source and the gate, its high functionality can reduce the number of transistors in terms of multiplexing control input technique, which yields the high performance in the critical path [3-4]. As a PTL-based circuit can consist of only one type of MOS transistor (generally an nMOS transistor), it has a low node capacitance. As a result, PTL enables high-speed and low-power circuits [4].

This paper describes the design and simulation results of an 8-bit multiplier based on CMOS design rule for low power and high speed applications. Non clocked pass gate logic has been chosen to implement the 8-bit multiplier circuit. This multiplier circuit has full adder circuits, which are designed using multiplexing control input techniques [4-6]. We have compared our results with five pass gate logics in terms of speed, area energy per instruction and power dissipation. We have observed that the power dissipation and delay is reduced very much in the designed 8 bit multipliers circuits.

II. Circuit Architecture, Implementation And Layout

Our multiplier circuit has been designed using by carry save array multiplier (CSA) techniques. The basic architecture of the CSA multiplier is utilized half adder, AND gate and full adder blocks. The half adder comprised the EX-OR and AND gates which are implemented by pass transistor logic. One efficient implementation of the carry save array multiplier is the regular layout of the adder array [6]. This multiplier is well performed for unsigned/signed operands. The carry save array multiplier is designed using of all full adder circuit, which is for regularity of the structures. The full adder block is designed using by multiplexing control input technique. The multiplexing control input techniques has logical control of A and A', B and B' inputs into differential node is sum of the outputs and complement of sum. The input Cin and Cin' is adding the input of the differential node of sum and it's complement. The optional cross coupling of the PFET devices are the pull up of output devices whichever is high, from the $V_{DD} - V_T$ [6]. The logic tree does not pass any direct current after the latch sets. Since the inputs drive only the NMOS transistors, the input gat capacitance loading typically three times smaller than CMOS circuits, which require complementary NMOS and PMOS transistors to be driven [7]. If input has n variable, then we can use *n-1* as a control input signal and only one as input data. Write an expression to include the product terms of the control signals and ANDed with the result of the minimized sum of product expression (this will leave either 0, 1, input data, or input data'). The full adder designed using this method, which is reducing number of transistor tremendously [1, 6].

II.1 Architecture of 4-bit multiplier

The basic 4x4 bit carry save array multiplier is shown in Fig.1. All the partial products A and B are computed in parallel, and then collected through a cascade of Carry Save array multiplier technique. The output of the array is noted in Carry Save, so an additional adder converts it (by the mean of carry propagation) into the classical notation. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. [7]. Real time computer application require fast multiplication by utilizing And gates and full adders. Multiplication can be implemented on the processor much in the same way as it is done by hand. The carry save multiplier circuit analyzed for different non-clocked pass transistor adder techniques. The five type of non clocked adder circuit is shown

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in Fig. 2(a) to Fig. 2 (e). The CPL non clocked pass transistor logic adder circuits have two kinds of nodes that are differential node and swing restoration mode. The Swing Restored Pass Gate Logic (SRPL) has derived from the basic pass transistor logic full adder circuit, the pass gate restoration node of sum and its complement has connected with output CMOS inverter reciprocally. The DCVS logic with the pass gate is a means of extending the performance benefits associated with DCVSL into pass gate topologies. Static DCVSL is a differential style of logic requiring both true and complementary signals to be routed to gates. Two (sum, sum complement (or) carry, carry complement) complementary NFET switching trees are connected to cross-coupled PFET transistors. Depending on the differential inputs, one of the outputs is pulled down by the corresponding NFET network. The cross-coupled PFET transistors then latch the differential output. EEPL reduces power consumption and delay by interrupting the feedback of the latches forming the load circuit in the structure and allowing reduction in the width of the NFET devices which comprise the evaluate tree. The device width reduction further contributes to the power reduction. The circuit action simultaneously provides regenerative positive feedback, providing shorter delays than comparative CPL circuits. EEPL will be a valuable logic element in low power applications where performance is still essential. The Push – Pull Pass transistor Logic (PPPL) is a new innovation addressed of recovering full V_{DD} levels while still exploiting the speed of differential pass gate trees. Both styles, however, the PFET and NFET devices in the load circuit still must include output node for getting full rail voltage of output signal polarity. Push Pull (Pull up and Pull down resistor) gates tree of the output node makes the tree into a differential complementary pass gate function. The Single – Ended Pass Gate Logic (SEPG), concentrates on synthesizing the function of full logic blocks rather than individual logic functions. The other name for the single ended pass transistors is LEAP logic. The output of the full adder LEAN buffer circuit produces the output of the circuit. The specialized LEAN inverter is essentially a simple inverter with half-latched "keeper" PFET devices which brings the inverter input the rest of the way up from $V_{DD} - V_T$ to V_{DD}.

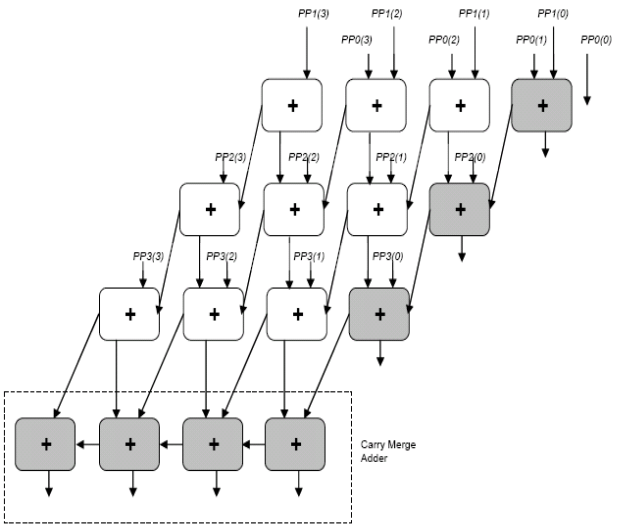

Fig. 1. 4x4 Carry save array multiplier

Assume that A and B are the two bit numbers where A is multiplicand and B is the multiplier. The multiplier circuit can be expressed as follows: [8]

$$A = \sum_{i=0}^{n-1} A_i 2^i \text{ -------- (1)}$$

$$B = \sum_{j=0}^{n-1} B_j 2^j \text{ -------- (2)}$$

The product of A and B is P and it can be written in the following form

$$P = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} A_i B_j e^{(i+j)} \text{ ------(3)}$$

To illustrate further, the multiplicand A and multiplier B can be represented as follows:

A Multiplicand $x_{n-1}x_{n-2}x_{n-3}\ldots.x_1x_0$
B Multiplier $y_{n-1}y_{n-2}y_{n-3}\ldots.y_1y_0$
P Product (A*B) $p_{2n-1}p_{2n-2}p_{2n-3}\ldots.p_1p_0$

Each of the partial product terms $P_n = A_iY_j$ is called the summand. Each partial product then gets stored in the arithmetic Logic Unit register, where it occupies memory space until the final partial product is obtained. [9]

III. Results And Discussions

The 5 types of pass gate multiplier circuit had designed and verified using DSCH3 CAD tools and the layout design and simulation are taken by the microwind 3 CAD tool. The propagation delay is calculated for worst-case pattern from11111111x10000000 to 11111111x11111111. The output maximum, average currents, power dissipation and delays are calculated at P15, which has the critical path output [10-11]. The propagation delay, power dissipation and power delay product (PDP) is determined for the various CMOS design rule feature size such as 0.12µm, 0.18µm, 0.25µm and 0.35µm. Our simulated result for various pass logic, using multiplexing control input technique as given in table I, which is clearly suggests that the power consumption, propagation delay and power delay product all are very low for designed circuit than other pass logic irrespective of the gate length. This shows the superiority of our designed circuit. The number of transistor reported to be 416 in our 4x4 multiplier circuit whereas Rakshith Krishnappa et.al [10] has used 528 transistors to implement only a 4-bit multiplier circuit using CPL. From the table I, it is clear that the CPL is more dominant in terms of power dissipation and propagation delays. Due to cross-coupling of inverter in the output node terminal, the CPL has logic transition from low to high (or) high to low is faster and consumed energy is low. The CPL circuits are dominant in ultra Deep Sub Micron process, due to shrinkage of wire capacitance, load capacitance and stray capacitances.

The high speed and low power Carry Save Array multipliers provides an improved functionality due to the implementation of the sum and carry processing logic, improved performance and improved power usage. The process of multiplying two numbers, A and B, requires the generation of a set of partial products followed by the sum of these partial products. The carry save array multiplier is used in the DSP circuit for increased speed of execution of data instruction. Code transformations that keep one operand constant or reduce the number of "1" bits in a carry save array multiplier are ways that the compiler can change the data to reduce the multiplier's energy. To gauge the importance of data, we used cycle accurate simulation to measure the power in the ALU when each MAC operation was active for the workloads [12]. The average power consumed by each instruction is calculated, when bits are transferred

from ALU to DSP circuits. The FFT (Fast Fourier Transformation) has the largest standard deviation and has the least accurate ALU estimates under all models. The FFT showed a bimodal distribution of energy in one of its MAC instructions, probably due to a large number of multiplications by zero. Improving accuracy for this problem would require moving to a model based on execution traces. The non-clocked pass transistor 8x8 bit multiplier Energy Per Instructions with corresponding speeds for various non-clocked pass gate logics are given in Table II. The EPI is increased when the feature size is decreased. This clearly shows that as instruction passed from the ALU, each instruction consume less power per instruction. Due to longer interconnection wire, load capacitance, layout capacitance, the power consumption is high in the deep submicron feature size than ultra deep submicron feature size.

TABLE I. 8X8 BIT MULTIPLIER RESULTS OF POWER DISSIPATION, PROPAGATION DELAY AND PDP OF CPL, DCVS, SRPG, EEPL and PPPL CIRCUITS

Feature size	Supply Voltage	Variable	CPL	DCVS	SRPG	EEPL	PPPL
0.35µm	3.5V	P.Dissipation(P_D) Watts	$8.081x10^{-3}$	$9.532x10^{-3}$	$19.631x10^{-3}$	$12.732x10^{-3}$	$38.99x10^{-3}$
		Delay (t_d) Sec	$1.2124\ x10^{-9}$	$1.1181\ x10^{-9}$	$1.096\ x10^{-9}$	$1.0691x10^{-9}$	$1.0731x10^{-9}$
		PDP(P_D x t_d) watts-sec	$9.7974x10^{-12}$	$1.0657x10^{-11}$	$2.1515x10^{-11}$	$1.3611x10^{-11}$	$4.184x10^{-11}$
0.25µm	2.5V	P.Dissipation(P_D) Watts	$4.039x10^{-3}$	$4.36x10^{-3}$	$9.699x10^{-3}$	$9.227x10^{-3}$	$23.026x10^{-3}$
		Delay (t_d) Sec	$7.4267x10^{-10}$	$7.5280x10^{-10}$	$7.4267x10^{-10}$	$7.099\ x10^{-10}$	$7.1708x10^{-10}$
		PDP(P_D x t_d) watts-sec	$2.9996x10^{-12}$	$3.2822x10^{-12}$	$7.2031x10^{-12}$	$6.5502x10^{-12}$	$1.6511x10^{-11}$
0.18µm	2.0V	P.Dissipation(P_D) Watts	$1.4138\ x10^{-3}$	$1.512\ x10^{-3}$	$3.673\ x10^{-3}$	$2.496\ x10^{-3}$	$10.738\ x10^{-3}$
		Delay (t_d) Sec	$1.3539x10^{-10}$	$1.3539x10^{-10}$	$4.8527x10^{-10}$	$4.554\ x10^{-10}$	$4.8157x10^{-10}$
		PDP(P_D x t_d) watts-sec	$1.9141x10^{-13}$	$2.047x10^{-13}$	$1.7823x10^{-12}$	$1.1366x10^{-12}$	$5.1710x10^{-12}$
0.12µm	1.2V	P.Dissipation(P_D) Watts	$0.103x10^{-3}$	$0.293\ x10^{-3}$	$0.137\ x10^{-3}$	$0.478\ x10^{-3}$	$2.565\ x10^{-3}$
		Delay (t_d) Sec	$1.0273x10^{-10}$	$1.0273x10^{-10}$	$3.3674x10^{-10}$	$3.2170x10^{-10}$	$3.3349x10^{-10}$
		PDP(P_D x t_d) watts-sec	$1.0581x10^{-14}$	$3.0099x10^{-14}$	$4.6133x01^{-14}$	$1.5377x10^{-13}$	$8.5540x10^{-13}$

TABLE II. 8X8 BIT MULTIPLIER RESULTS OF *EPI* OF CPL, DCVS, SRPG, EEPL and PPPL CIRCUITS

Feature size	Variable	CPL	DCVS	SRPG	EEPL	PPPL
035µm (3.5V)	Max.Operating frequency MHz	824.81	894.37	912.4	935.36	931.87
	EPI pJ	739.92	649.348	622.954	643.014	653.588
025µm (2.5V)	Max.Operating frequency GHz	1.346	1.328	1.346	1.408	1.394
	EPI pJ	355.643	380.256	255.844	279.595	353.613
018µm (2.0V)	Max.Operating frequency GHz	7.386	7.386	2.060	2.195	2.076
	EPI pJ	181.527	181.527	104.884	170.894	178.562
012µm (1.2V)	Max.Operating frequency GHz	9.737	9.734	2.969	3.108	2.998
	EPI pJ	60.258	59.260	31.243	47.460	50.995

TABLE III: POWER COMPARION OF 0.180µm FEATURE SIZE

	Multiplier type	Power m Watt	% improvement	Propagation delay	% of Improvement
Our designed	CAS	1.4138		$1.3539x10^{-10}$	
Amir *et.al* [13]	Pipeline	59.91	97.64	----	----
Rizwan *et.al* [14]	Array	2.633	46.30	$1.298x10^{-9}$	89.56
	Array architecture-I	1.842	23.24	$1.167x10^{-9}$	88.39
	Array Architecture-II	1.416	0.15	$1.159x10^{-9}$	88.31

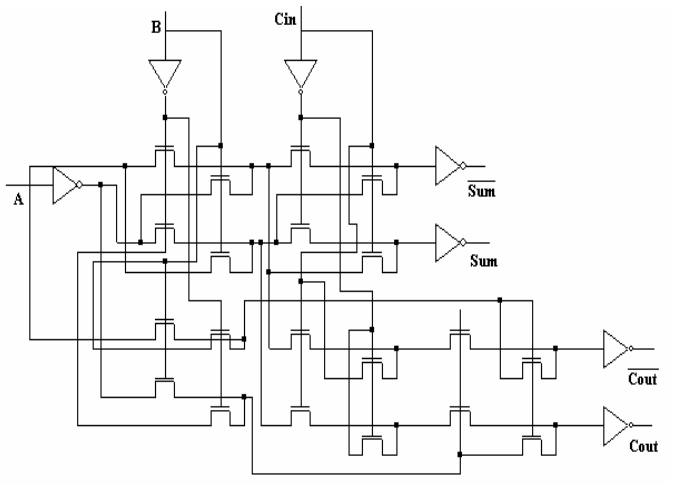

Fig 2 (a) CPL

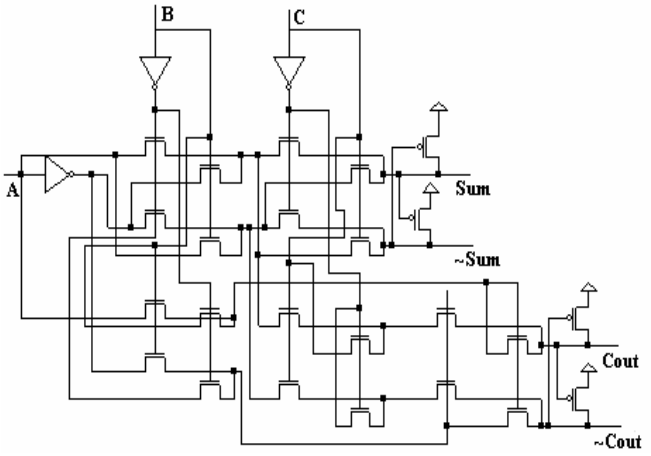

Fig.2(b) DCVS

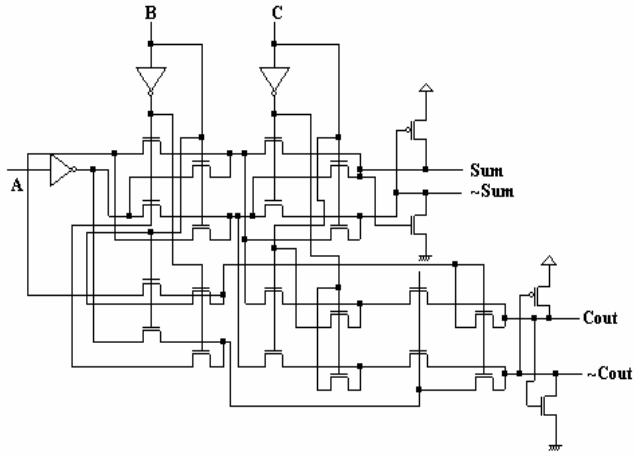

Fig.2 (c). EEPL

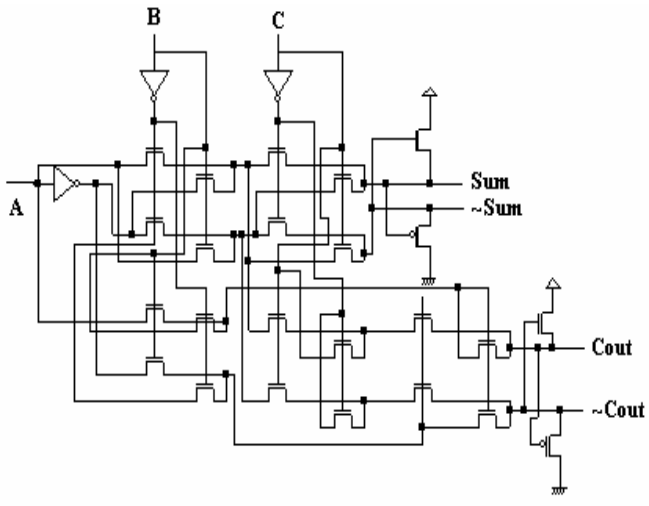

Fig.2(d) PPPL

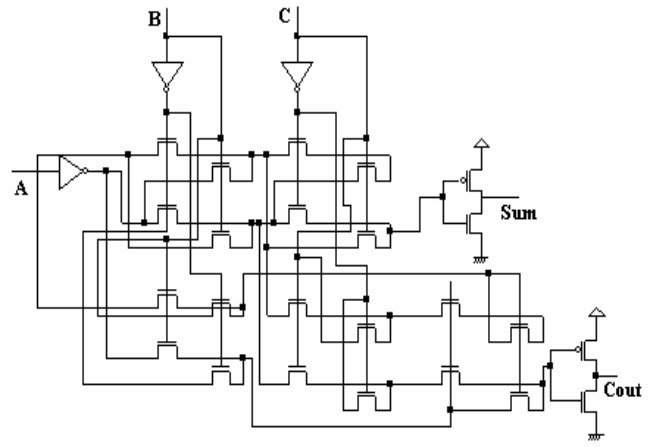

Fig. 2 (e) SEPG

Our non-clocked 8x8 bit multiplier circuits, designed by CSA multiplier technique are compared with other existing author circuits. The simulated CPL technique of our 8x8 bit multiplier results of our circuit and other existing authors 8x8 multipliers types are given in the table III. Our designed circuits shows approximately 98% improvement in terms of power when it is compared with Amir et.al [13]'s pipeline circuit. similarly, our circuit shows 46.30%, 23.24% and 0.15% improvement in terms of power dissipation in comparison to Rizwan *et.al* [14]'s different architecture. The propagation delay percentage improvement of our CPL multiplier circuits with Rizwan *et.al* [14] are 89.56%, 88.39% and 88.31% respectively.

CONCLUSION

We have designed different non-clocked pass transistor logic with CSA technique for low power and high performance of multiplier circuit. We have analyzed power dissipation, PDP, propagation delay and EPI which are calculated from the simulation results. These non-clocked pass transistor types multipliers are used in DSP circuits with inter instruction effects when building instruction-level energy

models for a specific DSP design. From the simulated results we have seen that our proposed multiplier circuit is very fast and consumes less power than other existing multiplier circuit.

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