Seung Jun Baek

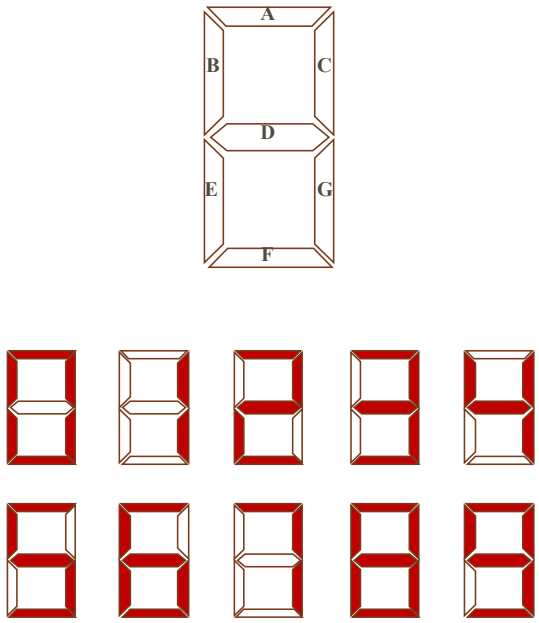


Figure 1: 7-segment display

1 Outline

In this assignment, you are asked to design a verilog module for 7-segment display of numbers from 0–9. In Fig. 1, we have the 7-segment display system. The segments are labelled by A,B,...,G. Each of the segment is controlled by 4 input signal named as `w,x,y,z`, each of which is a 1-bit signal. These 4 bits are interpreted as a 4-digit binary number, where `w` is the most significant bit. For example, the input of `w=0,x=1,y=0,z=1` represents a binary number 0101, which is 5. Our goal is to display the input number using 7-segment display, by activating (turning on) proper segments based on the input signal.

A segment is activated (turned ON) if its control module outputs 1, and is deactivated (turned OFF) if its control module outputs 0. The example is shown in Fig. 1. For example, when the input is given by `w=0,x=0,y=1,z=0`, then the input is number 2, and the segments A, C, D, E, F, is activated. The control module for segment A,B,...,G is denoted by $F_A, F_B, \ldots, F_G$. Each module is a function of `w,x,y,z`.

For example, when the input is given by `w=0, x=0, y=1, z=0`, we have that

$$
\begin{aligned}
F_A(w,x,y,z) = F_A(0,0,1,0) &= 1 \\
F_B(0,0,1,0) &= 0 \\
F_C(0,0,1,0) &= 1 \\
F_D(0,0,1,0) &= 1 \\
F_E(0,0,1,0) &= 1 \\
F_F(0,0,1,0) &= 1 \\
F_G(0,0,1,0) &= 0
\end{aligned}
$$

, in other words, segment A,C,D,E,F is ON.

2 Specification

In this assignment, you are asked to find function that controls segment B, or $F_B(w,x,y,z)$. Your module must have the following specification:

- module name: `num_7seg_B`
- Input signal: `w, x, y, z`
- Output signal: `out`

All the signal names are case sensitive.

IMPORTANT: YOU MUST PERFORM GATE-LEVEL MINIMIZATION YOUR BOOLEAN FUNCTION. THAT IS, FIND THE MOST SIMPLIFIED EXPRESSION OF YOUR FUNCTION.

3 What to submit

- Your module should be designed in `num_7seg_B.v` file in verilog.
- Upload your file at Blackboard before deadline (no late submission accepted).

4 How to test your module

In the blackboard, I have uploaded `h1_top.v` so that you can test your module. The file contains `TOP` module. The `TOP` module instantiates `num_7seg_B` module, and feeds the test input signal `num` to the module. Note that signals `w, x, y, z` are connected to the corresponding bits of `num`. `num` changes from 0 to 15, and by monitoring signal `out` using gtkwave tool.

You can run the following in your command line to compile `h1_top.v` and `num_7seg_B.v` together as follows:

- `iverilog -o h1.out h1_top.v num_7seg_B.v`

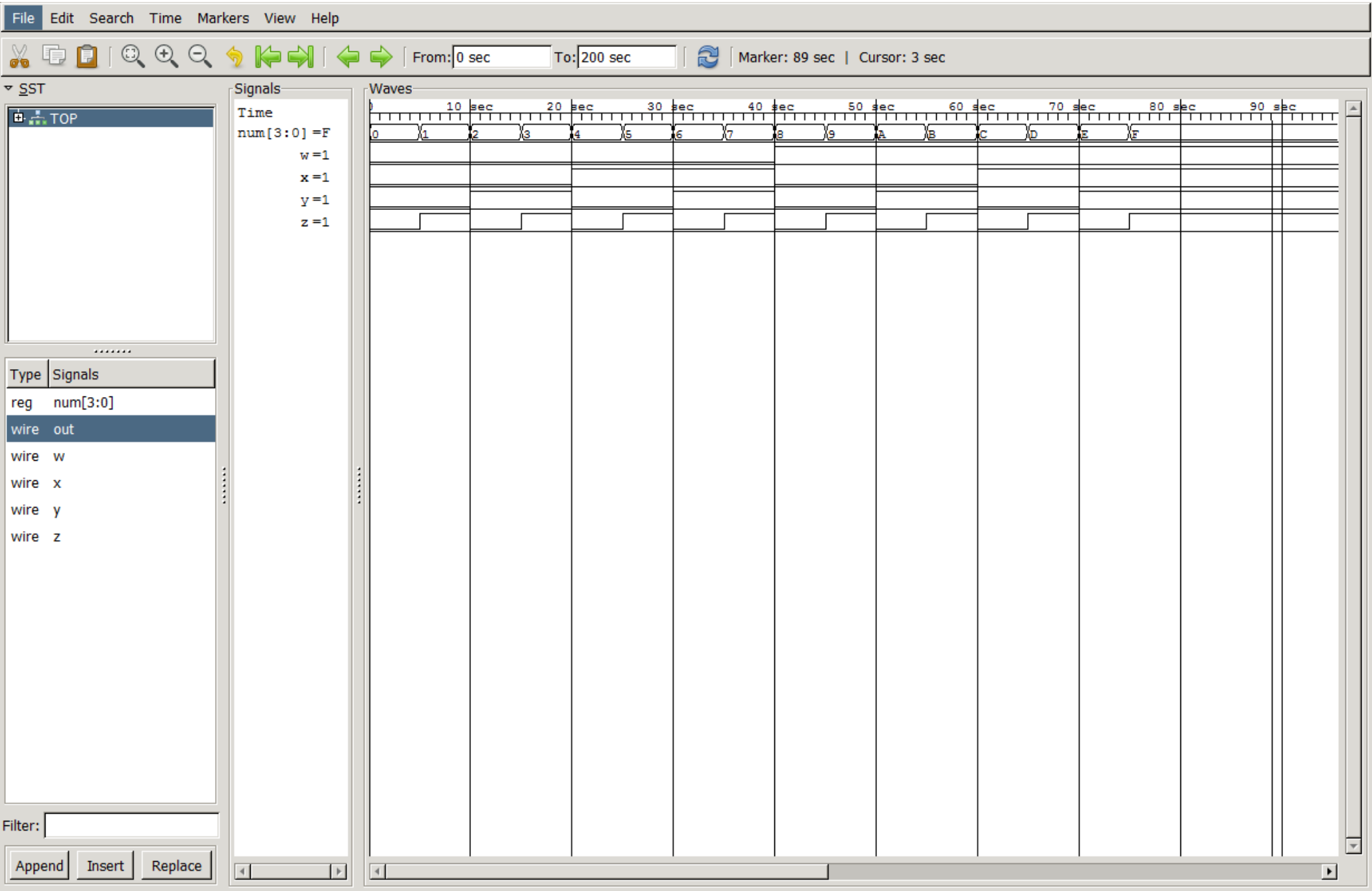
- `vvp h1.out`
- `gtkwave h1_output.vcd`

A screenshot is attached at the end of this document. You see that the value of `num` and `w,x,y,z` change over time. Your module should produce the correct waveform for `out`.

5 Grading

- 2 points if your module works correctly, that is, `out` signal is produced correctly for some test input signals `w,x,y,z` for grading, AND uses minimum expression logic
- 1 point if your module works correctly but did not use the minimum expression

The rest of case is 0 points, i.e., if you do not submit (or late), or if your file does not compile correctly, or produces wrong results.


File
Edit
Search
Time
Markers
View
Help
From: 0 sec
To: 200 sec
Marker: 89 sec | Cursor: 3 sec
SST
TOP
Signals
Time
num[3:0] =F
w =1
x =1
y =1
z =1
Waves
10 sec
20 sec
30 sec
40 sec
50 sec
60 sec
70 sec
80 sec
90 sec
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
Type
Signals
reg num[3:0]
wire out
wire w
wire x
wire y
wire z
Filter:
Append
Insert
Replace