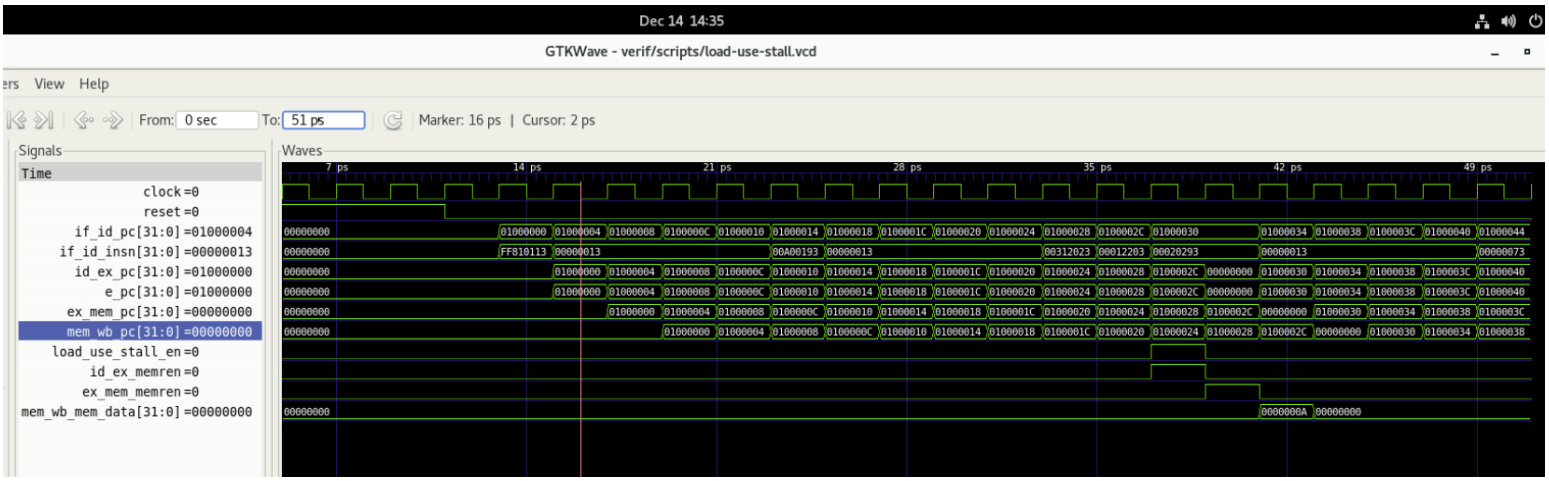
Team non

Members: Yousif Kndkji (218636118), Salman Kayani (219063635)

Testbench Results



Testbench waveform for load-use-stall micro-test.

The design passed all micro-tests and passed the BubbleSort, CheckVowel, SumArray, SwapShift, Swap, Fibonacci, and SimpleAdd benchmarks. I'm not sure if the design passed the gcd benchmark, since the gcd benchmark does not seem to have a pass/fail test.

I had really wanted to try implementing the 2-bit saturating branch predictor, but I unfortunately ran out of time while trying to fix the pattern check errors for tests 1 to 3. I understand the concept and I believe I know how to implement it, but I unfortunately could not get around to actually implementing it.

Challenges

1. The greatest challenge was trying to go through the different cases where a write decode stall was needed (to solve an instruction sequentially updating a register during its writeback in the same cycle another instruction is trying to read from that same register combinationally from the register file) and implement a stall for it without somehow breaking an earlier instruction in the pattern checker tests.
2. Another challenge was properly inserting a bubble or NOP or squashing instructions whenever they were needed, and figuring out the priority regarding whether to squash or stall.