Team non

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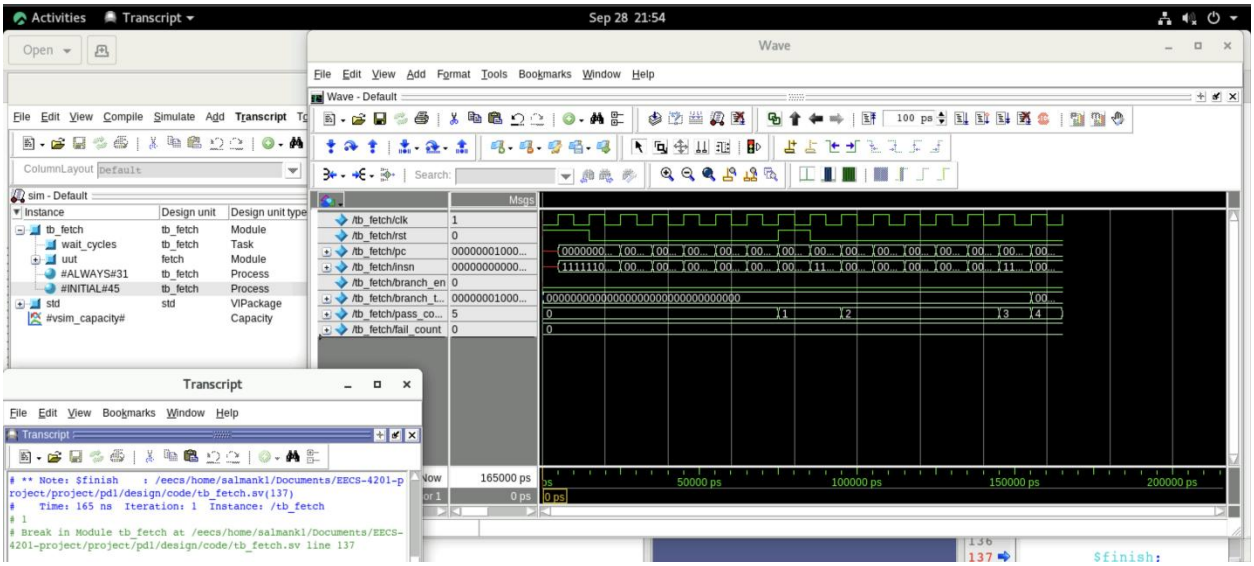
Testbench Results



Challenges

1. Ensuring proper instruction fetch timing for fetch.sv was difficult in the project deliverable, because the program counter and instruction outputs needed to update together at each clock cycle to maintain consistency in instruction sequencing, as timing differences between the program counter and instruction output resulted in incorrect instructions being retrieved from memory required re-evaluations of the fetch logic.

2. Managing simulation timing in ModelSim when using both always_ff and always_comb processes was challenging in the project deliverable, because the interaction between clocked and unclocked assignments occasionally caused the design to behave inconsistently across simulation cycles, as certain computed values were updated either too early or too late relative to the expected clock events, leading to mismatches between internal and external variables in the code, and the code had to be restructured to allow its associated sequential and combinational logic produced results at correct simulation times.