

Team non

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Testbench Results

N/A

Challenges

1. A major challenge involved implementing correct stall behavior without data forwarding, because ensuring that the program counter, the IF/ID pipeline register, and all dependent control signals were frozen in a consistent manner during a stall proved difficult, as even small mistakes in stalling for fetching and decoding caused instructions to advance or repeat incorrectly.
2. Challenges included ensuring that the pipeline maintained correct sequencing under conditional branches. Resolving cases where memory reads produced results only after multiple cycles added complexity to maintaining proper instruction flow.