Team non

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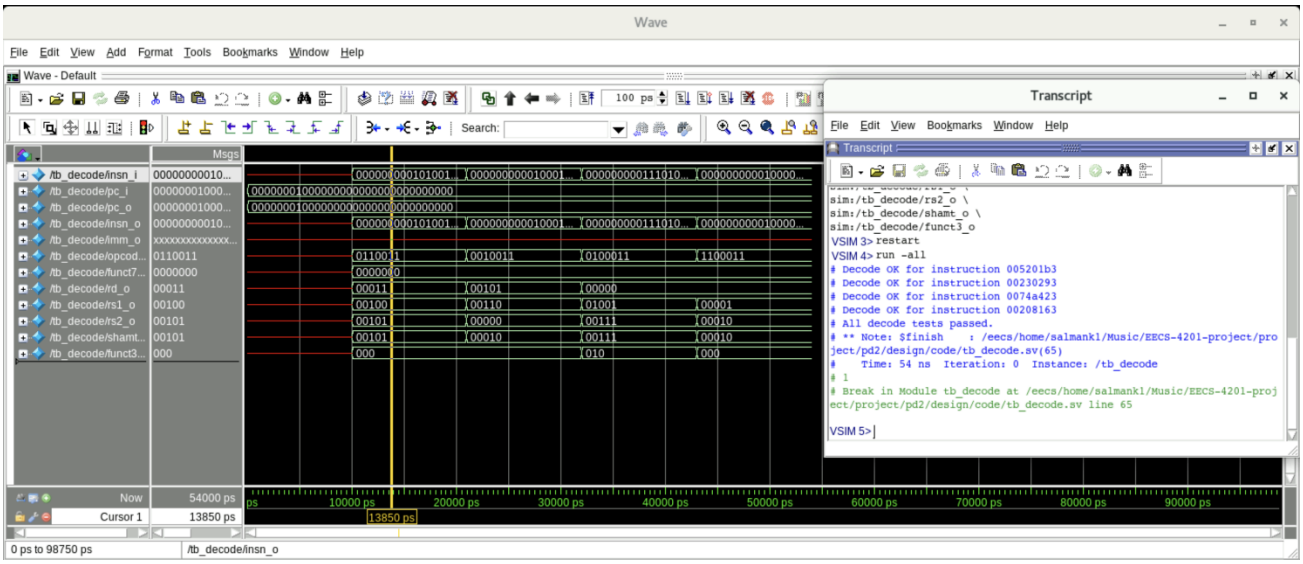
Testbench Results



Challenges

1. Decoding instructions in decode.sv presented a challenge in the project deliverable, because correctly extracting fields such as rd, rs1, rs2, funct3, funct7, and immediate values required precise handling of instruction formats across R, I, S, B, U, and J types. Incorrectly identifying these fields caused wrong register or immediate values to propagate through the pipeline, requiring careful verification and conditional logic to allow correct operation across all instruction types.

2. Implementing control signal generation in control.sv was challenging in the project deliverable, because determining appropriate values for regwren, memwren, pcsel, immsel, alusel, and writeback selection for every instruction type required a comprehensive understanding of RISC-V instruction semantics. Overlapping opcode with funct3 and funct7 patterns sometimes produced ambiguous control decisions, necessitating iterative refinements to produce reliable control outputs for all supported instructions.