Team non

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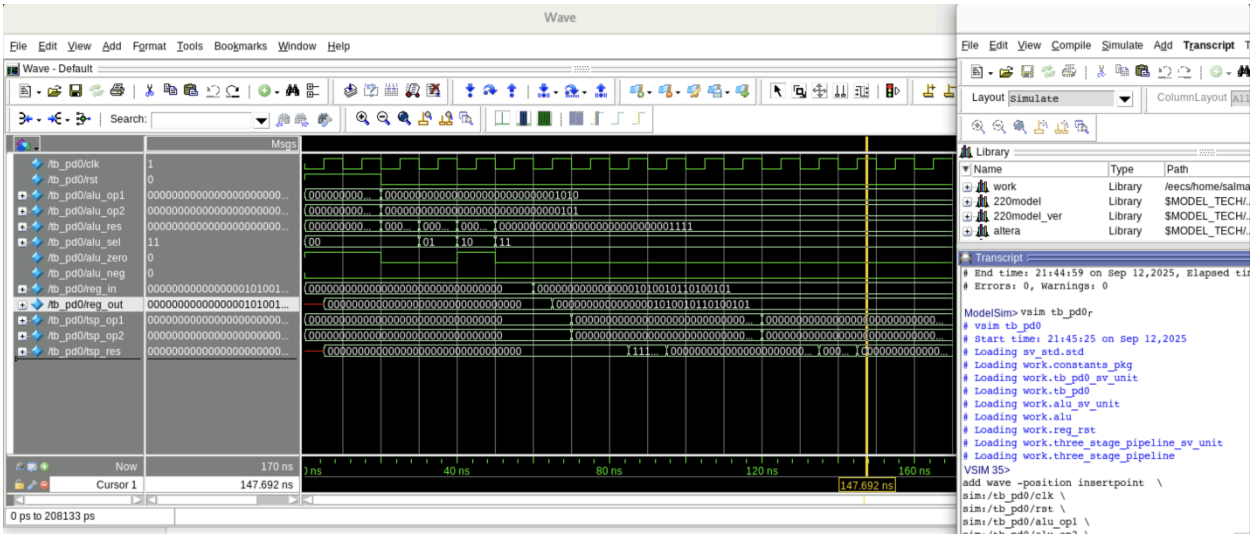
Testbench Results



Challenges

1. Designing the three-stage pipeline was difficult in the project deliverable, because each stage's output had to be properly registered before sending the output into the next stage since each stage's outputs needed to be registered on the rising edge of the clock before being passed forward to avoid interfering with the next stages and their output.

2. Writing the testbench, tb_pd0.sv for the ALU, write-enable register with synchronous reset, and three-stage pipeline was challenging in the project deliverable, including simulating the file in ModelSim in compiling multiple SystemVerilog files in the correct order and run the simulation from the terminal. This involved trial and error to make sure the simulation ran smoothly, the waveform viewer displayed the expected signals, and the $monitor output reflected the correct behavior.