

Practice (Synthesis and Physical Design)

1. ROBDD

Let F and G be the ROBDDs of Boolean functions $f = abc$ and $g = bd + b'd$, respectively, under the variable ordering index $a < b < c < d$.

- (a) Draw F and G .
- (b) Derive the ROBDD of $F \cdot G$ using `apply_ite()` procedure given in class. Show your `apply_ite()` steps.

Hint: `ite` operator for $F \cdot G$ is `ite(f, g, 0)`.

2. Two-Level Logic Minimization [Quine-McCluskey]

- (a) Find all prime implicants, and essential prime implicants of function F . $F(a, b, c, d) = (0, 6, 8, 12, 13, 14)$, given don't care set $d(a, b, c, d) = (2, 4, 11)$.
- (b) Find the minimum covering (sum of product form) that covers the Boolean function in (a).

3. Partitioning

Let the three tuple (u, v, w) denote an edge (u, v) with weight w . Given a circuit C of 6 vertices, n_1, n_2, \dots, n_6 , and 5 edges, $C = \{(n_1, n_4, 6), (n_4, n_2, 3), (n_2, n_3, 2), (n_2, n_5, 1), (n_3, n_6, 7)\}$, apply the Kernighan-Lin heuristic to find the balanced min-cut for C with the initial partitions $\{n_1, n_2, n_3\}$ and $\{n_4, n_5, n_6\}$. **Show all steps that lead to your answer.**

4. Floorplanning

Given the following Polish expression, $E = 12H3H45HVV67V$, where $H(V)$ represents a horizontal(vertical) cut.

- (a) Does the above expression have the balloting property? Justify your answer.
- (b) Is E a normalized Polish expression? If not, exchange an operator and its adjacent operand to transform E into a normalized Polish expressions E' .
- (c) Give the slicing tree corresponding to the expression E , or explain why no such a slicing tree exists. Also, give the slicing tree corresponding to the “resulting” normalized Polish expression E' , if E is not a normalized Polish expression.
- (d) Assume the modules 1, 2, ..., 7 have the widths and heights indicated in Figure 1. If all modules are rigid and have free orientations, what will be the size of the smallest bounding rectangle corresponding to E if it is a normalized Polish expression or E' otherwise? **Show all steps that lead to your answer.**

Module No.	Width	Height
1	3	1
2	2	2
3	4	3
4	3	1
5	1	3
6	3	3
7	3	3

Figure 1. The dimensions for the seven modules.

5. Placement

Consider the AND gate connected to other cells by wires as shown in Figure 2. The weights are specified beside the wires. The locations are indicated in the grid graph, e.g, Vdd is located at (0, 3), and Gnd is located at (3, 0). Please apply the force-directed method to find the zero-force location of the AND gate.

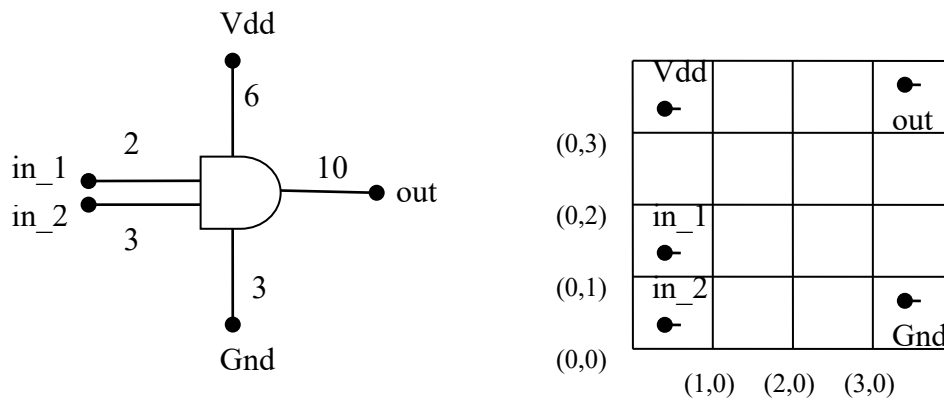


Figure 2. Placement of a AND gate.

6. Wire length estimation

For the four pins as shown below, give the wire length estimation for the following methods:

- Semi-perimeter approximation.
- Minimum rectilinear Steiner tree.
- Minimum rectilinear spanning tree.

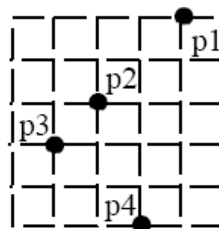


Figure 3. Wirelength estimation

7. Maze routing

Extend maze routing algorithm shown in class such that it generates a shortest path from source to target (sink) with the minimum number of bends.

8. Channel routing

Given the instance of the channel routing problem as shown below.

- What is the channel density? Find the set of nets that contribute the channel density.
- Draw the HCG and VCG.
- Can the basic left-edge algorithm apply to this channel routing instance? Route the instance if there exists a feasible routing solution; explain why the algorithm does not apply to this instance, otherwise.
- Can the constrained left-edge algorithm apply to this channel routing instance? Route the instance if there exists a feasible routing solution; explain why the algorithm does not apply to this instance, otherwise.

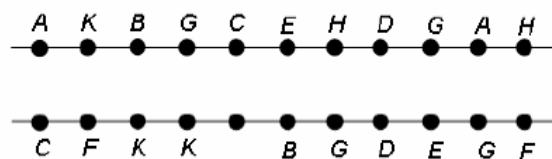
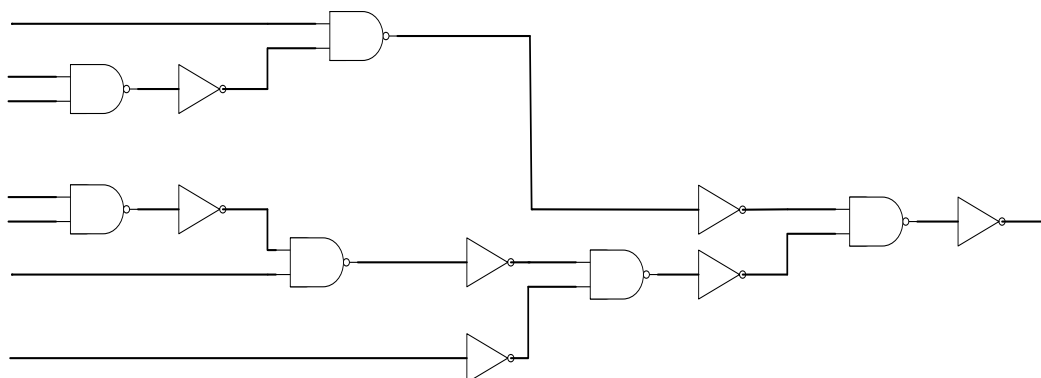


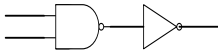
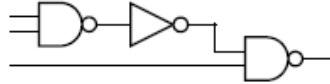
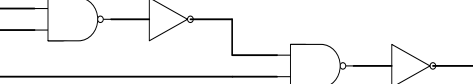
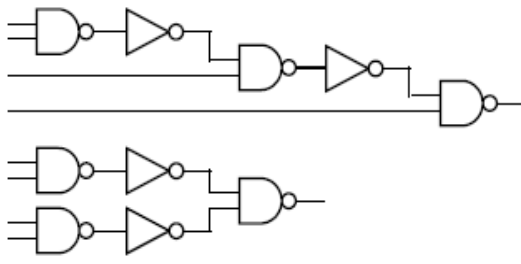
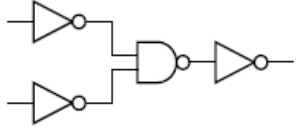
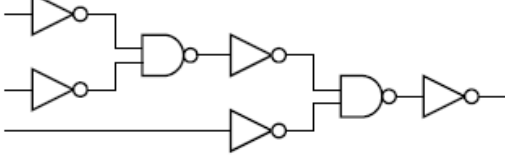
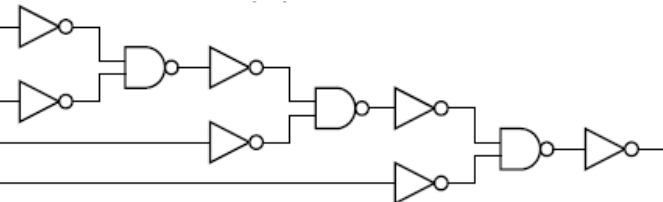
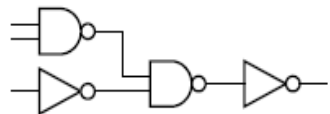


Figure 4. Routing Channel

9. Technology mapping

- What is the pattern graph of the 2-input XOR gate by using NAND and NOT as base functions?
- Find the minimum cost covering of the following logic network using the pattern graphs listed below it.



Type	Cost	Canonical Form
INV	1	
NAND2	2.5	
AND2	2	
NAND3	3.5	
AND3	3	
NAND4	4.5	
NOR2	3	
NOR3	4	
NOR4	5	
OI21	3	
AOI22	4.5	