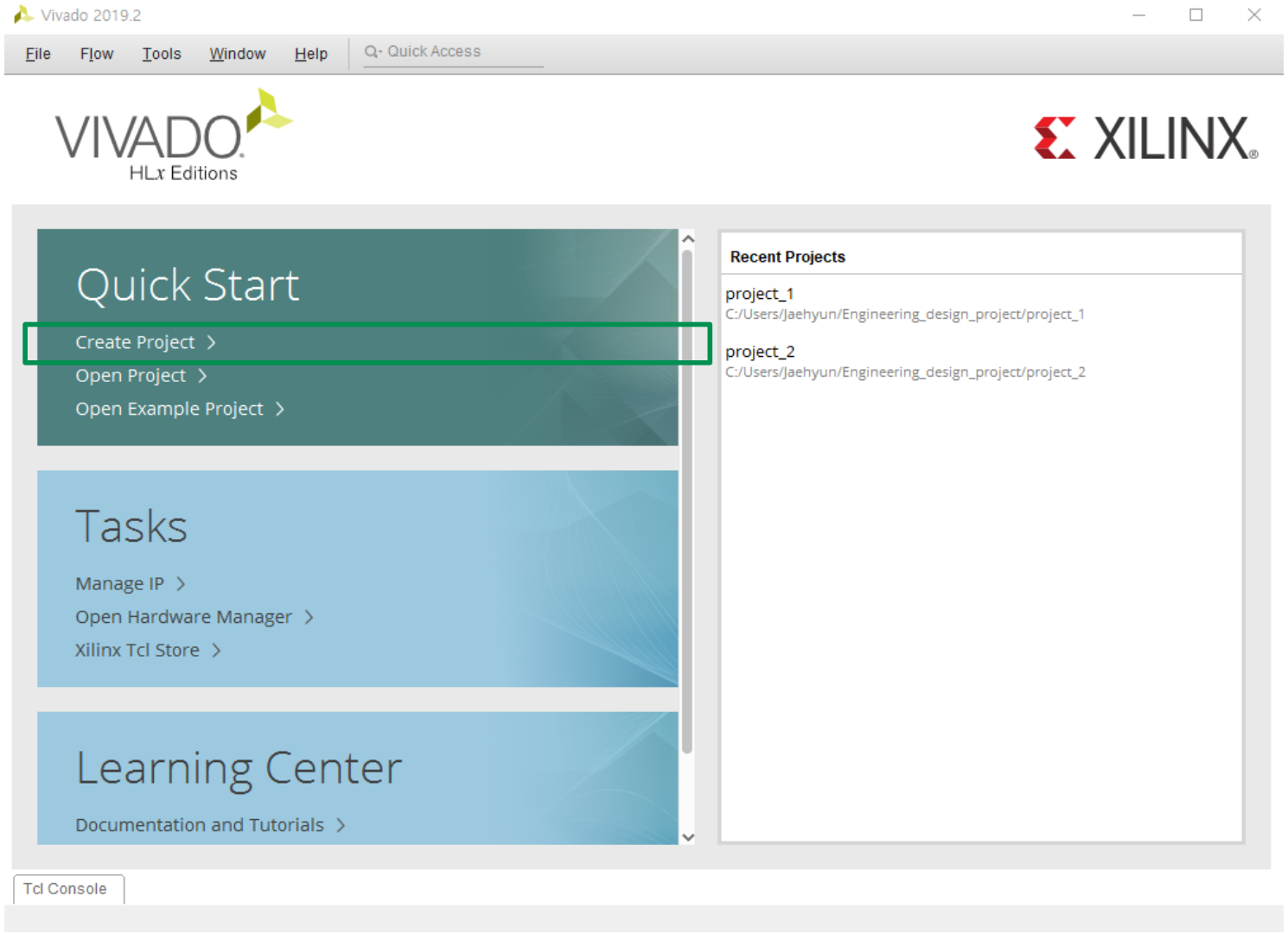
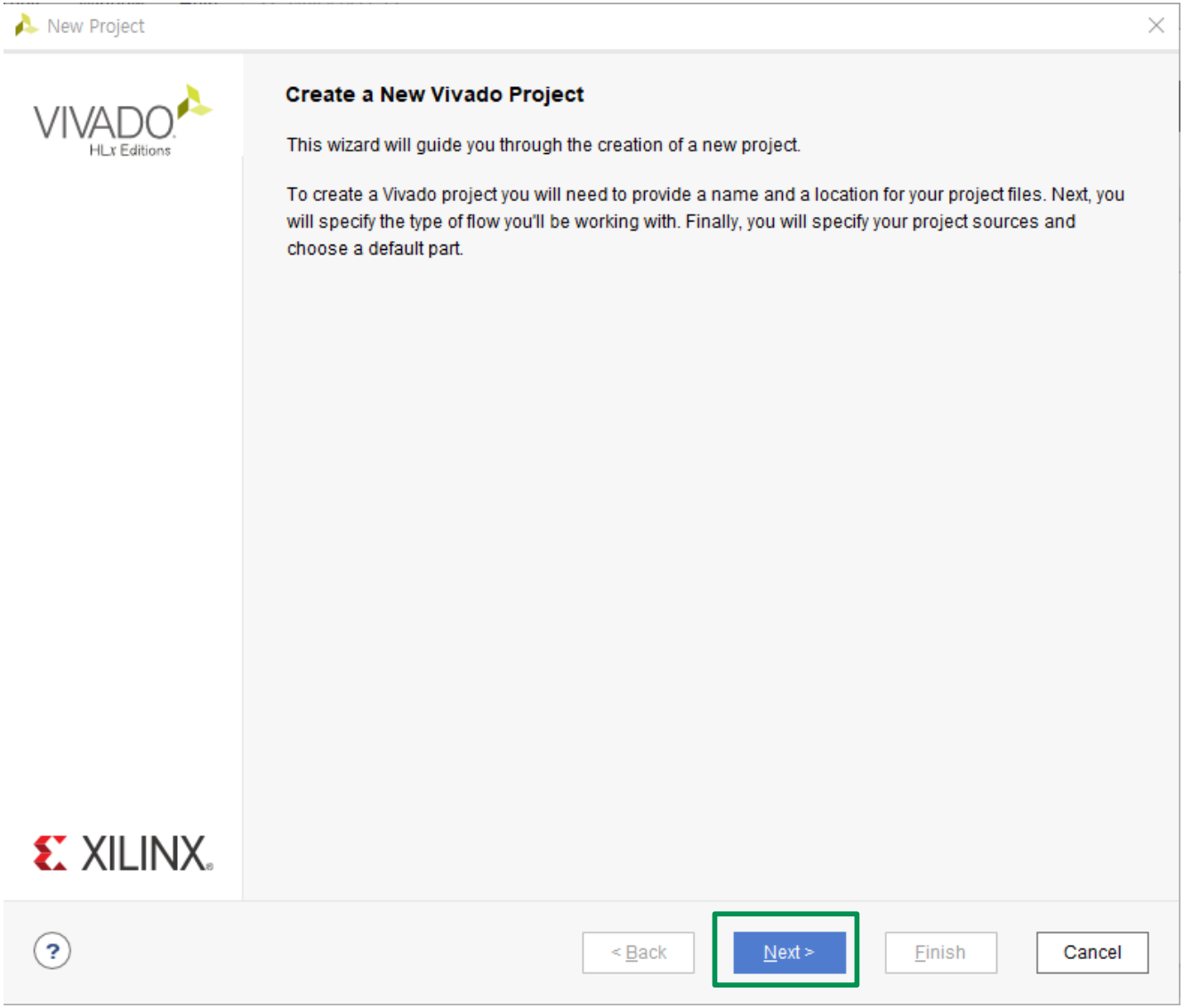
Xilinx Vivado Simulation

Create Project

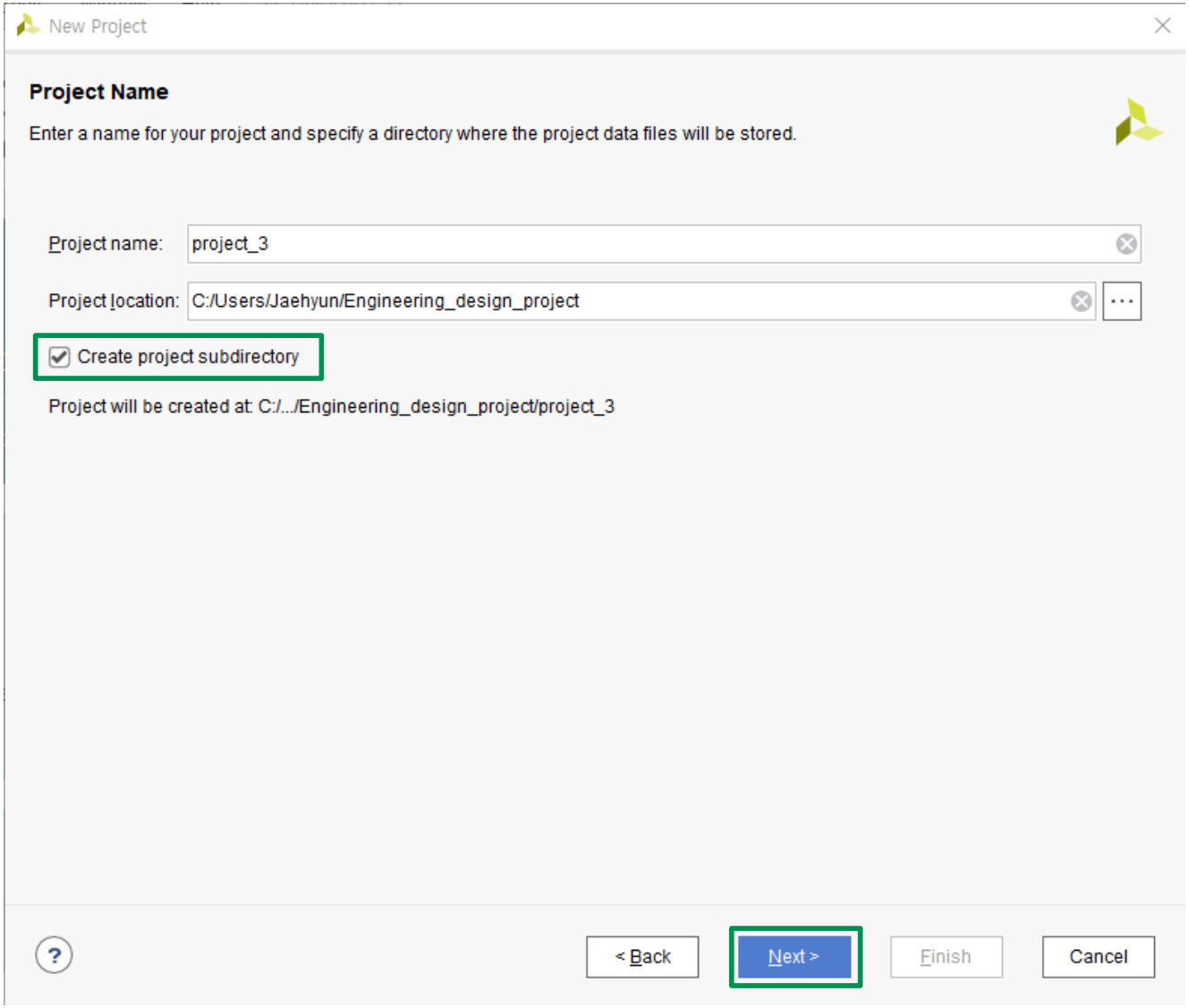
- Run Vivado



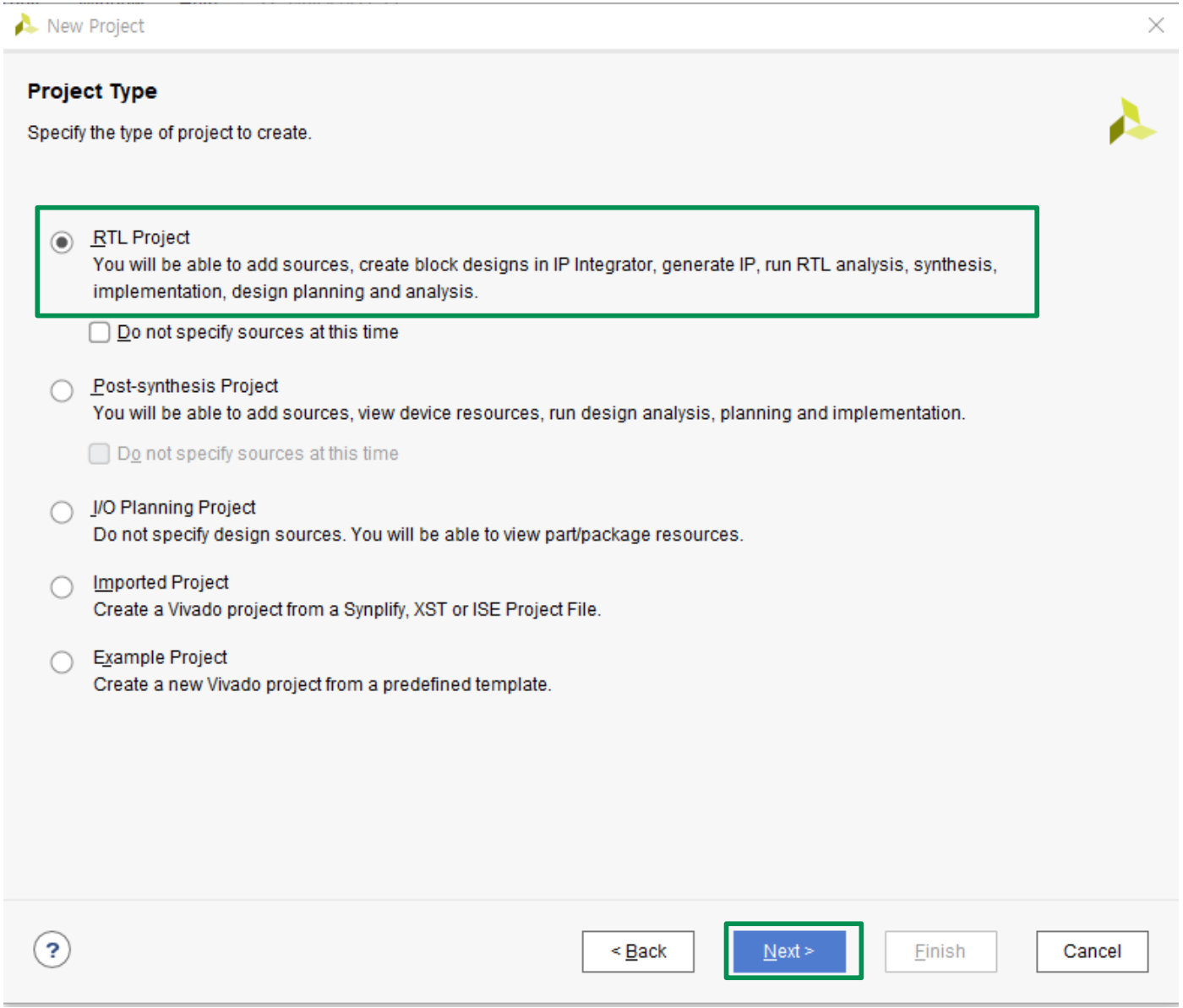
Create Project



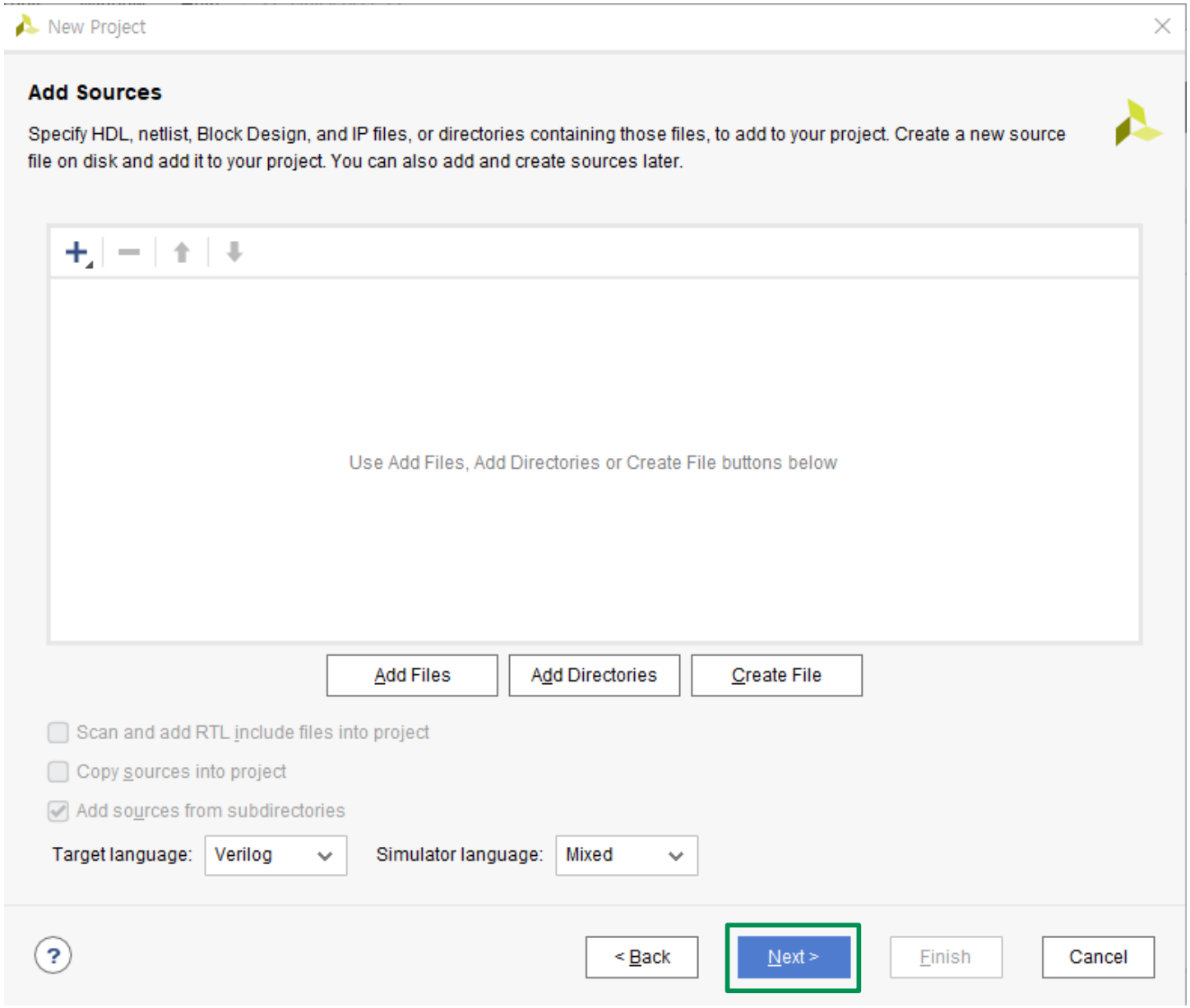
Create Project



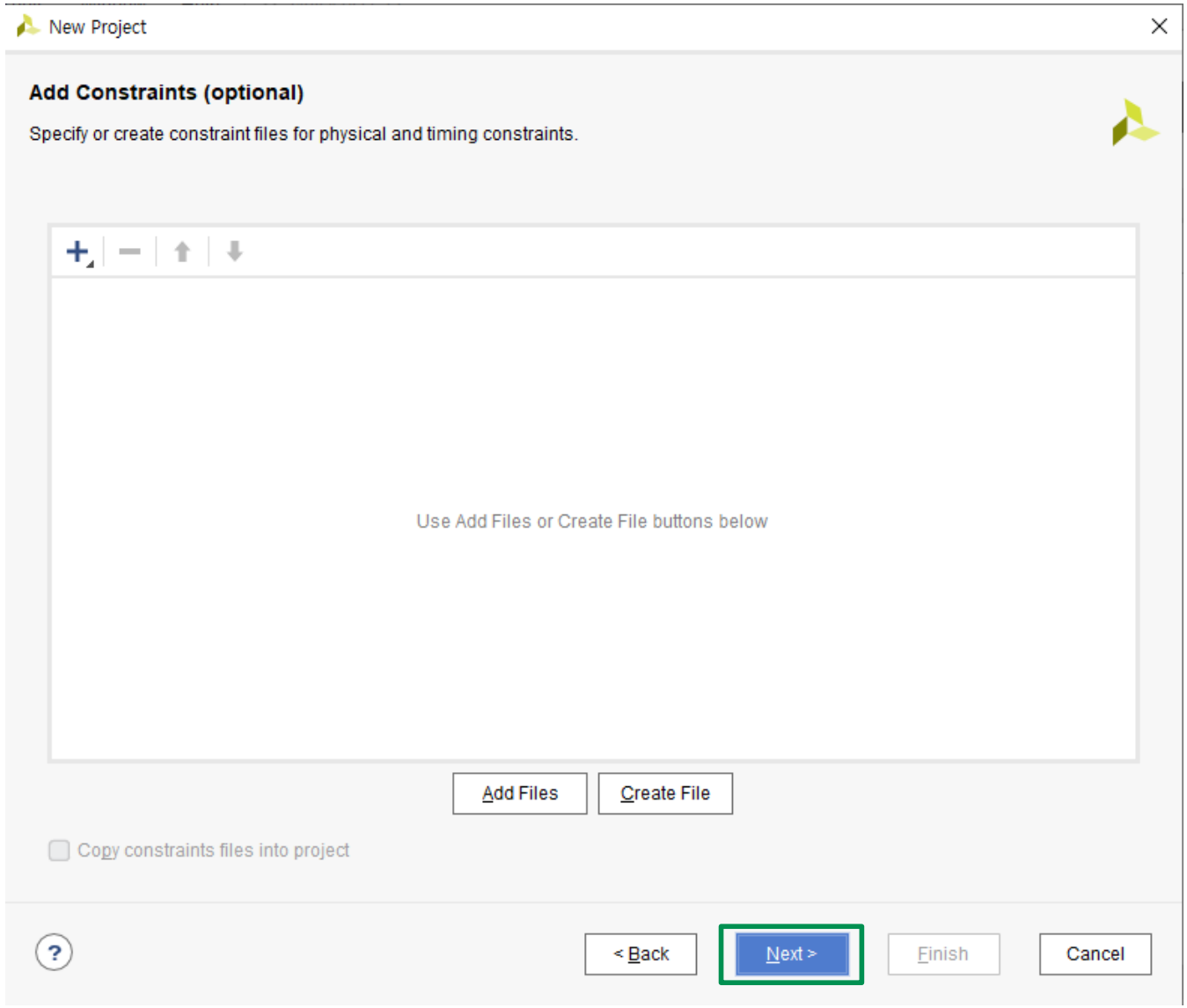
Create Project



Create Project

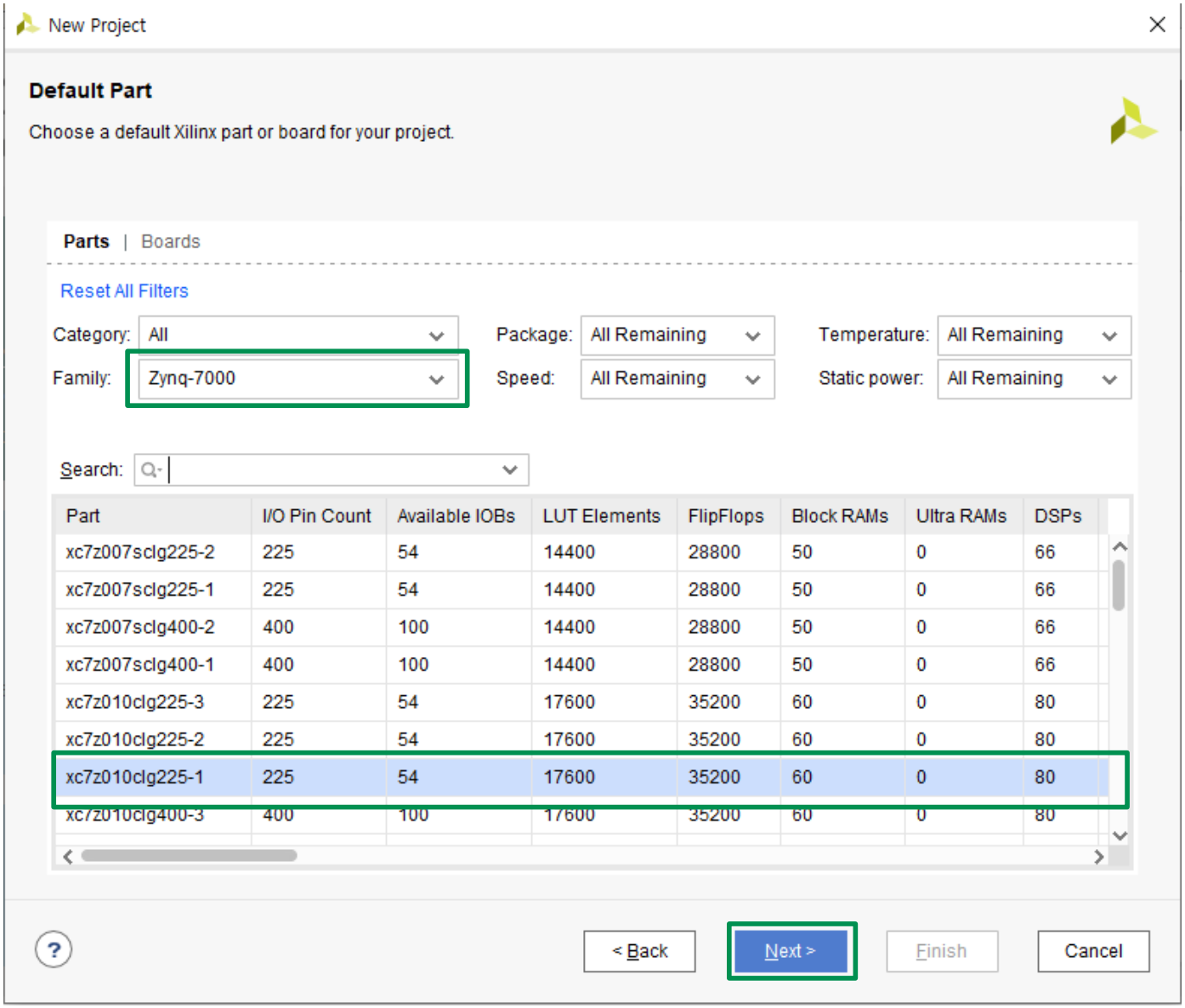


Create Project

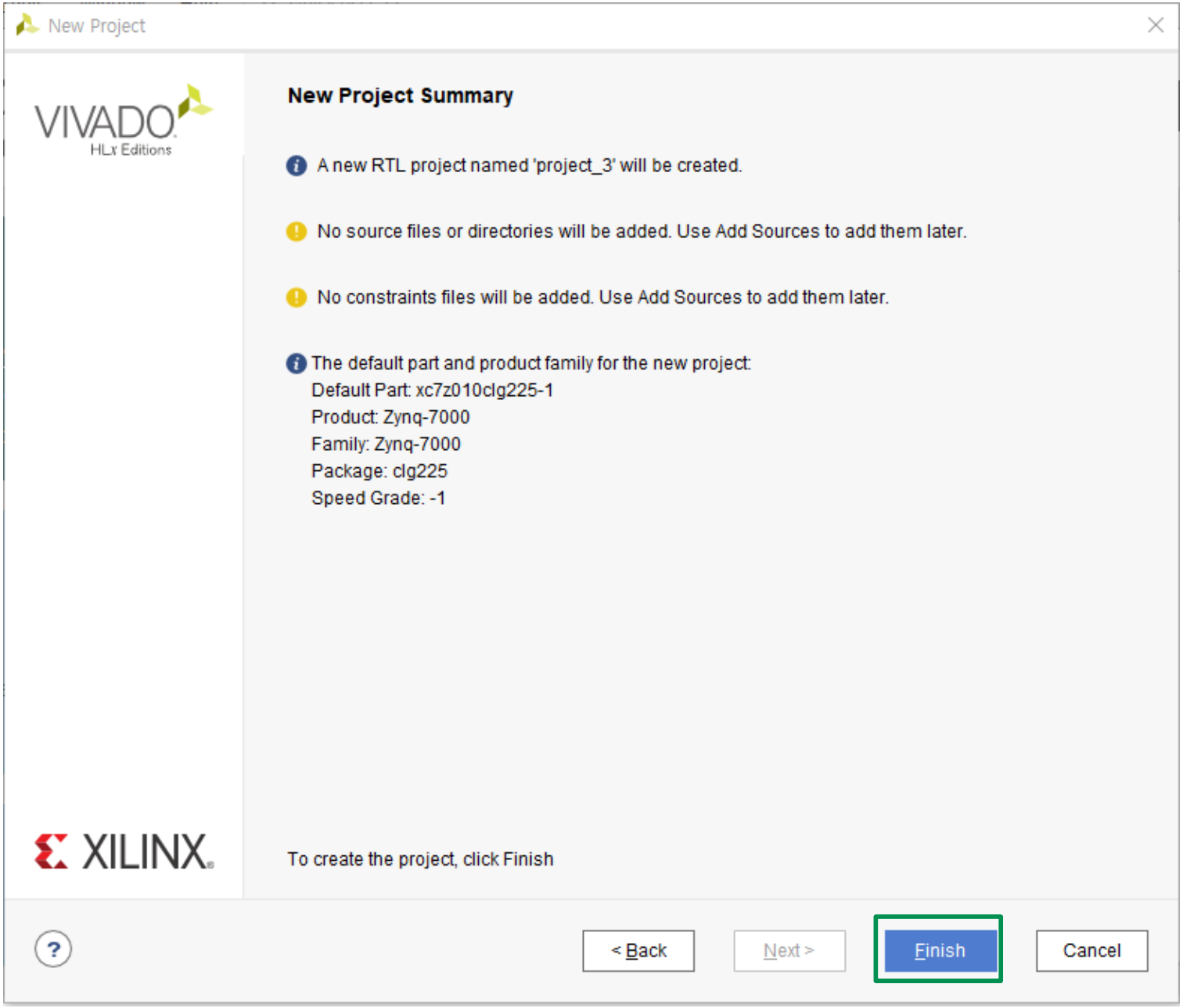


Create Project

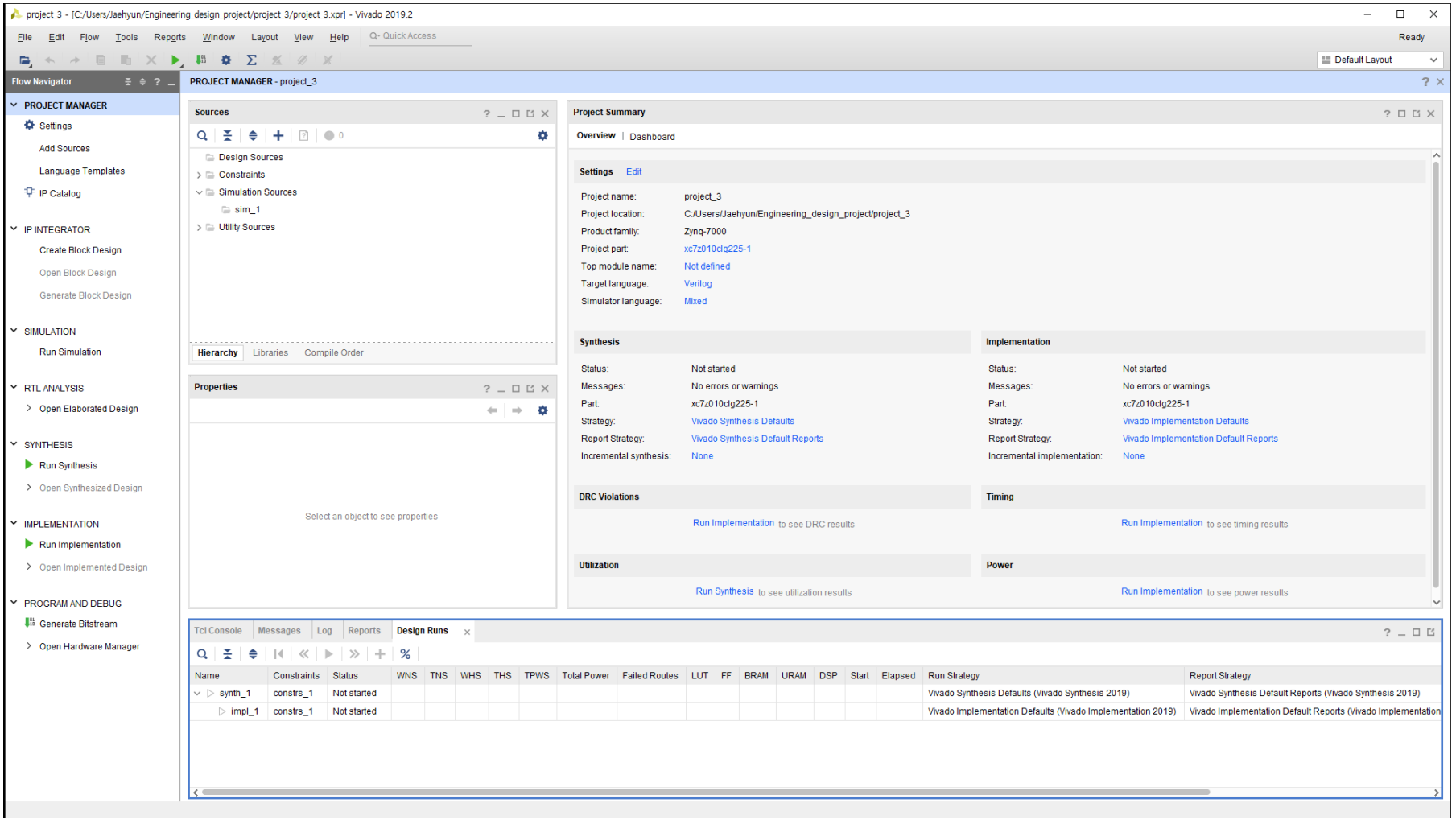
- Select xc7z010clg225-1 (just for simulation use)



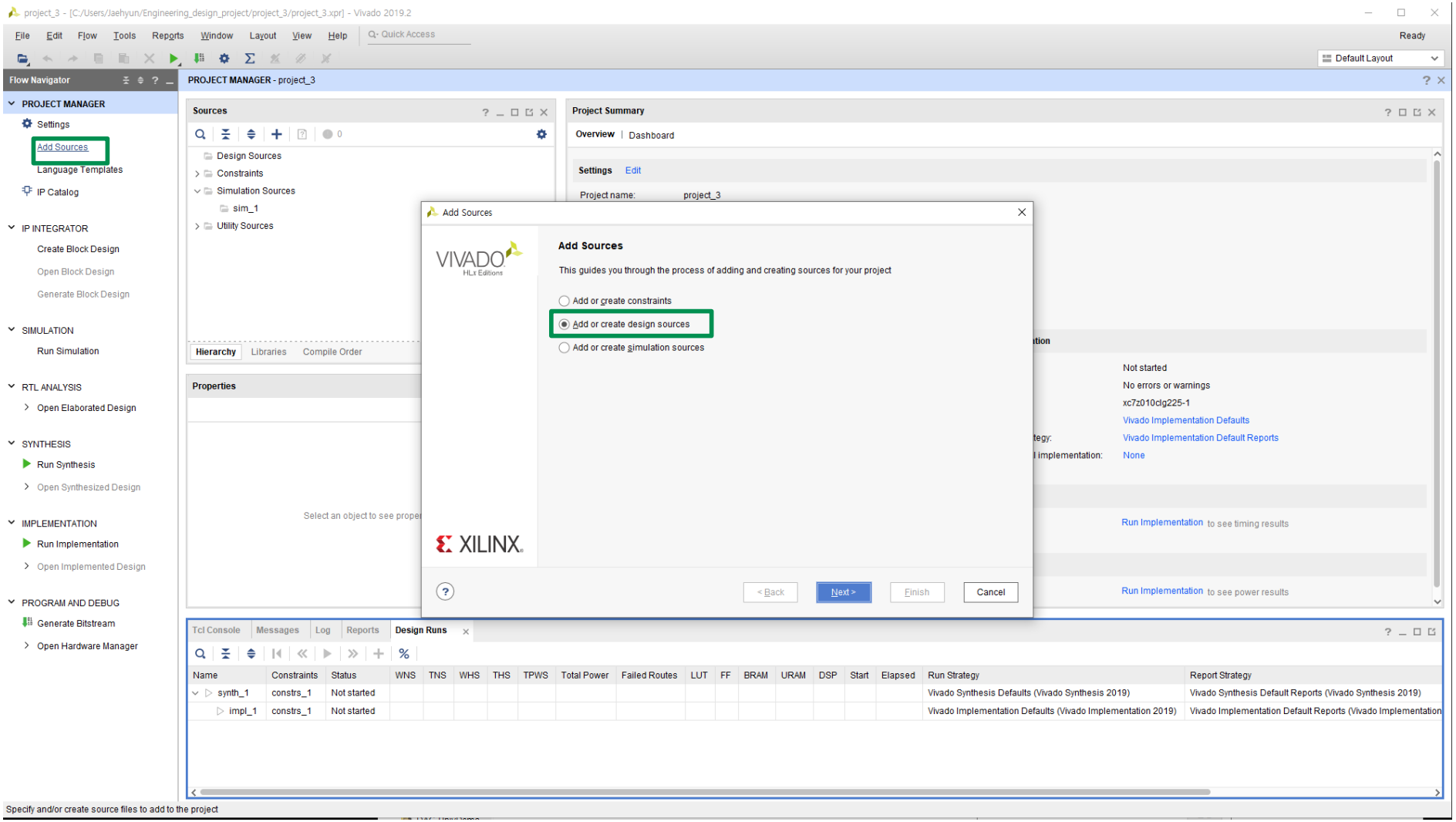
Create Project



Create Project

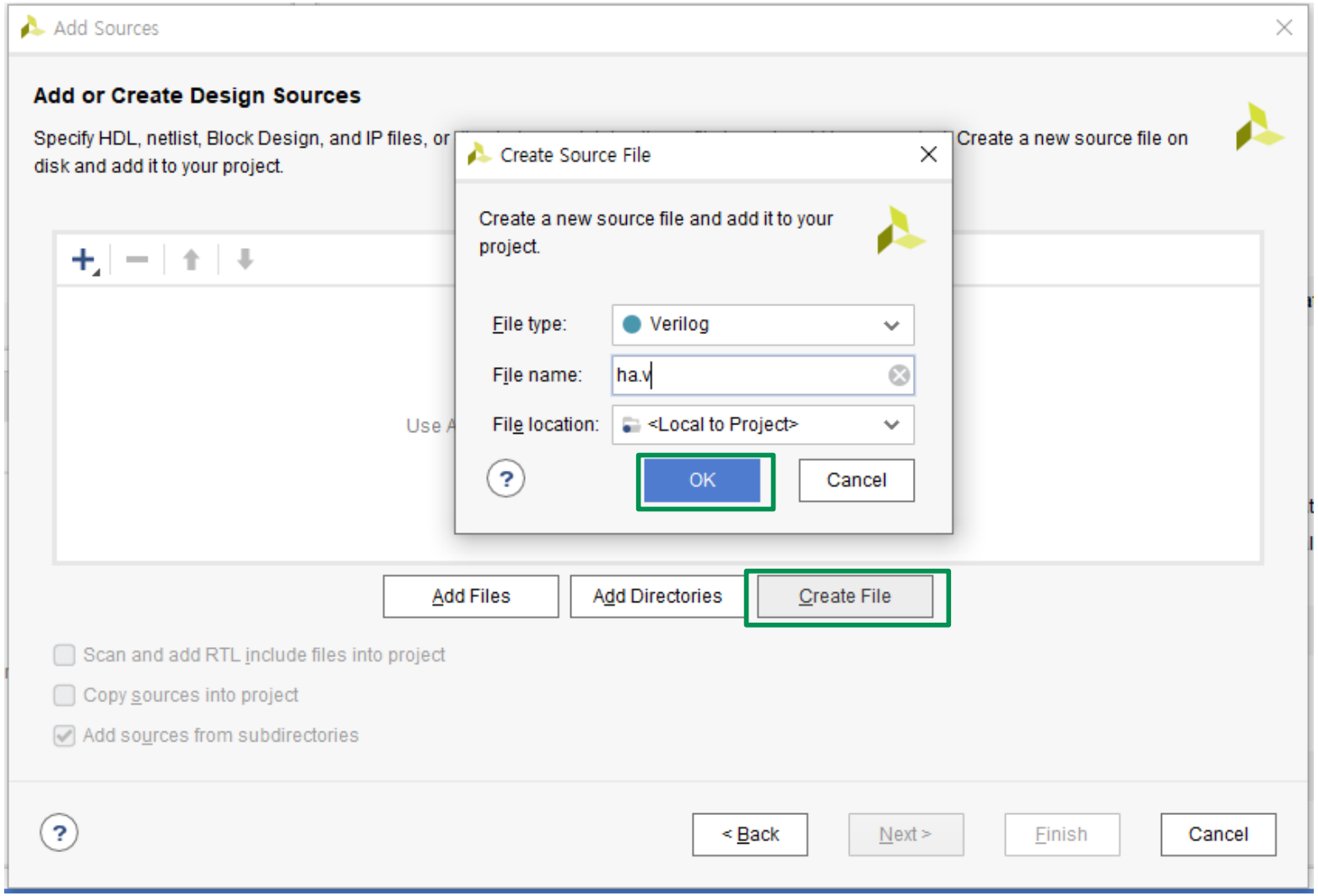


Write a Verilog Code

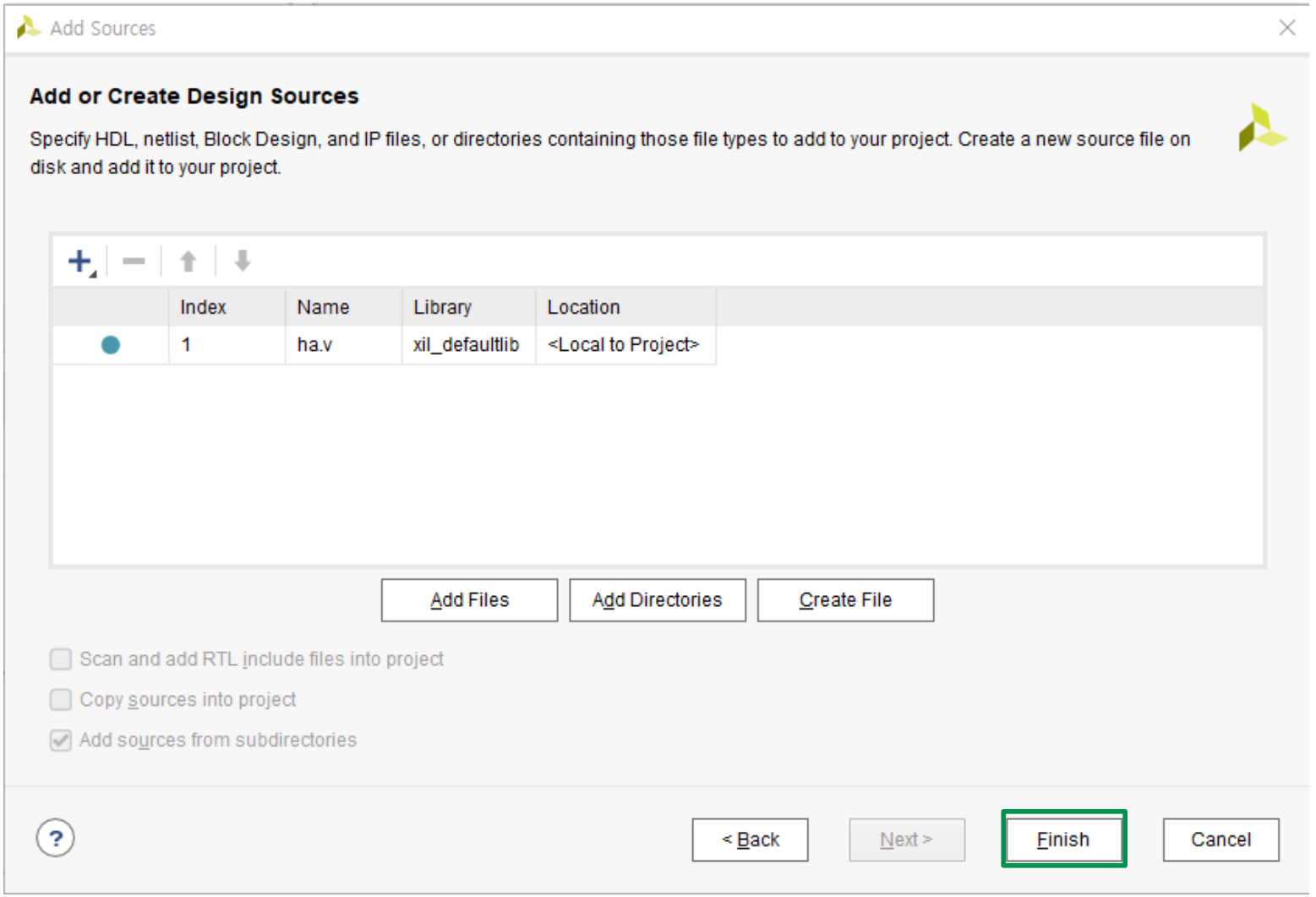


Write a Verilog Code

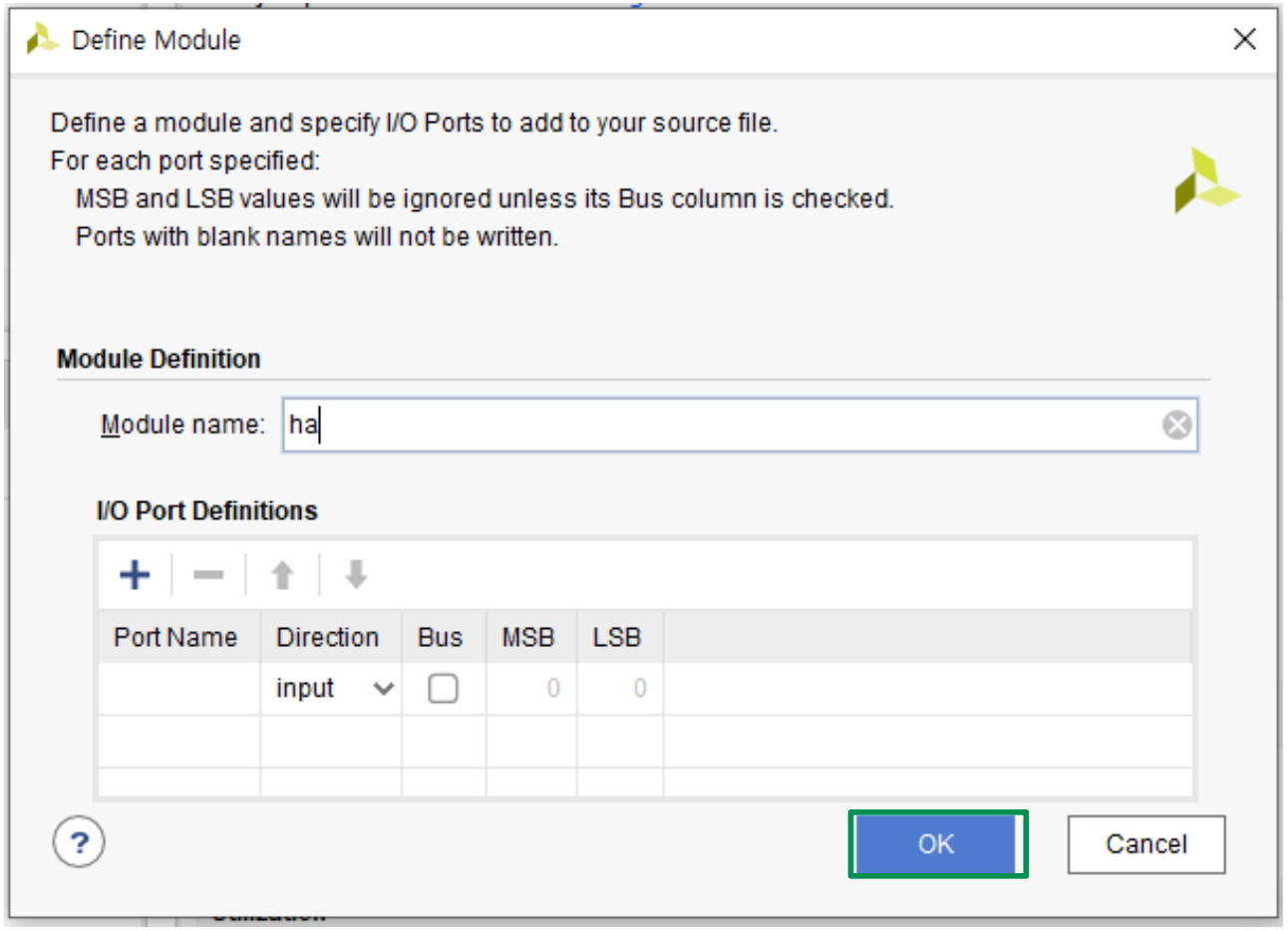
- Use a same file name as the module name



Write a Verilog Code

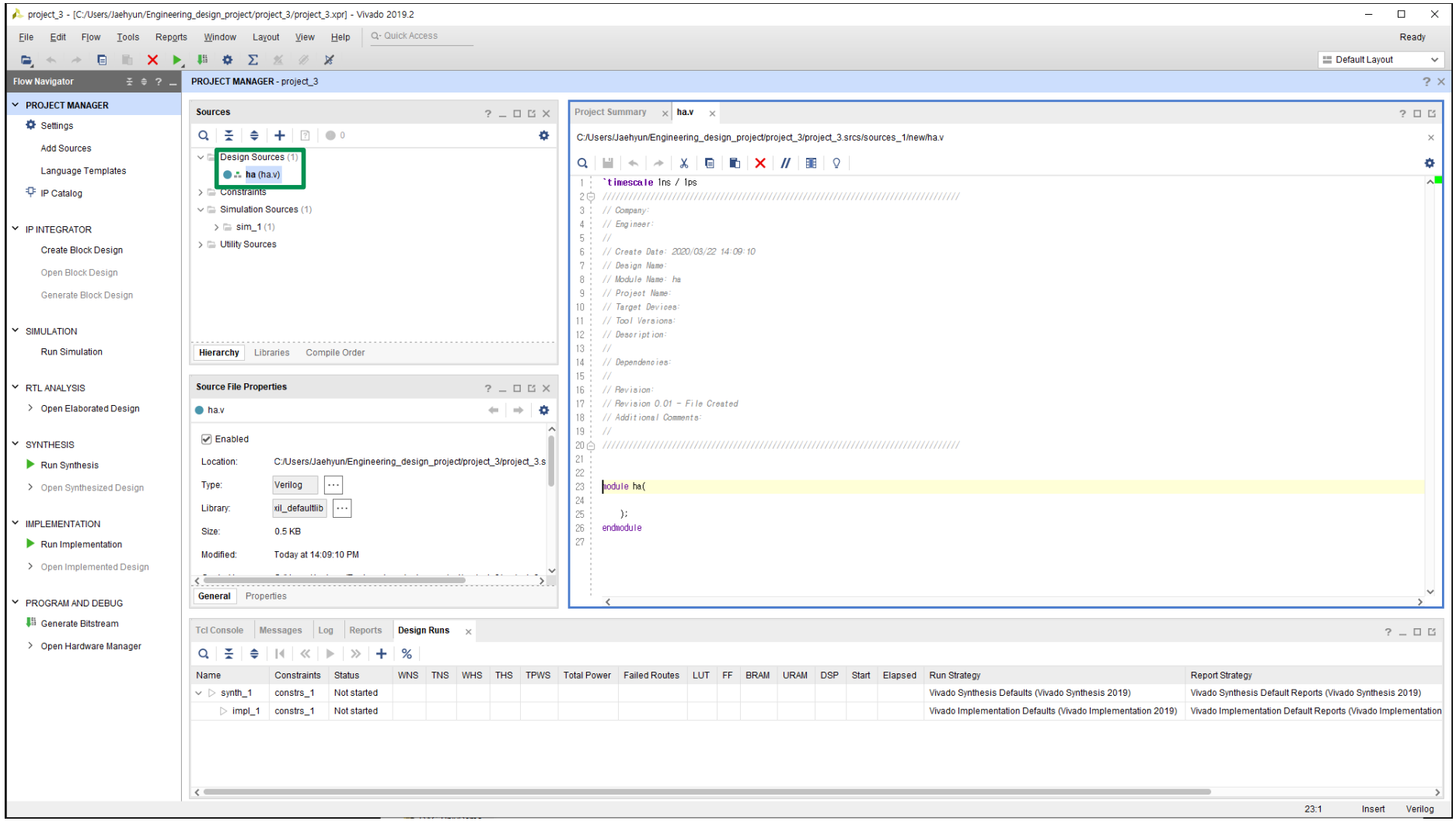


Write a Verilog Code



Write a Verilog Code

- Top module has a symbol at the left of source file



Write a Verilog Code

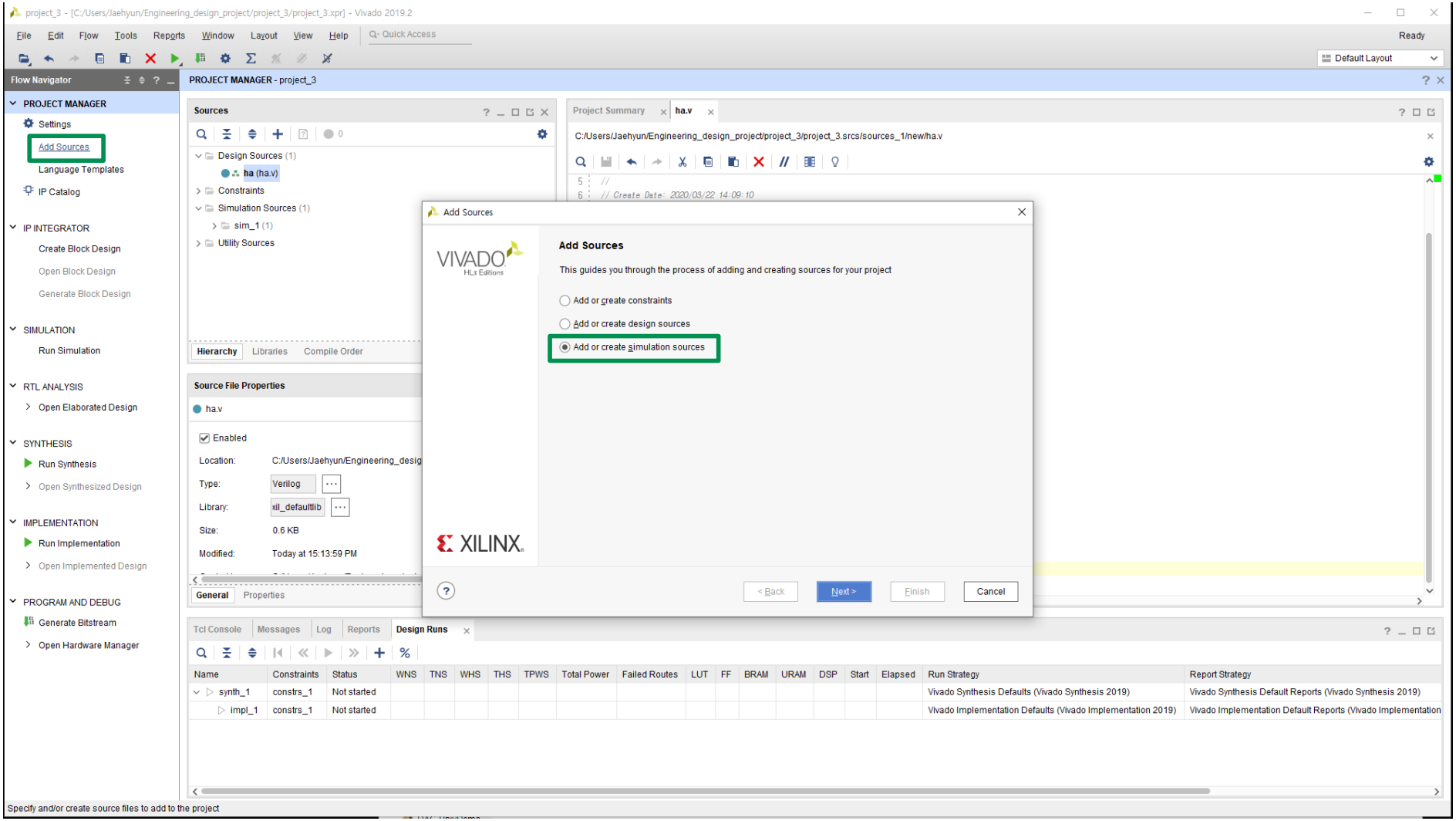
- Design a half adder

Project Summary | ha.v

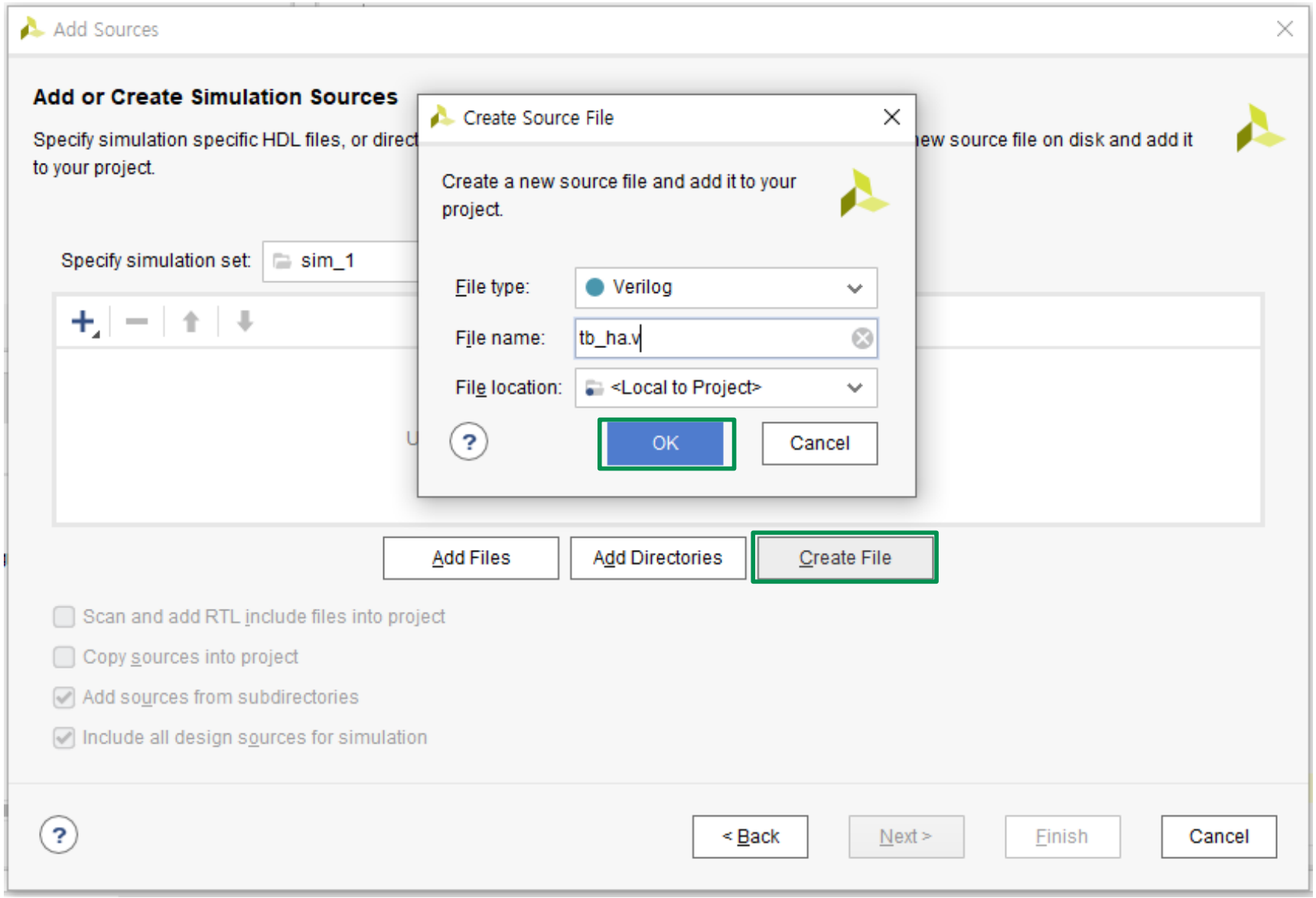
C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.srcs/sources_1/new/ha.v

```
5  //
6  // Create Date: 2020/03/22 14:09:10
7  // Design Name:
8  // Module Name: ha
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module ha(A, B, S, C);
24
25 input A;
26 input B;
27 output S;
28 output C;
29
30 assign S = A ^ B;
31 assign C = A & B;
32
33 endmodule
34
```

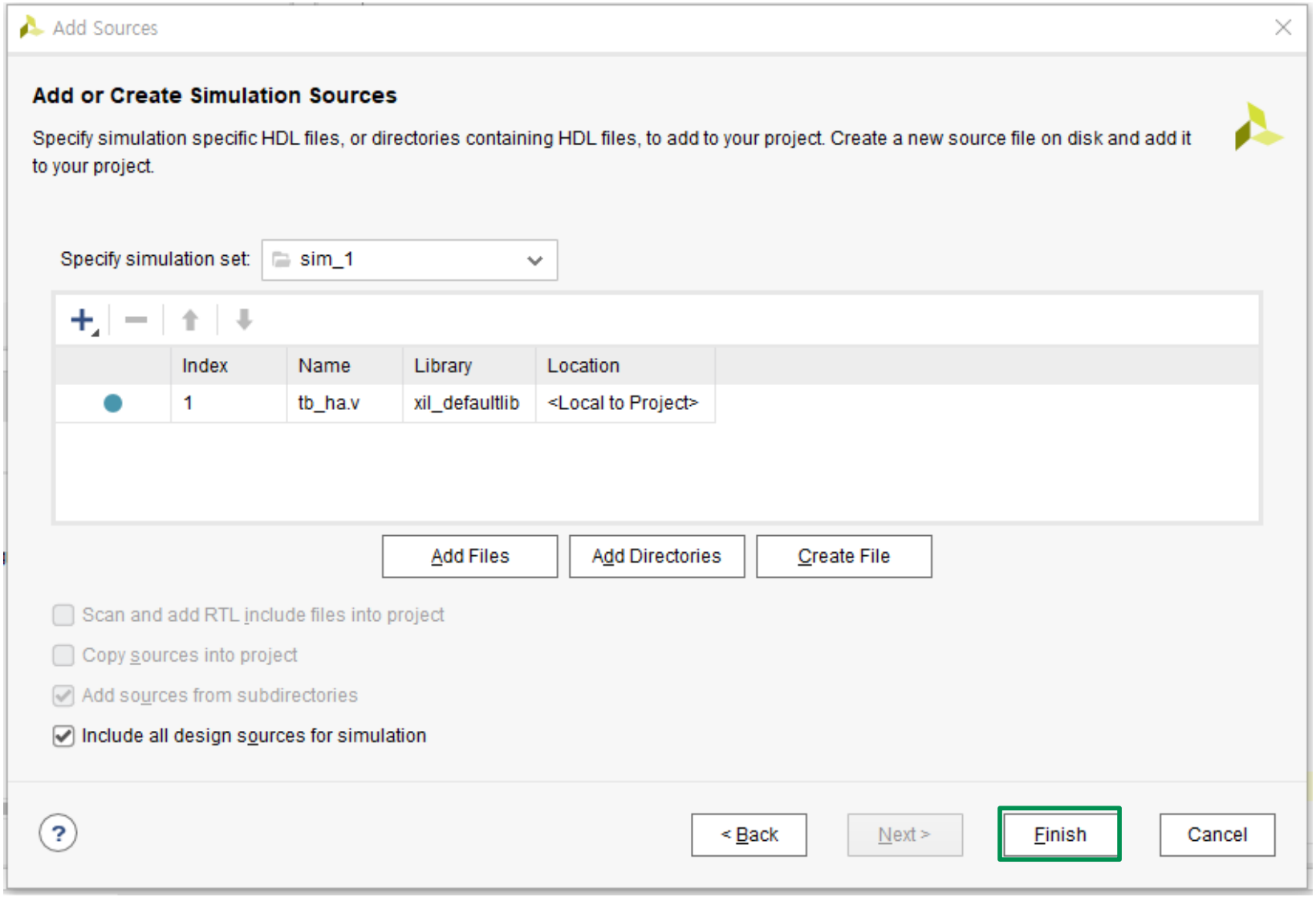
Run a Simulation



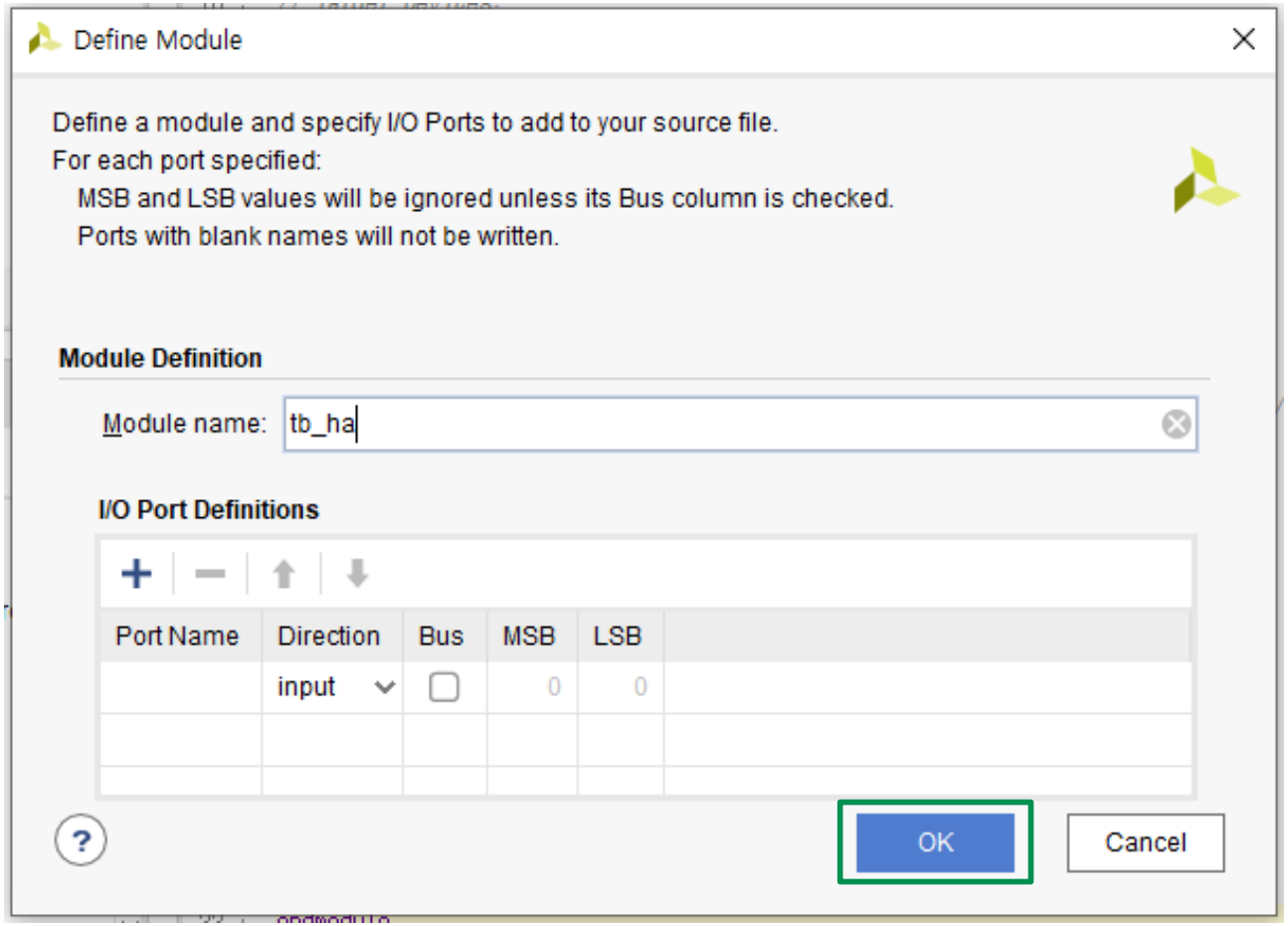
Run a Simulation



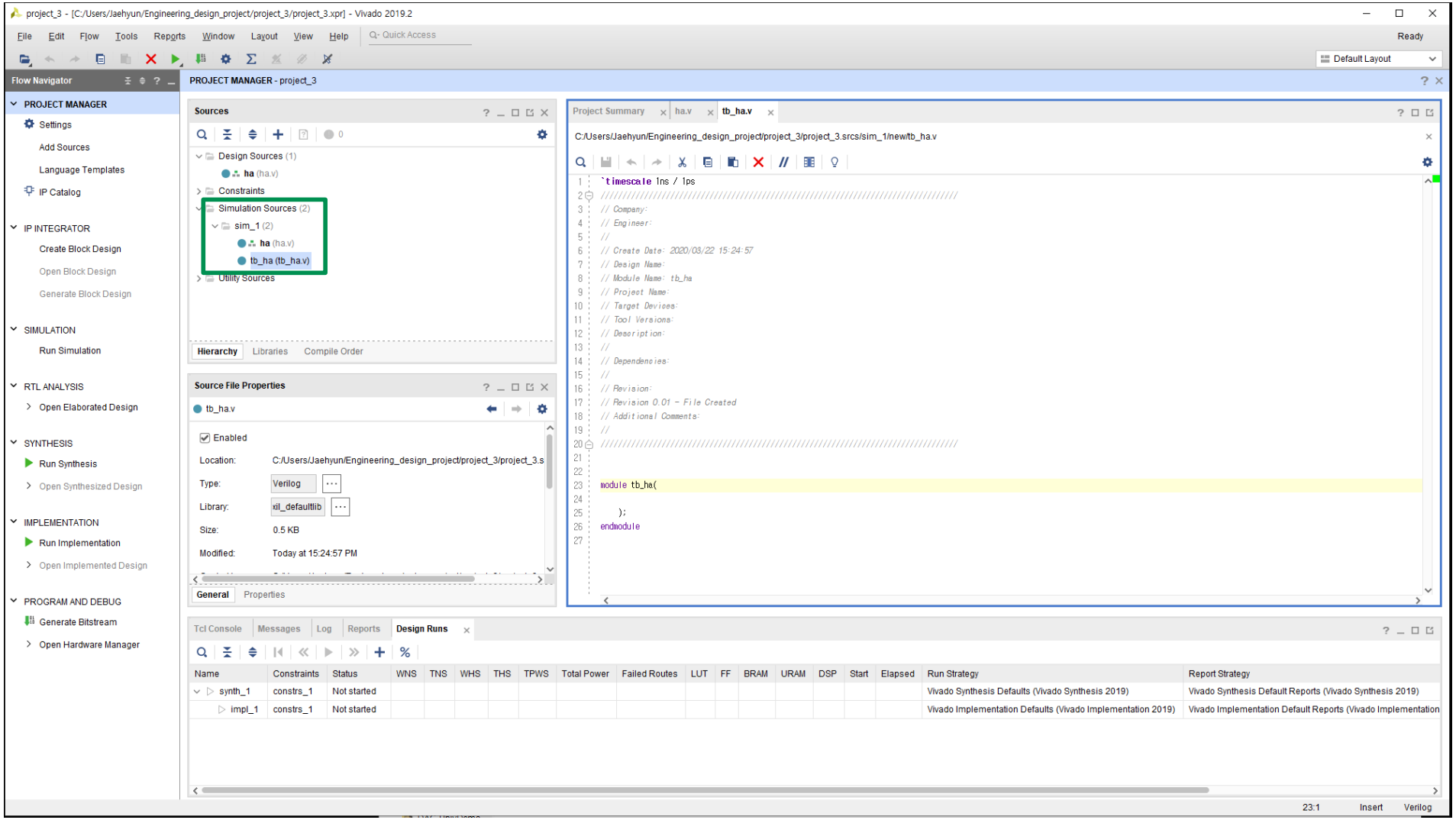
Run a Simulation



Run Simulation



Run a Simulation



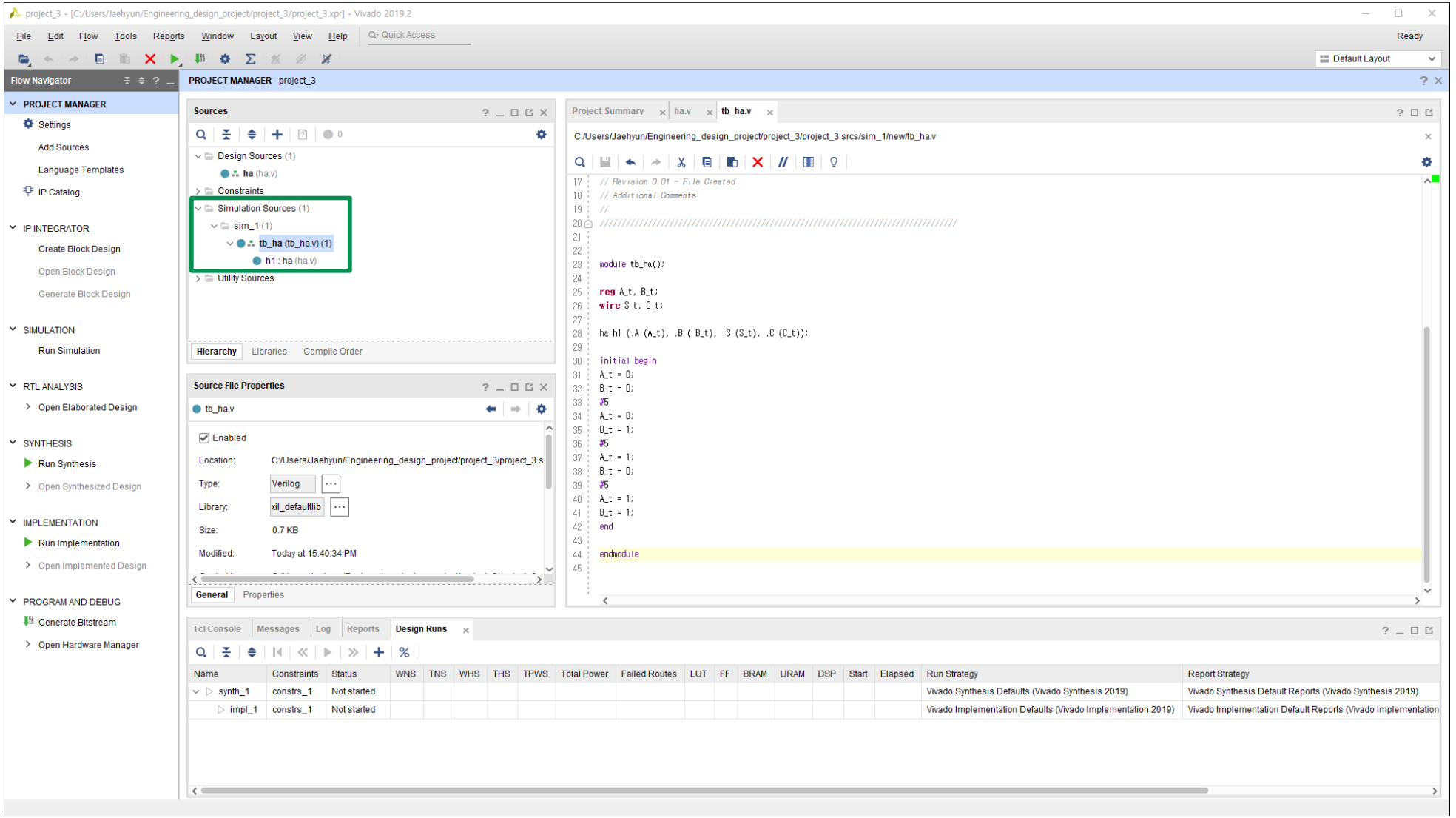
Run a Simulation

Project Summary | ha.v | tb_ha.v

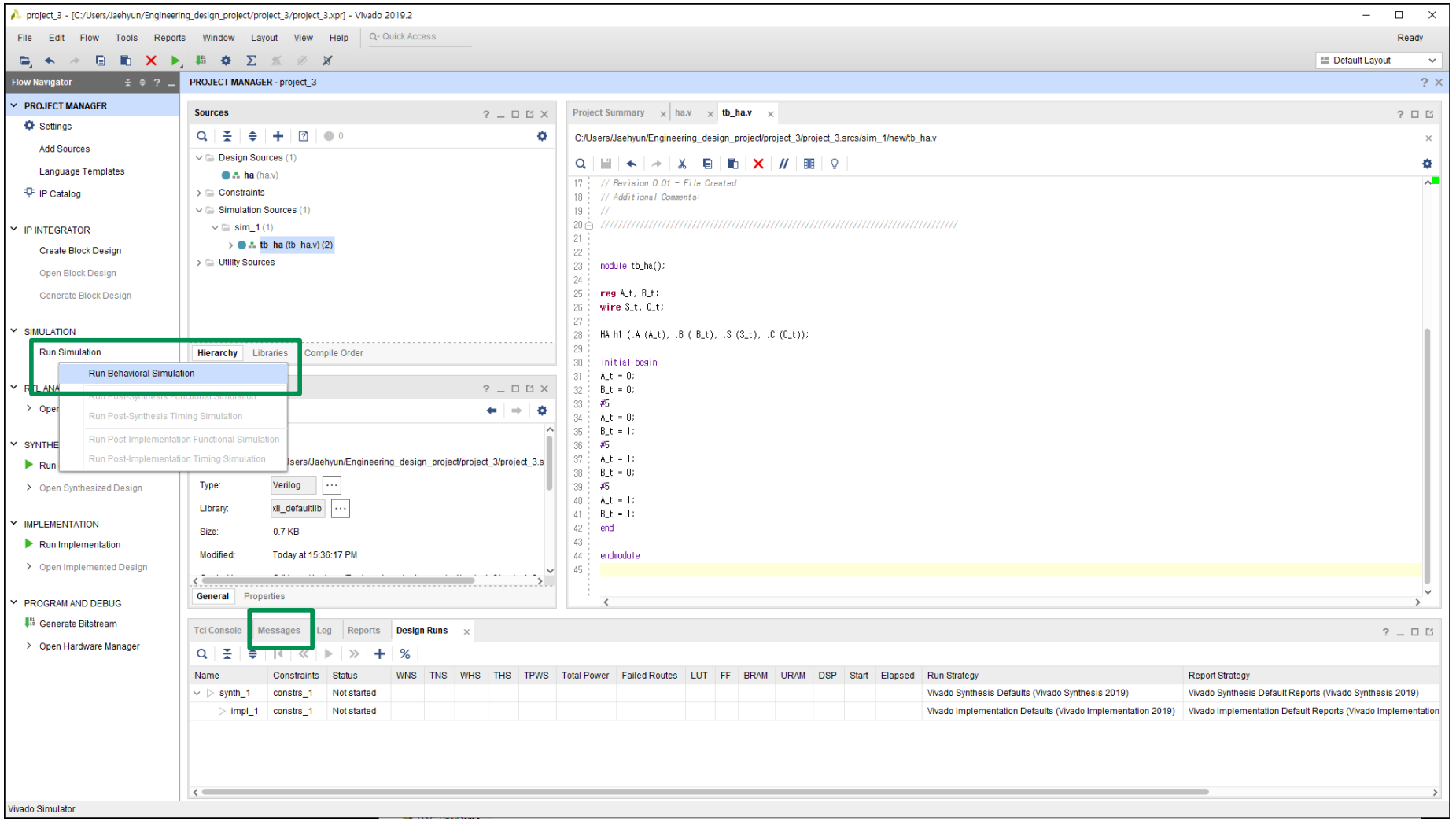
C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.srcs/sim_1/new/tb_ha.v

```
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module tb_ha();
24
25  reg A_t, B_t;
26  wire S_t, C_t;
27
28  ha h1 (.A (A_t), .B ( B_t), .S (S_t), .C (C_t));
29
30  initial begin
31  A_t = 0;
32  B_t = 0;
33  #5
34  A_t = 0;
35  B_t = 1;
36  #5
37  A_t = 1;
38  B_t = 0;
39  #5
40  A_t = 1;
41  B_t = 1;
42  end
43
44  endmodule
45
```

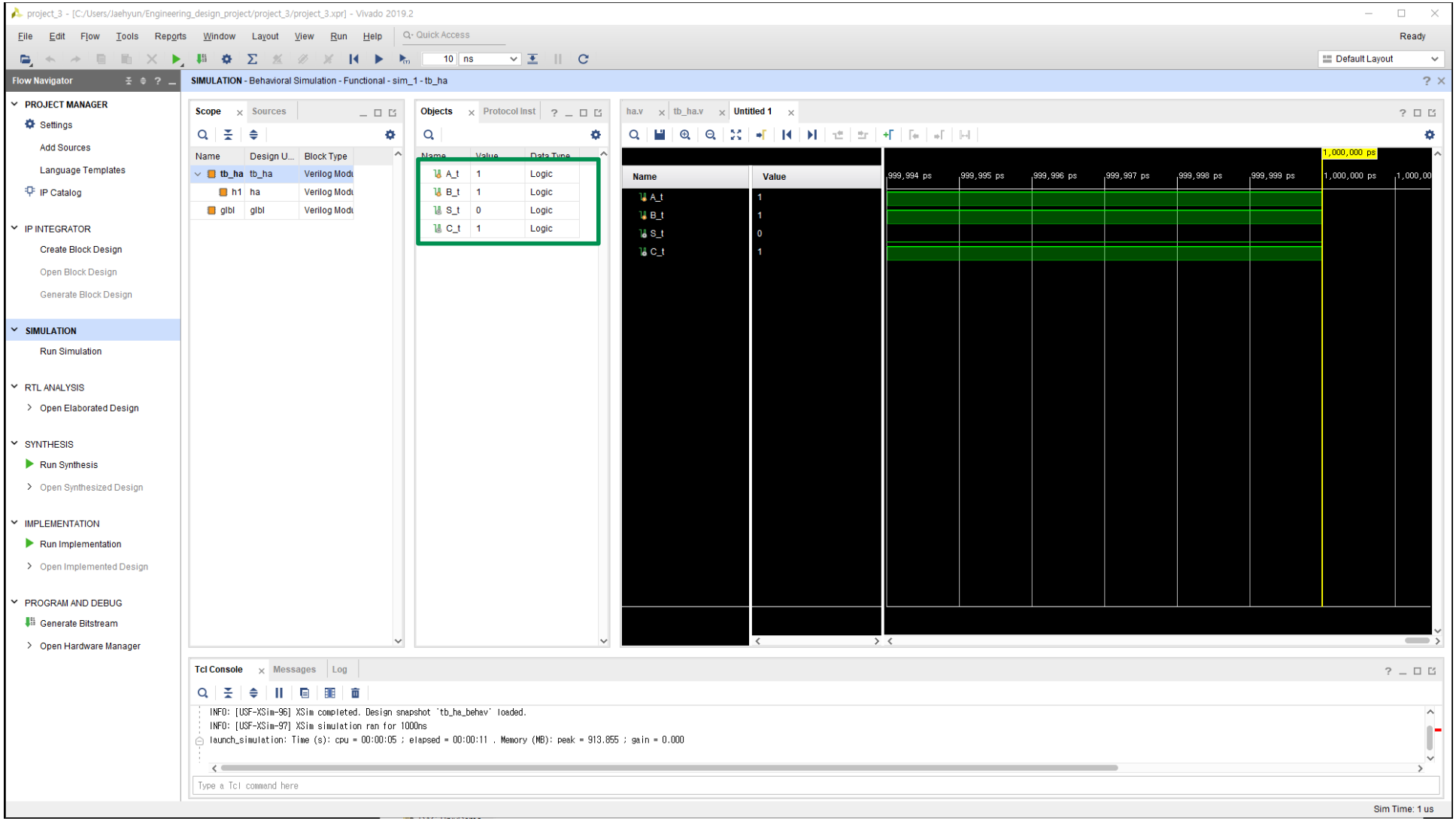
Run a Simulation



Run a Simulation

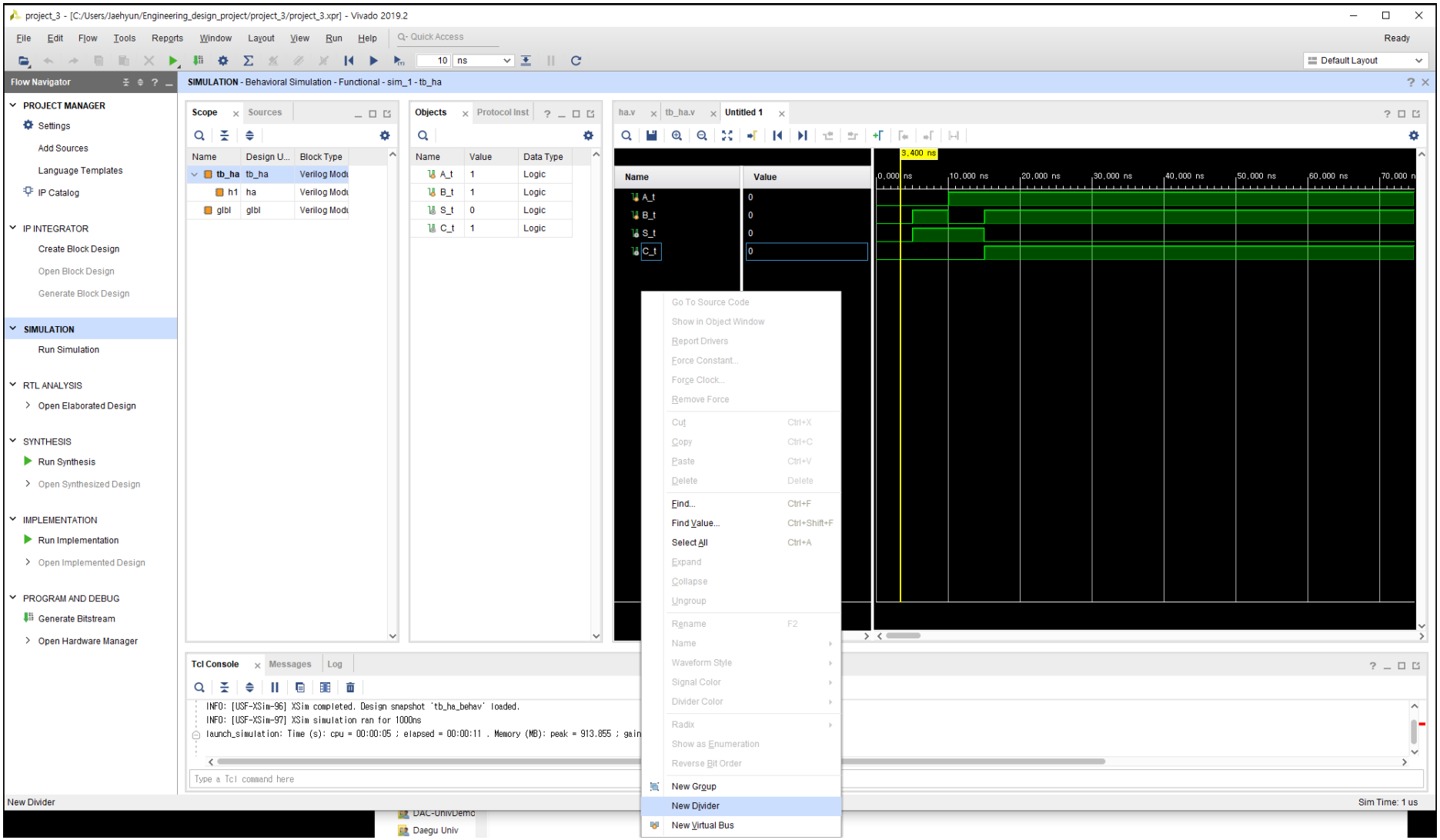


Run a Simulation

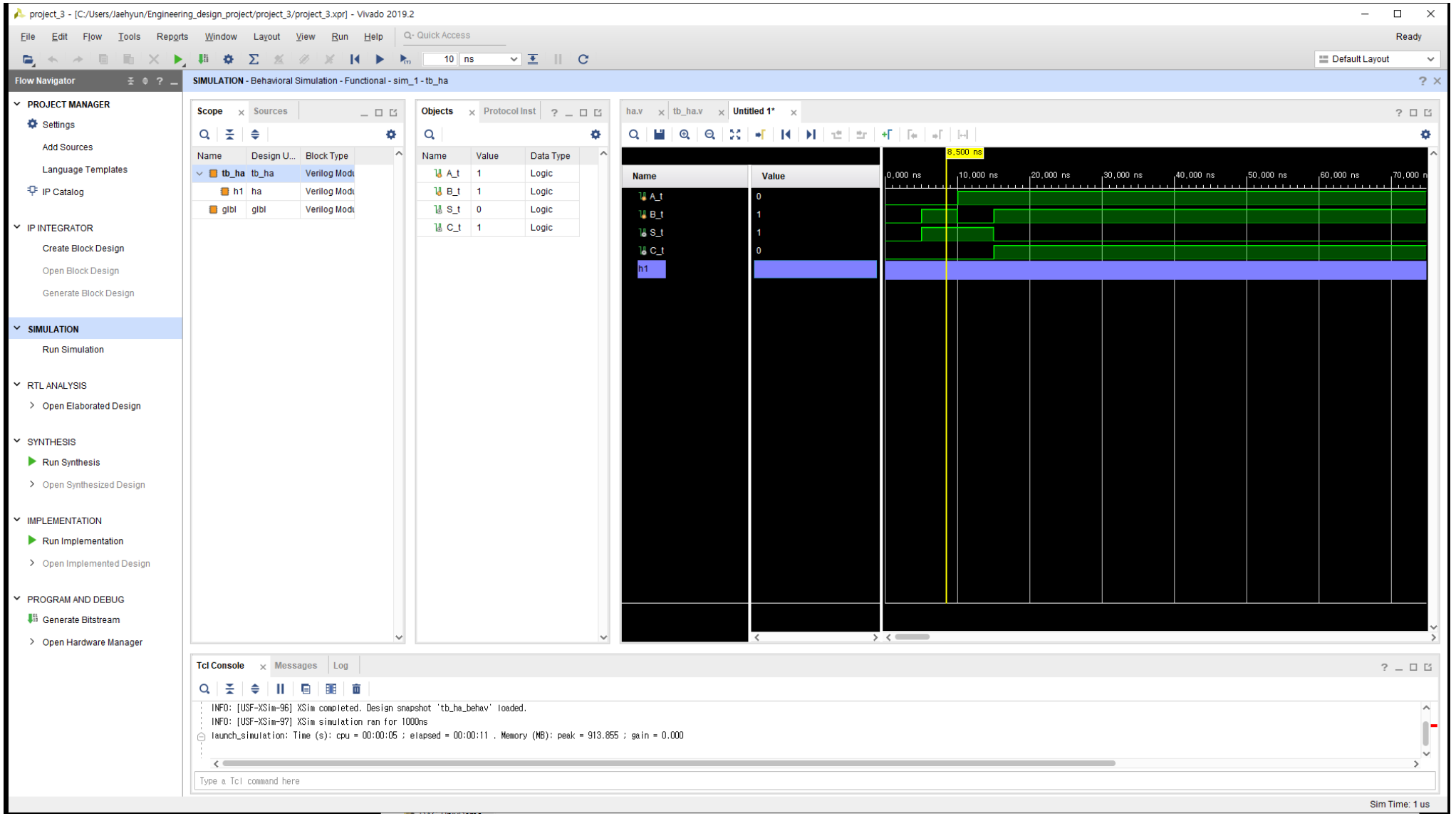


Run a Simulation

- Right click on a waveform

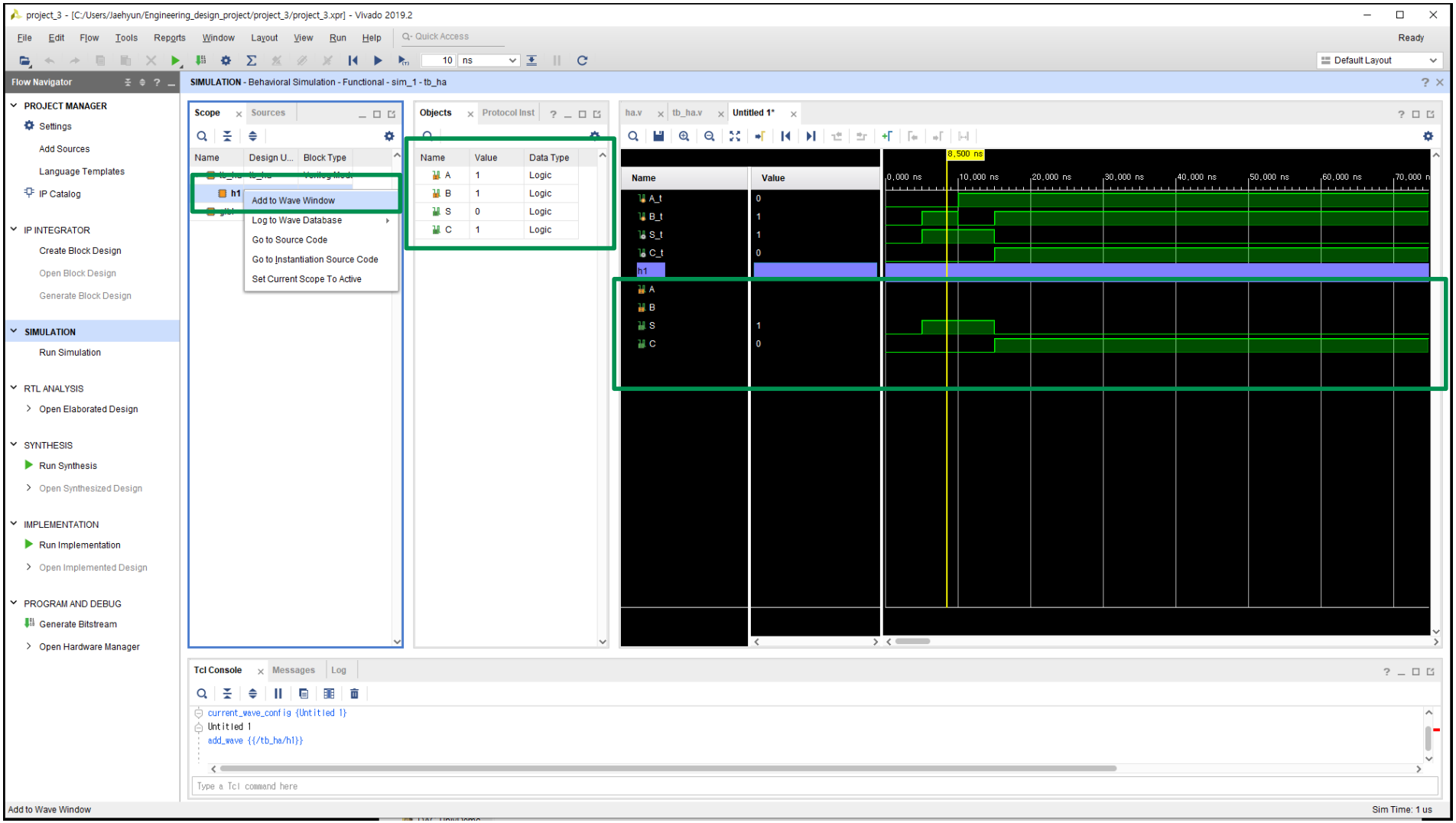


Run a Simulation



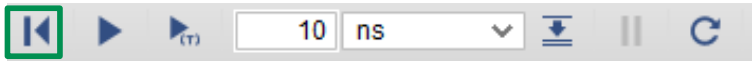
Run a Simulation

- Right click on a module

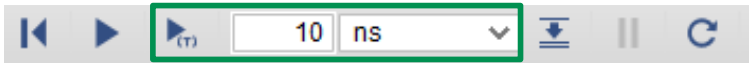


Run a Simulation

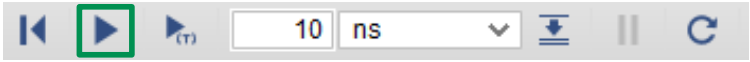
- Restart (Ctrl+Shift+F5)
  - Restart simulation without reflecting source code changes



- Run for …
  - Run a simulation for a specified time



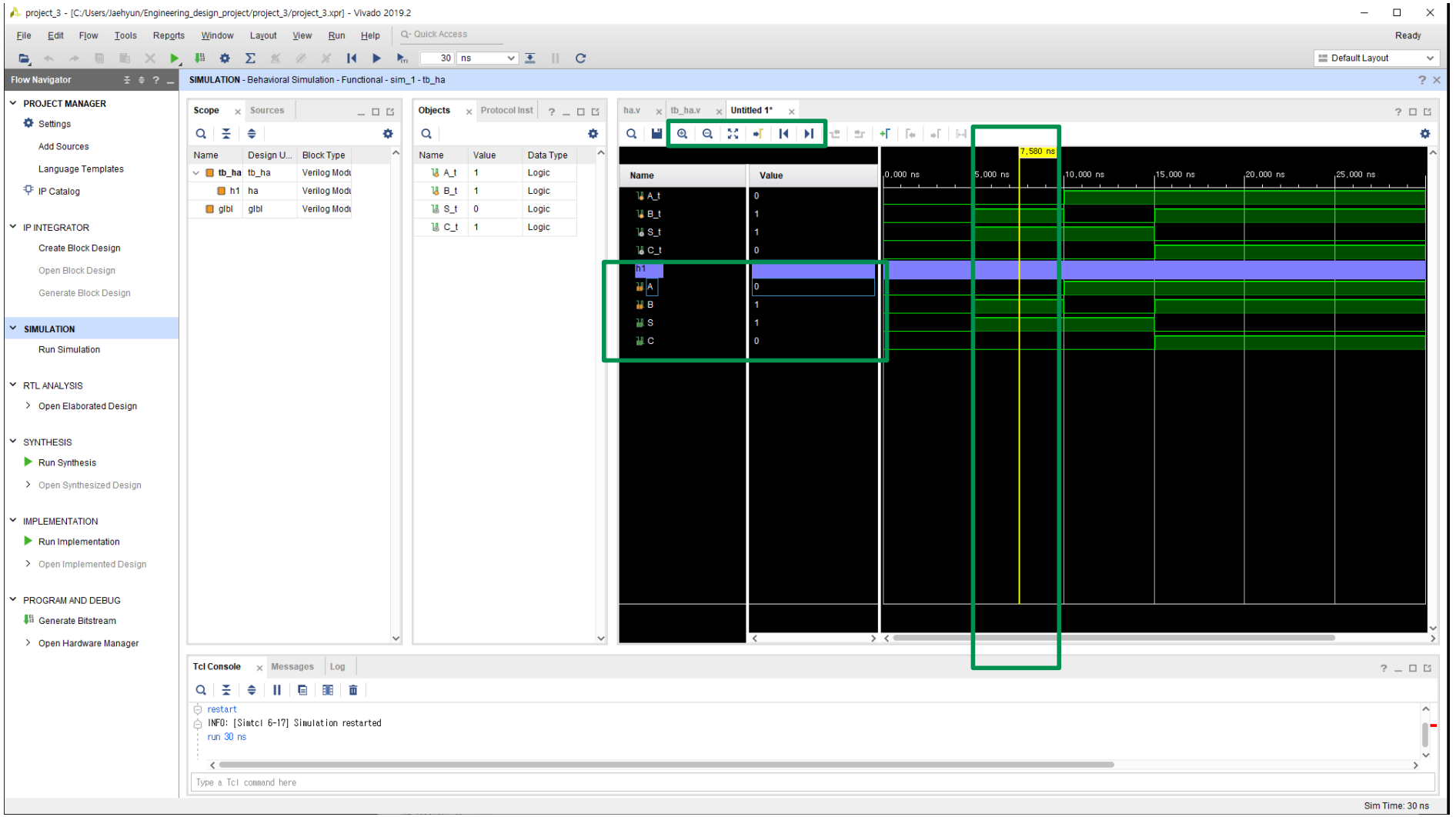
- Run All
  - Run a simulation until no signal changes for a time or it reaches $finish;



- Relaunch Simulation
  - Recompile source codes to reflect changes

Run a Simulation

- Restart and run a simulation for 30 ns



Run a Simulation

- Save Waveform configuration