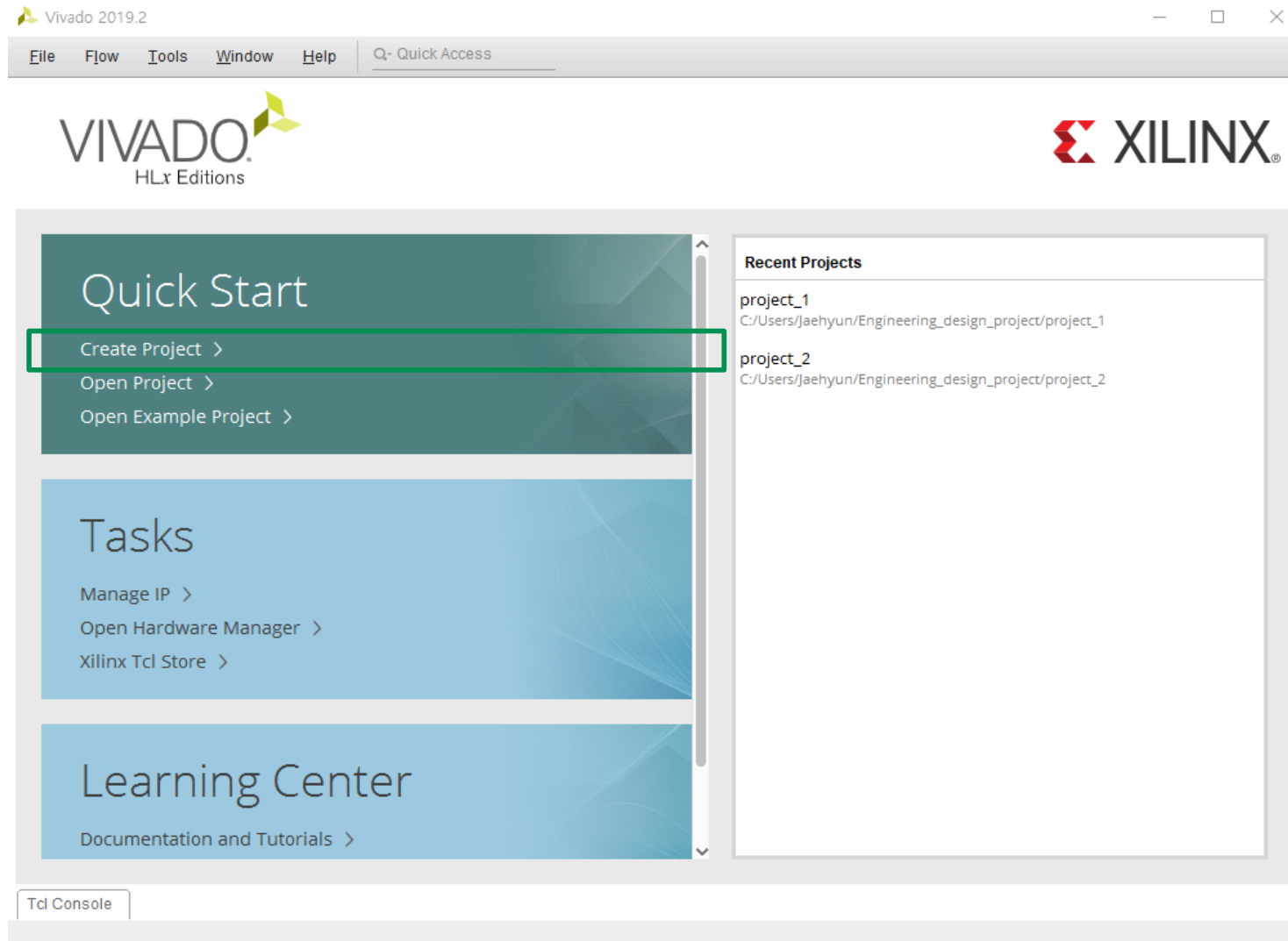


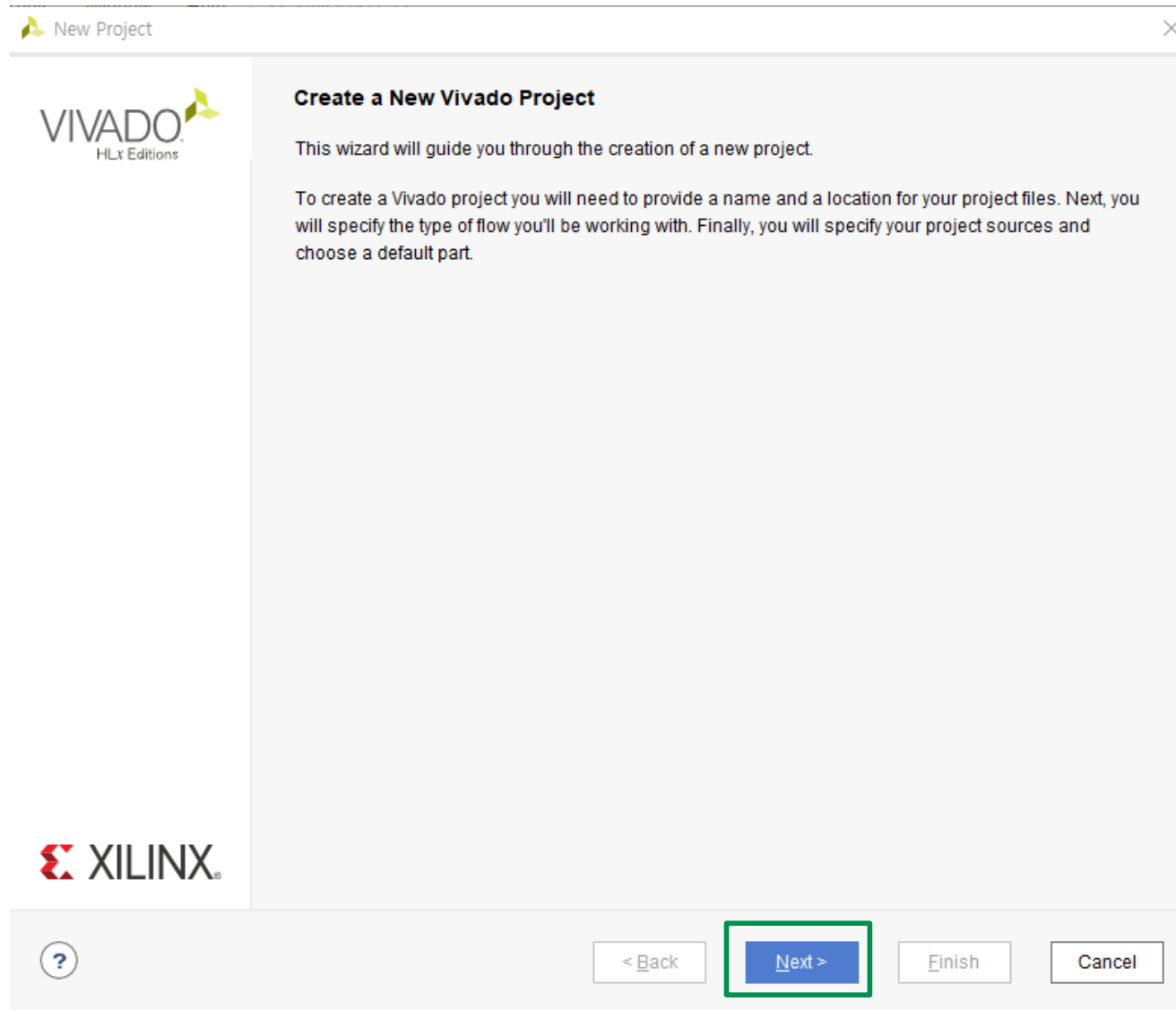
Xilinx Vivado Simulation

Create Project

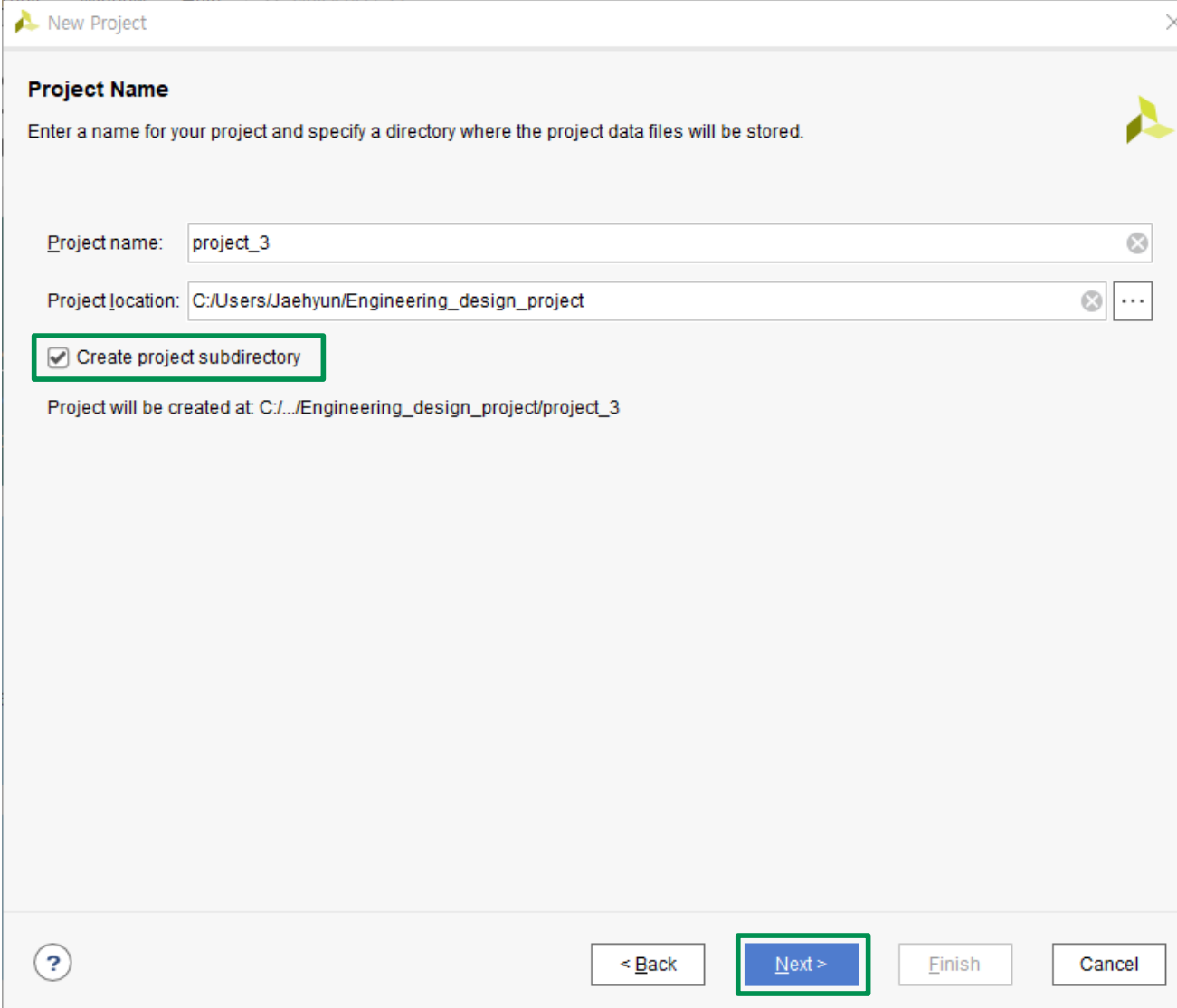
- Run Vivado



Create Project



Create Project



The image shows a 'New Project' dialog box with a title bar containing a yellow logo and a close button. The main area is titled 'Project Name' and contains instructions: 'Enter a name for your project and specify a directory where the project data files will be stored.' There are two text input fields: 'Project name:' with the value 'project_3' and 'Project location:' with the value 'C:/Users/Jaehyun/Engineering_design_project'. Below these is a checkbox labeled 'Create project subdirectory' which is checked. At the bottom, it states 'Project will be created at: C:/.../Engineering_design_project/project_3'. The bottom bar contains a help icon, a '< Back' button, a 'Next >' button (highlighted with a green border), a 'Finish' button, and a 'Cancel' button.

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: project_3


Project location: C:/Users/Jaehyun/Engineering_design_project

☒ Create project subdirectory


Project will be created at: C:/.../Engineering_design_project/project_3

? < Back Next > Finish Cancel

Create Project

 New Project ×

Project Type
Specify the type of project to create.



☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time


☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.




< Back


Next >

Finish





Cancel

Create Project

 New Project ×

Add Sources 

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

Add FilesAdd DirectoriesCreate File


☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

Target language: Verilog

Simulator language: Mixed




< Back


Next >

Finish





Cancel

Create Project

 New Project ×

Add Constraints (optional) 


Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below


Add FilesCreate File

☐ Copy constraints files into project

 < Back Next > Finish Cancel

Create Project

- Select xc7z010clg225-1 (just for simulation use)

 New Project ×

Default Part
Choose a default Xilinx part or board for your project.


Parts | Boards

[Reset All Filters](#)



Category: Package: Temperature:
Family: Speed: Static power:

Search:





Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs
xc7z007sclg225-2	225	54	14400	28800	50	0	66
xc7z007sclg225-1	225	54	14400	28800	50	0	66
xc7z007sclg400-2	400	100	14400	28800	50	0	66
xc7z007sclg400-1	400	100	14400	28800	50	0	66
xc7z010clg225-3	225	54	17600	35200	60	0	80
xc7z010clg225-2	225	54	17600	35200	60	0	80
xc7z010clg225-1	225	54	17600	35200	60	0	80
xc7z010clg400-3	400	100	17600	35200	60	0	80



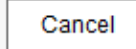
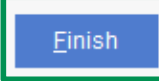

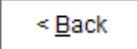

Create Project



New Project Summary

-  A new RTL project named 'project_3' will be created.
-  No source files or directories will be added. Use Add Sources to add them later.
-  No constraints files will be added. Use Add Sources to add them later.
-  The default part and product family for the new project:
 - Default Part: xc7z010clg225-1
 - Product: Zynq-7000
 - Family: Zynq-7000
 - Package: clg225
 - Speed Grade: -1

To create the project, click Finish



Create Project

project_3 - [C:/Users/jaehyun/Engineering_design_project/project_3/project_3.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Flow Navigator PROJECT MANAGER - project_3

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

Design Sources

- Constraints
- Simulation Sources
 - sim_1
- Utility Sources

Properties

Select an object to see properties

Project Summary

Overview | Dashboard

Settings Edit

Project name: project_3
Project location: C:/Users/Jaehyun/Engineering_design_project/project_3
Product family: Zynq-7000
Project part: xc7z010clg225-1
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed

Synthesis

Status: Not started
Messages: No errors or warnings
Part: xc7z010clg225-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None

Implementation

Status: Not started
Messages: No errors or warnings
Part: xc7z010clg225-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None

DRC Violations

Run Implementation to see DRC results

Timing

Run Implementation to see timing results

Utilization

Run Synthesis to see utilization results

Power

Run Implementation to see power results

Tcl Console Messages Log Reports Design Runs x

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Implementation 2019)

Write a Verilog Code

project_3 - [C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Flow Navigator PROJECT MANAGER - project_3

PROJECT MANAGER

- Settings
- Add Sources**
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1
- Utility Sources

Project Summary

Overview | Dashboard

Settings Edit

Project name: project_3

Add Sources

VIVADO HLS Editions

Add Sources

This guides you through the process of adding and creating sources for your project.

- ☐ Add or create constraints
- ☒ Add or create design sources
- ☐ Add or create simulation sources

XILINX

Properties

Select an object to see properties

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Implementation 2019)

Specify and/or create source files to add to the project

Not started

No errors or warnings

xc7z010clg225-1

[Vivado Implementation Defaults](#)

Legacy: [Vivado Implementation Default Reports](#)

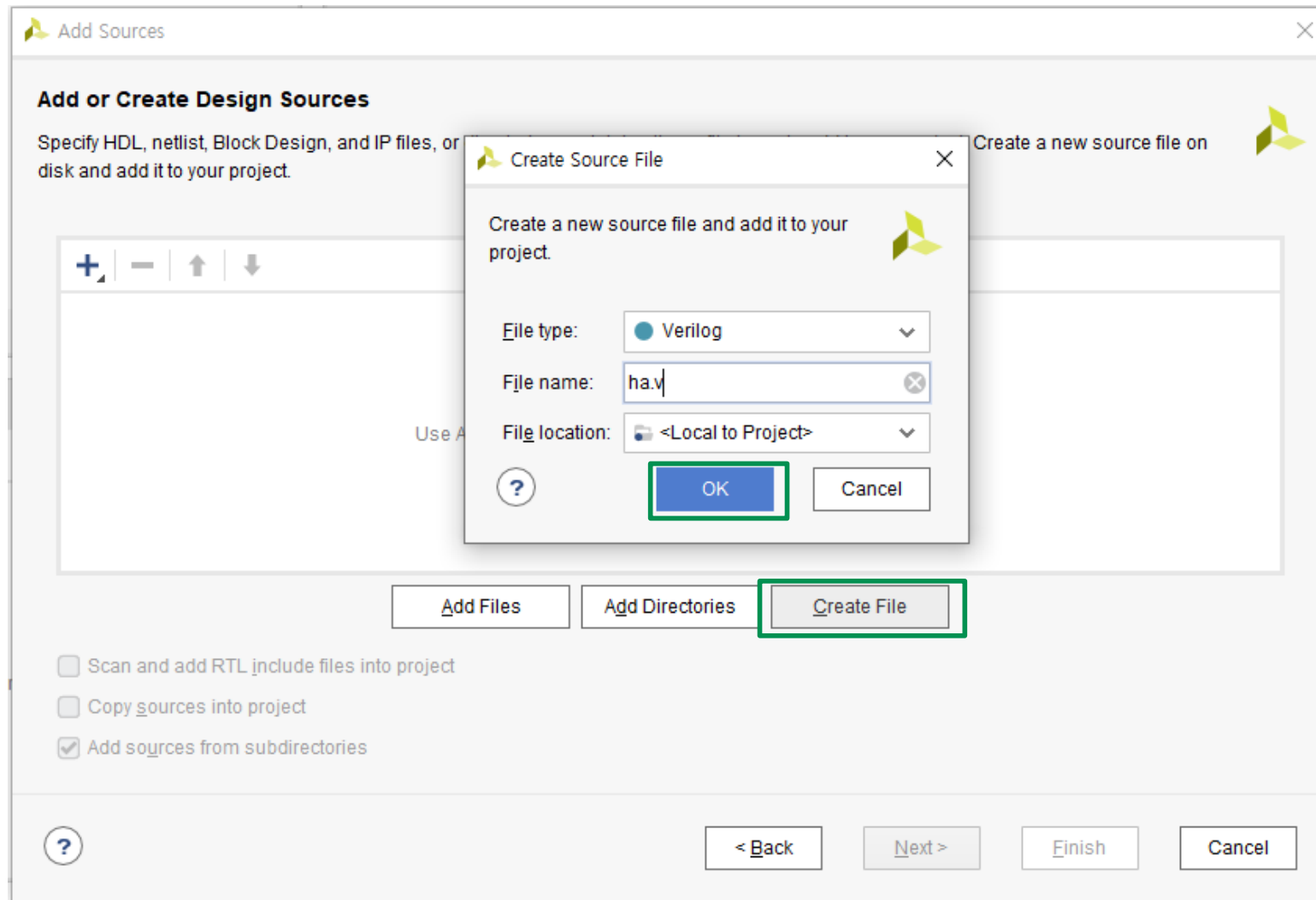
Implementation: None

[Run Implementation](#) to see timing results


[Run Implementation](#) to see power results


Write a Verilog Code

- Use a same file name as the module name








Write a Verilog Code

 Add Sources ×

Add or Create Design Sources 

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

	Index	Name	Library	Location
	1	ha.v	xil_defaultlib	<Local to Project>

Add Files


Add Directories

Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories



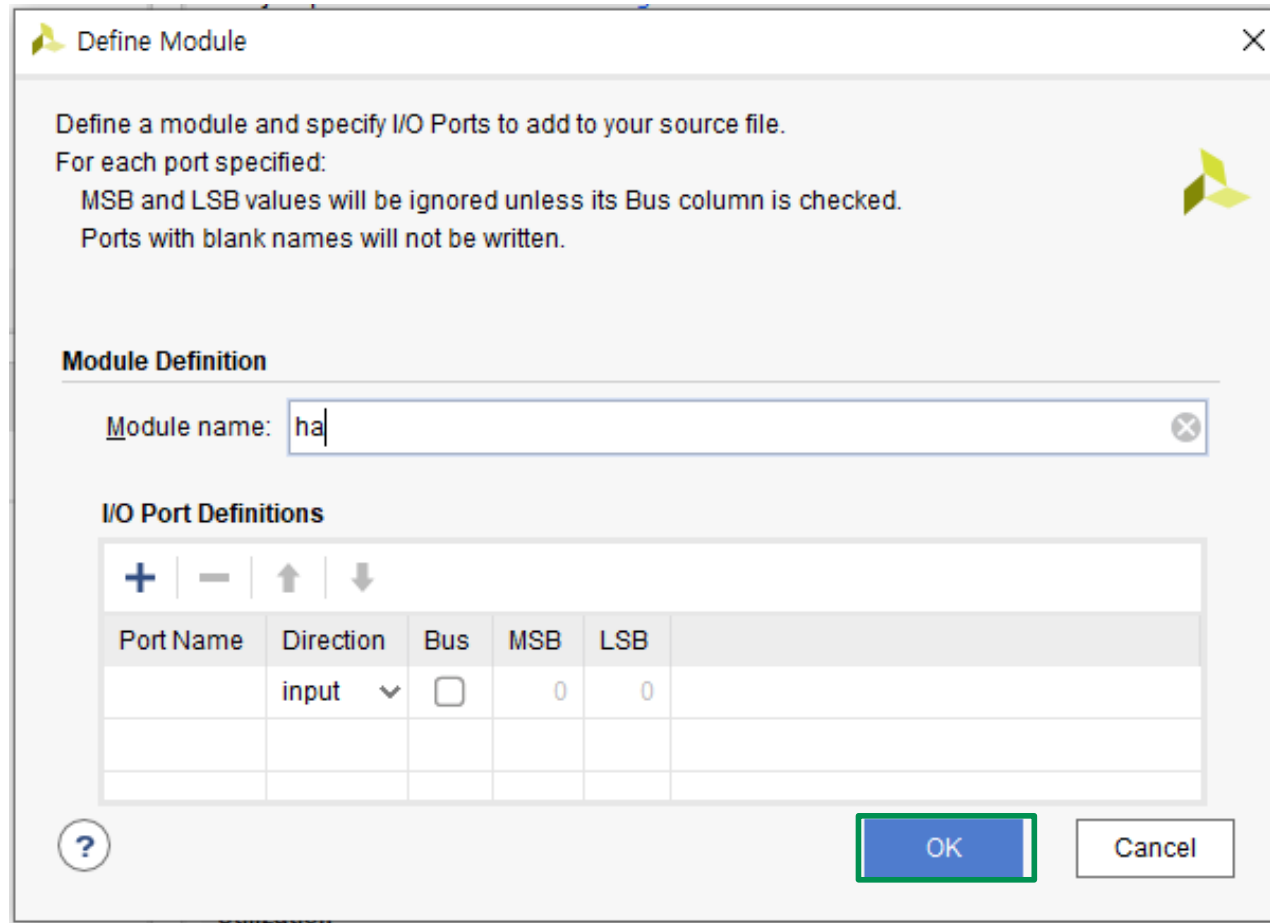
< Back

Next >

Finish

Cancel

Write a Verilog Code

The image shows a 'Define Module' dialog box from a software tool. It has a title bar with a yellow cube icon and a close button. The main area contains instructions: 'Define a module and specify I/O Ports to add to your source file. For each port specified: MSB and LSB values will be ignored unless its Bus column is checked. Ports with blank names will not be written.' Below this is a 'Module Definition' section with a text field for 'Module name' containing 'ha'. The 'I/O Port Definitions' section features a table with columns: Port Name, Direction, Bus, MSB, and LSB. The first row has 'input' in the Direction column, an unchecked checkbox in the Bus column, and '0' in the MSB and LSB columns. Above the table are icons for adding (+), removing (-), and moving up/down ports. At the bottom are a help icon (?), an 'OK' button, and a 'Cancel' button.

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name:

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
	input	<input type="checkbox"/>	0	0

?

OK Cancel

Write a Verilog Code

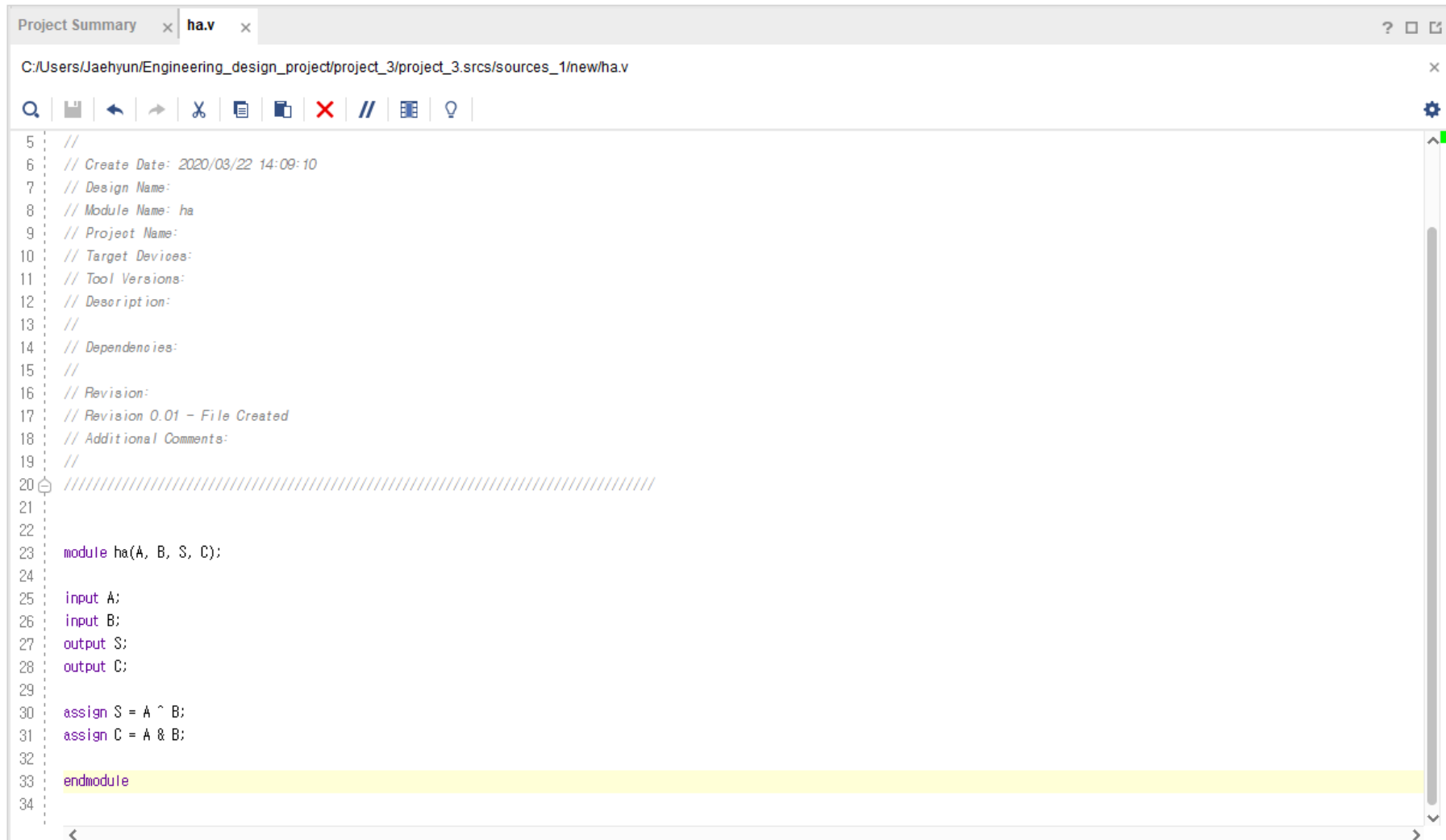
- Top module has a symbol at the left of source file

The screenshot displays the Vivado 2019.2 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The left sidebar shows the Flow Navigator with sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, RTL ANALYSIS, SYNTHESIS, IMPLEMENTATION, and PROGRAM AND DEBUG. The PROJECT MANAGER section is expanded, showing Design Sources (1) with a green box highlighting the top module 'ha (ha.v)'. Below this, the Source File Properties for 'ha.v' are shown, indicating it is a Verilog file of 0.5 KB. The main editor window displays the Verilog code for 'ha.v', which includes a header section with project information and a module definition 'module ha(' followed by a semicolon and 'endmodule'. The bottom panel shows the Design Runs table, which lists the synthesis and implementation runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Implementation 2019)

Write a Verilog Code

- Design a half adder



The screenshot shows a Verilog code editor window with a tab labeled 'ha.v'. The file path is 'C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.srscs/sources_1/new/ha.v'. The code is as follows:

```
5 //  
6 // Create Date: 2020/03/22 14:09:10  
7 // Design Name:  
8 // Module Name: ha  
9 // Project Name:  
10 // Target Devices:  
11 // Tool Versions:  
12 // Description:  
13 //  
14 // Dependencies:  
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////  
21  
22  
23 module ha(A, B, S, C);  
24  
25   input A;  
26   input B;  
27   output S;  
28   output C;  
29  
30   assign S = A ^ B;  
31   assign C = A & B;  
32  
33 endmodule  
34
```


Run a Simulation

The screenshot displays the Vivado 2019.2 IDE interface. The 'PROJECT MANAGER - project_3' window is open, showing the 'Sources' tab. The 'Add Sources' dialog box is in the foreground, with the 'Add or create simulation sources' option selected. The 'Source File Properties' window is also open, showing the 'General' tab for the file 'ha.v'. The 'Design Runs' table at the bottom shows the status of the simulation.

Source File Properties

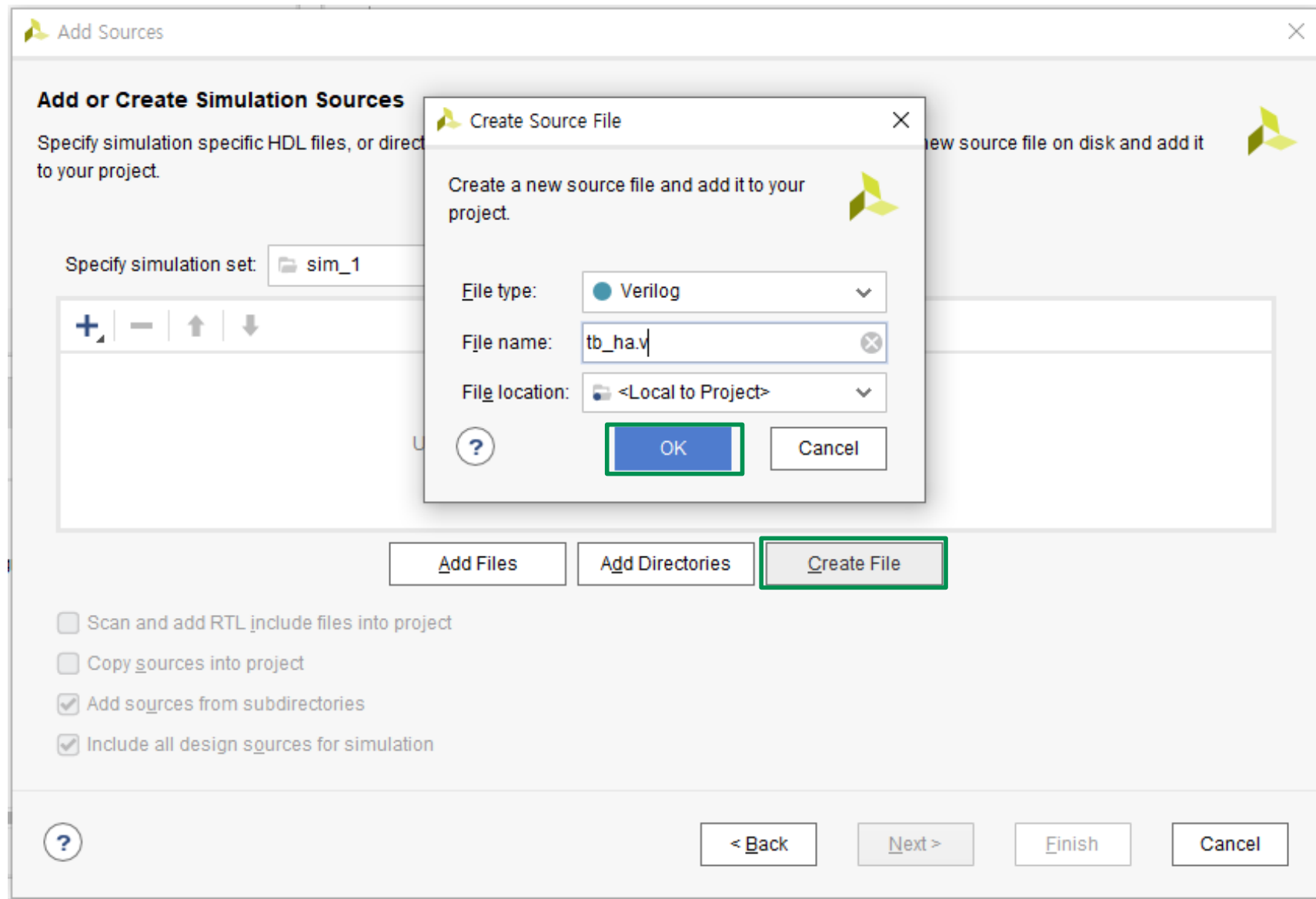
Source File Properties for **ha.v**

- ☒ Enabled
- Location: C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.srcs/sources_1/new/ha.v
- Type: Verilog
- Library: xil_defaultlib
- Size: 0.6 KB
- Modified: Today at 15:13:59 PM


Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Implementation 2019)

Run a Simulation








Run a Simulation

 Add Sources ✕

Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1 ▾

	Index	Name	Library	Location
	1	tb_ha.v	xil_defaultlib	<Local to Project>

Add Files

Add Directories


Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

☒ Include all design sources for simulation



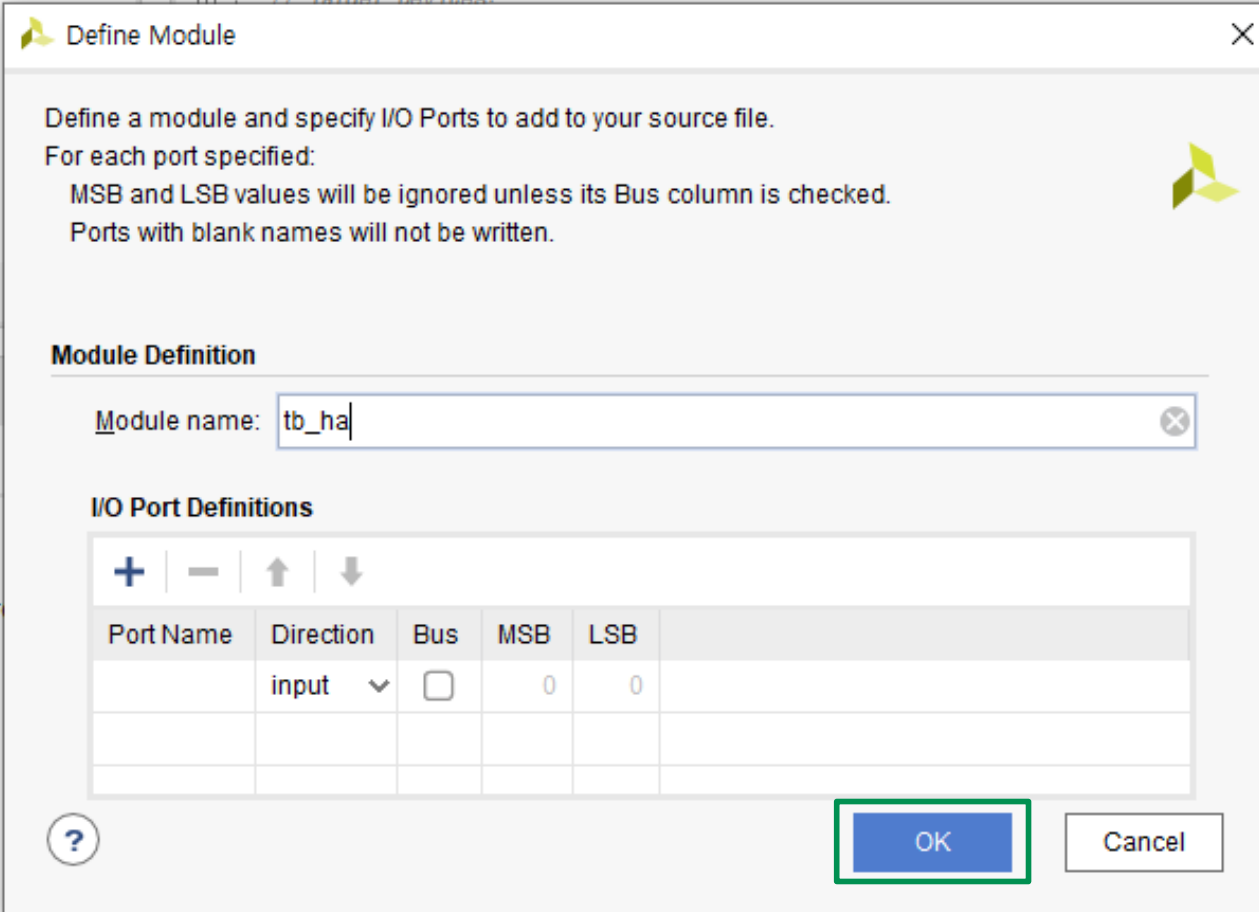
< Back

Next >

Finish

Cancel

Run Simulation




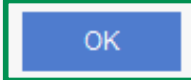
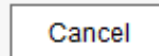
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name:

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
	input	<input type="checkbox"/>	0	0

Run a Simulation

The screenshot displays the Vivado 2019.2 IDE interface. The left sidebar contains the 'PROJECT MANAGER' tree, which is expanded to show 'Simulation Sources (2)'. Two sources are listed: 'ha (ha.v)' and 'tb_ha (tb_ha.v)'. The 'tb_ha (tb_ha.v)' source is highlighted with a green box. Below this, the 'Source File Properties' window for 'tb_ha.v' is open, showing it is 'Enabled' and located at 'C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.s'. The 'Type' is 'Verilog' and the 'Library' is 'xil_defaultlib'. The 'Size' is '0.5 KB' and it was 'Modified: Today at 15:24:57 PM'. The main editor window shows the Verilog code for 'tb_ha.v', which includes a 'timescale' directive and a 'module tb_ha' definition. The bottom status bar shows '23.1 Insert Verilog'.

project_3 - [C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.xpr] - Vivado 2019.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access

Flow Navigator

PROJECT MANAGER - project_3

Sources

Design Sources (1)

ha (ha.v)

Constraints

Simulation Sources (2)

sim_1 (2)

ha (ha.v)

tb_ha (tb_ha.v)

Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

tb_ha.v

Enabled

Location: C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.s

Type: Verilog

Library: xil_defaultlib

Size: 0.5 KB

Modified: Today at 15:24:57 PM

General Properties

Project Summary

ha.v tb_ha.v

C:/Users/Jaehyun/Engineering_design_project/project_3/srcs/sim_1/newtb_ha.v

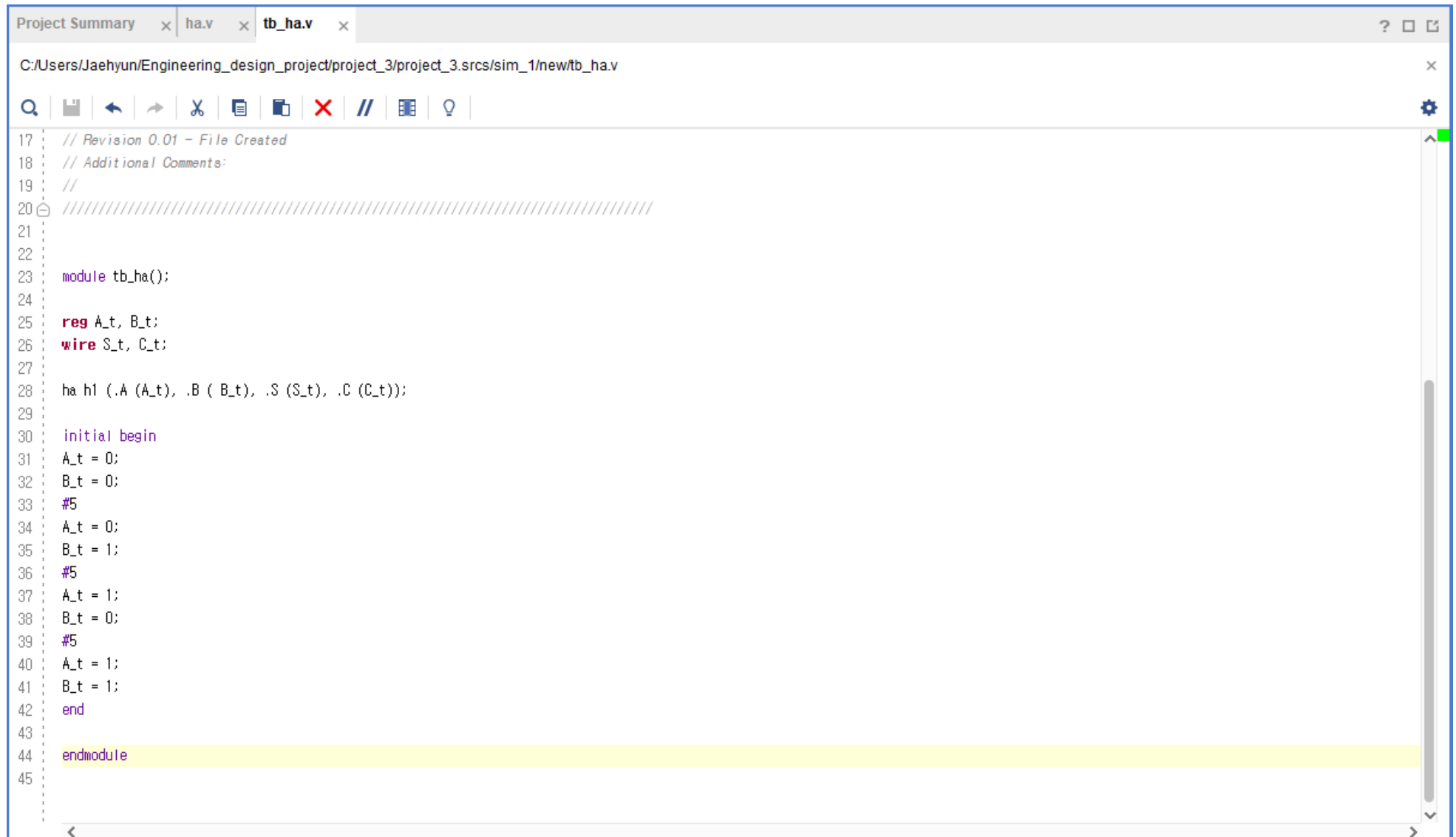
```
1 `timescale 1ns / 1ps
2 // Company:
3 // Engineer:
4 //
5 // Create Date: 2020/08/22 15:24:57
6 // Design Name:
7 // Module Name: tb_ha
8 // Project Name:
9 // Target Device:
10 // Tool Versions:
11 // Description:
12 //
13 // Dependencies:
14 //
15 // Revision:
16 // Revision 0.01 - File Created
17 // Additional Comments:
18 //
19 //
20 //
21
22 module tb_ha(
23
24 );
25
26 endmodule
27
```

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Implementation)

23.1 Insert Verilog

Run a Simulation



The screenshot shows a Verilog code editor with a tab titled 'tb_ha.v'. The file path is 'C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.srscs/sim_1/new/tb_ha.v'. The code is a testbench for a 4-bit adder module 'ha'. It includes comments, a module declaration, register and wire declarations, an instantiation of the 'ha' module, and an initial block with test vectors. The line 'endmodule' is highlighted in yellow.

```
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21
22
23 module tb_ha();
24
25     reg A_t, B_t;
26     wire S_t, C_t;
27
28     ha h1 (.A (A_t), .B (B_t), .S (S_t), .C (C_t));
29
30     initial begin
31         A_t = 0;
32         B_t = 0;
33         #5
34         A_t = 0;
35         B_t = 1;
36         #5
37         A_t = 1;
38         B_t = 0;
39         #5
40         A_t = 1;
41         B_t = 1;
42     end
43
44 endmodule
45
```

Run a Simulation

The screenshot displays the Vivado 2019.2 IDE interface for a project named 'project_3'. The left sidebar shows the 'PROJECT MANAGER' with various tabs like Settings, IP Catalog, and SIMULATION. The 'SIMULATION' tab is active, showing 'Run Simulation'. The main workspace is divided into three panes: 'Sources', 'Source File Properties', and 'Project Summary'.

Sources Pane: Shows the project hierarchy. Under 'Simulation Sources (1)', there is a sub-entry 'sim_1 (1)' which contains 'tb_ha (tb_ha.v) (1)'. This entry is highlighted with a green box. Below it is 'h1: ha (ha.v)'.

Source File Properties Pane: Shows properties for the selected file 'tb_ha.v'. It is 'Enabled', located at 'C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.s', and its type is 'Verilog'. The library is 'xil_defaultlib'. The size is '0.7 KB' and it was modified 'Today at 15:40:34 PM'.

Project Summary Pane: Displays the Verilog code for 'tb_ha.v'. The code includes a module definition for 'tb_ha()' with registers 'A_t', 'B_t', and 'C_t', and a testbench structure with 'initial' and 'endmodule' blocks.

Design Runs Pane: Shows a table of design runs. The table has columns for Name, Constraints, Status, WNS, TNS, WHS, THS, TPWS, Total Power, Failed Routes, LUT, FF, BRAM, URAM, DSP, Start, Elapsed, Run Strategy, and Report Strategy.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Implementation 2019)

Run a Simulation

The screenshot displays the Vivado 2019.2 IDE interface. The 'Run' button in the 'SIMULATION' section of the left-hand Project Manager is highlighted with a green rectangle. A context menu is open, showing 'Run Behavioral Simulation' as the selected option. The 'Messages' tab in the bottom status bar is also highlighted with a green rectangle.

Project Manager - project_3

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation (highlighted)
 - Hierarchy
 - Libraries
 - Compile Order
- RTL ANALYSIS
 - Run Post-Synthesis Functional Simulation
 - Run Post-Synthesis Timing Simulation
- SYNTHESIS
 - Run Post-Implementation Functional Simulation
 - Run Post-Implementation Timing Simulation
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources (1)
 - ha (ha.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - tb_ha (tb_ha.v) (2)
- Utility Sources

Project Summary

tb_ha.v

C:/Users/Jaehyun/Engineering_design_project/project_3/srcs/sim_1/new/tb_ha.v

```
// Revision 0.01 - File Created
// Additional Comments:
//
//
//
module tb_ha();
    reg A_t, B_t;
    wire S_t, C_t;

    HA hl (.A (A_t), .B (B_t), .S (S_t), .C (C_t));

    initial begin
        A_t = 0;
        B_t = 0;
        #5
        A_t = 0;
        B_t = 1;
        #5
        A_t = 1;
        B_t = 0;
        #5
        A_t = 1;
        B_t = 1;
        #5
        end
endmodule
```

General Properties

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2019)	Vivado Synthesis Default Reports (Vivado Synthesis 2019)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2019)	Vivado Implementation Default Reports (Vivado Implementation 2019)

Vivado Simulator

Run a Simulation

project_3 - [C:/Users/laehyun/Engineering_design_project/project_3/project_3.xpr] - Vivado 2019.2

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Flow Navigator

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SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_ha

Scope x Sources

Name	Design U...	Block Type
tb_ha	tb_ha	Verilog Mod
h1	ha	Verilog Mod
gbl	gbl	Verilog Mod

Objects x Protocol Inst

Name	Value	Data Type
A_t	1	Logic
B_t	1	Logic
S_t	0	Logic
C_t	1	Logic

ha.v x tb_ha.v x Untitled 1 x

Name	Value	999,994 ps	999,995 ps	999,996 ps	999,997 ps	999,998 ps	999,999 ps	1,000,000 ps	1,000,001 ps
A_t	1								
B_t	1								
S_t	0								
C_t	1								

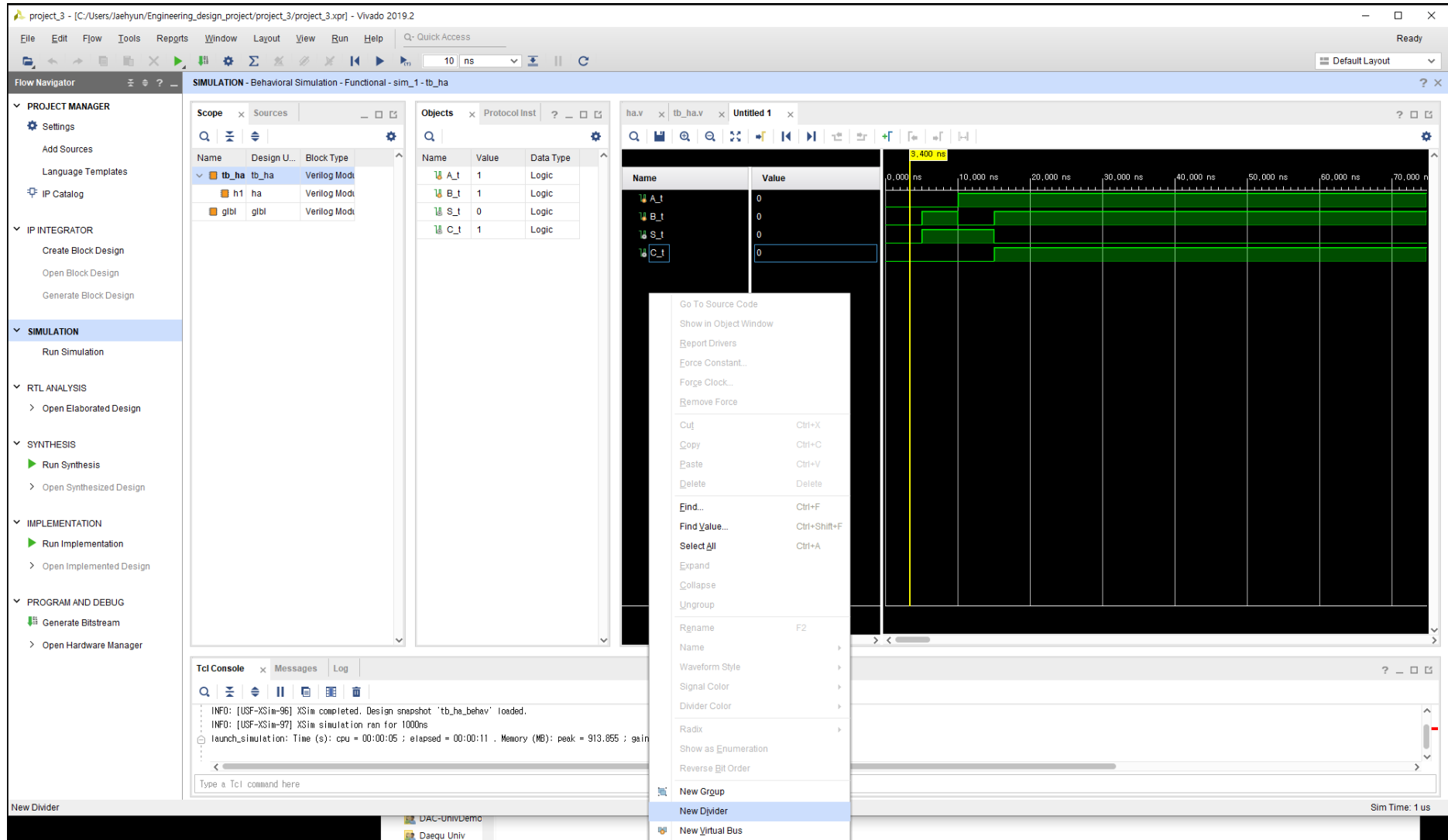
Tcl Console x Messages Log

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_ha_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:11 . Memory (MB): peak = 913.855 ; gain = 0.000
```

Sim Time: 1 us

Run a Simulation

- Right click on a waveform



Run a Simulation

project_3 - [C:/Users/Jaehyun/Engineering_design_project/project_3/project_3.xpr] - Vivado 2019.2

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SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_ha

Scope Sources

Name	Design U...	Block Type
tb_ha	tb_ha	Verilog Modu
h1	ha	Verilog Modu
gbl	gbl	Verilog Modu

Objects Protocol Inst

Name	Value	Data Type
A_t	1	Logic
B_t	1	Logic
S_t	0	Logic
C_t	1	Logic

ha.v x tb_ha.v x Untitled 1*

Name	Value
A_t	0
B_t	1
S_t	1
C_t	0
h1	

0,000 ns 10,000 ns 20,000 ns 30,000 ns 40,000 ns 50,000 ns 60,000 ns 70,000 ns

8,500 ns

Tcl Console Messages Log

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_ha_behav' loaded.  
INFO: [USF-XSim-97] XSim simulation ran for 1000ns  
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:11 , Memory (MB): peak = 913.855 ; gain = 0.000
```

Type a Tcl command here

Sim Time: 1 us

Run a Simulation

- Right click on a module

The screenshot shows the Vivado 2019.2 interface during a behavioral simulation. The 'Scope' window is open, displaying a list of signals (A, B, S, C) and their values. The 'Objects' window shows a table of signal values. The 'Waveform' window displays a timing diagram with a yellow vertical line at 8,500 ns. The 'Tcl Console' at the bottom shows the command 'add_wave {{/tb_ha/h1}}'.

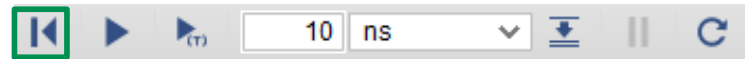
Name	Value	Data Type
A	1	Logic
B	1	Logic
S	0	Logic
C	1	Logic

Waveform signals: A, B, S, C, h1. Time scale: 0.000 ns to 70.000 ns. Yellow vertical line at 8,500 ns.

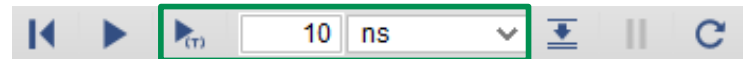
```
Tcl Console
current_wave_config {Untitled 1}
add_wave {{/tb_ha/h1}}
```

Run a Simulation

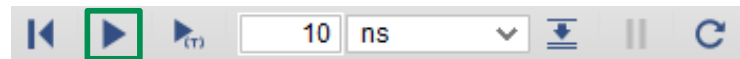
- Restart (Ctrl+Shift+F5)
 - Restart simulation without reflecting source code changes



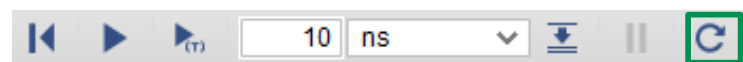
- Run for ...
 - Run a simulation for a specified time



- Run All
 - Run a simulation until no signal changes for a time or it reaches \$finish;



- Relaunch Simulation
 - Recompile source codes to reflect changes



Run a Simulation

- Restart and run a simulation for 30 ns

The screenshot displays the Vivado 2019.2 interface during a behavioral simulation. The top toolbar includes a 'Run' button (a green play icon) which is highlighted with a green box. The 'Scope' window on the left shows a list of signals: tb_ha, h1, gbl, and gbl. The 'Objects' window in the center shows a table of signals: A_t, B_t, S_t, and C_t. The 'Simulation' window on the right shows a waveform plot with a yellow vertical line at 7,500 ns. The 'Tcl Console' at the bottom shows the command 'restart' and the output 'INFO: [Simtcl 6-17] Simulation restarted'.

Name	Value	Data Type
A_t	1	Logic
B_t	1	Logic
S_t	0	Logic
C_t	1	Logic

Tcl Console

```
restart  
INFO: [Simtcl 6-17] Simulation restarted  
run 30 ns
```

Sim Time: 30 ns

Run a Simulation

- Save Waveform configuration

