**硬件管脚连接：**

**GPC0---LEND GPC1---VCLK GPC2—VCLINE**

**GPC4---VM GPC5---USB\_EN GPC6--- LCDVF1**

**GPC7—LCDVF2 GPG4---LCD\_PWR**

**GPC8-15 :VD0-VD7 GPD0-GPD15 :VD8-VD23**

**关闭WATCHDOG**

WTCON = 0; //，寄存器写0

**Clock 时钟寄存器**

\* 设置CLKDIVN，令分频比为：FCLK:HCLK:PCLK=1:2:4，

\* FCLK=200MHz,HCLK=100MHz,PCLK=50MHz

\*/

FCLK is used by ARM920T

HCLK is used for AHB bus, which is used by the ARM920T, the memory Controller, the interrupt controller, the LCD controller, the DMA and USB host block.

PCLK is used for APB bus, which is used by the peripherals such as WDT, IIS, I2C, PWM timer, MMC interface,

ADC, UART, GPIO, RTC and SPI.

CLKDIVN: CLOCK DIVIDER CONTROL (CLKDIVN) REGISTER

|  |  |  |  |
| --- | --- | --- | --- |
| **CLKDIVN** | **Bit** | **Description** | **Initial State** |
| DIVN\_UPLL | [3] | UCLK select register(UCLK must be 48MHz for USB)  0: UCLK = UPLL clock  1: UCLK = UPLL clock / 2  Set to 0, when UPLL clock is set as 48Mhz  Set to 1. when UPLL clock is set as 96Mhz. | 0 |
| HDIVN | [2:1] | 00 : HCLK = FCLK/1.  01 : HCLK = FCLK/2.  10 : HCLK = FCLK/4 when CAMDIVN[9] = 0.  HCLK= FCLK/8 when CAMDIVN[9] = 1.  11 : HCLK = FCLK/3 when CAMDIVN[8] = 0.  HCLK = FCLK/6 when CAMDIVN[8] = 1. | 00 |
| PDIVN | [0] | 0: PCLK has the clock same as the HCLK/1.  1: PCLK has the clock same as the HCLK/2. | 0 |

这里CLKDIVN = 0x03; // FCLK:HCLK:PCLK=1:2:4, HDIVN=1,PDIVN=1

/\* 如果HDIVN非0，CPU的总线模式应该从“fast bus mode”变为“asynchronous bus mode” \*/

#define S3C2410\_MPLL\_200MHZ ((0x5c<<12)|(0x04<<4)|(0x00))

#define S3C2440\_MPLL\_200MHZ ((0x5c<<12)|(0x01<<4)|(0x02))

/\*

\* 对于MPLLCON寄存器，[19:12]为MDIVMain divider control，[9:4]为PDIVPre-divider control，[1:0]为SDIVPost divider control

\* 有如下计算公式：

\* S3C2410: MPLL(FCLK) = (m \* Fin)/(p \* 2^s)

\* S3C2410: MPLL(FCLK) = (2 \* m \* Fin)/(p \* 2^s)

\* 其中: m = MDIV + 8, p = PDIV + 2, s = SDIV

\* 对于本开发板，Fin = 12MHz

**CLOCK CONTROL REGISTER (CLKCON)**

GPIO [13] Control PCLK into GPIO block.

0 = Disable, 1 = Enable

1

**GPIO REGISTER:**

GPCUP = 0xffffffff; // 禁止内部上拉

|  |  |  |
| --- | --- | --- |
| **GPCUP** | **Bit** | **Description** |
| GPC[15:0] | [15:0] | 0: the pull up function attached to to the corresponding port pin is enabled.  1: the pull up function is disabled. |

GPCCON = 0xaaaaaaaa; // GPIO管脚用于VD[7:0],LCDVF[2:0],VM,VFRAME,VLINE,VCLK,LEND

|  |  |  |
| --- | --- | --- |
| **GPCCON** | **Bit** | **Description** |
| GPC15 | [31:30] | 00 = Input 01 = Output  10 = VD[7] 11 = Reserved |
| GPC14 | [29:28] | 00 = Input 01 = Output  10 = VD[6] 11 = Reserved |
| GPC13 | [27:26] | 00 = Input 01 = Output  10 = VD[5] 11 = Reserved |
| GPC12 | [25:24] | 00 = Input 01 = Output  10 = VD[4] 11 = Reserved |
| GPC11 | [23:22] | 00 = Input 01 = Output  10 = VD[3] 11 = Reserved |
| GPC10 | [21:20] | 00 = Input 01 = Output  10 = VD[2] 11 = Reserved |
| GPC9 | [19:18] | 00 = Input 01 = Output  10 = VD[1] 11 = Reserved |
| GPC8 | [17:16] | 00 = Input 01 = Output  10 = VD[0] 11 = Reserved |
| GPC7 | [15:14] | 00 = Input 01 = Output  10 = LCD\_LPCREVB 11 = Reserved |
| GPC6 | [13:12] | 00 = Input 01 = Output  10 = LCD\_LPCREV 11 = Reserved |
| GPC5 | [11:10] | 00 = Input 01 = Output  10 = LCD\_LPCOE 11 = Reserved |
| GPC4 | [9:8] | 00 = Input 01 = Output  10 = VM 11 = I2SSDI |
| GPC3 | [7:6] | 00 = Input 01 = Output  10 = VFRAME 11 = Reserved |
| GPC2 | [5:4] | 00 = Input 01 = Output  10 = VLINE 11 = Reserved |
| GPC1 | [3:2] | 00 = Input 01 = Output  10 = VCLK 11 = Reserved |
| GPC0 | [1:0] | 00 = Input 01 = Output  10 = LEND 11 = Reserved |

GPDUP = 0xffffffff; // 禁止内部上拉

|  |  |  |
| --- | --- | --- |
| **GPDUP** | **Bit** | **Description** |
| GPD[15:0] | [15:0] | 0: the pull up function attached to to the corresponding port pin is enabled.  1: the pull up function is disabled. |

GPDCON = 0xaaaaaaaa; // GPIO管脚用于VD[23:8]

|  |  |  |
| --- | --- | --- |
| **GPDCON** | **Bit** | **Description** |
| GPD15 | [31:30] | 00 = Input 01 = Output  10 = VD[23] 11 = nSS0 |
| GPD14 | [29:28] | 00 = Input 01 = Output  10 = VD[22] 11 = nSS1 |
| GPD13 | [27:26] | 00 = Input 01 = Output  10 = VD[21] 11 = Reserved |
| GPD12 | [25:24] | 00 = Input 01 = Output  10 = VD[20] 11 = Reserved |
| GPD11 | [23:22] | 00 = Input 01 = Output  10 = VD[19] 11 = Reserved |
| GPD10 | [21:20] | 00 = Input 01 = Output  10 = VD[18] 11 = SPICLK1 |
| GPD9 | [19:18] | 00 = Input 01 = Output  10 = VD[17] 11 = SPIMOSI1 |
| GPD8 | [17:16] | 00 = Input 01 = Output  10 = VD[16] 11 = SPIMISO1 |
| GPD7 | [15:14] | 00 = Input 01 = Output  10 = VD[15] 11 = Reserved |
| GPD6 | [13:12] | 00 = Input 01 = Output  10 = VD[14] 11 = Reserved |
| GPD5 | [11:10] | 00 = Input 01 = Output  10 = VD[13] 11 = Reserved |
| GPD4 | [9:8] | 00 = Input 01 = Output  10 = VD[12] 11 = Reserved |
| GPD3 | [7:6] | 00 = Input 01 = Output  10 = VD[11] 11 = Reserved |
| GPD2 | [5:4] | 00 = Input 01 = Output  10 = VD[10] 11 = Reserved |
| GPD1 | [3:2] | 00 = Input 01 = Output  10 = VD[9] 11 = Reserved |
| GPD0 | [1:0] | 00 = Input 01 = Output  10 = VD[8] 11 = Reserved |

GPGCON = (GPGCON & (~(3<<8))) | (3<<8); // GPG4用作LCD\_PWREN

GPGUP = (GPGUP & (~(1<<4))) | (1<<4); // 禁止内部上拉

GPGCON |= (3<<8); // GPG4 AS LCD\_PWREN

|  |  |  |
| --- | --- | --- |
| GPG4 | [9:8] | 00 = Input 01 = Output  10 = EINT[12] 11 = LCD\_PWRDN |
|  |  |  |

Power enable (PWREN) function is available only when LCD panel has its own power on/off control port and when port is connected to LCD\_PWREN pin.

初始化LCD控制器

\* 设置LCD控制器的控制寄存器LCDCON1~5

\* 1. LCDCON1:

\* 设置VCLK的频率：VCLK(Hz) = HCLK/[(CLKVAL+1)x2]

\* 选择LCD类型: TFT LCD

\* 设置显示模式: 8BPP

\* 先禁止LCD信号输出

|  |  |  |  |
| --- | --- | --- | --- |
| LCDCON1 | Bit | Description | Initial State |
| LINECNT (read only) | [27:18] | Provide the status of the line counter. Down count from LINEVAL to 0 | 0000000000 |
| CLKVAL | [17:8] | Determine the rates of VCLK and CLKVAL[9:0].  STN: VCLK = HCLK / (CLKVAL x 2) ( CLKVAL ≥2)  TFT: VCLK = HCLK / [(CLKVAL+1) x 2] ( CLKVAL ≥ 0 ) | 0000000000 |
| MMODE | [7] | Determine the toggle rate of the VM.  0 = Each Frame 1 = The rate defined by the MVAL | 0 |
| PNRMODE | [6:5] | Select the display mode.  00 = 4-bit dual scan display mode (STN)  01 = 4-bit single scan display mode (STN)  10 = 8-bit single scan display mode (STN)  11 = TFT LCD panel | 00 |
| BPPMODE | [4:1] | Select the BPP (Bits Per Pixel) mode.  0000 = 1 bpp for STN, Monochrome mode  0001 = 2 bpp for STN, 4-level gray mode  0010 = 4 bpp for STN, 16-level gray mode  0011 = 8 bpp for STN, color mode (256 color)  0100 = packed 12 bpp for STN, color mode (4096 color)  0101 = unpacked 12 bpp for STN, color mode (4096 color)  0110 = 16 bpp for STN, color mode (4096 color)  1000 = 1 bpp for TFT  1001 = 2 bpp for TFT  1010 = 4 bpp for TFT  1011 = 8 bpp for TFT  1100 = 16 bpp for TFT  1101 = 24 bpp for TFT | 0000 |
| ENVID | [0] | LCD video output and the logic enable/disable.  0 = Disable the video output and the LCD control signal.  1 = Enable the video output and the LCD control signal. | 0 |

LCDCON1 = (7<<8) | (3<<5) | (13<<1);

\* 2. LCDCON2/3/4:

\* 设置控制信号的时间参数

\* 设置分辨率，即行数及列数

\* 现在，可以根据公式计算出显示器的频率：

\* 当HCLK=100MHz时，

\* Frame Rate = 1/[{(VSPW+1)+(VBPD+1)+(LIINEVAL+1)+(VFPD+1)}x

\* {(HSPW+1)+(HBPD+1)+(HFPD+1)+(HOZVAL+1)}x

\* {2x(CLKVAL+1)/(HCLK)}]

\* = 60Hz

/\* 垂直方向的时间参数

\* 根据数据手册

\* bit[31:24]: VBPD, VSYNC之后再过多长时间才能发出第1行数据

\* LCD手册 2

\* VBPD=17

\* bit[23:14]: 多少行, 320, 所以LINEVAL=320-1=319

\* bit[13:6] : VFPD, 发出最后一行数据之后，再过多长时间才发出VSYNC

\* LCD手册2

\* bit[5:0] : VSPW, VSYNC信号的脉冲宽度, LCD手册tvp=1, 所以VSPW=1-1=0

\*/

|  |  |  |  |
| --- | --- | --- | --- |
| LCDCON2 | Bit | Description | Initial State |
| VBPD | [31:24] | TFT: Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period.  STN: These bits should be set to zero on STN LCD. | 0x00 |
| LINEVAL | [23:14] | TFT/STN: These bits determine the vertical size of LCD panel. | 0000000000 |
| VFPD | [13:6] | TFT: Vertical front porch is the number of inactive lines at the end of a frame, before vertical synchronization period.  STN: These bits should be set to zero on STN LCD. | 00000000 |
| VSPW | [5:0] | TFT: Vertical sync pulse width determines the VSYNC pulse's high level width by counting the number of inactive lines.  STN: These bits should be set to zero on STN LCD. | 000000 |

LCDCON2 = (2<<24) | (319<<14) | (2<<6) | (0<<0);

LCDCON3:

/\* 水平方向的时间参数

\* bit[25:19]: HBPD, VSYNC之后再过多长时间才能发出第1行数据

\* LCD手册 20

\* bit[18:8]: 多少列, 240, 所以HOZVAL=240-1=239

\* bit[7:0] : HFPD, 发出最后一行里最后一个象素数据之后，再过多长时间才发出HSYNC

\* LCD手册10

\*/

|  |  |  |  |
| --- | --- | --- | --- |
| LCDCON3 | Bit | Description | Initial state |
| HBPD (TFT) | [25:19] | TFT: Horizontal back porch is the number of VCLK periods between the falling edge of HSYNC and the start of active data. | 0000000 |
| WDLY (STN) | STN: WDLY[1:0] bits determine the delay between VLINE and VCLK  by counting the number of the HCLK. WDLY[7:2] are reserved.  00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK |
| HOZVAL | [18:8] | TFT/STN: These bits determine the horizontal size of LCD panel.  HOZVAL has to be determined to meet the condition that total bytes of 1 line are 4n bytes. If the x size of LCD is 120 dot in mono mode, x=120 cannot be supported because 1 line consists of 15 bytes. Instead, x=128 in mono mode can be supported because 1 line is composed of 16 bytes (2n). LCD panel driver will discard the additional 8 dot. | 00000000000 |
| HFPD (TFT) | [7:0] | TFT: Horizontal front porch is the number of VCLK periods between the end of active data and the rising edge of HSYNC. | 0X00 |
| LINEBLANK (STN) | STN: These bits indicate the blank time in one horizontal line duration time. These bits adjust the rate of the VLINE finely.  The unit of LINEBLANK is HCLK x 8.  Ex) If the value of LINEBLANK is 10, the blank time is inserted to  VCLK during 80 HCLK. |

LCDCON3 = (20<<19) | (239<<8) | (10<<0);

|  |  |  |  |
| --- | --- | --- | --- |
| LCDCON4 | Bit | Description | Initial state |
| MVAL | [15:8] | STN: These bit define the rate at which the VM signal will toggle if the MMODE bit is set to logic '1'. | 0X00 |
| HSPW(TFT) | [7:0] | TFT: Horizontal sync pulse width determines the HSYNC pulse's high level width by counting the number of the VCLK. | 0X00 |
| WLH(STN) | STN: WLH[1:0] bits determine the VLINE pulse's high level width by counting the number of the HCLK.  WLH[7:2] are reserved.  00 = 16 HCLK, 01 = 32 HCLK, 10 = 48 HCLK, 11 = 64 HCLK |

LCDCON4:

/\* 水平方向的同步信号

\* bit[7:0] : HSPW, HSYNC信号的脉冲宽度, LCD手册HSPW=10

\*/

LCDCON4 = 10; //HSPW\_240320;

\* LCDCON5:

/\* 信号的极性

\* bit[11]: 1=565 format, 对于24bpp这个不用设

\* bit[10]: 0 = The video data is fetched at VCLK falling edge

\* bit[9] : 1 = HSYNC信号要反转,即低电平有效

\* bit[8] : 1 = VSYNC信号要反转,即低电平有效

\* bit[6] : 0 = VDEN不用反转

\* bit[3] : 0 = PWREN输出0

\*

\* BSWP = 0, HWSWP = 0, BPP24BL = 0 : 当bpp=24时,2440会给每一个象素分配32位即4字节,哪一个字节是不使用的? 看2440手册P412

\* bit[12]: 0, LSB valid, 即最高字节不使用

\* bit[1] : 0 = BSWP

\* bit[0] : 0 = HWSWP

\*/

|  |  |  |  |
| --- | --- | --- | --- |
| LCDCON5 | Bit | Description | Initial state |
| Reserved | [31:17] | This bit is reserved and the value should be ‘0’. | 0 |
| VSTATUS | [16:15] | TFT: Vertical Status (read only).  00 = VSYNC 01 = BACK Porch  10 = ACTIVE 11 = FRONT Porch | 00 |
| HSTATUS | [14:13] | TFT: Horizontal Status (read only).  00 = HSYNC 01 = BACK Porch  10 = ACTIVE 11 = FRONT Porch | 00 |
| BPP24BL | [12] | TFT: This bit determines the order of 24 bpp video memory.  0 = LSB valid 1 = MSB Valid | 0 |
| FRM565 | [11] | TFT: This bit selects the format of 16 bpp output video data.  0 = 5:5:5:1 Format 1 = 5:6:5 Format | 0 |
| INVVCLK | [10] | STN/TFT: This bit controls the polarity of the VCLK active edge.  0 = The video data is fetched at VCLK falling edge  1 = The video data is fetched at VCLK rising edge | 0 |
| INVVLINE | [9] | STN/TFT: This bit indicates the VLINE/HSYNC pulse polarity.  0 = Normal 1 = Inverted | 0 |
| INVVFRAME | [8] | STN/TFT: This bit indicates the VFRAME/VSYNC pulse polarity.  0 = Normal 1 = Inverted | 0 |
| INVVD | [7] | STN/TFT: This bit indicates the VD (video data) pulse polarity.  0 = Normal 1 = VD is inverted. | 0 |

|  |  |  |  |
| --- | --- | --- | --- |
| LCDCON5 | Bit | Description | Initial state |
| INVVDEN | [6] | TFT: This bit indicates the VDEN signal polarity.  0 = normal 1 = inverted | 0 |
| INVPWREN | [5] | STN/TFT: This bit indicates the PWREN signal polarity.  0 = normal 1 = inverted | 0 |
| INVLEND | [4] | TFT: This bit indicates the LEND signal polarity.  0 = normal 1 = inverted | 0 |
| PWREN | [3] | STN/TFT: LCD\_PWREN output signal enable/disable.  0 = Disable PWREN signal 1 = Enable PWREN signal | 0 |
| ENLEND | [2] | TFT: LEND output signal enable/disable.  0 = Disable LEND signal 1 = Enable LEND signal | 0 |
| BSWP | [1] | STN/TFT: Byte swap control bit.  0 = Swap Disable 1 = Swap Enable | 0 |
| HWSWP | [0] | STN/TFT: Half-Word swap control bit.  0 = Swap Disable 1 = Swap Enable | 0 |

LCDCON5 = (0<<10) | (1<<9) | (1<<8) | (0<<12) | (0<<1) | (0<<0);

\* 设置LCD控制器的地址寄存器LCDSADDR1~3

\* 帧内存与视口(view point)完全吻合，

\* 图像数据格式如下(8BPP时，帧缓冲区中的数据为调色板中的索引值)：

\* |----PAGEWIDTH----|

\* y/x 0 1 2 239

\* 0 idx idx idx ... idx

\* 1 idx idx idx ... idx

\* 1. LCDSADDR1: **STN/TFT**: Frame buffer start address 1 register

\* 设置LCDBANK、LCDBASEU

|  |  |  |  |
| --- | --- | --- | --- |
| LCDSADDR1 | Bit | Description | Initial State |
| LCDBANK | [29:21] | These bits indicate A[30:22] of the bank location for the video buffer in the system memory. LCDBANK value cannot be changed even when moving the view port. LCD frame buffer should be within aligned 4MB region, which ensures that LCDBANK value will not be changed when moving the view port. So, care should be taken to use the malloc() function. | 0x00 |
| LCDBASEU | [20:0] | For dual-scan LCD : These bits indicate A[21:1] of the start address of the upper address counter, which is for the upper frame memory of dual scan LCD or the frame memory of single scan LCD.  For single-scan LCD : These bits indicate A[21:1] of the start address of the LCD frame buffer. | 0x000000 |

LCDSADDR1 = (BUFFER\_START<<1) &~(3<<30);

\* 2. LCDSADDR2:

\* 设置LCDBASEL: 帧缓冲区的结束地址A[21:1]

LCDSADDR2 =((BUFFER\_START+BUFFER\_LEN)>>1)+1;

|  |  |  |  |
| --- | --- | --- | --- |
| LCDSADDR2 | Bit | Description | Initial State |
| LCDBASEL | [20:0] | For dual-scan LCD: These bits indicate A[21:1] of the start address of the lower address counter, which is used for the lower frame memory of dual scan LCD.  For single scan LCD: These bits indicate A[21:1] of the end address of the LCD frame buffer.  LCDBASEL = ((the frame end address) >>1) + 1  = LCDBASEU +  (PAGEWIDTH+OFFSIZE) x (LINEVAL+1) | 0x0000 |

\* 3. LCDSADDR3:

|  |  |  |  |
| --- | --- | --- | --- |
| LCDSADDR3 | Bit | Description | Initial State |
| OFFSIZE | [21:11] | Virtual screen offset size (the number of half words).  This value defines the difference between the address of the last half word displayed on the previous LCD line and the address of the first half word to be displayed in the new LCD line. | 00000000000 |
| PAGEWIDTH | [10:0] | Virtual screen page width (the number of half words).  This value defines the width of the view port in the frame. | 000000000 |

\* OFFSIZE等于0，PAGEWIDTH等于(240/2)

LCDSADDR3 = (240\*32/16);

/\* 禁止临时调色板寄存器 \*/

TPAL = 0;

/\* 启动LCD \*/

lcd\_regs->lcdcon1 |= (1<<0); /\* 使能LCD控制器 \*/

lcd\_regs->lcdcon5 |= (1<<3); /\* 使能LCD本身: LCD\_PWREN \*/

/\*gpbdat |= 1; /\* MINI2440的背光电路也是通过LCD\_PWREN来控制的, 不需要单独的背光引脚 \*/

xsize = 240;

ysize = 320;