

BIRKBECK, UNIVERSITY OF LONDON

Computer Systems Coursework 1

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Answers

1. (a)
 - 1 LOAD r3, M
 - 2 LOAD r0, #1 // $f(n-2)$
 - 3 LOAD r1, #1 // $f(n-1)$
 - 4 LOAD r2, #1 // $f(n)$
 - 5 SUB r3, r3, #1
 - 6 ADD r4, r1, r0
 - 7 MUL r4, r4, r2
 - 8 LOAD r0, r1
 - 9 LOAD r1, r2
 - 10 LOAD r2, r4
 - 11 BNE 5, r3, #3 // jump to instruction 5 if r3 not equal to 3
 - 12 STOR M, r2

where # indicates immediate addressing and BNE stands for "branch if not equal"

- (b) other point

(c) Below is the pipeline for execution of program where $k = 5$

	F	D	IW	R	E	W	Comments
1	I1						
2	I2	I1					
3	I3	I2			I1		I1 skips R
4	I4	I3	I2			I1	
5	I5	I4	I3			I2	I3 skip R,E
6	I6	I5	I4			I3	I4 skips R,E
7	I7	I6		I5		I4	
8	I8	I7		I6	I5		
9	I9	I8	I7		I6	I5	r3 = 4
10	I10	I9	I7, I8			I6	r4 not ready
11	I11	I10	I8, I9	I7			Read busy
12	I12	I11	I9, I10	I8	I7		Read busy for I9
13		I12	I11, I10	I9		I7	I8, I9, I10 skips E and W busy
14			I11, I12	I10		I8	R busy
15			I12	I11		I9	
16			I12	X	I11	I10	Condition holds
17			I12	X		I11	PC updated, I12 discarded
18	I5			X			
19	I6	I5		X			
20	I7	I6		I5			
21	I8	I7		I6	I5		
22	I9	I8	I7		I6	I5	r3 = 3
23	I10	I9	I7, I8			I6	r4 not ready
24	I11	I10	I8, I9	I7			Read busy
25	I12	I11	I9, I10	I8	I7		Read busy for I9
26		I12	I10, I11	I9		I7	I8, I9, I10 skips E and w busy
27			I11, I12	I10		I8	R busy
28			I12	I11		I9	
29			I12	X	I11	I10	Condition fails
30				I12			No need to update PC
31					I12		

Table 1: Table for pipeline execution for $k = 5$.

2. $15 \text{ ns} = 15 \times 10^{-9} \text{ seconds}$
 $85 \text{ ns} = 85 \times 10^{-9} \text{ seconds}$
 $10 \text{ ms} = 1 \times 10^{-2} \text{ seconds}$

Probability of being in main memory is 0.7 and cache hit ratio is 0.4.

Therefore time to load is:

$$0.7 \times 1 \times 10^{-2} + 0.3 \times (0.4 \times 15 \times 10^{-9} + 0.6 \times 85 \times 10^{-9})$$