Birkbeck, University of London

Computer Systems Coursework Part 1

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Answers

1. (a)

```
1 LOAD r3, M
2 LOAD r0, #1        // f(n − 2)
3 LOAD r1, #1        // f(n − 1)
4 LOAD r2, #1        // f(n)
5 SUB r3, r3, #1
6 ADD r4, r1, r0
7 MUL r4, r4, r2
8 LOAD r0, r1
9 LOAD r1, r2
10 LOAD r2, r4
11 BNE 5, r3, #3     // jump to instruction 5 if r3 not equal to 3
12 STOR M, r2
```

where # indicates immediate addressing and BNE stands for ”branch if not equal”

(b) F (fetch) stage is first stage for all the instructions, where they loaded onto CPU. D (decode) is the stage where fetched instructions decoded. We assume data transfer between main memory and CPU happens E (execution) stage and using immediate addressing skips R (read) and E stages. For immediate addressing data is written back to register in W (write) stage. All arithmetic instructions will go through R, E stages and written back to register in W stage. If any instruction that can not move forward to further stages after the D stage for any reason, will be hold in IW (instruction window) until the restriction of the instruction is lifted. For example E stage is busy while next stage is execution or register instruction depends on is not ready for read.

(c) Below is the pipeline for execution of program where k = 5

	F	D	IW	R	E	W	Comments
1	I1						
2	I2	I1					
3	I3	I2			I1		I1 skips R
4	I4	I3	I2			I1	
5	I5	I4	I3			I2	I2, I3 skip R,E
6	I6	I5	I4			I3	I4 skips R,E
7	I7	I6		I5		I4	
8	I8	I7		I6	I5		
9	I9	I8	I7		I6	I5	r3 = 4
10	I10	I9	I7, I8			I6	r4 not ready
11	I11	I10	I8, I9	I7			Read busy
12	I12	I11	I9, I10	I8	I7		Read busy for I9
13		I12	I11, I10	I9		I7	I8, I9, I10 skips E and W busy
14			I11, I12	I10		I8	R busy
15			I12	I11		I9	
16			I12	**X**	I11	I10	Condition holds
17			I12	**X**		I11	PC updated, I12 discarded
18	I5			**X**			
19	I6	I5		**X**			
20	I7	I6		I5			
21	I8	I7		I6	I5		
22	I9	I8	I7		I6	I5	r3 = 3
23	I10	I9	I7, I8			I6	r4 not ready
24	I11	I10	I8, I9	I7			Read busy
25	I12	I11	I9, I10	I8	I7		Read busy for I9
26		I12	I10, I11	I9		I7	I8, I9, I10 skips E and w busy
27			I11, I12	I10		I8	R busy
28			I12	I11		I9	
29			I12	**X**	I11	I10	Condition fails
30				I12			No need to update PC
31					I12		

Table 1: Table for pipeline execution for k = 5.

2. 15 ns = $15{\times}10^{-9}$ seconds
   85 ns = $85{\times}10^{-9}$ seconds
   10 ms = 1 $\times10^{-2}$ seconds

   Probability of being in main memory is 0.7 and cache hit ratio is 0.4. Therefore average time to load is:
   $0.7 \times (1 \times 10^{-2} + 85 \times 10^{-9} + 15 \times 10^{-9}) + 0.3 \times (0.4 \times 15 \times 10^{-9} + 0.6 \times (85 \times 10^{-9} + 15 \times 10^{-9}))$
   $0,70000198 \times 10^{-2} seconds$
   $\approx 0,7ms$