Trabalho 2 - FIFO ASYNC

Disciplina: Projeto de Sistemas Integrados II

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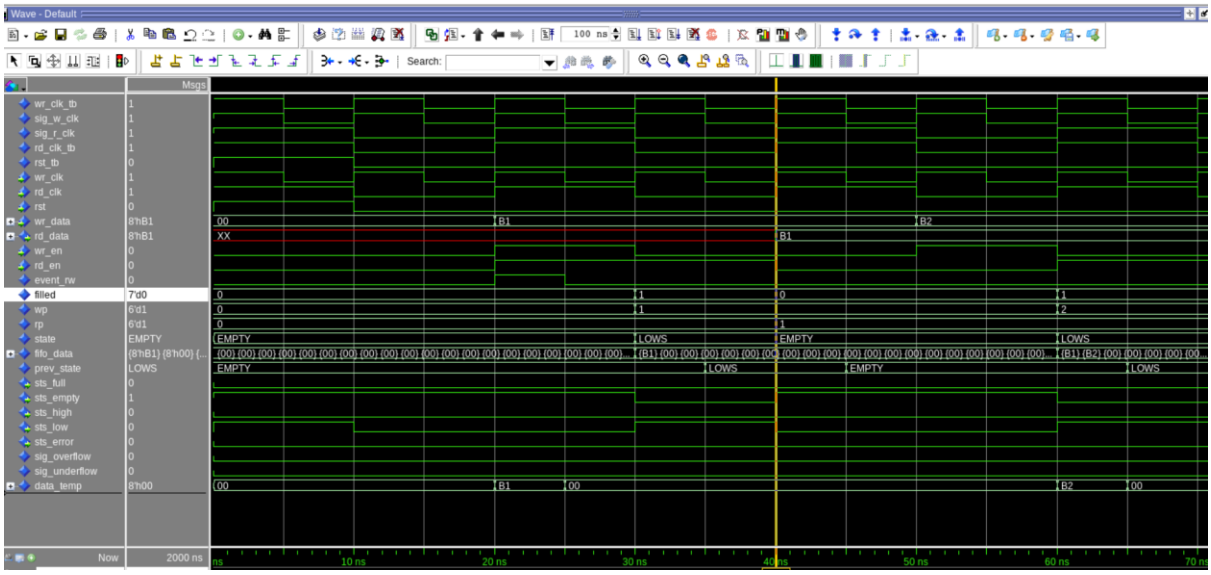

Síntese – Cadence Genus:

- Acessando via SSH à paxos, você deverá carregar o módulo do Genus no Terminal aberto.

```
source /soft64/source_gaph
module load genus
genus
```

- Definição da biblioteca que será utilizada neste projeto.

```
set_db library /soft64/design-kits/stm/65nm-cmos065_536/CORE65GPSVT_5.1/libs/CORE65GPSVT_nom_1.00V_25C.lib
```

- Leitura do(s) arquivo(s) VHDL que compõe o projeto. Neste exemplo o código fonte foi nomeado como “fifo_sync.vhd”

```
read_hdl -vhdl fifo_sync.vhd
```

- Elaboração do projeto. Neste exemplo a entidade do projeto foi nomeada como “fifo_sync”.

```
elaborate fifo_sync
```

```
fifo_async.vhd  fifo_async_tb.vhd
@genus:root: 5> read_hdl -vhdl fifo_async.vhd
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'fifo_async.vhd' on line 37.
        : The specified construct has no effect on synthesis. In some cases (such as 'after' clauses in signal assignments) may cause a mismatch between and s
imulation.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'fifo_async.vhd' on line 38.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'fifo_async.vhd' on line 39.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'fifo_async.vhd' on line 39.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'fifo_async.vhd' on line 40.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'fifo_async.vhd' on line 40.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'fifo_async.vhd' on line 43.
Warning : Concurrent assertion statements are ignored for synthesis. [VHDL-645]
        : in file 'fifo_async.vhd' on line 50.
        : The specified construct has no effect on synthesis. In some cases (such as 'after' clauses in signal assignments) may cause a mismatch between and s
imulation.
Warning : Report statements are ignored for synthesis. [VHDL-643]
        : in file 'fifo_async.vhd' on line 83.
        : The specified construct has no effect on synthesis. Some constructs (such as 'after' clauses in signal assignments) may cause a mismatch between sim
ulation and synthesis.
Warning : Report statements are ignored for synthesis. [VHDL-643]
        : in file 'fifo_async.vhd' on line 108.
@genus:root: 6> elaborate fifo_async
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'fifo_async' from file 'fifo_async.vhd'.
```

```
        : in file 'fifo_async.vhd' on line 108.
@genus:root: 6> elaborate fifo_async
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'fifo_async' from file 'fifo_async.vhd'.
Info    : Binding to architecture. [ELAB-5]
        : Elaborating architecture 'rtl' for entity 'fifo_async'.
Warning : Using default parameter value for module elaboration. [CDFG-818]
        : Elaborating block 'fifo_async' with default parameters value.
Info    : Done Elaborating Design. [ELAB-3]
        : Done elaborating 'fifo_async'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
------------------------------------------------------
| Trick             | Accepts | Rejects | Runtime (ms) |
------------------------------------------------------
| ume_constant_bmux |       0 |       0 |         0.00 |
------------------------------------------------------
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: fifo_async, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: fifo_async, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)
Info    : To insure proper verification, preserved netlist point(s) because they are involved in combinational loop(s). To disable this, set the 'cb_preserve_
ports_nets' root attribute to 'false'. [ELABUTL-133]
        : Preserved 4 user net(s)  Set the 'print_ports_nets_preserved_for_cb' root attribute to 'true' to print out the affected nets and hierarchical instan
ces.

UM:   flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:*                                                                 elaborate
design:fifo_async
@genus:root: 7>
```

- Síntese Lógica para Células Genéricas:

```
syn_generic
```

-

- Síntese Lógica para células da biblioteca alvo do projeto:

```
syn_map
```

Ambos juntos ao acoplados ao zip.