Work 3.1 – UART Receiver Module

Course: Integrated Systems Design II

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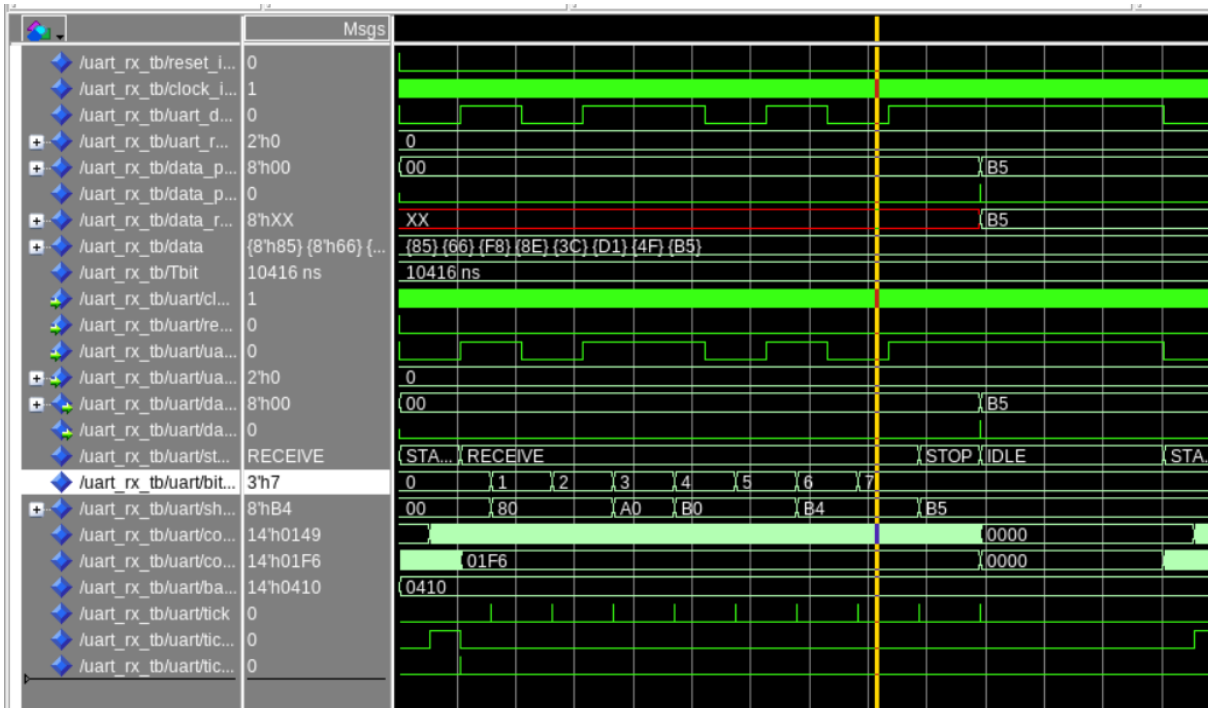

```
# -- Loading package std_logic_1164
# -- Loading package NUMERIC_STD
# -- Compiling entity uart_rx
# -- Compiling architecture rtl of uart_rx
# End time: 22:59:06 on May 26,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
# Model Technology ModelSim SE-64 vcom 2021.3 Compiler 2021.07 Jul 13 2021
# Start time: 22:59:07 on May 26,2025
# vcom -reportprogress 300 uart_rx_tb.vhd
# -- Loading package STANDARD
# -- Loading package TEXTIO
# -- Loading package std_logic_1164
# -- Loading package NUMERIC_STD
# -- Compiling entity uart_rx_tb
# -- Compiling architecture tb of uart_rx_tb
# -- Loading entity uart_rx
# End time: 22:59:07 on May 26,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# End time: 22:59:55 on May 26,2025, Elapsed time: 0:07:12
# Errors: 8, Warnings: 0
# vsim -wlf /sim/uart_rx_tb -voptargs=""+acc"" -wlfdeleteonquit uart_rx_tb
# Start time: 22:59:55 on May 26,2025
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.uart_rx_tb(tb)#1
# Loading work.uart_rx(rtl)#1
# ** Note: Byte recebido: 181
#    Time: 109541 ns  Iteration: 0  Instance: /uart_rx_tb
# ** Note: Byte recebido: 79
#    Time: 239711 ns  Iteration: 0  Instance: /uart_rx_tb
# ** Note: Byte recebido: 209
#    Time: 369881 ns  Iteration: 0  Instance: /uart_rx_tb
# ** Note: Byte recebido: 60
#    Time: 500051 ns  Iteration: 0  Instance: /uart_rx_tb
# ** Note: Byte recebido: 142
#    Time: 630221 ns  Iteration: 0  Instance: /uart_rx_tb
# ** Note: Byte recebido: 248
#    Time: 760391 ns  Iteration: 0  Instance: /uart_rx_tb
# ** Note: Byte recebido: 102
#    Time: 890561 ns  Iteration: 0  Instance: /uart_rx_tb
# ** Note: Byte recebido: 133
#    Time: 1020731 ns  Iteration: 0  Instance: /uart_rx_tb
```

Síntese – Cadence Genus:

- Acessando via SSH à paxos, você deverá carregar o módulo do Genus no Terminal aberto.

```
source /soft64/source_gaph
module load genus
genus
```

- Definição da biblioteca que será utilizada neste projeto.

```
set_db library /soft64/design-kits/stm/65nm-cmos065_536/CORE65GPSVT_5.1/libs/CORE65GPSVT_nom_1.00V_25C.lib
```

- Leitura do(s) arquivo(s) VHDL que compõe o projeto. Neste exemplo o código fonte foi nomeado como “fifo_sync.vhd”

```
read_hdl -vhdl fifo_sync.vhd
```

- Elaboração do projeto. Neste exemplo a entidade do projeto foi nomeada como “fifo_sync”.

```
elaborate fifo_sync
```

```
@genus:root: 4> read_hdl -vhdl uart_rx
uart_rx.vhd  uart_rx_tb.vhd
@genus:root: 4> read_hdl -vhdl uart_rx.vhd
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 21.
        : The specified construct has no effect on synthesis. In some cases (such as 'after' clauses in signal assignments) may cause a mismatch between and simulation.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 22.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 23.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 24.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 25.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 26.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 27.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 28.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_rx.vhd' on line 29.
```

```
@genus:root: 6> elaborate uart_rx
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'uart_rx' from file 'uart_rx.vhd'.
Info    : Binding to architecture. [ELAB-5]
        : Elaborating architecture 'rtl' for entity 'uart_rx'.
Info    : Done Elaborating Design. [ELAB-3]
        : Done elaborating 'uart_rx'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
-----------------------------------------------------------
| Trick             | Accepts | Rejects | Runtime (ms) |
-----------------------------------------------------------
| ume_constant_bmux |       0 |       0 |         0.00 |
-----------------------------------------------------------
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: uart_rx, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: uart_rx, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)
      flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:*                                                                  elaborate
design:uart_rx
@genus:root: 7>
```

\read.sdc constraints.sdc:

```
@genus:root: 9> read_sdc ./constraints.sdc
Warning : Replacing existing clock definition. [TIM-101]
        : The clock name is 'clock_in'
        : A new clock has been defined with the same name as an existing clock.
Info    : Replacing an existing timing exception with another. [TIM-304]
        : Existing timing exception is 'path_groups/clock_in'.
        : Existing exception had a name conflict with the newly created exception. The exception created at a later time is maintained.
Statistics for commands executed by read_sdc:
"all_outputs"              - successful      2 , failed      0 (runtime  0.00)
"create_clock"             - successful      1 , failed      0 (runtime  0.00)
"get_ports"                - successful     17 , failed      0 (runtime  0.00)
"set_input_transition"     - successful     16 , failed      0 (runtime  0.00)
"set_load"                 - successful      2 , failed      0 (runtime  0.00)
"set_load_unit"            - successful      1 , failed      0 (runtime  0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
@genus:root: 10>
```

5. Ainda no terminal do Genus aplique as *constraints* ao projeto, e realize a síntese lógica do projeto observando os impactos de cada etapa no diagrama esquemático apresentado na interface gráfica da ferramenta:

```
read_sdc ./constraints.sdc
synthesize -to_generic -effort low
synthesize -to_mapped -effort low
```

```
synthesize -to_generic -effort high
synthesize -to_mapped -effort high
```

```
read_sdc completed in 00:00:00 (hh:mm:ss)
@genus:root: 10> synthesize -to_generic -effort low
Error   : The selected flow setting has been removed. [SYNTH-29] [synthesize]
        : The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
        : Contact Cadence support to understand current flows.
The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
@genus:root: 11> synthesize -to_mapped -effort low
Error   : The selected flow setting has been removed. [SYNTH-29] [synthesize]
        : The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
@genus:root: 12> synthesize -to_generic -effort high
Error   : The selected flow setting has been removed. [SYNTH-29] [synthesize]
        : The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
@genus:root: 13> synthesize -to_mapped -effort high
Error   : The selected flow setting has been removed. [SYNTH-29] [synthesize]
        : The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
The 'synthesize' command has been removed. Use 'syn_gen', 'syn_map' and 'syn_opt'.
@genus:root: 14>
```

The following four commands failed to execute due to deprecation. They should be replaced with the updated equivalents shown below:

- Síntese Lógica para Células Genéricas:

  syn_generic

- Síntese Lógica para células da biblioteca alvo do projeto:

  syn_map

Shell reports and sector documents can be found in the specified directory.

Report_power:

```
@genus:root: 16> report_power
Info     : Joules engine is used. [RPT-16]
         : Joules engine is being used for the command report_power.
Info     : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
         : uart_rx
Info     : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info     : ACTP-0001 Activity propagation ended for stim#0
Info     : PWRA-0001 [PwrInfo] compute_power effective options
         : -mode : vectorless
         : -skip_propagation : 1
         : -frequency_scaling_factor : 1.0
         : -use_clock_freq : stim
         : -stim :/stim#0
         : -fromGenus : 1
Info     : ACTP-0001 Timing initialization started
Info     : ACTP-0001 Timing initialization ended
Info     : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
         : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
         : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
         : of power analysis, ignored this option.
Info     : PWRA-0002 Started 'vectorless' power computation.
Info     : PWRA-0009 [PwrInfo] Power Computation Progress Report : 100%
Info     : PWRA-0002 Finished power computation.
Info     : PWRA-0007 [PwrInfo] Completed successfully.
         : Info=6, Warn=2, Error=0, Fatal=0
Instance: /uart_rx
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total     Row%
  ------------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
    register     5.72437e-06  4.69050e-05  4.57751e-06  5.72069e-05   52.09%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
       logic     7.92827e-06  9.90905e-06  2.88357e-05  4.66730e-05   42.50%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
       clock     0.00000e+00  0.00000e+00  5.94000e-06  5.94000e-06    5.41%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
  ------------------------------------------------------------------------------
    Subtotal     1.36526e-05  5.68141e-05  3.93532e-05  1.09820e-04  100.00%
  Percentage          12.43%       51.73%       35.83%      100.00%  100.00%
  ------------------------------------------------------------------------------
@genus:root: 17>
```

```
Open   *h.sh
~/3trab

#!/bin/bash

echo "
|-----------------------------------------------||===============================================|
|---------------------- SIM ---------------------||-----------------------------------------------|
|-----------------------------------------------||------------------ Logic Synthesize ------------|
|source /soft64/source_gaph                     ||-----------------------------------------------|
|                                               ||source /soft64/source_gaph                     |
|module load modelsim                           |                                               |
|                                               ||module load genus                              |
|vsim &                                         ||                                               |
|                                               ||genus                                          |
|_______________________________________________||                                               |
|set_db library /soft64/design-kits/stm/65nm-cmos065_536/CORE65GPSVT_5.1/libs/CORE65GPSVT_nom_1.00V_25C.lib
                                                |                                               |
                                                |read_hdl -vhdl <c.f.>.vhd                      |
                                                |                                               |
                                                |elaborate fifo_sync                            |
                                                |-----------------------------------------------|
                                                |------------------ Constraints ----------------|
                                                |-----------------------------------------------|
                                                |read_sdc ./constraints.sdc                     |
                                                |                                               |
                                                |syn_generic -effort low                        |
                                                |                                               |
                                                |----||---------                                |
                                                |syn_generic -effort high                       |
                                                |                                               |
                                                |syn_map -effort high                           |
                                                |                                               |
                                                |----||---------                                |
                                                |report_timing                                  |
                                                |                                               |
                                                |report_power                                   |
                                                |                                               |
                                                |-----------------------------------------------|
                                                |                                               |
                                                |syn_generic                                    |
                                                |                                               |
                                                |syn_map                                        |
                                                |_______________________________________________|"
```