Work 3.2– UART Transmiter Module

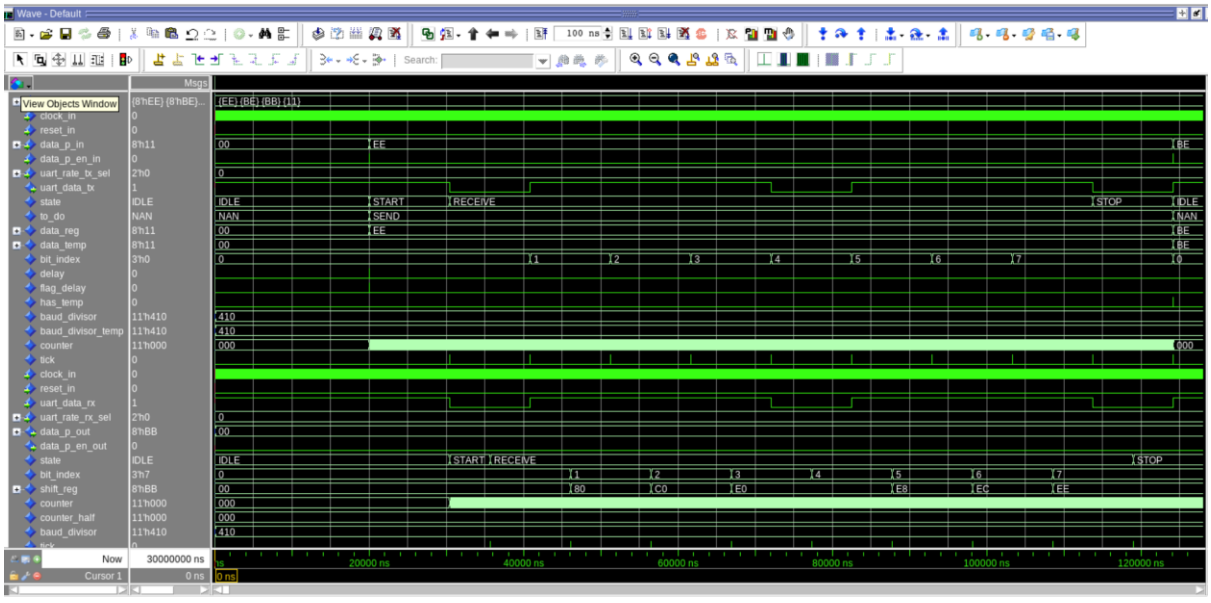
Course: Integrated Systems Design II

Student: Bruno Bavaresco Zaffari

Professor: Marlon Moraes

```
Transcript
# Errors: 0, Warnings: 0
# End time: 09:18:59 on Jun 03,2025, Elapsed time: 0:03:29
# Errors: 0, Warnings: 0
# vsim -wlf /sim/uart_tx_tb2 -voptargs=""+acc"" -wlfdeleteonquit uart_tx_tb2
# Start time: 09:18:59 on Jun 03,2025
# ** Note: (vsim-8009) Loading existing optimized design _opt
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.std_logic_arith(body)
# Loading ieee.std_logic_unsigned(body)
# Loading ieee.numeric_std(body)
# Loading work.uart_tx_tb2(tb)#1
# Loading work.uart_tx2(rtl)#1
# Loading work.uart_rx(rtl)#1
# ** Note: -
#    Time: 20 us  Iteration: 0  Instance: /uart_tx_tb2
# ** Note: TX has received <--------238
#    Time: 20015 ns  Iteration: 0  Instance: /uart_tx_tb2/duv
# ** Note: -
#    Time: 124120 ns  Iteration: 0  Instance: /uart_tx_tb2
# ** Note: TX has received <--------190
#    Time: 124135 ns  Iteration: 0  Instance: /uart_tx_tb2/duv
# ** Note: TX has successfully send ->238
#    Time: 124135 ns  Iteration: 0  Instance: /uart_tx_tb2/duv
# ** Note: RX has read: 238
#    Time: 129365 ns  Iteration: 0  Instance: /uart_tx_tb2/rx
# ** Note: -
#    Time: 228240 ns  Iteration: 0  Instance: /uart_tx_tb2
# ** Note: TX has received <--------187
#    Time: 228255 ns  Iteration: 0  Instance: /uart_tx_tb2/duv
# ** Note: -
#    Time: 332360 ns  Iteration: 0  Instance: /uart_tx_tb2
# ** Note: TX has received <--------17
#    Time: 332375 ns  Iteration: 0  Instance: /uart_tx_tb2/duv
# ** Note: TX has successfully send ->187
#    Time: 332375 ns  Iteration: 0  Instance: /uart_tx_tb2/duv
# ** Note: RX has read: 187
#    Time: 337605 ns  Iteration: 0  Instance: /uart_tx_tb2/rx

VSIM 3>
```



**Síntese – Cadence Genus:**

- Acessando via SSH à paxos, você deverá carregar o módulo do Genus no Terminal aberto.

```
source /soft64/source_gaph
module load genus
genus
```

.

- Definição da biblioteca que será utilizada neste projeto.

```
set_db library /soft64/design-kits/stm/65nm-cmos065_536/CORE65GPSVT_5.1/libs/CORE65GPSVT_nom_1.00V_25C.lib
```

.

- Leitura do(s) arquivo(s) VHDL que compõe o projeto. Neste exemplo o código fonte foi nomeado como "fifo_sync.vhd"

```
read_hdl -vhdl fifo_sync.vhd
```

---

- Elaboração do projeto. Neste exemplo a entidade do projeto foi nomeada como "fifo_sync".

```
elaborate fifo_sync
```

```
@genus:root: 6> read_hdl -vhdl uart_tx2.vhd
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 24.
        : The specified construct has no effect on synthesis. In some cases (such as 'after' clauses in signal assignments) may cause a mismatch between and s
imulation.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 27.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 29.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 30.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 31.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 32.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 32.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 33.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 36.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 36.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 37.
Warning : Initial values are ignored for synthesis. [VHDL-639]
        : in file 'uart_tx2.vhd' on line 38.
Warning : Report statements are ignored for synthesis. [VHDL-643]
        : in file 'uart_tx2.vhd' on line 102.
        : The specified construct has no effect on synthesis. Some constructs (such as 'after' clauses in signal assignments) may cause a mismatch between sim
ulation and synthesis.
Warning : Report statements are ignored for synthesis. [VHDL-643]
        : in file 'uart_tx2.vhd' on line 173.
@genus:root: 7> elaborate uart_tx2
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'uart_tx2' from file 'uart_tx2.vhd'.
Info    : Binding to architecture. [ELAB-5]
        : Elaborating architecture 'rtl' for entity 'uart_tx2'.
Info    : Done Elaborating Design. [ELAB-3]
        : Done elaborating 'uart_tx2'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
-------------------------------------------------------
| Trick             | Accepts | Rejects | Runtime (ms) |
-------------------------------------------------------
| ume_constant_bmux |       0 |       0 |         0.00 |
-------------------------------------------------------
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: uart_tx2, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: uart_tx2, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)
UM:   flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:*                                                                 elaborate
design:uart_tx2
@genus:root: 8>
```

read_sdc constraints.sdc

```
        : in file 'uart_tx2.vhd' on line 173.
@genus:root: 7> elaborate uart_tx2
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'uart_tx2' from file 'uart_tx2.vhd'.
Info    : Binding to architecture. [ELAB-5]
        : Elaborating architecture 'rtl' for entity 'uart_tx2'.
Info    : Done Elaborating Design. [ELAB-3]
        : Done elaborating 'uart_tx2'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks
-------------------------------------------------------
| Trick            | Accepts | Rejects | Runtime (ms) |
-------------------------------------------------------
| ume_constant_bmux |       0 |       0 |         0.00 |
-------------------------------------------------------
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: uart_tx2, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: uart_tx2, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)
UM:   flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:*                                                                 elaborate
design:uart_tx2
@genus:root: 8> read_sdc const2.sdc
Statistics for commands executed by read_sdc:
 "create_clock"             - successful      1 , failed      0 (runtime  0.00)
 "get_ports"                - successful     19 , failed      0 (runtime  0.01)
 "set_input_transition"     - successful     16 , failed      0 (runtime  0.00)
 "set_load"                 - successful      2 , failed      0 (runtime  0.00)
 "set_load_unit"            - successful      1 , failed      0 (runtime  0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
@genus:root: 9>
```

5. Ainda no terminal do Genus aplique as *constraints* ao projeto, e realize a síntese lógica do projeto observando os impactos de cada etapa no diagrama esquemático apresentado na interface gráfica da ferramenta:

```
read_sdc ./constraints.sdc
synthesize -to_generic -effort low
synthesize -to_mapped -effort low
```

```
synthesize -to_generic -effort high
synthesize -to_mapped -effort high
```

Devido ao fato de serem grandes os arquivos foram salvos em .txt junto a esse diretório.

Report_timing:

```
@genus:root: 20> report_timing
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.12-s068_1
  Generated on:           Jun 03 2025  04:55:42 pm
  Module:                 uart_tx2
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (9470 ps) Setup Check with Pin counter_reg[10]/CP->D
          Group: clock_in
     Startpoint: (R) counter_reg[0]/CP
          Clock: (R) clock_in
       Endpoint: (F) counter_reg[10]/D
          Clock: (R) clock_in

                    Capture       Launch
       Clock Edge:+   10000            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=  10000            0

             Setup:-     54
     Required Time:=   9946
      Launch Clock:-      0
         Data Path:-    476
             Slack:=   9470

#-------------------------------------------------------------------------------------------------------
#   Timing Point    Flags    Arc   Edge       Cell        Fanout Load Trans Delay Arrival Instance
#                                                           (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------
  counter_reg[0]/CP -       -      R     (arrival)           45    -     0     0       0    (-,-)
  counter_reg[0]/Q  -       CP->Q  R     HS65_GS_DFPQX9       3  6.9    24    58      58    (-,-)
  g11198__5477/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    42     100    (-,-)
  g11161__2802/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    40     140    (-,-)
  g11139__6131/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    40     181    (-,-)
  g11137__5122/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    40     221    (-,-)
  g11122__2802/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    40     262    (-,-)
  g11111__2398/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    40     302    (-,-)
  g11096__9945/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    40     342    (-,-)
  g11089__2802/CO   -       B0->CO R     HS65_GS_HA1X4        1  2.4    21    40     383    (-,-)
  g11085__8428/CO   -       B0->CO R     HS65_GS_HA1X4        1  4.5    29    46     428    (-,-)
  g11083__5107/Z    -       B->Z   R     HS65_GSS_XNOR2X6     1  2.7    26    33     462    (-,-)
  g11081__2398/Z    -       A->Z   F     HS65_GS_NOR2X5       1  2.3    30    14     476    (-,-)
  counter_reg[10]/D <<<     -      F     HS65_GS_DFPQX9       1    -     -     0      476    (-,-)
#-------------------------------------------------------------------------------------------------------
```

Report_power:

```
@genus:root: 21> report_power
Info    : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Info    : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
        : uart_tx2
Info    : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info    : ACTP-0001 Activity propagation ended for stim#0
Info    : PWRA-0001 [PwrInfo] compute_power effective options
        : -mode : vectorless
        : -skip_propagation : 1
        : -frequency_scaling_factor : 1.0
        : -use_clock_freq : stim
        : -stim :/stim#0
        : -fromGenus : 1
Info    : ACTP-0001 Timing initialization started
Info    : ACTP-0001 Timing initialization ended
Info    : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
        : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
        : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
        : of power analysis, ignored this option.
Info    : PWRA-0002 Started 'vectorless' power computation.
Info    : PWRA-0009 [PwrInfo] Power Computation Progress Report : 100%
Info    : PWRA-0002 Finished power computation.
Info    : PWRA-0007 [PwrInfo] Completed successfully.
        : Info=6, Warn=2, Error=0, Fatal=0
Instance: /uart_tx2
Power Unit: W
PDB Frames: /stim#0/frame#0
  ---------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ---------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     4.66720e-06  3.65974e-05  2.21943e-06  4.34840e-05  59.40%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     4.25062e-06  1.29683e-05  7.54738e-06  2.47663e-05  33.83%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  4.95000e-06  4.95000e-06   6.76%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ---------------------------------------------------------------------------
    Subtotal     8.91782e-06  4.95657e-05  1.47168e-05  7.32003e-05  99.99%
  Percentage          12.18%       67.71%       20.10%      100.00% 100.00%
  ---------------------------------------------------------------------------
@genus:root: 22>
```

Report_area:

```
  ---------------------------------------------------------------------------
@genus:root: 22> report_area
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.12-s068_1
  Generated on:           Jun 03 2025  04:56:26 pm
  Module:                 uart_tx2
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance Module  Cell Count  Cell Area  Net Area   Total Area     Wireload
-----------------------------------------------------------------------------
uart_tx2               176    787.800     0.000      787.800 area_0Kto1K (S)
  (S) = wireload was automatically selected
@genus:root: 23>
```