EECS 343: Homework 2 - Solution

Memory Management and Virtual Memory

Fall 2014

Important Dates

Out: October 20, 2014.

Due: October 27, 2014 (11:59PM CST).

Submitting your assignment: Please use the course submission site. There is a link to it from the class site. **Submit only ASCII text files.**

Problems

1. Consider a swapping system in which memory consists of the following hole sizes in memory order: 10 KB, 4 KB, 20 KB, 18 KB, 7 KB, 9 KB, 12 KB, and 15 KB. Which hole is taken for successive segment requests of

   (a) 12 KB
   (b) 10 KB
   (c) 8 KB

   for First Fit? Now repeat the question for Best Fit, Worst Fit, and Next Fit.

   Answer: *First fit takes 20 KB, 10 KB, 18 KB. Best fit takes 12 KB, 10 KB, and 9 KB. Worst fit takes 20 KB, 18 KB, and 15 KB. Next fit takes 20 KB, 18 KB, and 9 KB.*

2. What is the difference between a physical address and a virtual address?

   Answer: *Real memory uses physical addresses. These are the numbers that the memory chips react to on the bus. Virtual addresses are the logical addresses that refer to a process' address space. Thus a machine with a 32-bit word can generate virtual address up to 4 GB regardless of whether the machine has more or less memory than 4GB.*

3. A computer has four page frames. The time of loading, time of last access and the R and M bits for each page are as shown below (the times are in clock ticks):

Page	Loaded	Last ref.	R	M
0	126	280	1	0
1	230	265	0	1
2	140	270	0	0
3	110	285	1	1

For each of these algorithms, Which page will be replaced?

Answer:

(a) NRU: *2*

(b) FIFO: *3*

(c) LRU: *1*

(d) Second Chance: *2*

4. You are given the following data bout a virtual machine system:

   (a) The TLB can hold 1024 entries and can be accessed in 1 clock cycle (1 nsec)

   (b) A page table entry can be found in 100 clock cycles or 100 nsec

   (c) The average page replacement time is 6 msec

   If page references are handled by the TLB 99% of the time and only 0.01% lead to a page fault, what is the effective address-translation time?

   Answer: *The chance of a hit is 0.99 for the TLB, 0.0099 for the page table, and 0.0001 for a page fault (i.e., only 1 in 10,000 references will cause a page fault). The effective address translation time in nsec is then:*

$$0.99 * 1 + 0.099 * 100 + 0.0001 * 6 * 10^6 \approx 602 \; clock \; cycles.$$

   Note that the effective address translation time is quite high because it is dominated by the page replacement time even when page faults only occur once in 10,000 references.

5. When segmentation and paging are both being used, as in MULTICS, first the segment descriptor must be looked up, then the page descriptor. Does the TLB also work this way, with two level of lookup?

   Answer: *No. The search key uses both the segment number and the virtual number, so the exact page can be found in a single match.*