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EECS 361 Computer Architecture

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Quiz #5

1) How many cycles does a load operation take in our multicycle datapath?

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2) What are the main operations performed in each of these cycles?

Instruction Fetch
Instruction Decode/Register Read
Address Calculation
Memory Read
Writeback

3) Assume that the maximum frequency of the single cycle datapath in our lecture notes is 100 MHz. Also, assume that the datapath can be run at 450 MHz after converting it to a multicycle design. Give example code segments (in other words sequence of instruction(s)), that will
a) result in the multicycle datapath to have a higher performance

A code segment with any mix of instructions of branch and arithmetic

b) result in the singlecycle datapath to have a higher performance

A segment with load instructions