1. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.2. P2 has a 2.6 GHz clock rate and a CPI of 1.0. P3 has a 4.25 GHz clock rate and has a CPI of 3.

a. Which processor has the highest performance expressed in instructions per second?

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

2. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.25 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3.5 GHz and CPIs of 2, 2, 2, and 3.
Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D,

a. Which implementation is faster?

b. What is the global CPI for each implementation?

c. Find the clock cycles required in both cases.

3. [15] < § 1.6> Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.15E9 and has an execution time of 1.15 s, while compiler B results in a dynamic instruction count of 1.6E9 and an execution time of 1.75 s.

a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

c. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

4. Assume a 15 cm diameter wafer has a cost of 13.5, contains 74 dies, and has 0.020 defects/cm^2. Assume a 21 cm diameter wafer has a cost of 16, contains 110 dies, and has 0.031 defects/cm^2.

a. Find the yield for both wafers.

b. Find the cost per die for both wafers.

c. If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.

d. Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200mm^2.

5. For the following C statement, what is the corresponding MIPS assembly code? Assume that the variables `i` and `j` are assigned to registers `$s0` and `$s1`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6` and `$s7`, respectively, and assume that the elements of both arrays are 4-byte words.

```
B[8] = A[i-j];
```

6. Translate the following C code to MIPS. Assume that the variables `i` and `j` are assigned to registers `$s0` and `$s1`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6` and `$s7`, respectively, and assume that the elements of both arrays are 4-byte words.

```
B[8] = A[i] - A[j];
```

7. Provide the type and assembly language instruction for the following binary value: `0000 0010 0001 0000 1000 0000 0010 0010`$_{two}$

8. Provide the binary representation of following instruction:

```
sw $t3, 32($t4)
```