Last Name: _____

Northwestern University
Department of Electrical Engineering and Computer Science
EECS 361 Computer Architecture

Instructor: Gokhan Memik (memik@eecs.northwestern.edu)

Quiz 2

1) Assume that you have the option of implementing an enhancement to a processor that reduces the number of instructions in an average program by 10%. In addition, assume that due to this enhancement, the clock cycle time is increased by 5% (i.e., clock frequency is reduced by 5%). What is the overall gain of this enhancement?

$ExecutionTime_{base}$ = 1.0 IC * CPI * 1.0 CycleTime
$ExecutionTime_{enhancement}$ = 0.9 IC * CPI * 1.05 CycleTime

$Performance_{enhancement} / Performance_{base}$ = $ExecutionTime_{base} / ExecutionTime_{enhancement}$
= 1 / (0.9 * 1.05) = 1 / 0.945
= 1.058

Therefore, the enhancement will result in 5.8% increase in performance

2) Assume that you implemented an enhancement to a processor that can be applied 60% of the execution time. If the speed-up for the applicable portion is 2, what is the overall speed-up achieved?

Using Amdahl's Law:
$Speedup_{overall}$ = 1 / (0.6 / 2 + (1 – 0.6)) = 1 / 0.7
= 1.42
Hence, the overall speed-up is 42%.

3) Give an example of a displacement addressing mode.

lw $r1, 100($r2), which would load the value from the memory at address '100 + $r2' (in other words M[100+$r2]) into $r1.