Name: _____

Northwestern University
Department of Electrical and Computer Engineering
ECE 361 Computer Architecture

Question	Score
1	/ 20
2	/ 25
3	/ 30
4	/ 25
Total	/ 100

NOTE: Please show your work clearly for all the questions. Use the space provided for your answers as much as possible. If necessary feel free to use the back of the sheets and/or additional sheets.

Question 1) (20 points = 5 * 4 points) For each subpart (1.a) to (1.e) below, circle ***all*** correct answers from among the four given - note that ***more than one*** answer may be correct!

1.a) The following is true about the instruction-set architecture level of a modern computer:

(a) it is the lowest software level.

(b) the number of registers in the computer can be discovered by reading its specification.

(c) the size of the cache in the computer can be discovered by reading its specification.

1.b) Judging by current trends, the following are predicted as some of the primary challenges in designing future computers:

(a) designing complex instructions that can do the work of many current-day instructions in modern general-purpose computers.

(b) reducing the CPU's power consumption.

(c) designing ISAs with an increasing number of program registers.

(d) developing designs with larger on-chip memories.

1.c) A set-associative cache

(a) reduces misses due to address conflicts compared to a direct-mapped cache.

(b) eliminates misses due to address conflicts.

(c) is built of SRAM memory technology.

(d) takes advantage of spatial locality better than a direct-mapped cache.

1.d) A write buffer

(a) can result in fewer DRAM accesses for multiple writes to the same address.

(b) is more valuable with a write-back cache than a write-through cache.

(c) is usually implemented as a direct-mapped cache.

1.e) A pipelined processor

(a) will always have a better performance than a single-cycle processor

(b) will have a larger CPI than a single-cycle processor.

(c) will always have a smaller CPI than a multi-cycle processor.

(d) will always have a clock cycle that is greater than or equal to the clock cycle of the multi-cycle design it is based on.

Question 2) (25 points) A computer executes a total of x dynamic instructions at an average of *ipc* instructions per cycle. Memory instructions are a fraction *mem* of the total number of dynamic instructions. The cache hit rate is a fraction h and the cache miss latency is M cycles. What fraction of the program's execution time is devoted to servicing cache misses?

Question 3) (30 points) Consider the following code segment:

```
1       ld Mem[r2+4] → r5
2       add r5 + r3 → r1
3       beq r1, r0, instruction#5
4       ld Mem[r2 + 8] → r6
5       st r2 → Mem[r5]
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3.a) (10 points) Identify the data hazards (RAW, WAR, and WAW). For each type of dependence (RAW, WAR and WAW), make a list of the dependencies of that type found in the above code. Note that such dependencies are independent of a machine type.

3.b) (10 points) Consider a processor with a simple pipeline with stages IF, ID/RF, EX, MEM, WR (note that this is identical to the pipelined machine described in the lecture notes). The processor has maximum forwarding capability. Assume the branch (instruction #3) is NOT taken. Show the timing of the instruction execution in this processor. Note that you do not have to draw the processor itself, a diagram similar to that of lecture 12 – slide 22 is sufficient.

3.c) (10 points) Now consider a processor with a six-cycle pipeline. This increase is caused by a two-cycle memory access (instead of a single cycle). The resulting pipeline has the stages: IF, ID/RF, EX, MEM, MEM, WR. As in part (b), assume the branch (instruction #3) is NOT taken and that it is correctly predicted. Complete the timing diagram of the execution of the instructions. You can use a diagram similar to the one used in part (b).

Question 4) (25 points) Consider a 64-bit machine (the virtual addresses are 64-bits) with 16KB pages and maximum 1GB of physical memory (i.e., 30-bit physical address). Assume that each Page Table Entry (PTE) contains one Physical Page Number (PPN) only.

4.a) (10 points) How much storage is needed for a single-level page table?

4.b) (15 points) How much total storage is needed for a two-level page table? Assume the first level table holds full physical addresses and each 2nd level table is 16KB in size.