EECS 361 - Computer Architecture
Syllabus

Instructor

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Teaching Assistants

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Office Hours: Monday 11am – noon, Tech L458 (or by appointment)

Location and Time

Searle 1441: Tu/Th 12:30pm – 1:50pm

Prerequisites

1. ECE 205 (or 213)
2. ECE 303 (or 355)

If you haven't taken these classes, discuss it with the instructor before enrolling in the class.

Textbook

D. Patterson and J. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, Morgan Kaufmann, 5th edition, 2013

Quizzes

There will be several quizzes designed to test basic knowledge you acquire. They will not be graded. However, you can get up to 5% bonus points by taking the quizzes.

Homeworks

There will be 3 or 4 homework assignments related to the topics covered in the class.

Lab Project

There will be a lab project. The design tools that will be used in the final project will be used for this relatively simple project. You will be designing your components in structural VHDL. Each student will work individually for this project and will design an ALU. The designed ALU can later be used in the Final Project.

Group Projects

There will be two projects entailing the designing a single cycle processor, a cache structure, and their evaluation using simple programs. The projects will also include written reports discussing the design decisions made, explaining obstacles encountered during the process, and showing the outcome of the projects.

Exams

There will be one late exam. The schedule is not determined, but tentatively the exam will be held on the last week of classes.

Grading

Quizzes - Bonus points up to 5%
Homework assignments and Lab - 30 % (20% homeworks and 10% lab project)
Group Projects - 40 %
Exam - 30%

Late Policy

For each **calendar day** after the due date for the homework or the lab project, there is a 10% penalty. For example, after 1 day, you will lose 10/100 points, after 2 days you lose 20/100 points, etc. No homeworks will be accepted after the solutions are posted.

Objectives and Philosophy

When a student completes this course, he/she should be able to:

1. Understand the architecture of a basic computer system and its components, and the role of performance in designing computer systems.
2. Understand how to design and instruction set and its impact on processor design. To design ALU and processor datapath and control.
3. Design pipeline processor including datapath and control, and design to detect and resolve hazards.
4. Understand memory hierarchy design and its impact on overall processor performance. Design cache memory based on the characteristics of the expected workload. Understand the workings of virtual memory and efficient design for TLBs
5. Understand the I/O system and its design. Be Knowledgeable about busses and bandwidth requirements to support heterogeneous I/O devices. Understand the disk technology and its impact on performance.
6. Know about terms such as Branch Prediction, Hyper-Threading, Hyper Pipelining, and Instruction-Level Parallelism.

Schedule

Week 1: Introduction, ISA definition, the effect of technology on computer systems, trends in computing, performance, benchmarking, design metrics, Amdahl's Law

Week 2: ISA: Instruction Formats, Sequencing, Languages and Compilers, Delayed Branch, Procedures, MIPS ISA

Week 3: Design Decisions, Arithmetic Units, ALU design

Week 4: Division, Datapath, Single-Cycle Processor Design

Week 5: Designing Control, Multi-Cycle Datapath

Week 6: Pipelining, Designing a Pipelined Processor

Week 7: Introduction to Memory Subsystem, Caches

Week 8: Virtual Memory, I/O

Week 9: Disks

Week 10: Overview, discussion of advanced techniques: Hyper-Threading, Hyper-Pipelining, and Instruction-Level Parallelism