HW 12
CS 411

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- x2 32-bit words sent in 1 clk
- x4 32-bit available on registers per access
- 1st access → 5 clks, each following sequential access → 4 clks
- 50 MHz clk, → Period of 20ns

For the I/O Device to get 512 words when the device uses 4 as the word count

a.) 512 words / 4 words per transaction = 128 transactions

clks/transaction = 1 * 5 clks + 4 clks = 9 clks per transaction

↑ 1 access per transaction + ↑ load words & bus idle

$\sum$ = Total transactions * clks/transaction

Total clks = 128 * 9

↳ = 1152 clks

Period ↓

Total time = total clks * T

23,040ns = 1,152 clks * 20ns

b.) Transactions/second = Total transactions / Total time = 128 / $23{,}040 \times 10^{-9}$ s

↓

= 5.56 M transactions per second

c Bandwidth = total bytes / total time =

↳ 512 Words * 4 bytes/word

= 2048 bytes

= 2048 bytes / $23{,}040 \times 10^{-9}$ s

Bandwidth = $\frac{2.048 \times 10^{3}\ B}{2.304 \times 10^{-5}\ s}$ = 88.89 MBps

For I/O device to get 512 words when the devices uses 32 as word Count

d.) total transactions = total words / words per transaction

↳ = 512/32 = 16 transactions

accesses per transaction = $\frac{\text{Words per transaction}}{\text{Words per access}}$

↳ = 32/4 = 8 accesses/transaction

∴ CLKS/transaction = 1*5clks + 7*4clks + 4clks
(1st access; following seq accesses; non-overlapping transfers)

= 37 clock cycles per transaction

↳ Total Clock cycles = $\frac{\text{CLKS}}{\text{transactions}}$ * total transactions

= 37(clks per tran) * 16 transactions = 592 clks

Total time = total clks * clk period = 592 x 20ns

↳ = 11.84 μs = **11840 ns**

e.) Transactions per second:

= Total transactions / total time = $16 / 11.84 \times 10^{-6}$ s

↳ **Transactions per sec = 1.351 Million transactions per sec**

f.) bandwidth = Total bytes / total time

= 2048 B / 11.84 μs = $\frac{2.048 \times 10^{3}\ B}{11.84 \times 10^{-6}\ s}$

↳ **Bandwidth = 172.972 MBps**