UIC ECE464 (Fall 2019)

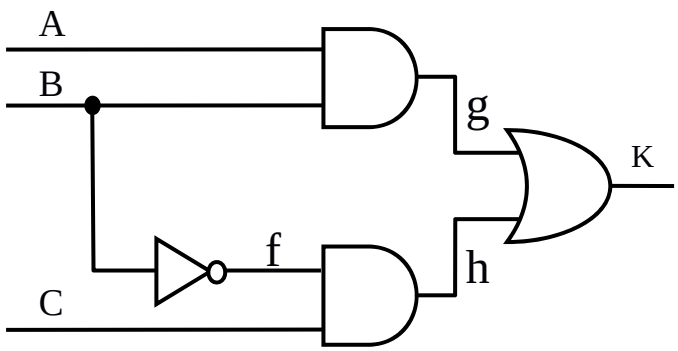
Project 1: Fault Simulation & Detection

In this project, you will work with a group to come up with a Python program for the following functionalities:

1) (20%) Generate Full Fault List:

- Input: a circuit netlist file (default: circuit.bench)
- Output: a text file containing all the possible single-stuck-at faults (in every input, and around every gate) with a final total count (default: full_f_list.txt)

For example, for the circuit bench below, the full fault list file is shown on the right.




```
# circuit.bench
# 3 inputs
# 1 output
# 4 gates

INPUT(A)
INPUT(B)
INPUT(C)

OUTPUT(K)

f = NOT(B)
g = AND(A, B)
h = AND(f, C)
K = OR(g, h)
```

```
# circuit.bench
# full SSA fault list

A-SA-0
A-SA-1
B-SA-0
B-SA-1
C-SA-0
C-SA-1
f-SA-0
f-SA-1
f-IN-B-SA-0
f-IN-B-SA-1
g-SA-0
g-SA-1
g-IN-A-SA-0
g-IN-A-SA-1
g-IN-B-SA-0
g-IN-B-SA-1
h-SA-0
h-SA-1
h-IN-f-SA-0
h-IN-f-SA-1
h-IN-C-SA-0
h-IN-C-SA-1
K-SA-0
K-SA-1
K-IN-g-SA-0
K-IN-g-SA-1
K-IN-h-SA-0
K-IN-h-SA-1

# total faults: 28
```

2) (80%) Fault Simulation

- Input: three files
  - a circuit netlist file (default: circuit.bench)
  - a fault list file (default: f_list.txt)
  - a test vector input file (default: input.txt)
- Output: simulation results (default: fault_sim_result.txt)

For example:

```
# circuit.bench
# 3 inputs
# 1 output
# 4 gates

INPUT(A)
INPUT(B)
INPUT(C)

OUTPUT(K)

f = NOT(B)
g = AND(A, B)
h = AND(f, C)
K = OR(g, h)
```

```
# test vector file
# for circuit.bench
# input.txt

010
111
110
```

```
# fault list file
# for circuit.bench
# f_list.txt

A-SA-0
A-SA-1
g-IN-B-SA-1
f-SA-1
h-SA-1
```

```
# fault sim result
# input: circuit.bench
# input: input.txt
# input: f_list.txt


tv1 = 010 -> 0 (good)
detected:
A-SA-1: 010 -> 1
h-SA-1: 010 -> 1

tv2 = 111 -> 1 (good)
detected:
A-SA-0: 111 -> 0

tv3 = 110 -> 1 (good)
detected:
A-SA-0: 110 -> 0

total detected faults: 3

undetected faults: 2
g-IN-B-SA-1
f-SA-1

fault coverage: 3/5 = 60%
```

3) (extra credit 10%) Test Vector Set Generation:

- Input: two files
  - a circuit netlist file (default: circuit.bench)
  - a fault list file (default: f_list.txt)
- Output: a test vector set that can cover > 90% of the faults (default: tv_set.txt)

Deadlines: (Late submission / evaluation will NOT be accepted)

- GitHub link submission deadline: week 4 Friday September 20, 2019 11:59:00 PM
  - This will be used by instructors to assign credits for different group members according to work done.
- Final Submission window: week 5 Tue – week 6 Mon
  - September 24, 2019 12:00:00 AM - September 30, 2019 11:59:00 PM
- Peer Evaluation window: week 6 Tue – week 7 Mon
  - October 1, 2019 12:00:00 AM - October 7, 2019 11:59:00 PM