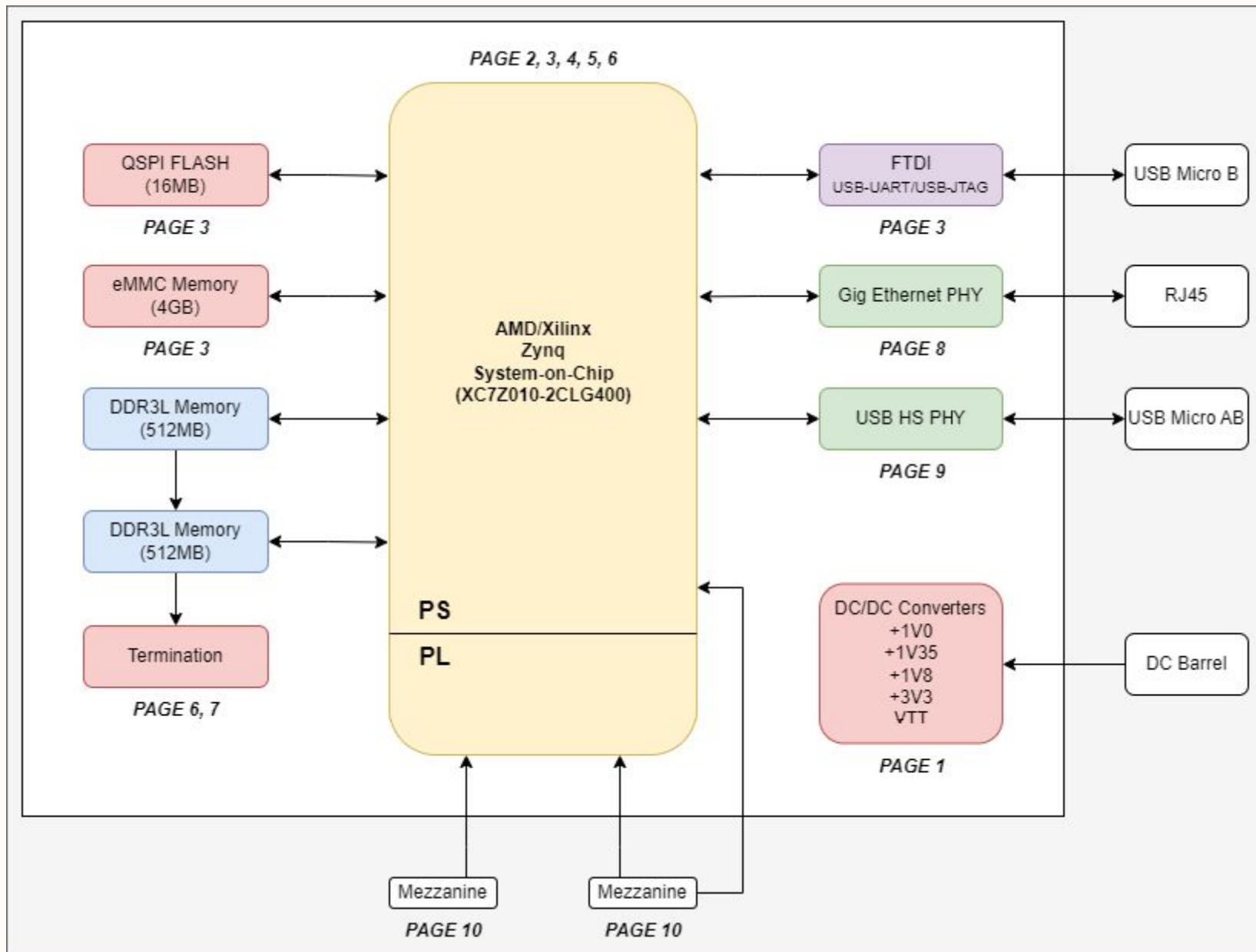


ZettBrett Reloaded - Overview

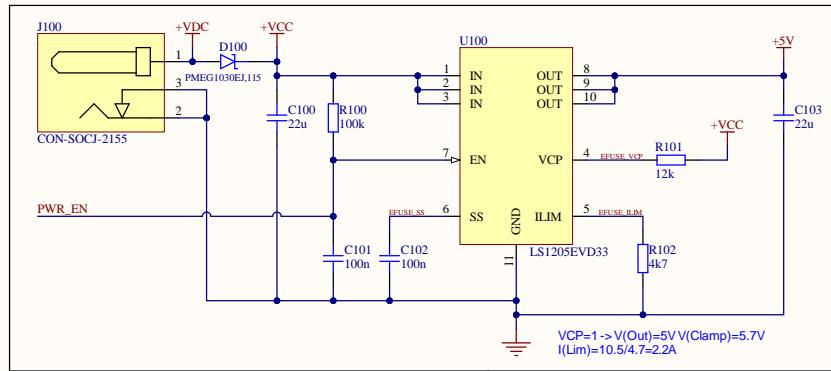


Rev B

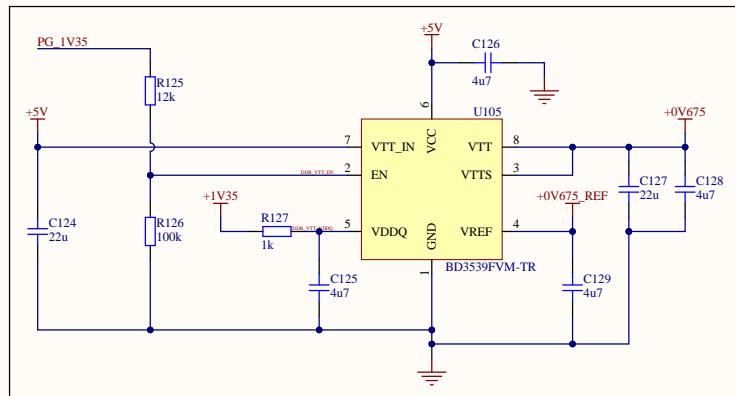
ZettBrett Reloaded

[1] Power

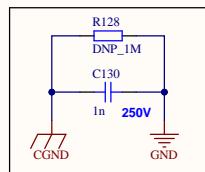
Input Power & eFuse



DDR3L VTT Regulator

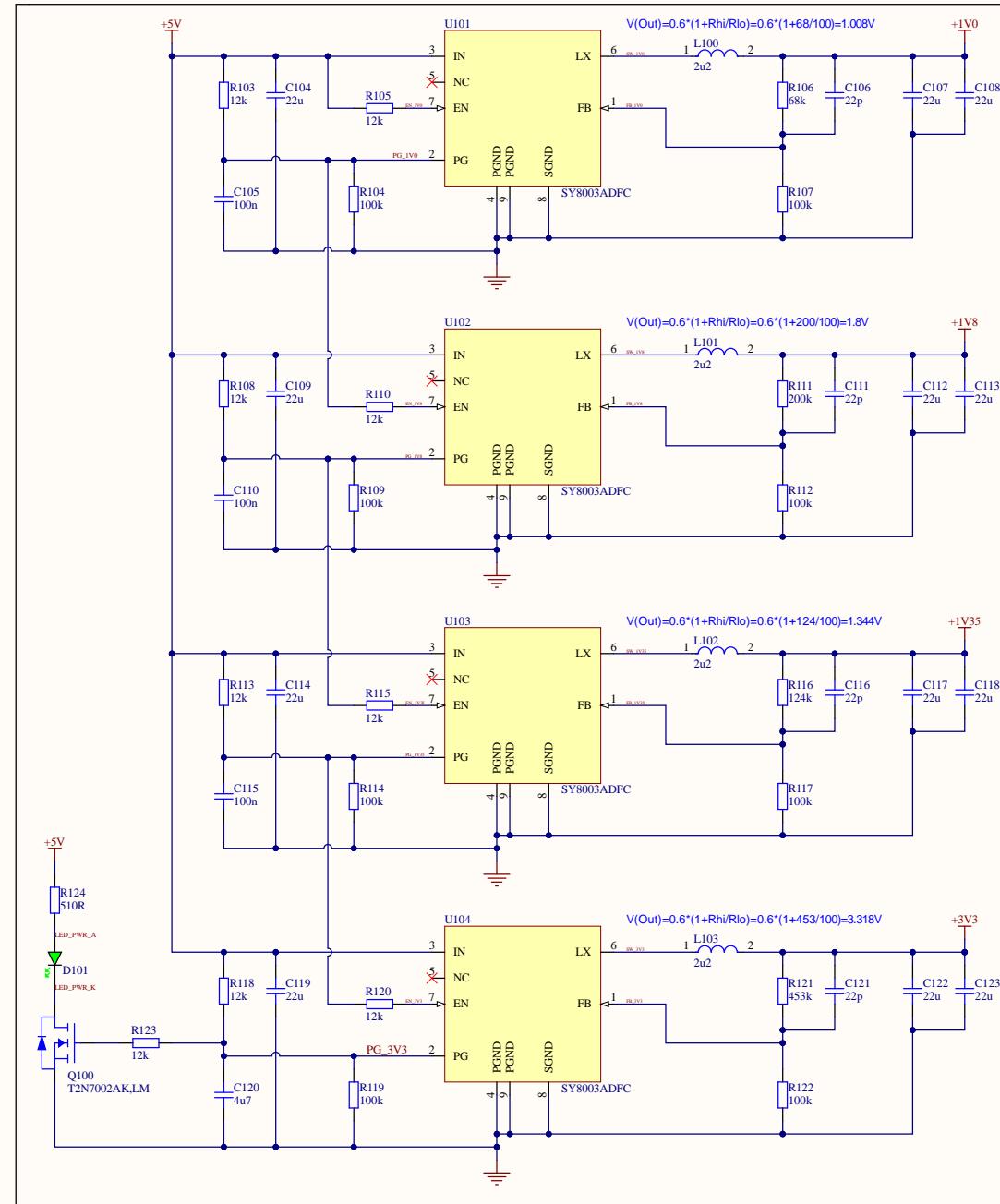


Chassis GND Connection



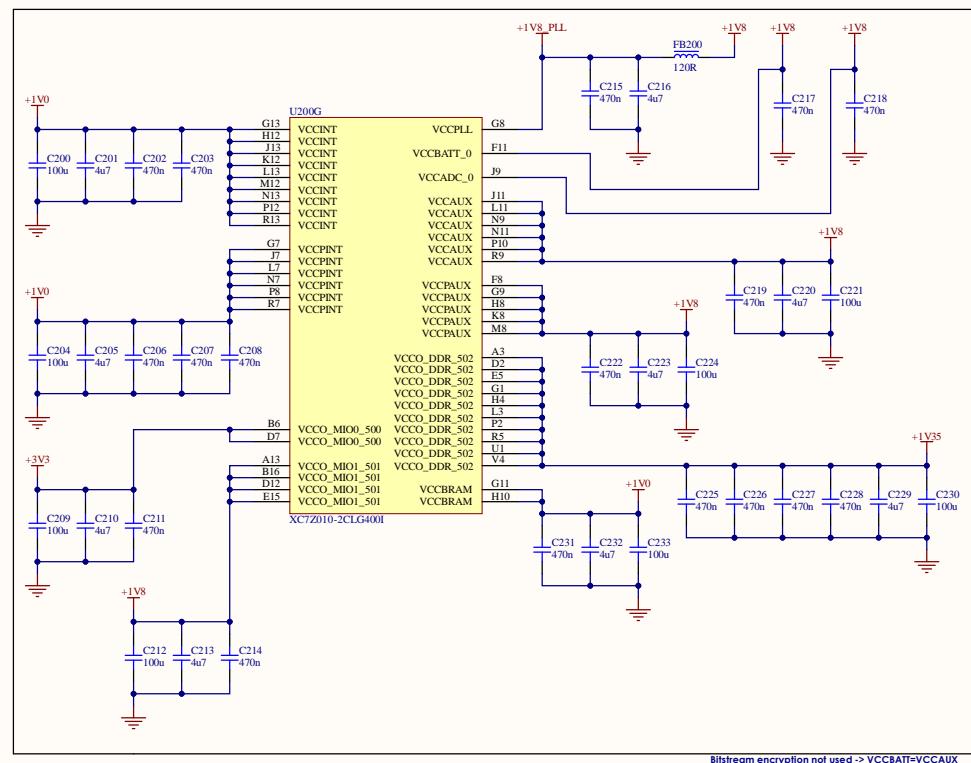
Buck Converters

Power sequence: +1V0 -> +1V8 -> +1V35 -> +3V3

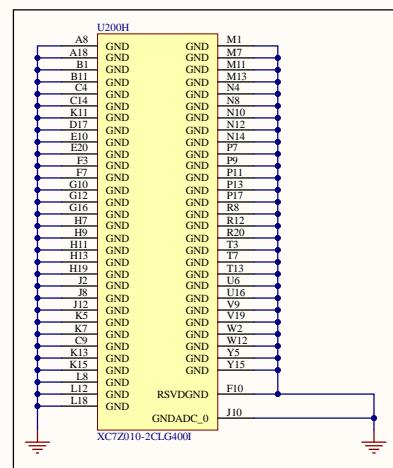


[2] Zynq Power and Decoupling

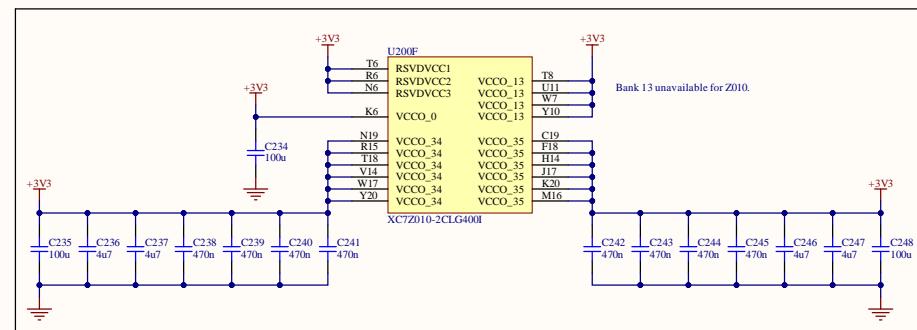
Main Supplies (INT, AUX, DDR, MIO)



GND Connections



Bank Supplies (0, 34, 35)



Xilinx Recommend Decoupling Caps

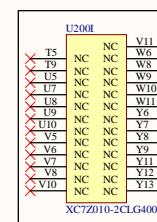
Table 3-2: Required PCB Capacitor Quantities per Device (PS)

Package	Device	V_{CCPIN}	$V_{CCPAUX}^{(1)}$	V_{CCO_DDR}	V_{CCO_MIO}	V_{CCO_MIO1}	$V_{CCPLL}^{(2)(3)}$
		100 μ F	4.7 μ F	100 μ F	4.7 μ F	100 μ F	4.7 μ F
CLG225	Z-7007S	1	1	3	1	1	1
CLG400	Z-7007S	1	1	3	1	1	1
CLG225	Z-7010	1	1	3	1	1	1
CLG400	Z-7010	1	1	3	1	1	1

Table 3-1: Required PCB Capacitor Quantities per Device (PL)

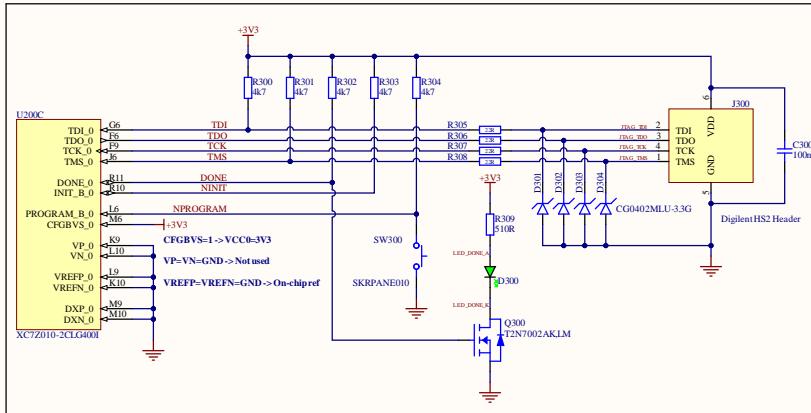
Package	Device	V_{CCINT}	V_{CCBRAM}	V_{CCAUX}	V_{CCALUX}	$V_{CCO_per\ Bank}^{(3)(4)}$	Bank 0
		680 μ F	330 μ F	100 μ F	4.7 μ F	47 μ F	47 μ F
CLG225	Z-7007S	0	0	1	1	NA	NA
CLG400	Z-7007S	0	0	1	2	NA	NA
CLG225	Z-7010	0	0	1	1	NA	NA
CLG400	Z-7010	0	0	1	2	0	1

Unused Pins

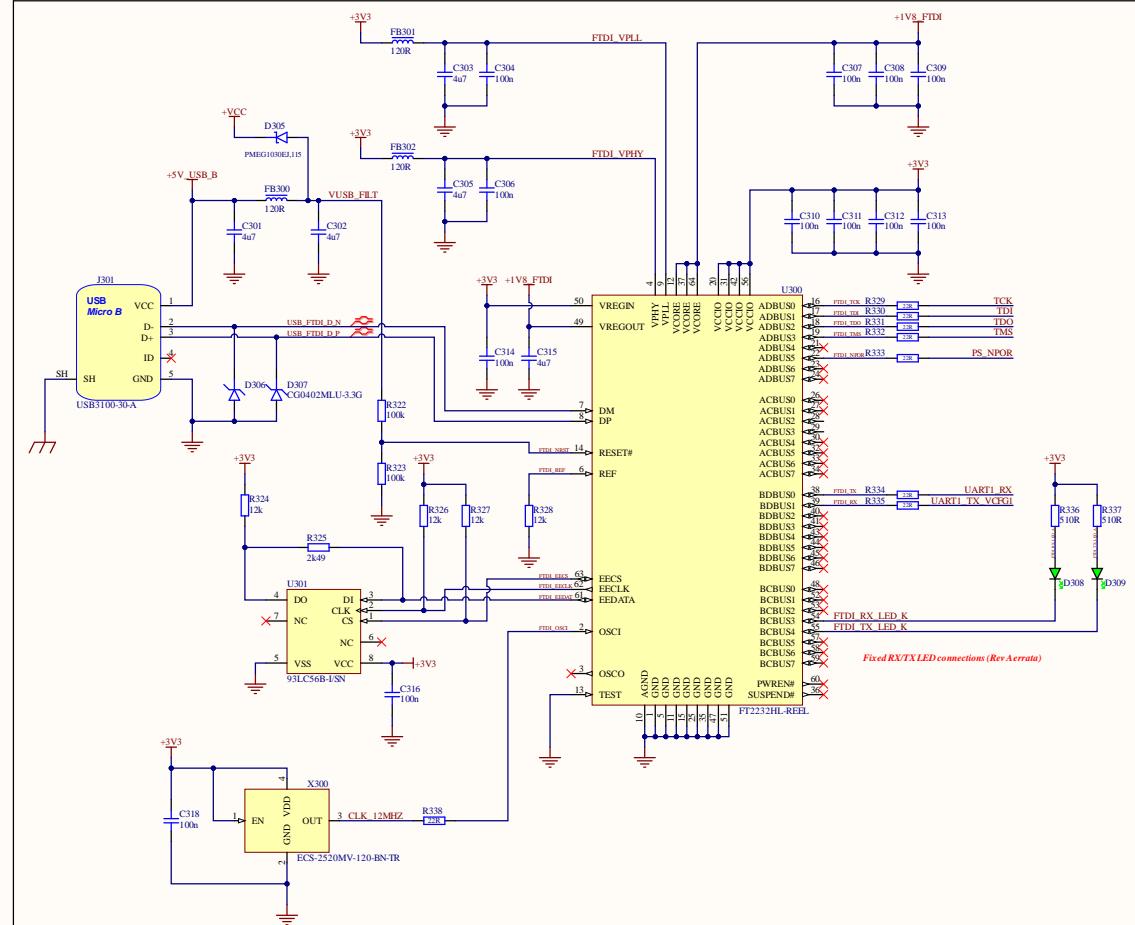


[3] Zynq Config, JTAG, Debug

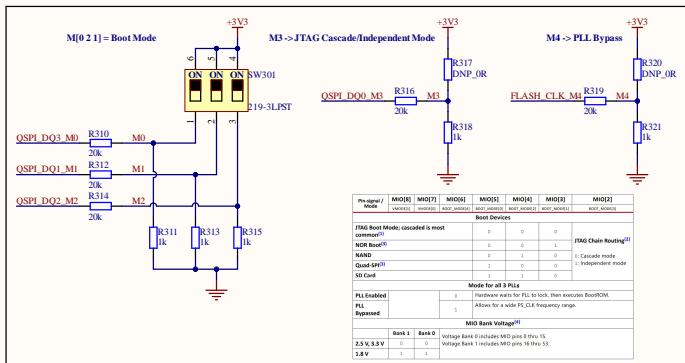
Zynq Config, JTAG



FTDI JTAG Programmer and USB-to-UART



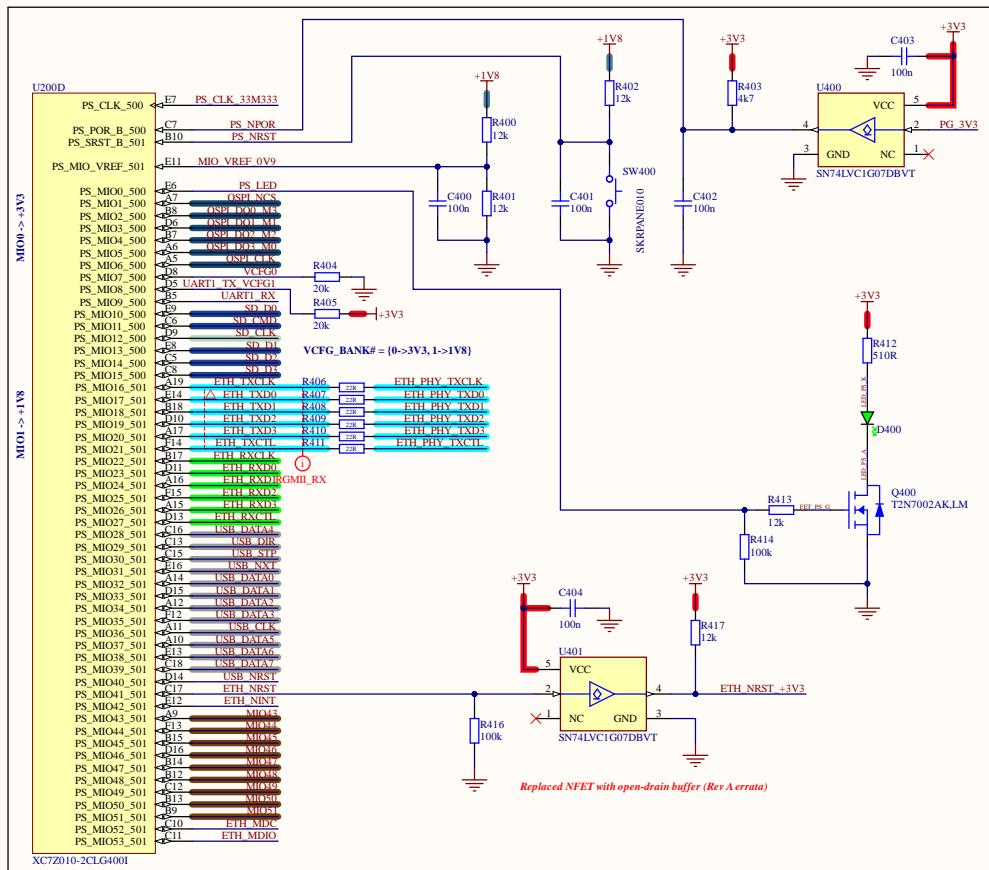
Boot Mode MIO Strapping Pins (Zynq TRM p167)



ZettBrett Reloaded

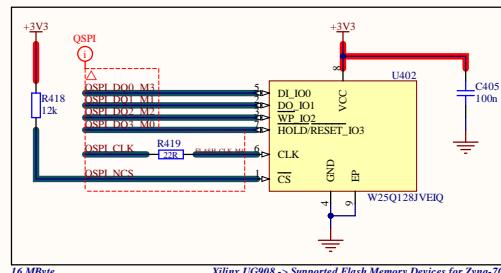
[4] Zynq Processing System (PS)

Zyng PS (Bank 500 & 501)

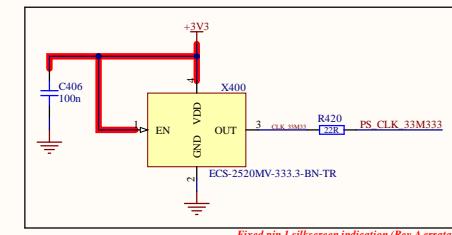


Bank 1 I/O Voltage = 1.8V due to HSTL requirement (high-speed for USB + Ethernet)

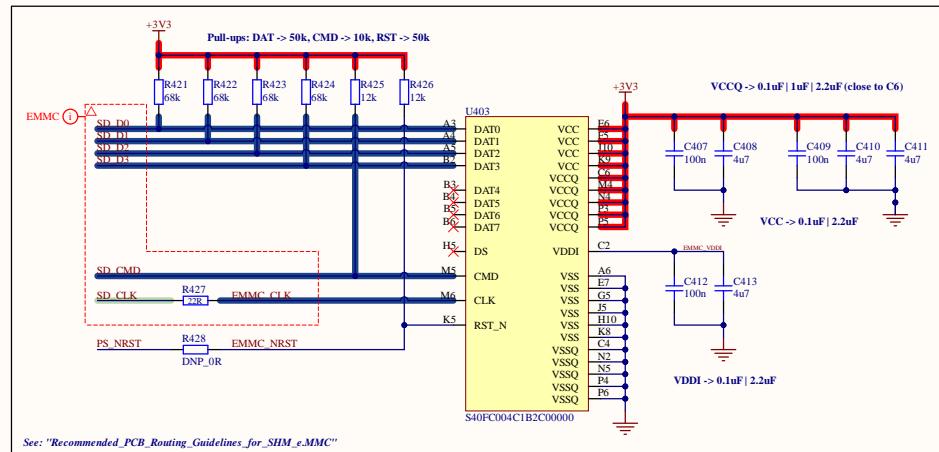
QSPI Flash Memory (128MBit)



PS Clock (33.33 MHz)



EMMC Memory



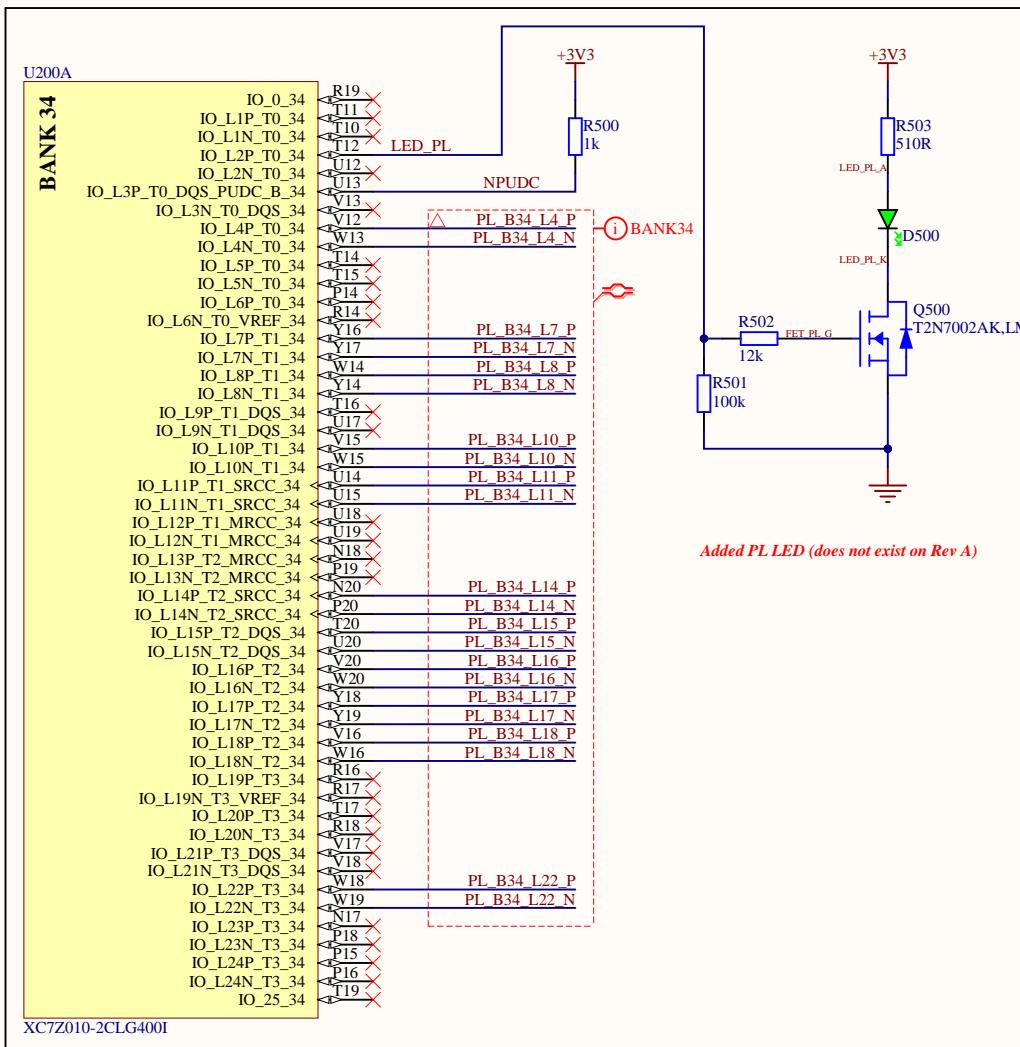
See: "Recommended PCB Routing Guidelines for SHM eMMC"

Alternative industrial temperature version: S40EC004C1B2J00000

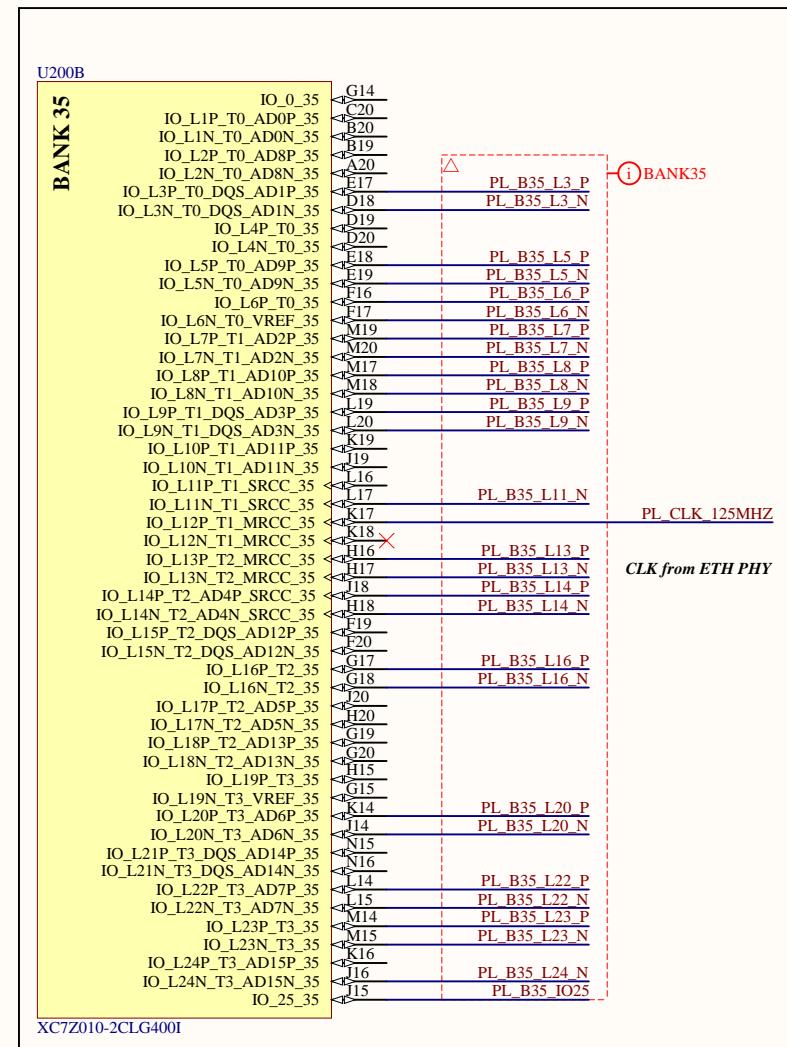
ZettBrett Reloaded

[5] Zynq Programmable Logic (PL)

Bank 34



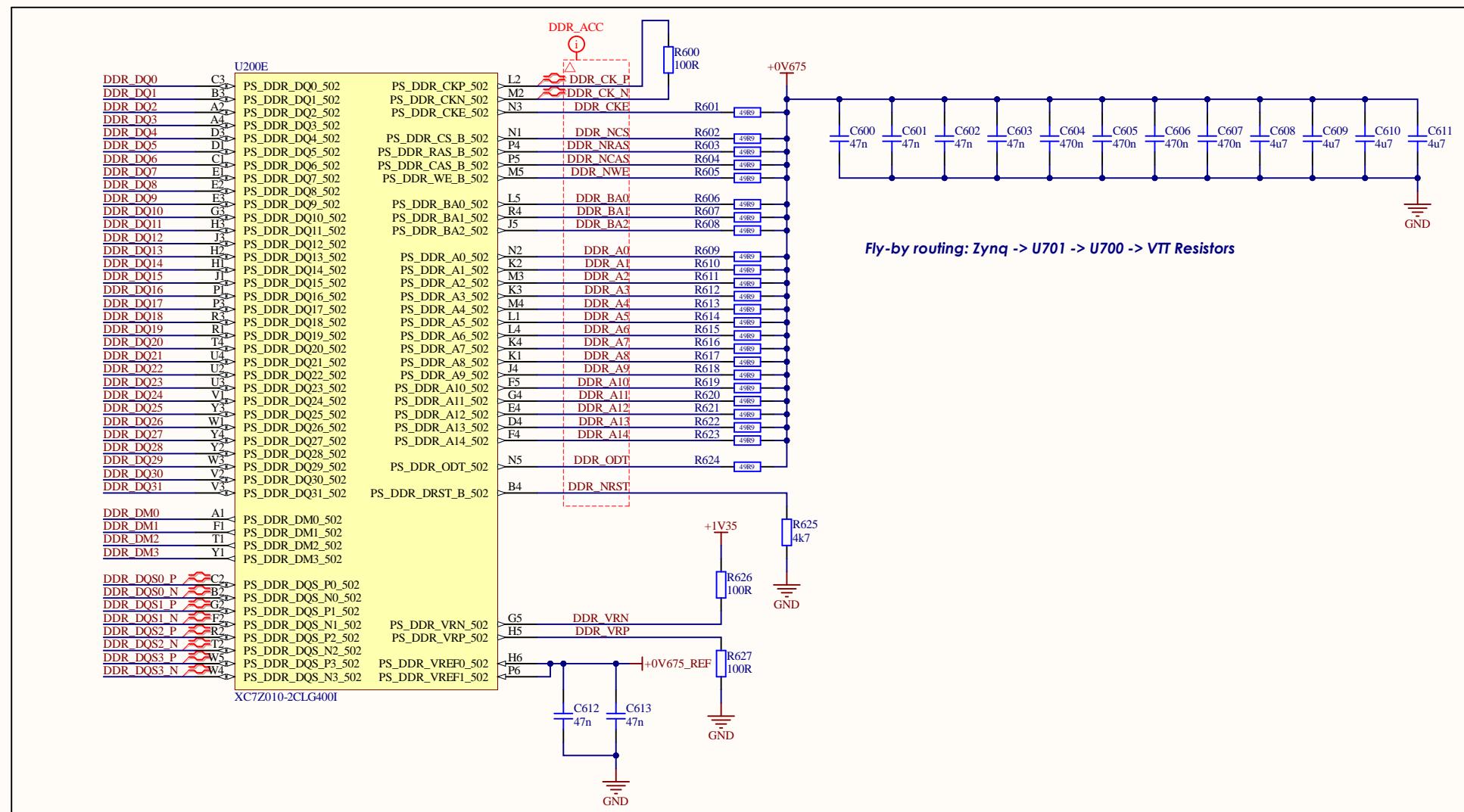
Bank 35



Zynq Programmable Logic			
DATE	REVISION	DRAWN BY	PAGE
3/23	B	PS	5/10

[6] Zynq DDR Interface & Termination

Zynq DDR Interface



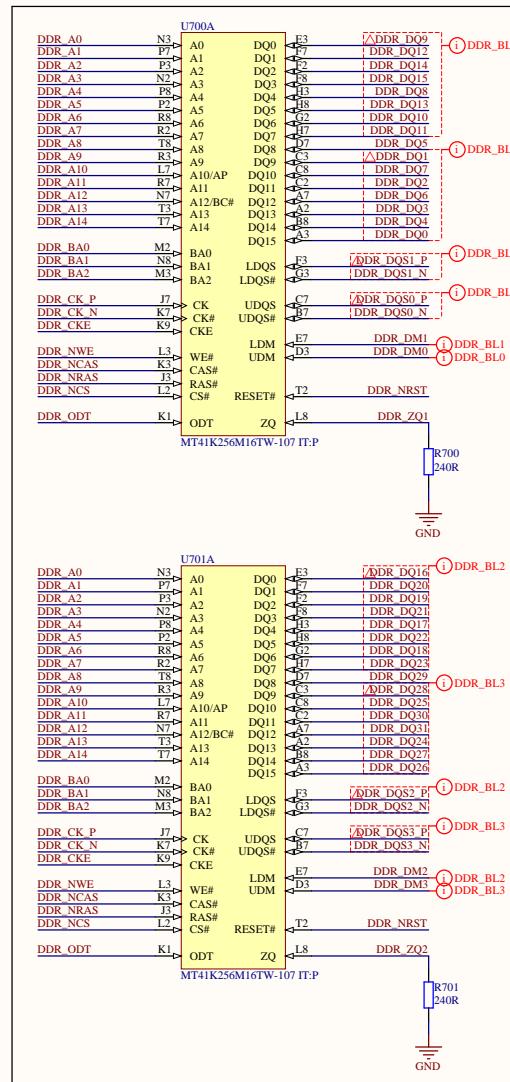
Bit/byte-lane swapping done at memory devices

TITLE			
Zynq DDR Interface			
DATE	REVISION	DRAWN BY	PAGE
3/23	B	PS	6/10

ZettBrett Reloaded

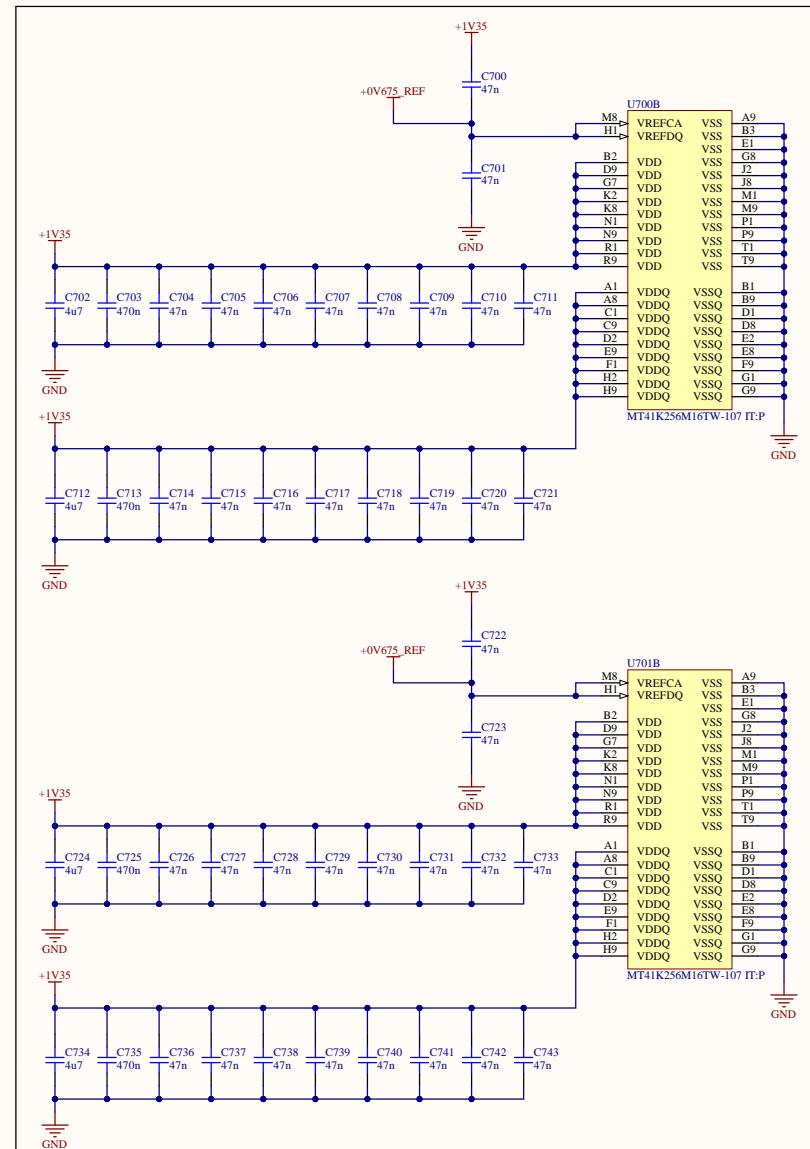
[7] 1GB DDR3L Modules

ACC & DAT Connections

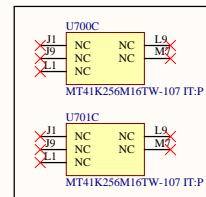


DDR_NRST pull-down, termination resistors on [6] Zynq DDR

Power and Decoupling



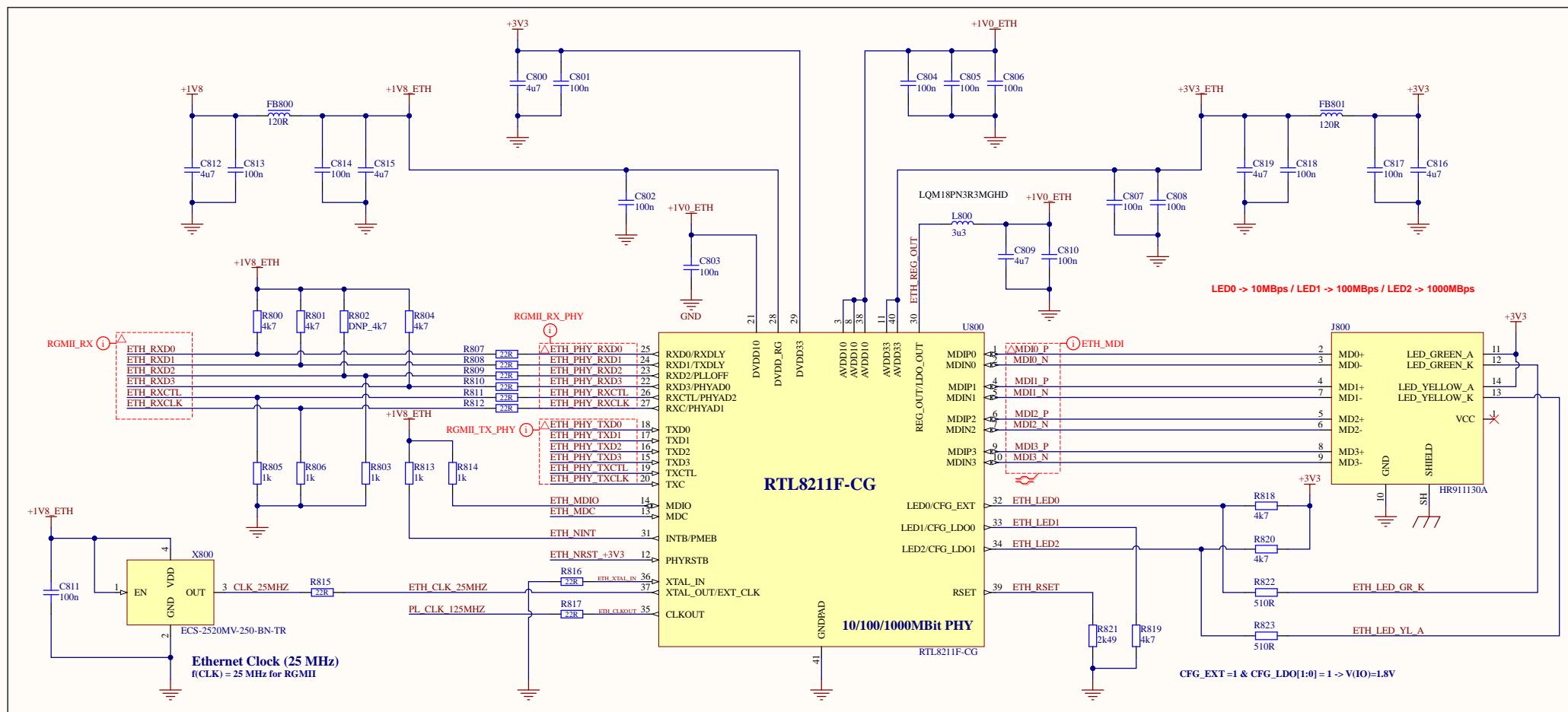
Unused Pins



ZettBrett Reloaded

[8] Gigabit Ethernet

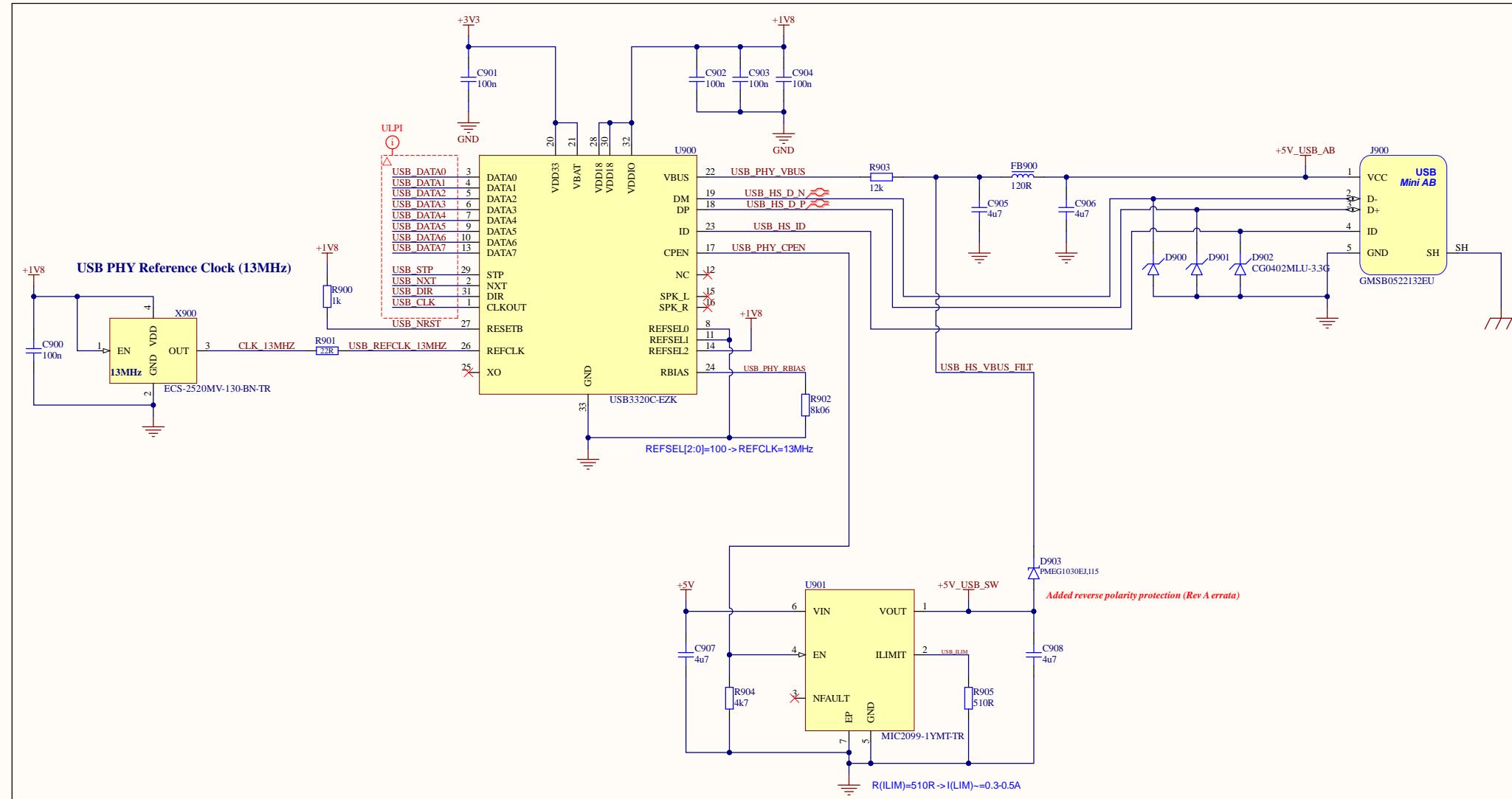
Ethernet PHY & RJ45 Connector



ZettBrett Reloaded

[9] USB 2.0 High-Speed (OTG)

USB HS PHY & Mini AB Connector

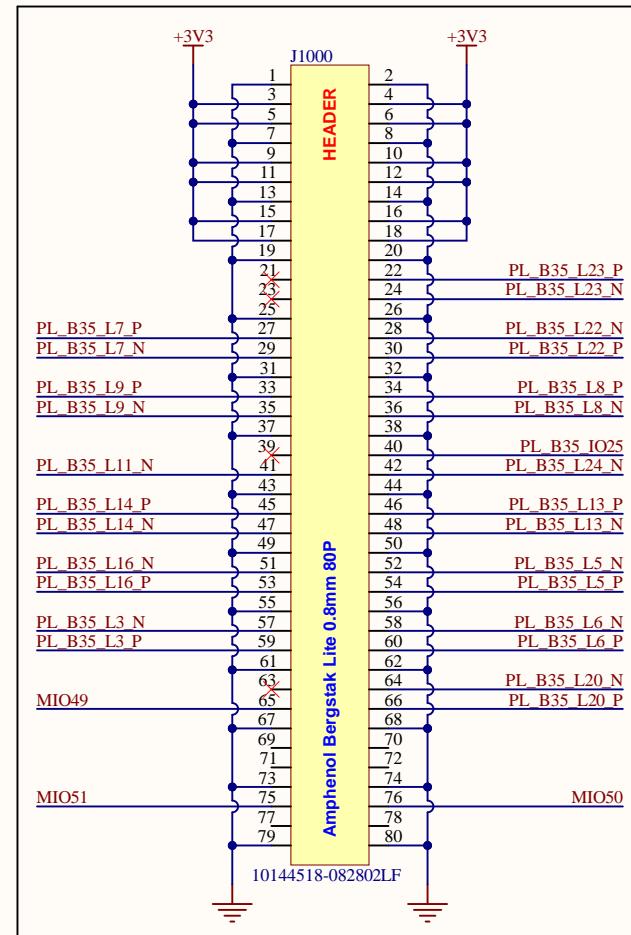


TITLE		USB 2.0 HS			WWW.PHILS-LAB.NET	
DATE	REVISION	DRAWN BY	PS	PAGE	9/10	
3/23	B		PS			

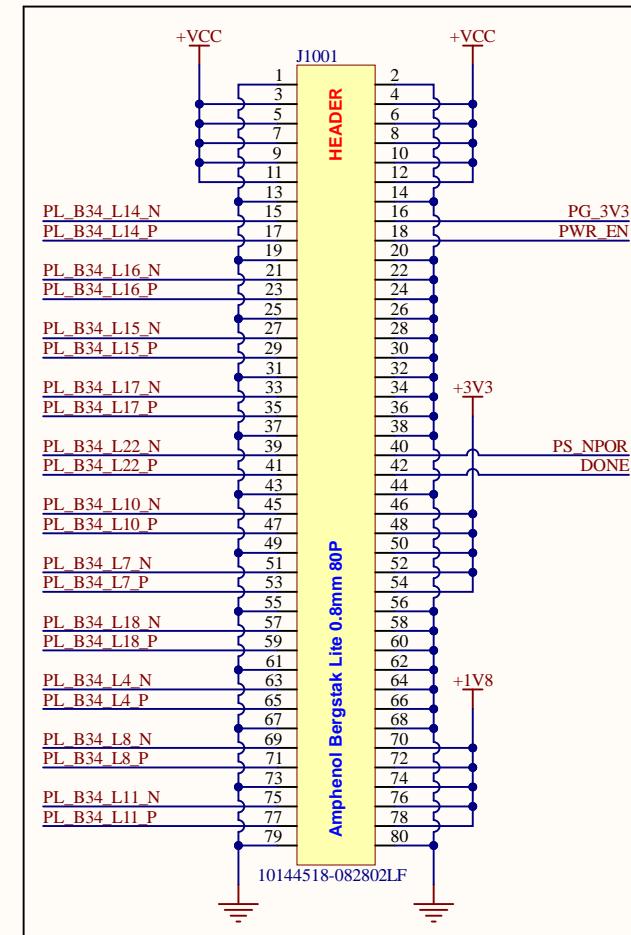
ZettBrett Reloaded

[10] Mezzanine Connectors

PS MIO & PL Bank 35 (SE)



PL Bank 34 (DIFF)



TITLE	Expansion (Mezzanine)			WWW.PHILS-LAB.NET
DATE	REVISION	DRAWN BY	PAGE	PHIL'S LAB
3/23	B	PS	10/10	

A

A

B

B

C

C

D

D