

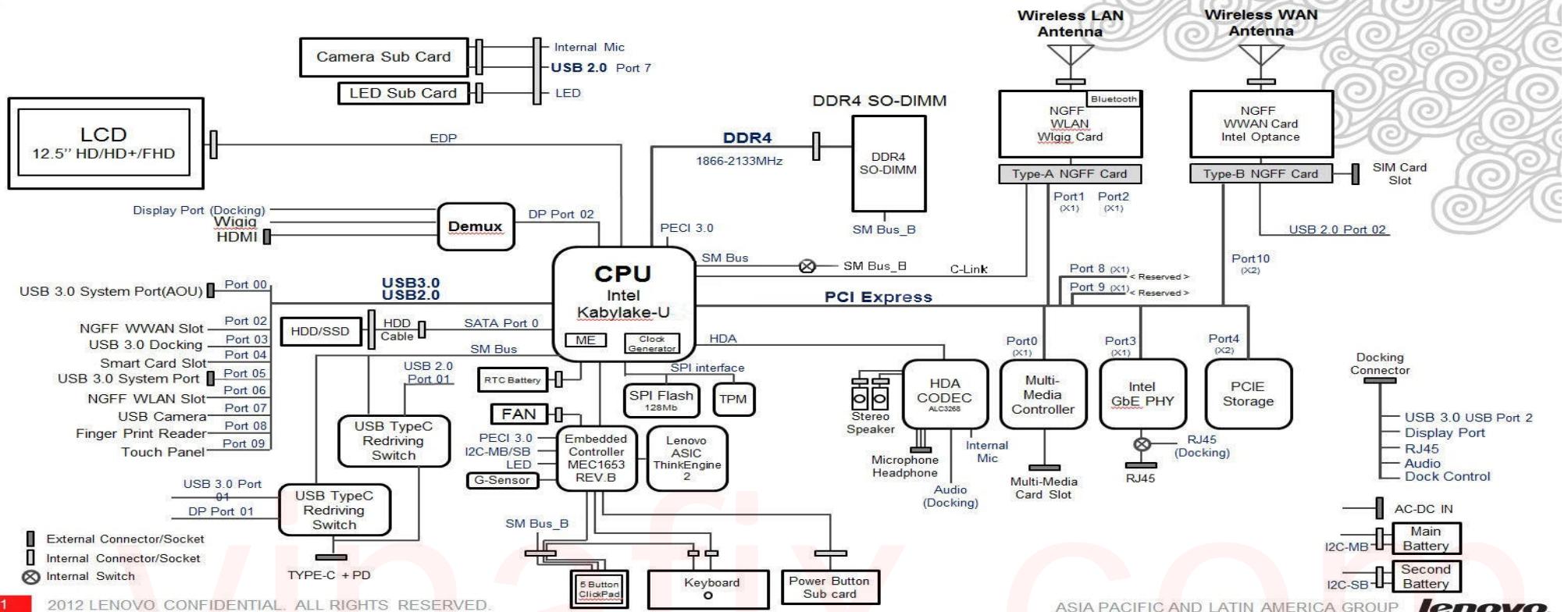
WV-4 SIT LOGIC SCHEMATICS

WV-4
6/27/2016

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020.RTC BATTERY
021.SPI FLASH
022.DDR4 SO DIMM
023.TYPE_C_CONTROLLER
024.TYPE-C_MUX
025.BLANK
026.BLANK
027.BLANK
028.DP SWITCH
029.DP DEMUX
030.BLANK
031.BLANK
032.BLANK
033.BLANK
034.BLANK
035.BLANK

036.BLANK
037.RF COMPONENT
038.LCD/LID/MIC/CAMERA/PWR SW
039.BLANK
040.HDMI CONNECTOR
041.DISPLAY PORT CONNECTOR
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043.SATA HDD CONN
044.USB POWER/CONN
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050.PCIE MINI CARD SLOT
051.MEDIA CARD CONTROLLER
052.MEDIA CARD INTERFACE
053.SMART CARD I/F
054.AUDIO ALC3245-GRT
055.AUDIO CONNECTOR
056.AUDIO JACK SENSE
057.AUDIO EXT MIC I/F
058.AUDIO SPEAKER
059.AUDIO BEEP
060.DOCKING CONNECTOR
061.MEC1653(1/3)
062.MEC1653(2/3)
063.MEC1653(3/3)
064.KEYBOARD/TRACK POINT
065.TOUCH PAD/NFC/FPR
066.BLANK
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068.G-SENSOR
069.TPM
070.SMBUS SW/LPC DEBUG PORT
071.THINK ENGINE(1/2)
072.THINK ENGINE(2/2)
073.DC-IN
074.BATTERY INPUT
075.BATTERY CHARGER(BQ25700)
076.BLANK
077.BLANK
078.DC/DC VCC5M/VCC3M(TPS51285B)
079.DC/DC IMVP8(NCP81208)
080.DC/DC CPUCORE(NCP81382)
081.DC/DC VCCGFXCORE_I(NCP81381)
082.DC/DC VCCSA(NCP81380)
083.DC/DC VCC1R0_SUS(TPS51367R)
084.BLANK
085.DC/DC VCC1R2A(TPS51716)
086.DC/DC VCC1R8_SUS(RT8068A)
087.BLANK
088.DC/DC VCC2R5A(RT8068A)
089.BLOCK DIAGRAM
090.BLANK
091.BLANK
092.LOAD SW PCH SUS/TRACK POINT
093.LOAD SW LAN
094.LOAD SW CPU
095.LOAD SW B
096.LOAD SW WWAN & WLAN
097.BLANK
098.PTH FOR SCREW HOLES
099.BLOCK DIAGRAM
100.NEC LED BOARD

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Issued Date	Deciphered Date	Rev	TITLE PAGE
2016/2/3	2015/8/10	0.3	
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Custom		Date:	Tuesday, December 20, 2016



ASIA PACIFIC AND LATIN AMERICA GROUP lenovo

Voltage Rails (O --> Means ON , X --> Means OFF)

	Power Plane			
State	VSYS	VCC3M	VCC1R2A	VCC3SW
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

EC SMBus1 address EC SMBus2 address

Device	Address	Device	Address
G-Senor (KX023)	0011 110Xb	BATTERY Charger PU101	0x12H (0001001bX)

PCH SM Bus address PCH SM Bus0 address

Device	Address	Device	Address
CH-A DDR DIMMO (J21)	1001 0000b	Intel Lan_I219	0XC8
Touch Pad	\$2C	NFC	?????

EC SMBus0 address EC SMBus7 address

Device	Address	Device	Address
Main Battery	0x16	Second Battery	0 X16

EC SMBus5 address

Device	Address
Type C controller	000B

BOM Structure Table

BOM Structure	BOM Item
I3@	Not stuff
I5@	CPU I3 KABYlake U
I5@	CPU I5 KABYlake U
I7@	CPU I7 KABYlake U
VPRO@	For VPRO part
NVPRO@	For NVPRO part
TI@	For TI TUS8546 Type C Switch
PA@	For Parade 8743 Type C Switch
ME@	ME part(connector, hole)
CONN@	ME part(connector, hole)
RF@	RF component
RF_NS@	RF reserved components
EMC_NS@	EMC reserved components
EMC@	EMC components
KABY@	For Kabylake use
SKYU@	For skylake U use
SKYI3@	CPU I3 SKYLAKE U
SKYI5@	CPU I5 SKYLAKE U
SKYI7@	CPU I7 SKYLAKE U
SKYI5_VPRO@	For I5 VPRO SKYLAKE CPU
SKYI7_VPRO@	For I7 VPRO SKYLAKE CPU
i5_VPRO@	For I5 VPRO KABYLAKE CPU
i7_VPRO@	For I7 VPRO KABYLAKE CPU

Security Classification LC Future Center Secret Data

Issued Date	2014/08/10	Deciphered Date	2015/08/10
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Title BLOCK DIAGRAM



Size Document Number

WOLVERINE4 UMA

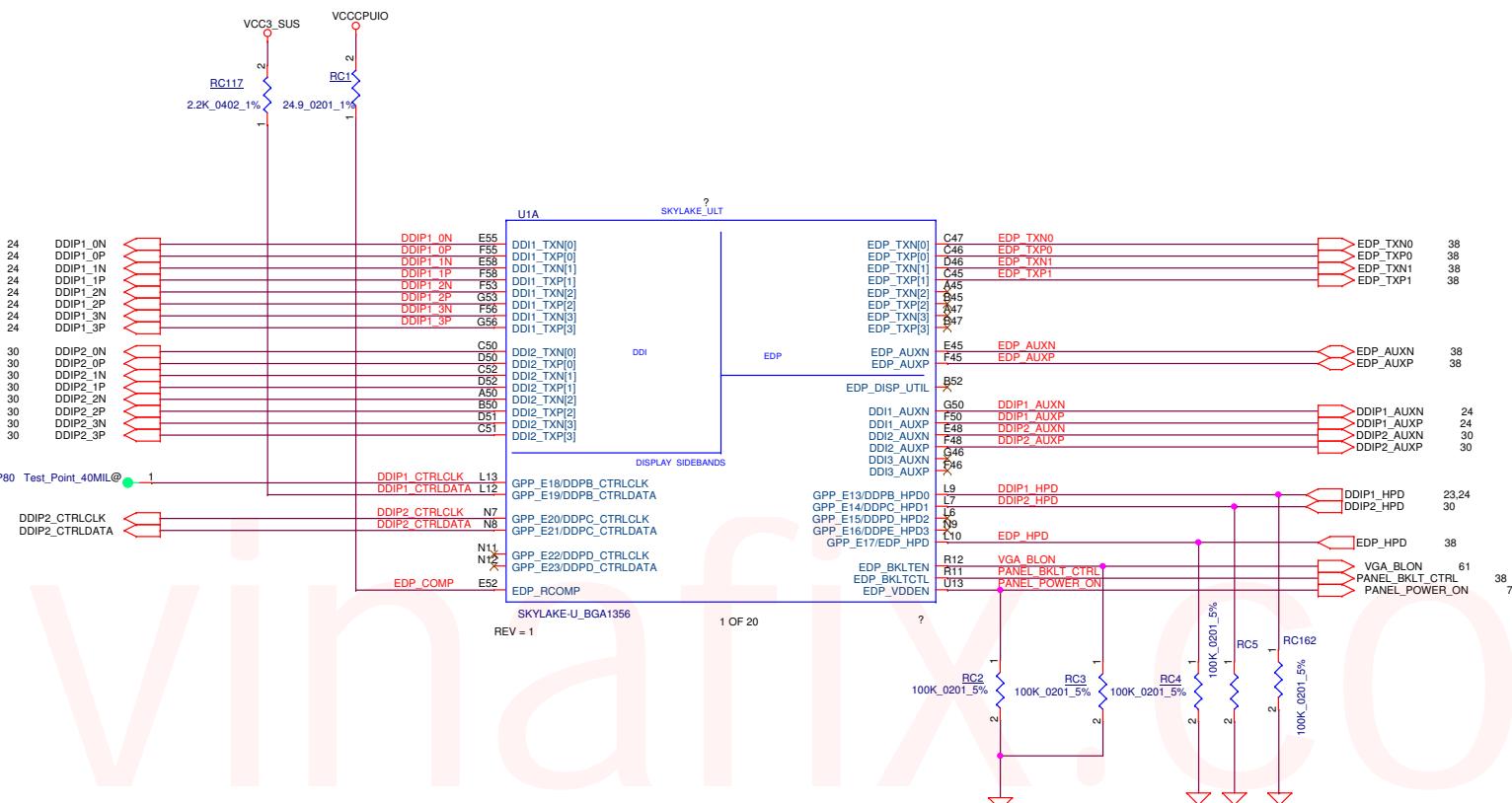
Rev. 0.3

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ZZZ
NM-B061
DAZ12F00100

Type C DDI

1 to 3 DP HUB



S IC FJ8067702739738 SR2ZW H0 2.4G 01 I, A.5
SA000080720
I3@



S IC FJ8067702739739 SR2ZU H0 2.5G 01 I, A.4
SA000080320
I5@



S IC FJ8067702739740 SR2ZV H0 2.7G 01 I, A.4
SA000080420
I7@



S IC FJ8067702739633 SR340 H0 2.6G 01 I, A.3
SA000086M10
I5 VPRO@



S IC FJ8067702739628 SR33Z H0 2.8G 01 I, A.3
SA000086N10
I7 VPRO@



S IC FJ8066201931106 QLB3 D1 2G BGA 1356, A.3
SA000082E20
SKY13@



S IC FJ8066201930409 SR2EY D1 2.3G 01 I, A.3
SA00007GP30
SKY15@



S IC FJ8066201930408 SR2EZ D1 2.5G 01 I, A.3
SA00007GM30
SKY17@

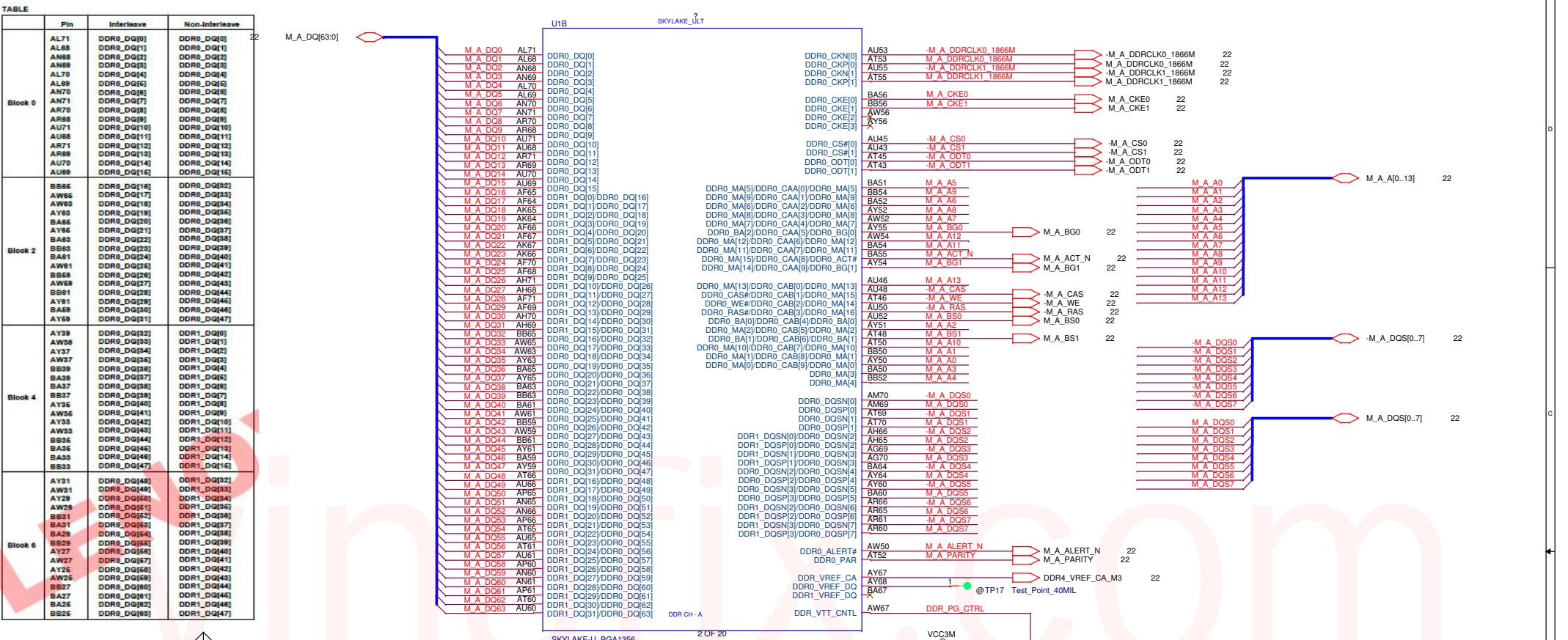


S IC FJ8066201924931 SR2F0 D1 2.4G BGA 1356 01 I, A.3
SA00007GN20
SKY15 VPRO@



S IC FJ8066201924950 SR2F1 D1 2.6G 01 I, A.5
SA00007GL30
SKY17 VPRO@

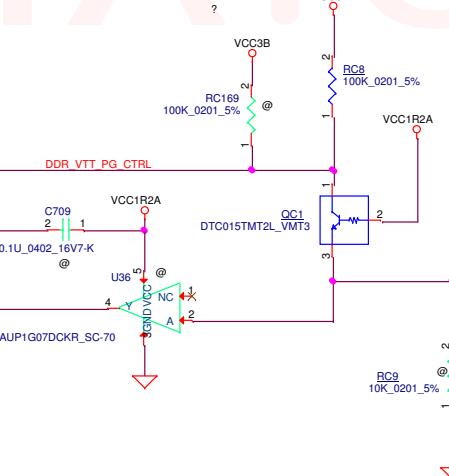
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TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

LOGIC



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	2015/08/10

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TABLE

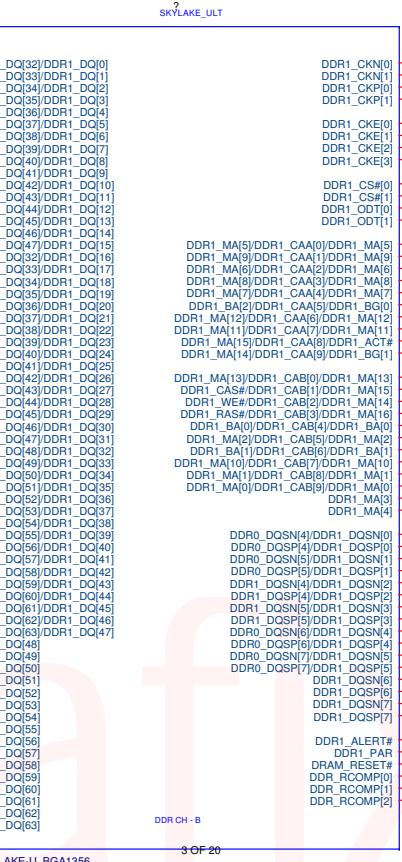
Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY51	DDR0_MA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[4]	DDR0_BA[0]
AY52	DDR0_BA[0]	DDR0_CAB[5]	DDR0_MA[2]
AY51	DDR0_BA[2]	DDR0_CAB[6]	DDR0_BA[1]
AT48	DDR0_BA[1]	DDR0_CAB[7]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[8]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[9]	DDR0_MA[1]
AY50	DDR0_MA[0]	Not Used	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

TABLE

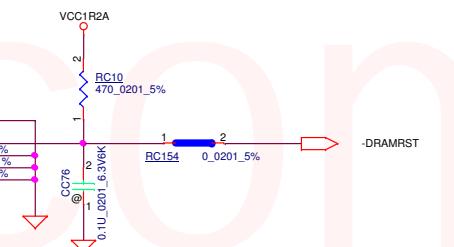
Title	Document Number	Rev
CPU(2/16) : DDR4		0.3
LCFC	WOLVERINE4 UMA	

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TABLE			
	Pin	Interleave	Non-Interleave
Block 1	AF65 AF64 AK65 AK64 AF66 AF67 AK67 AK68 AF68 AF70 AH71 AH72 AF71 AF72 AF69 AH73 AH74 AH75 AH76 AH77 AH78 AH79 AH80	DDR1_DQ[0] DDR1_DQ[1] DDR1_DQ[2] DDR1_DQ[3] DDR1_DQ[4] DDR1_DQ[5] DDR1_DQ[6] DDR1_DQ[7] DDR1_DQ[8] DDR1_DQ[9] DDR1_DQ[10] DDR1_DQ[11] DDR1_DQ[12] DDR1_DQ[13] DDR1_DQ[14] DDR1_DQ[15]	DDR0_DQ[18] DDR0_DQ[17] DDR0_DQ[16] DDR0_DQ[15] DDR0_DQ[20] DDR0_DQ[21] DDR0_DQ[22] DDR0_DQ[23] DDR0_DQ[24] DDR0_DQ[25] DDR0_DQ[26] DDR0_DQ[27] DDR0_DQ[28] DDR0_DQ[29] DDR0_DQ[30] DDR0_DQ[31]
Block 3	AT68 AU68 AP66 AN65 AN66 AP68 AT66 AU65 AP65 AU61 AP61 AN60 AN61 AP61 AT69 AU69	DDR1_DQ[16] DDR1_DQ[17] DDR1_DQ[18] DDR1_DQ[19] DDR1_DQ[21] DDR1_DQ[22] DDR1_DQ[23] DDR1_DQ[24] DDR1_DQ[25] DDR1_DQ[26] DDR1_DQ[27] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[30] DDR1_DQ[31]	DDR0_DQ[48] DDR0_DQ[49] DDR0_DQ[50] DDR0_DQ[51] DDR0_DQ[52] DDR0_DQ[53] DDR0_DQ[54] DDR0_DQ[55] DDR0_DQ[56] DDR0_DQ[57] DDR0_DQ[58] DDR0_DQ[59] DDR0_DQ[60] DDR0_DQ[61]
Block 6	AU40 AT40 AT37 AT37 AR40 AP40 AP37 AR37 AT33 AU33 AU30 AT30 AR33 AP33 AR30 AP30	DDR1_DQ[32] DDR1_DQ[33] DDR1_DQ[34] DDR1_DQ[35] DDR1_DQ[36] DDR1_DQ[37] DDR1_DQ[38] DDR1_DQ[39] DDR1_DQ[40] DDR1_DQ[41] DDR1_DQ[42] DDR1_DQ[43] DDR1_DQ[44] DDR1_DQ[45] DDR1_DQ[46]	DDR1_DQ[18] DDR1_DQ[17] DDR1_DQ[18] DDR1_DQ[19] DDR1_DQ[20] DDR1_DQ[21] DDR1_DQ[22] DDR1_DQ[23] DDR1_DQ[24] DDR1_DQ[25] DDR1_DQ[26] DDR1_DQ[27] DDR1_DQ[28] DDR1_DQ[29] DDR1_DQ[30]
Block 7	AU27 AT27 AT26 AU26 AN27 AN26 AP26 AT22 AU22 AU21 AU20 AN22 AP22 AP21 AN21	DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[50] DDR1_DQ[51] DDR1_DQ[52] DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[55] DDR1_DQ[56] DDR1_DQ[57] DDR1_DQ[58] DDR1_DQ[59] DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[62]	DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[51] DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[55] DDR1_DQ[56] DDR1_DQ[57] DDR1_DQ[58] DDR1_DQ[59] DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[63]



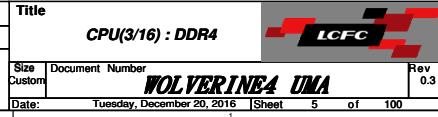
Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]



	Pin	Interleave	Non-Interleave
Block 1	AH66 AH65 AG69 AG70	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]
Block 3	AR66 AR65 AR61 AR60	DDR1_DQSN[2] DDR1_DQSP[2] DDR1_DQSN[3] DDR1_DQSP[3]	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]
Block 5	AT38 AR38 AT32 AR32	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]	DDR1_DQSN[2] DDR1_DQSP[2] DDR1_DQSN[3] DDR1_DQSP[3]
Block 7	AR25 AR27 AR22 AR21	DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]	DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]

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Update description

```
For DCI debug
RC113 OP, RC148 short(XDP_TDO-> PCH_TDO)
RC138 OP, RC145 short(XDP_TMS-> PCH_TMS)
RC137 OP, RC147 short(XDP_TRST-> PCH_TRST)
RC142 OP, RC143 short(XDP_TCK0-> JTAGX)
RC139 OP, RC146 short(XDP_TDI-> PCH_TDI)
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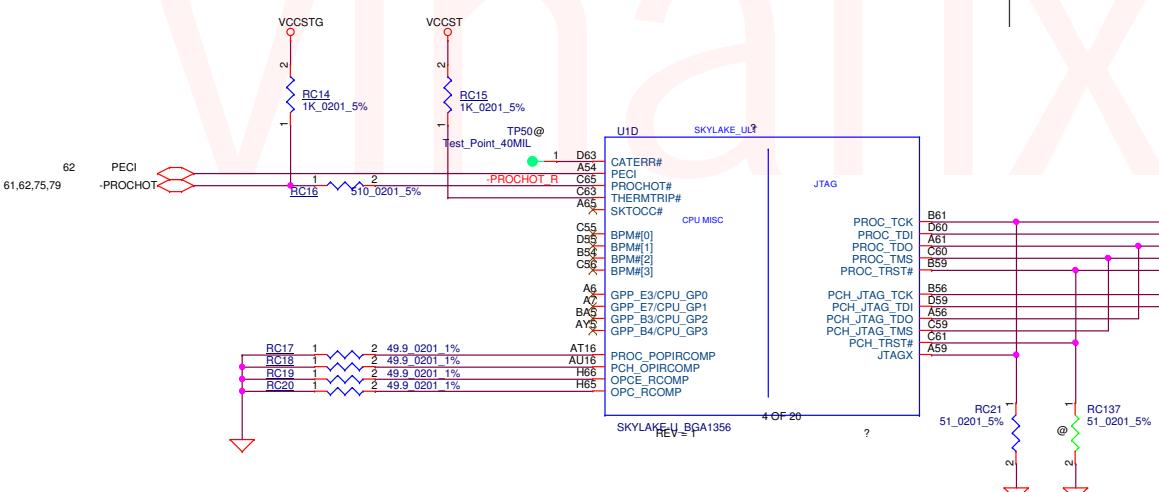
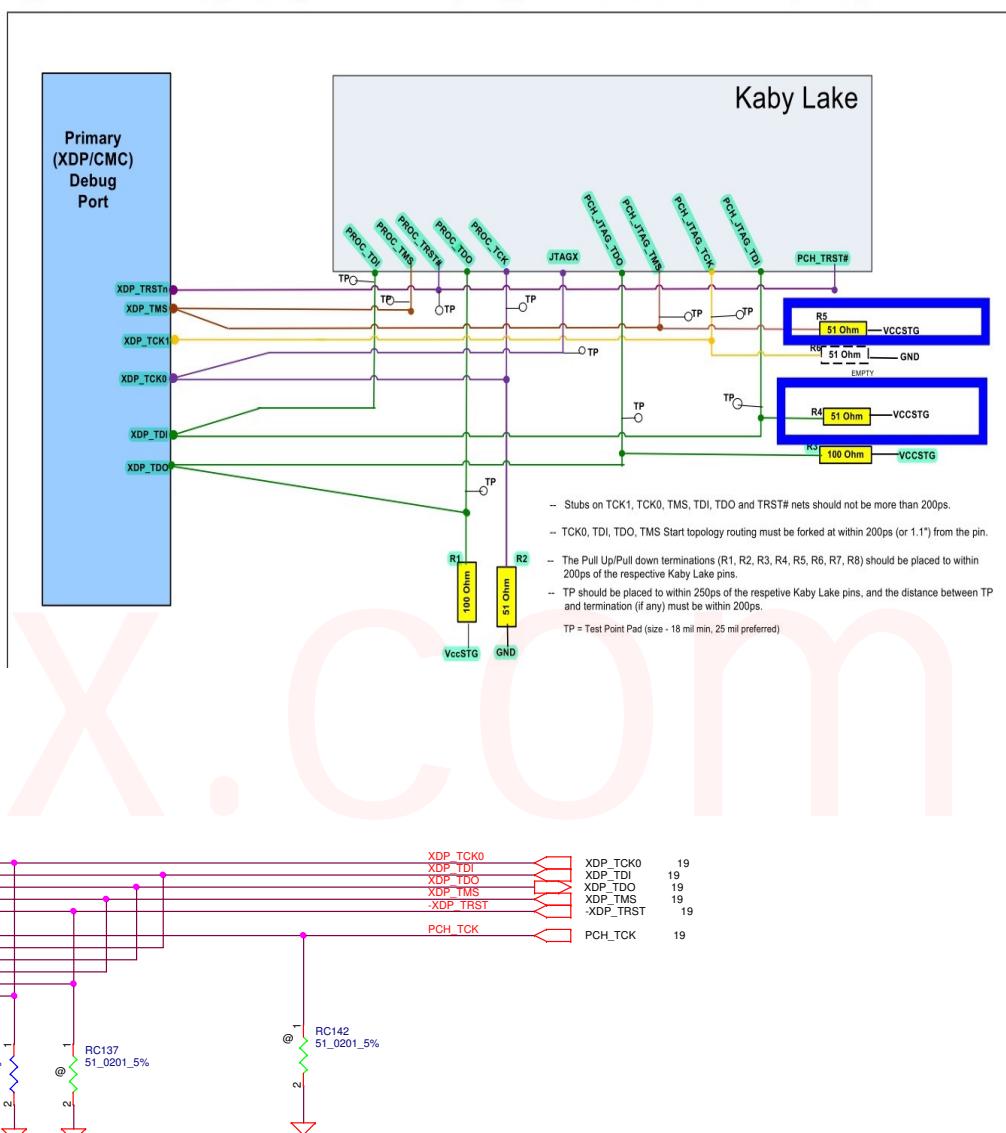


Figure 43-1. Primary Debug Port-JTAG Topology for Dual Scan Chain Only Design



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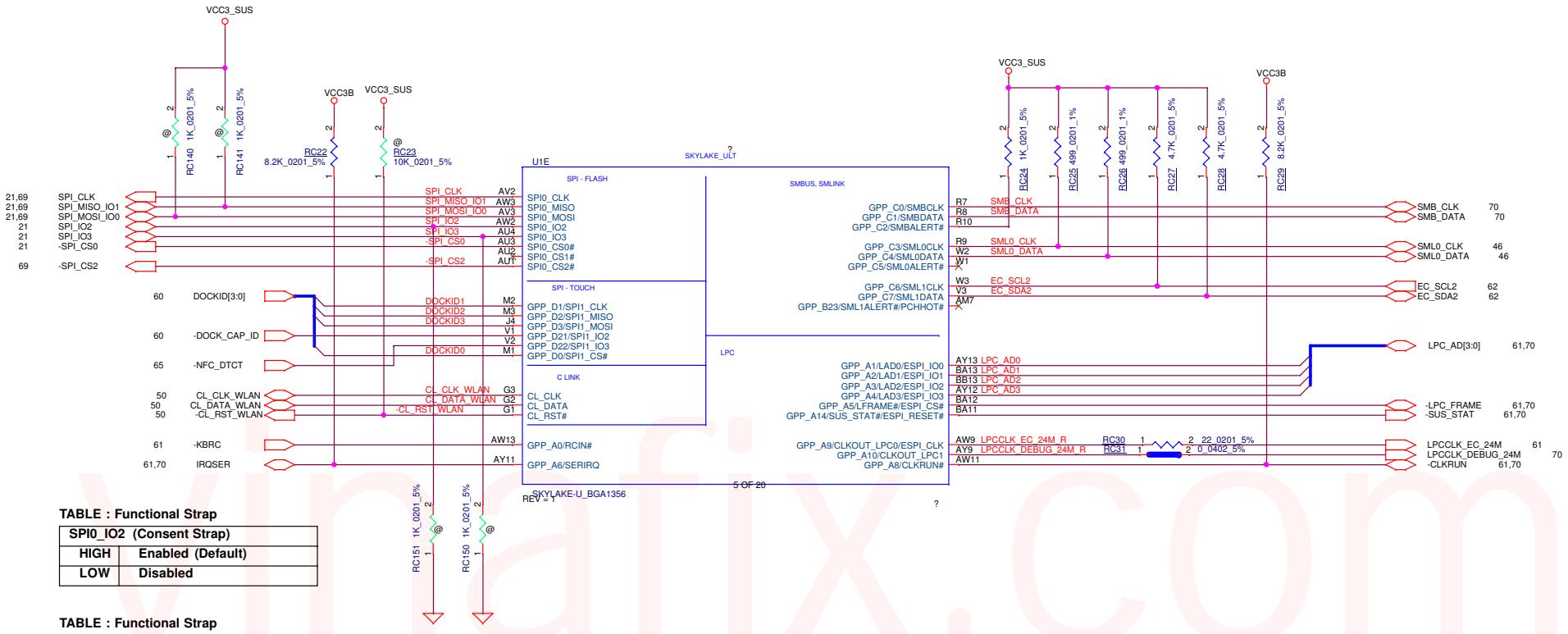


TABLE : Functional Strap	
SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

TABLE : Functional Strap	
SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

TABLE : Functional Strap	
GPP_C5_SMLOALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

TABLE : Functional Strap	
GPP_C2_SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

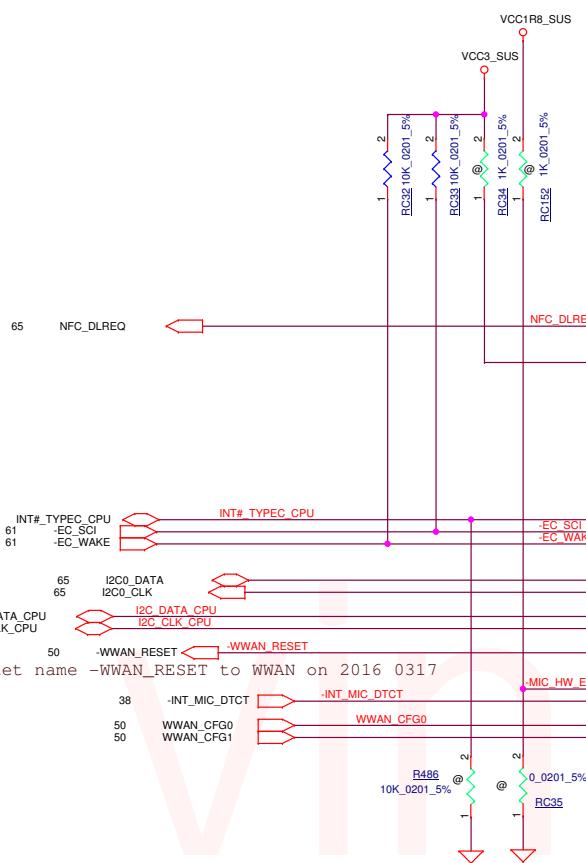
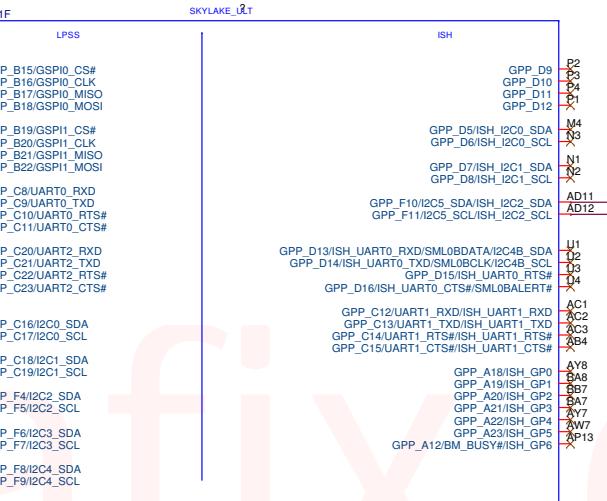


TABLE : Functional Strap

GPP_B18/GSPI0 MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)



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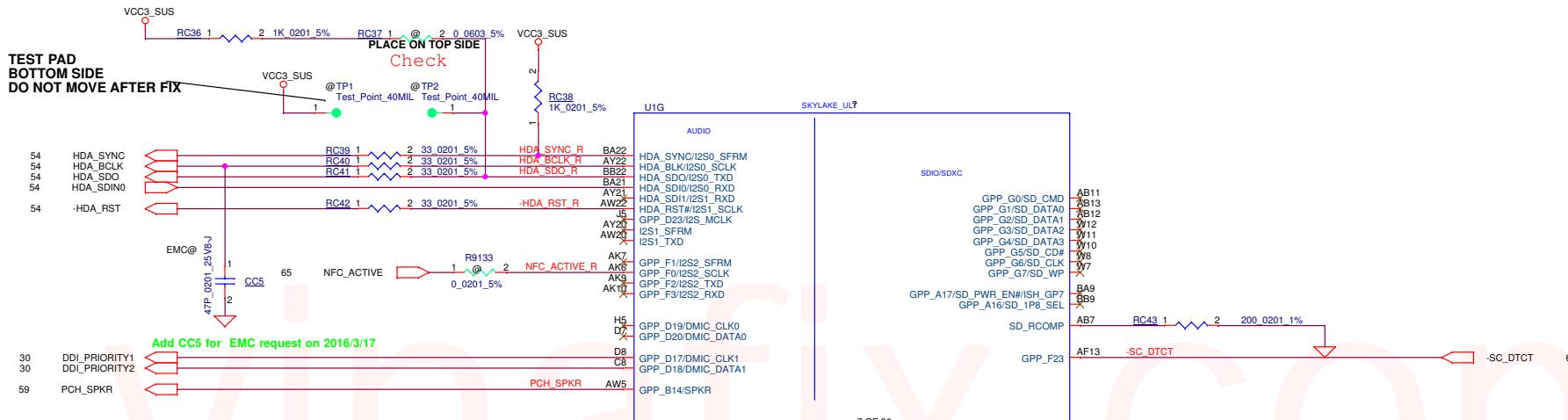
Title
CPU(6/16) : LPSS/ISH



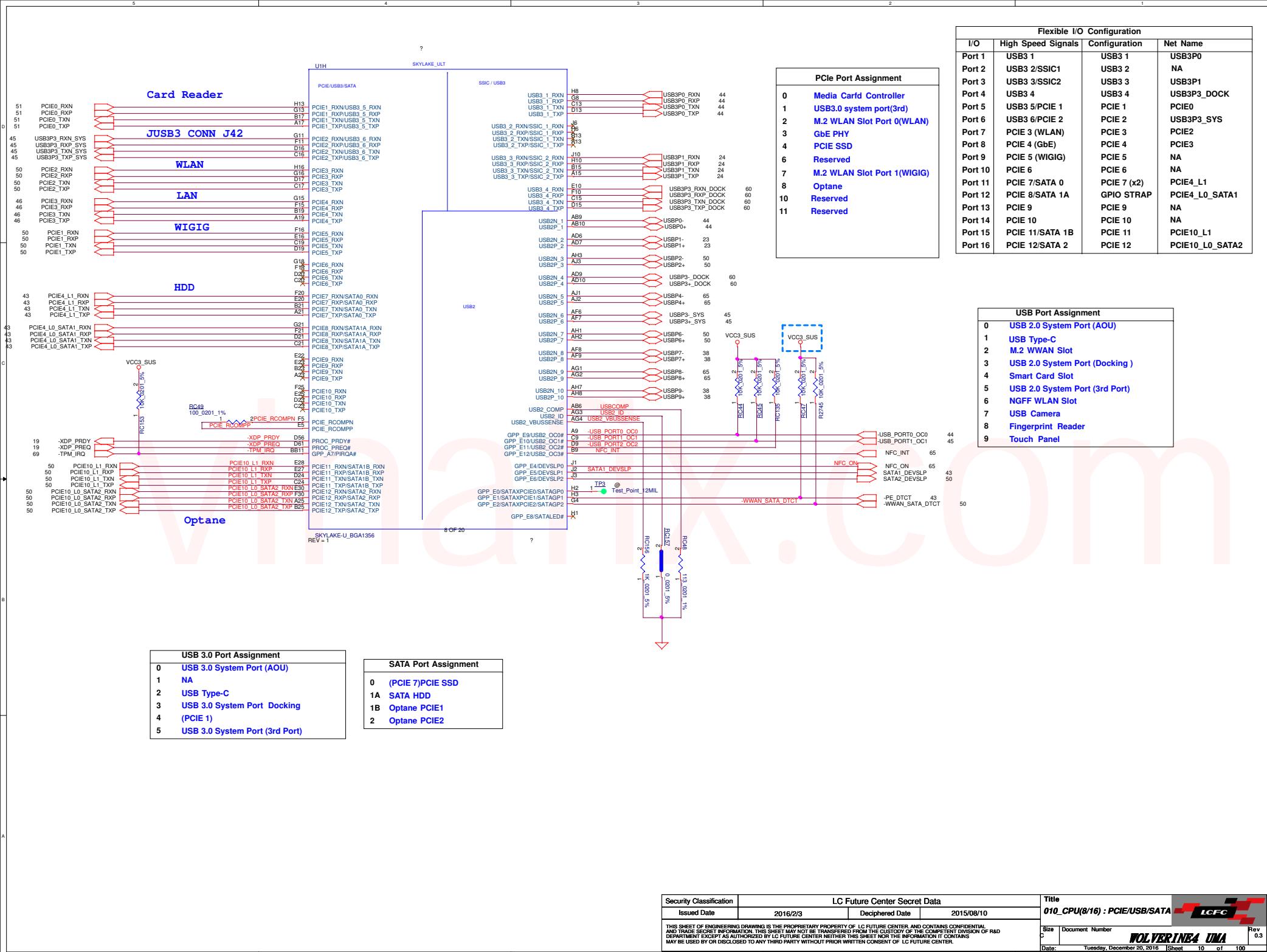
Size Custom Document Number WOLVERINE4_UMA Rev 0.3
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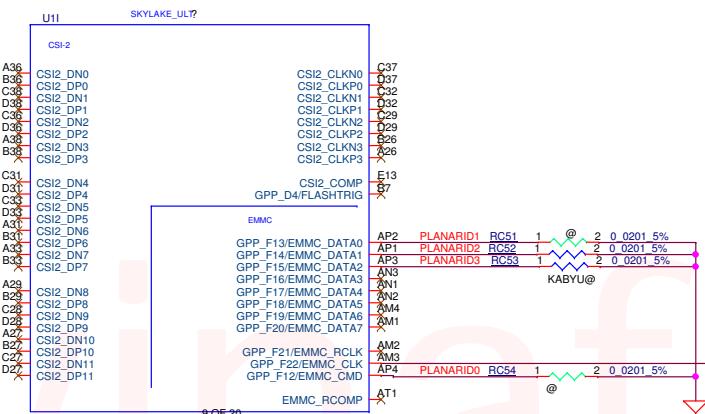
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HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

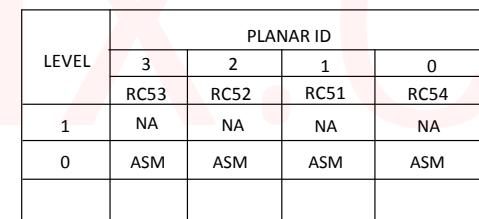


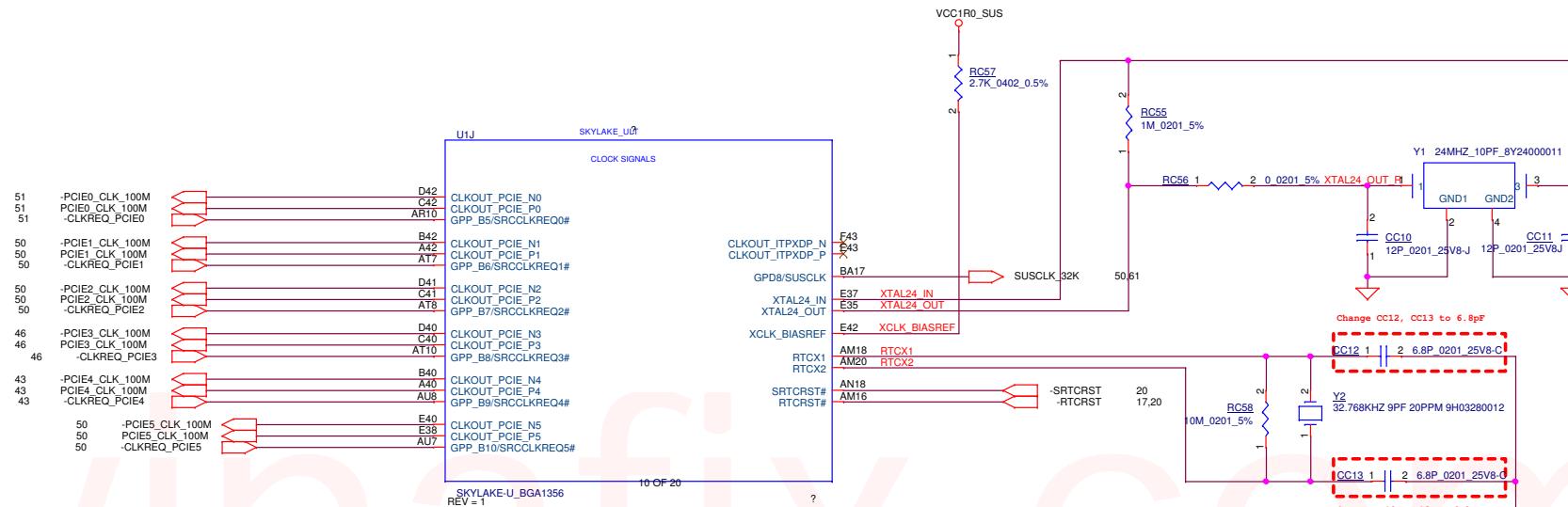
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Kabylake	PLANAR ID[3..0]	SKYLAKE	PLANAR ID[3..0]
SDV	0000		
FVT	0001		
SIT	0010		
SVT	0011	SIT	1011





Y2 32.768KHZ

Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
KDS	50K ohm Max	SJ100069400	1TJF090DJ1A000B	50K ohm Max
SEIKO	50K ohm Max	SJ10000IX00	X1A000141000200	50K ohm Max
TXC	50K ohm Max	SJ10000J900	9H3280012	50K ohm Max

Y1 24MHZ

Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
TXC	50 ohm Max	SJ10000HH0J	8Y24000011	50 ohm Max
KDS	50 ohm Max	SJ10000P100	1ZZHAE24000BC0D	50 ohm Max

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Title

CPU(10/16) : CLOCK SIGNALS

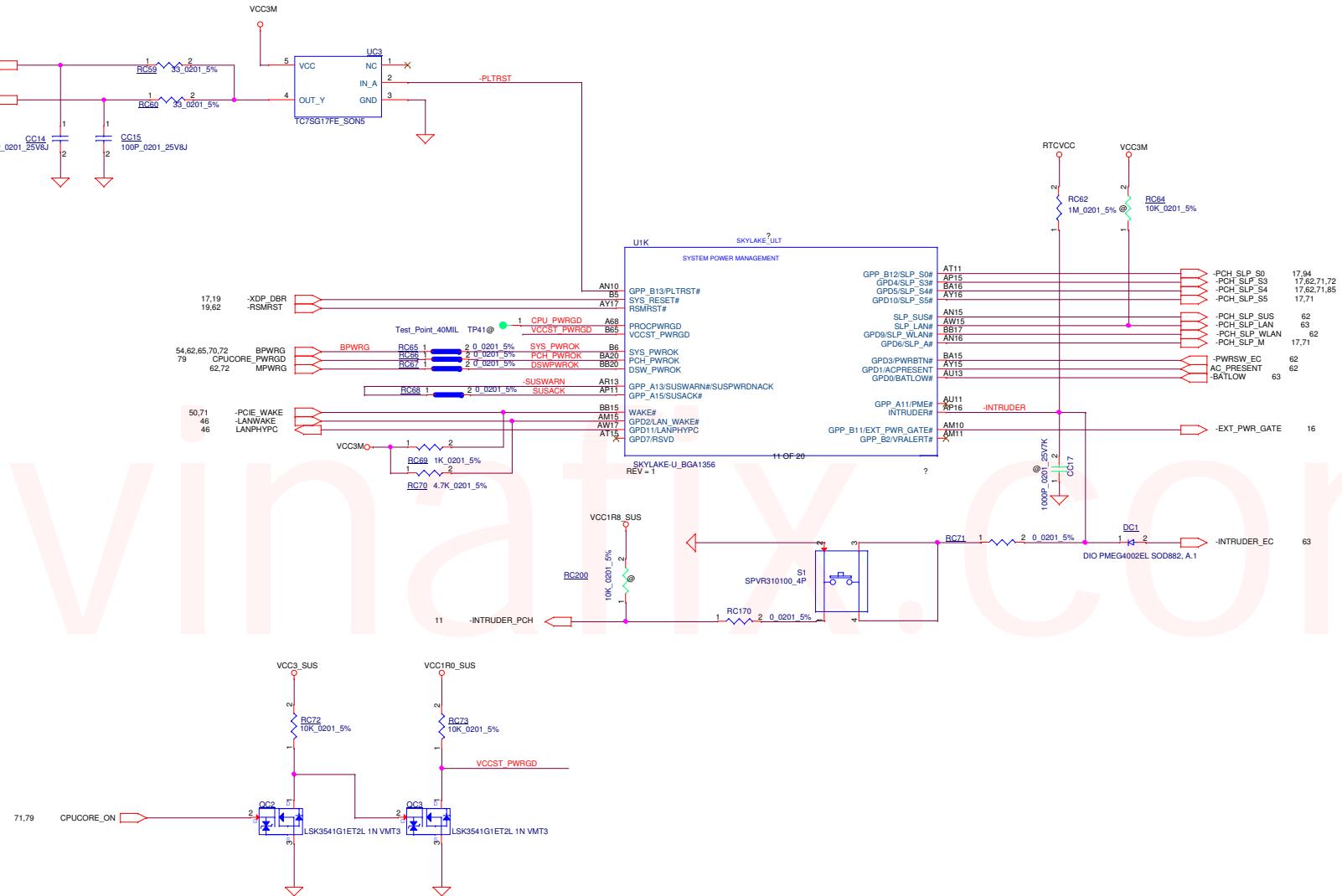


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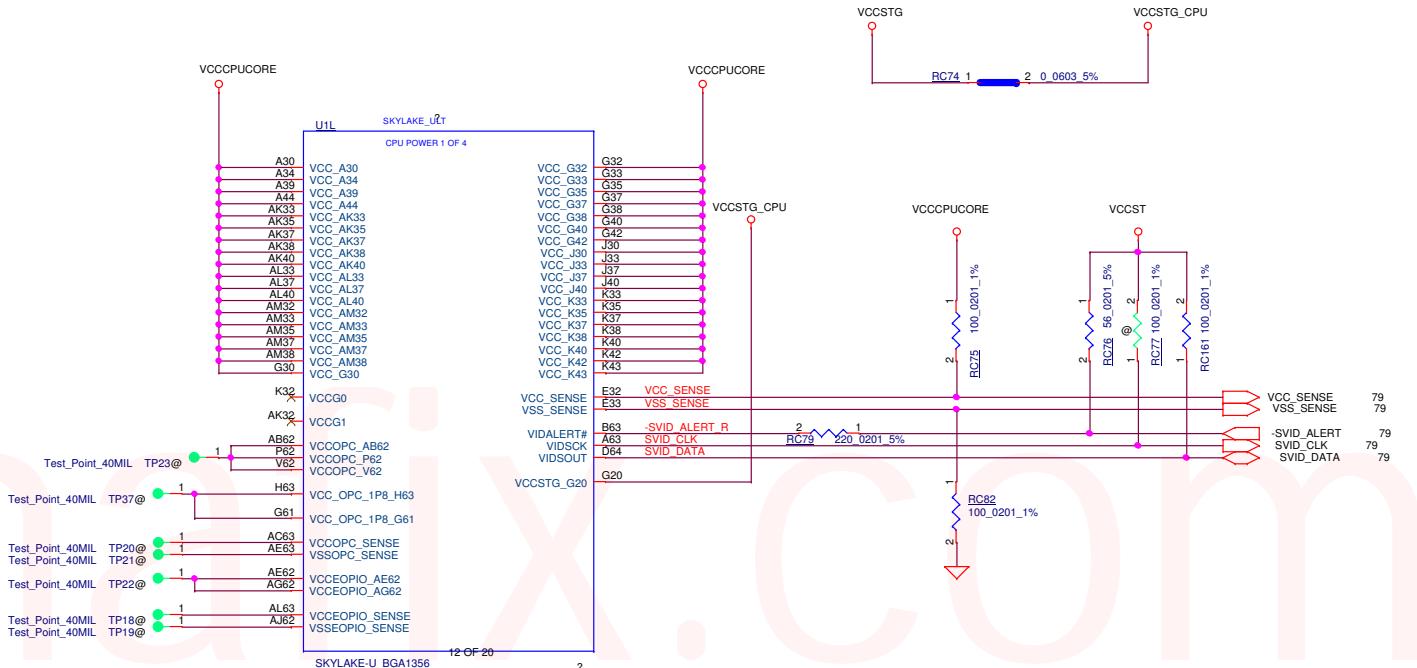
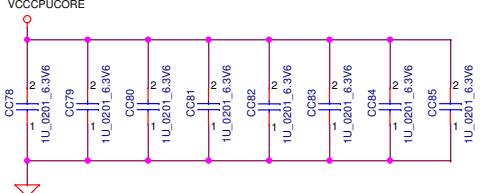
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Title

CPU(12/16) : CPU POWER

LCFC

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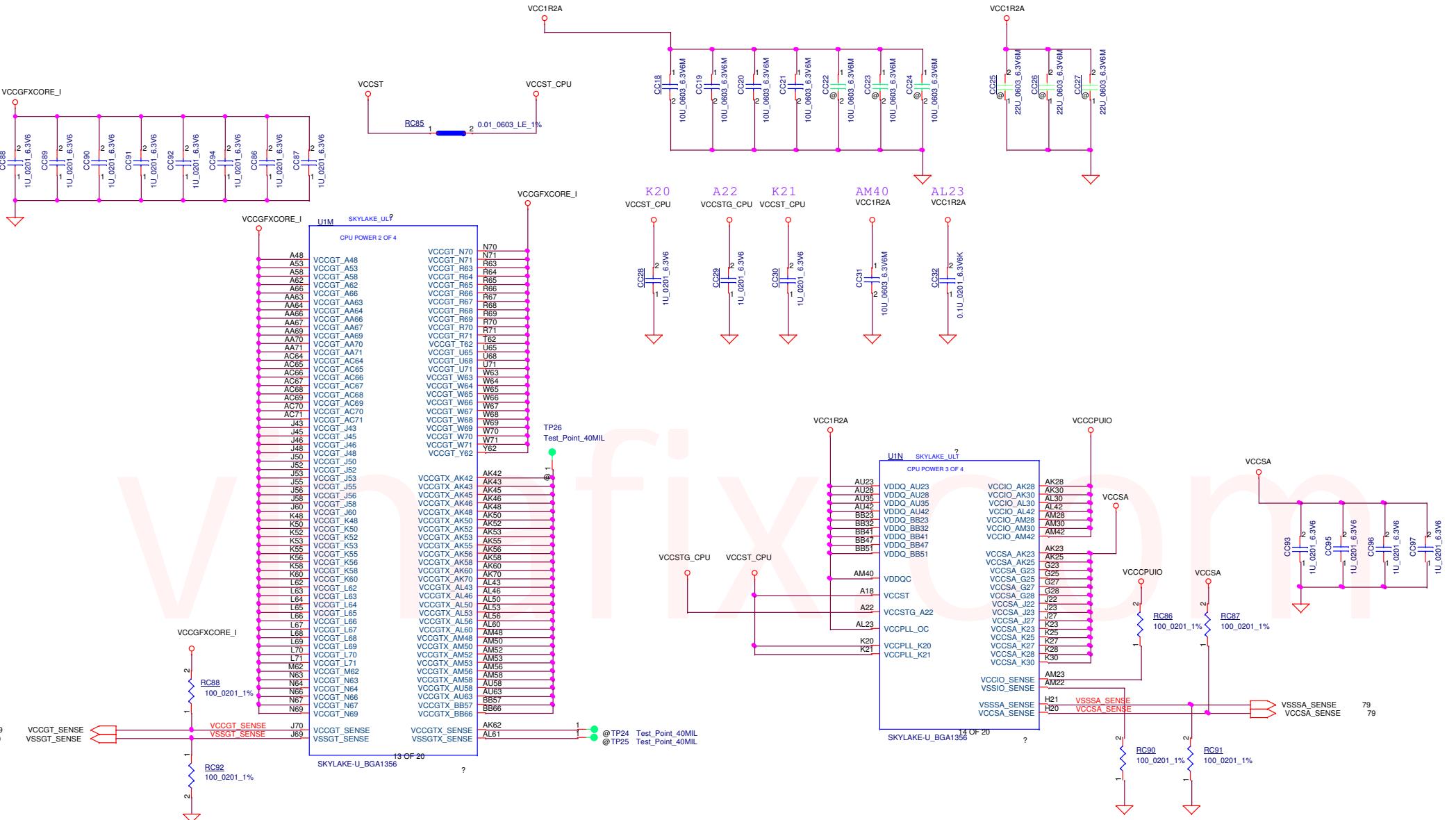
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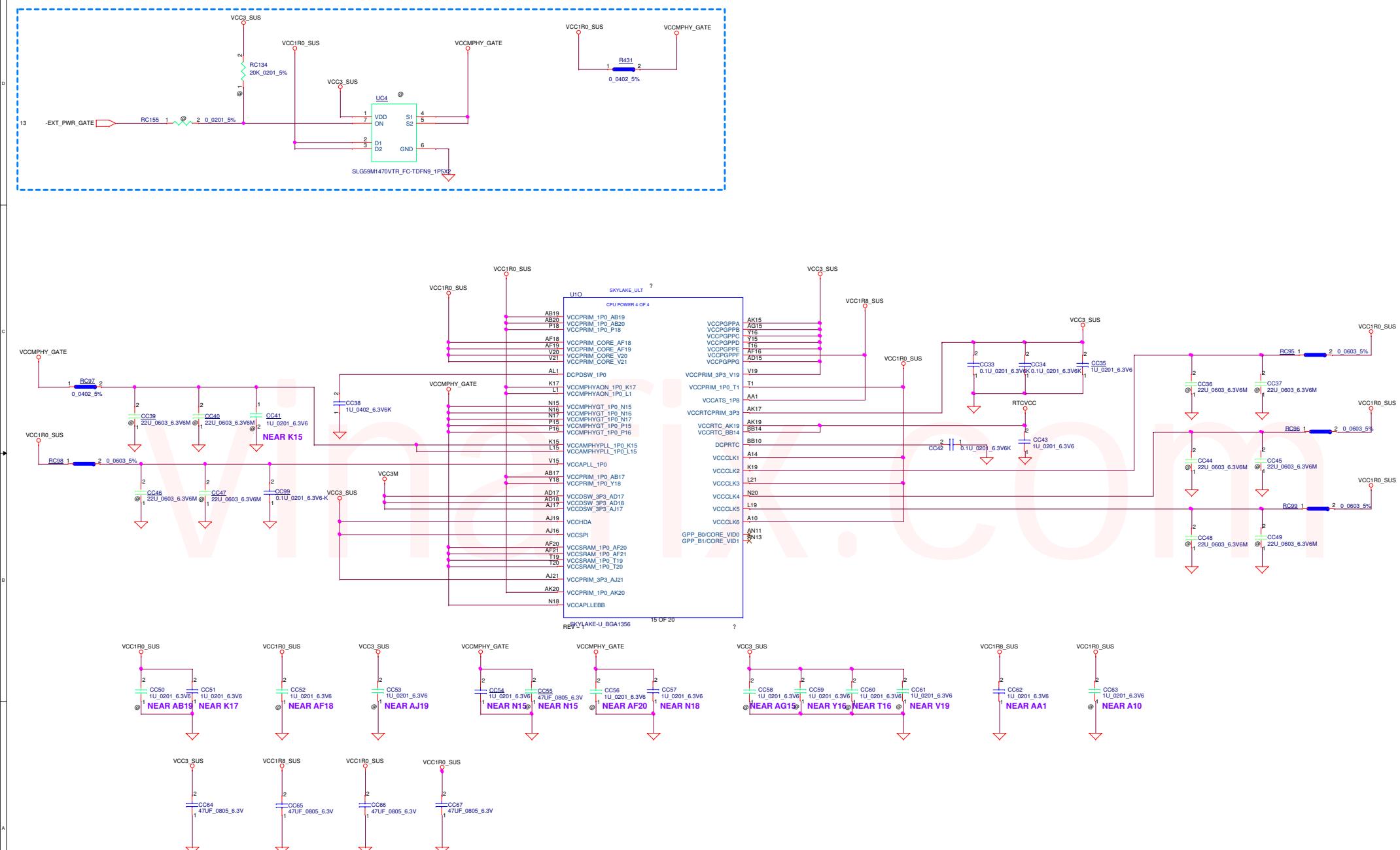
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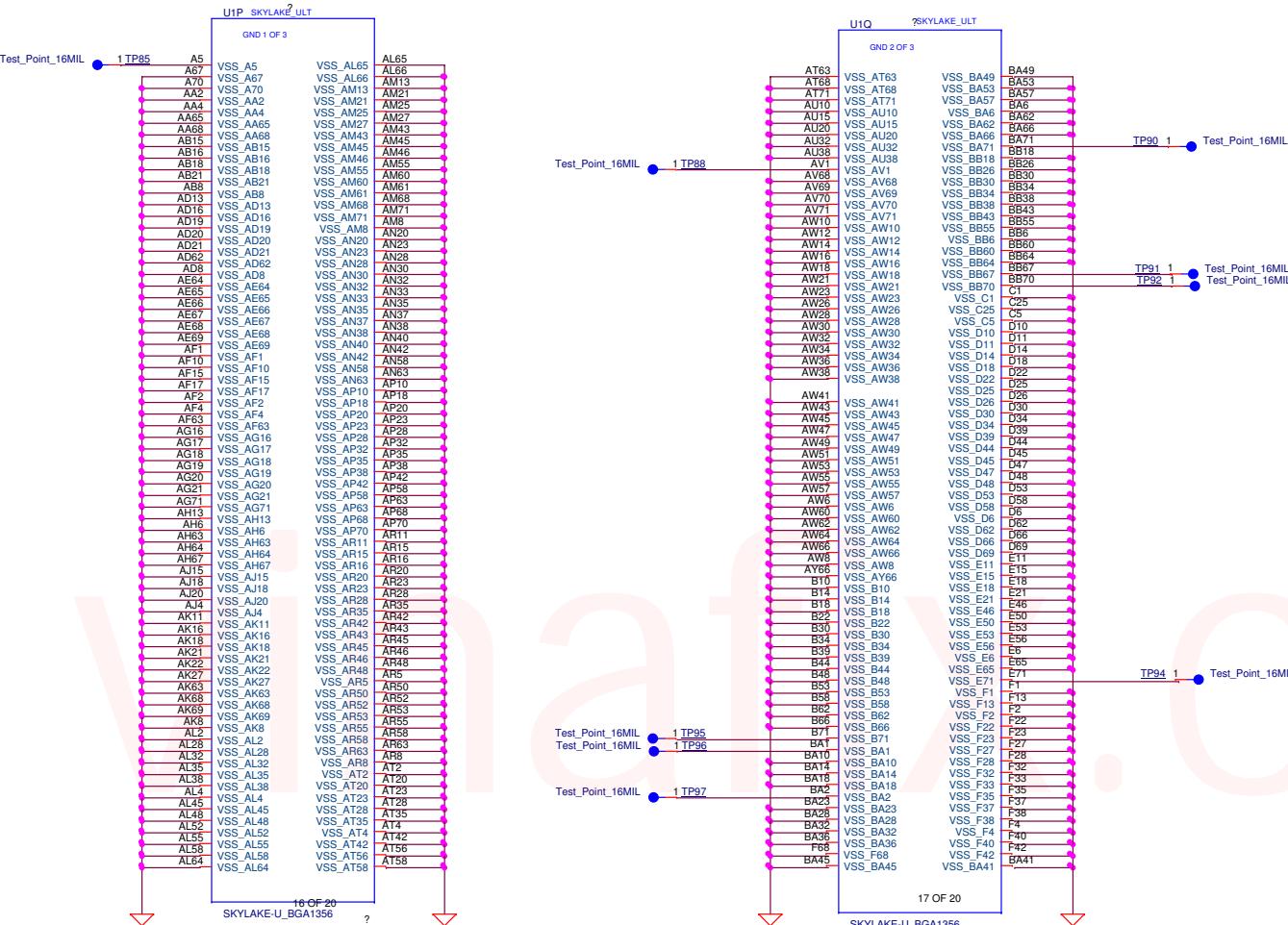


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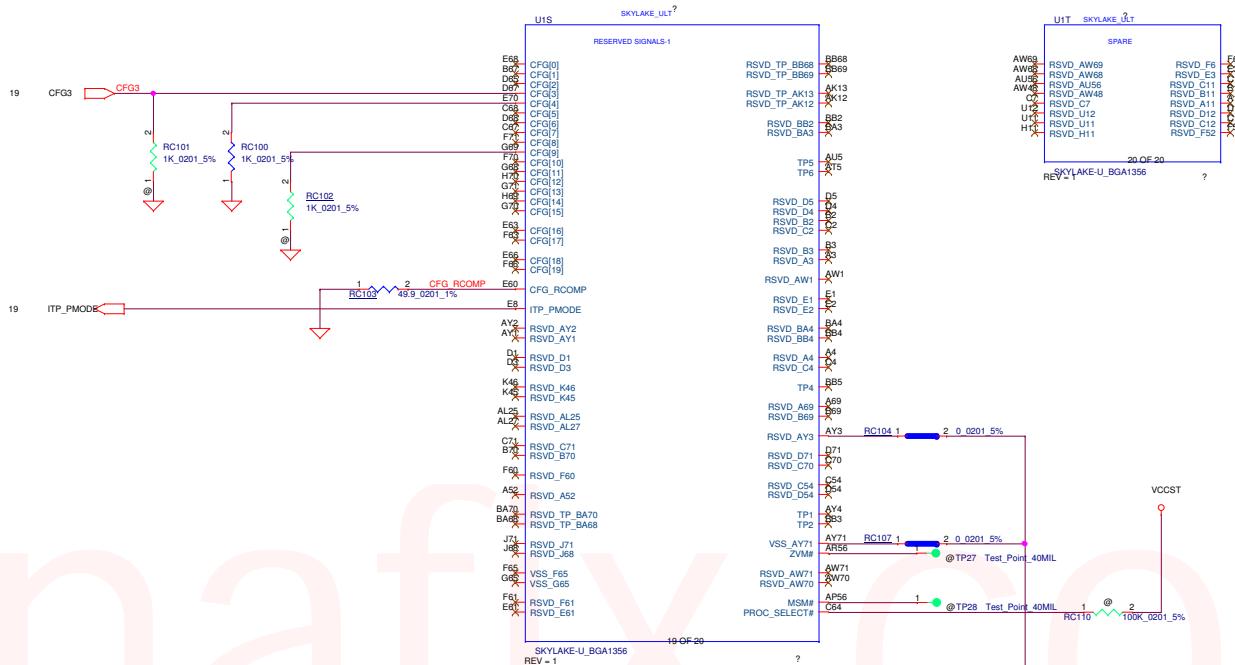
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CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM



TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall
CFG4 : eDP Enable
1 : Disabled
0 : Enabled
CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled



-XDP_DBR Pull Up 10k to VCC3_SUS on 2016/3/17

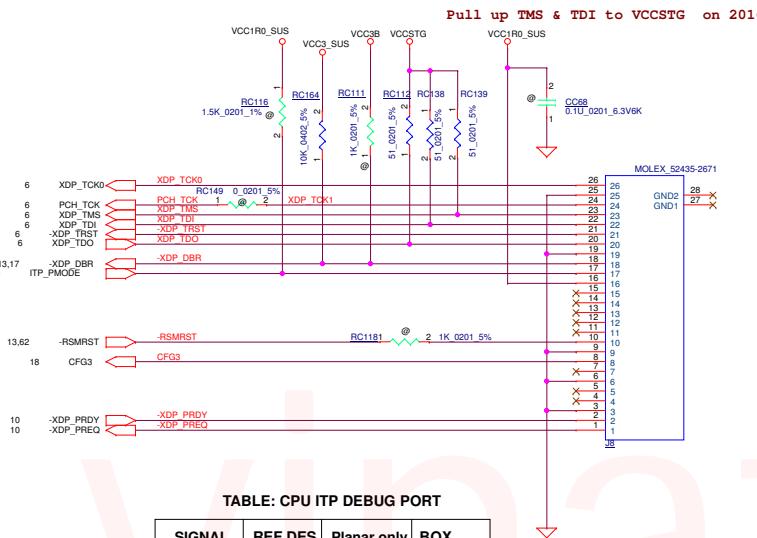


TABLE: CPU ITP DEBUG PORT

SIGNAL	REF DES	Planar only	BOX
TDO	RC109	ASM	ASM
TRST#	RC113	ASM	ASM
DBRST#	RC110	ASM	ASM
RESET#	RC111	ASM	ASM
PWRGD	RC112	ASM	ASM
CONNECTOR	J8	ASM	NO ASM

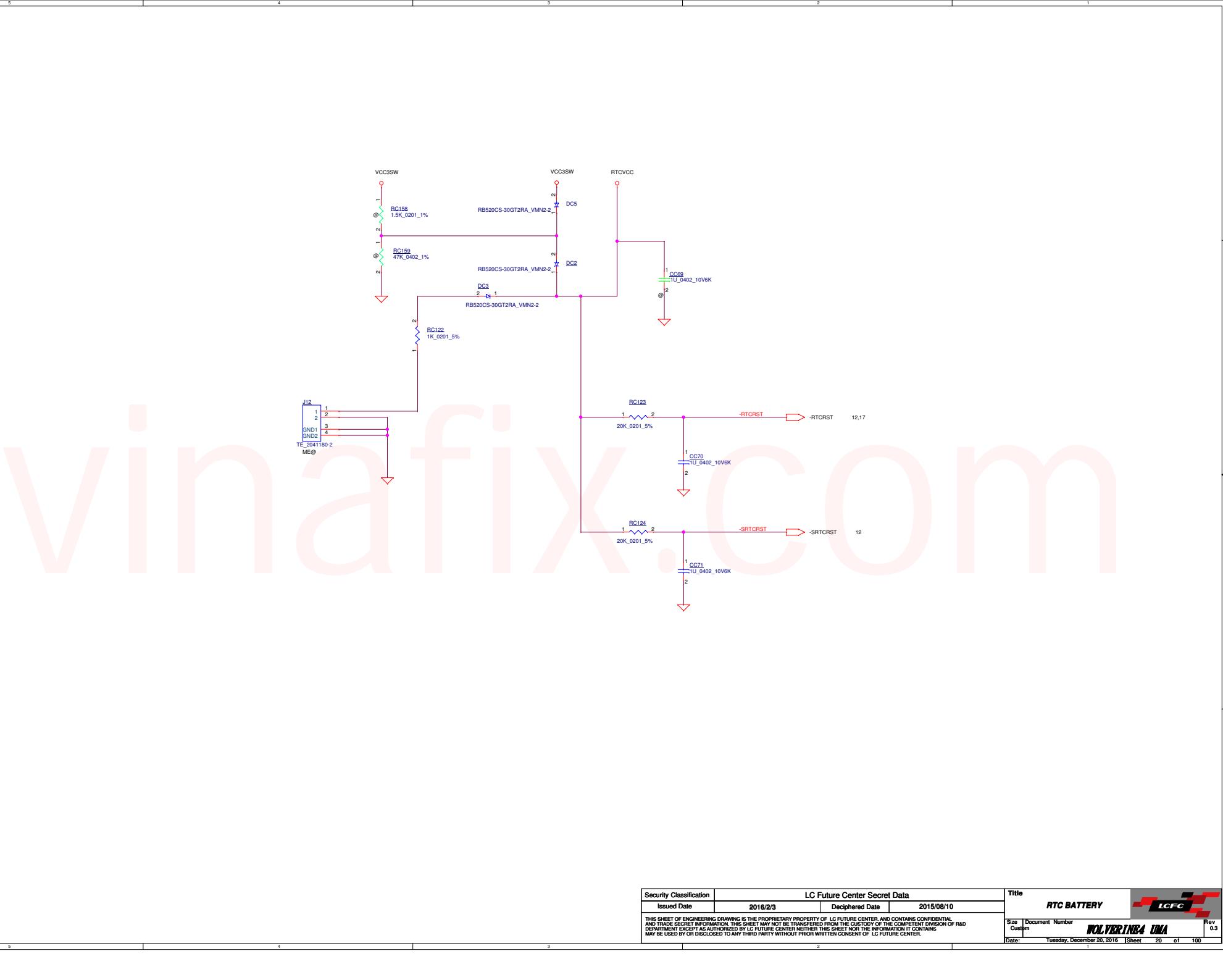
NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

TABLE: PCH ITP DEBUG port

SIGNAL	REF DES	Planar only	BOX
TDO	RC114	ASM	ASM
TMS	RC116	ASM	ASM
TDI	RC115	ASM	ASM
TCK	RC117	ASM	ASM
CPUCORE_PWRGD	RC118	ASM	ASM
-RSMRST	RC119	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

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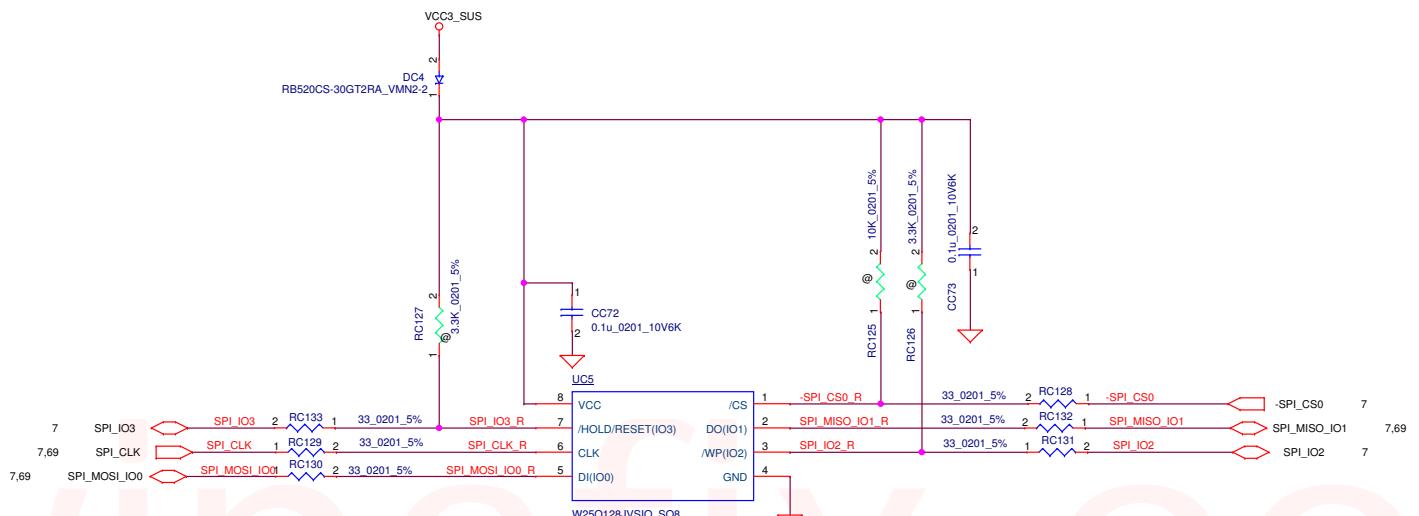


TABLE of SPI ROM (UC5)		
Vendor	MODEL	LCFC P/N
WINBOND	W25Q128JVSIQ	SA00008A300
MXIC	MX25L12873FM2I-10	SA00005VM00

TABLE					
SF100 PIN HEADER INTERFACE (TOP VIEW)					
1 VCC	DC4.1	GND	2		
3 CS#	RC128.2	RC129.2	4		
5 MISO (KEY)	RC132.2	RC130.2	6		
7	N/A	N/A	8		

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Title

SPI FLASH



Size

Custom

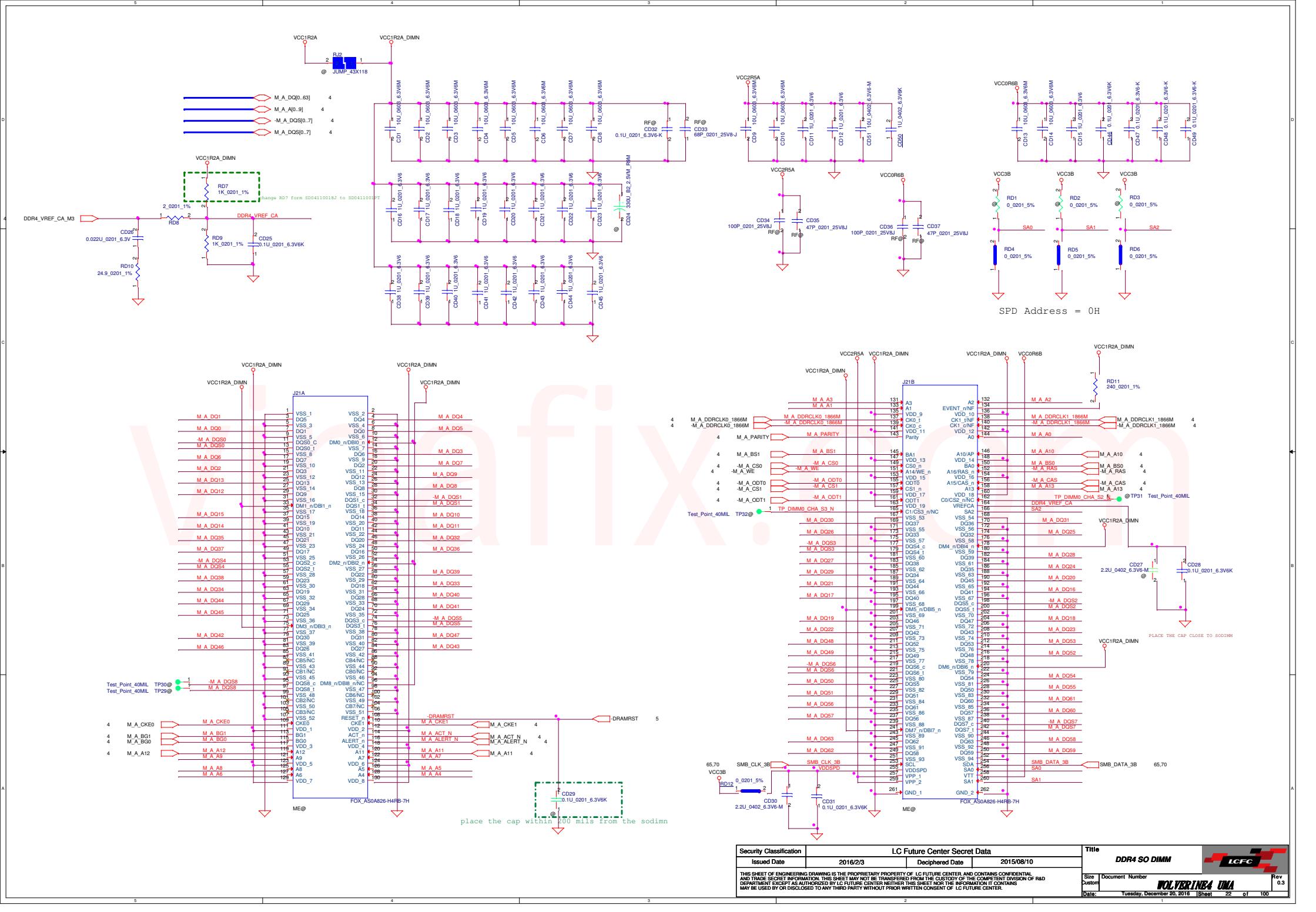
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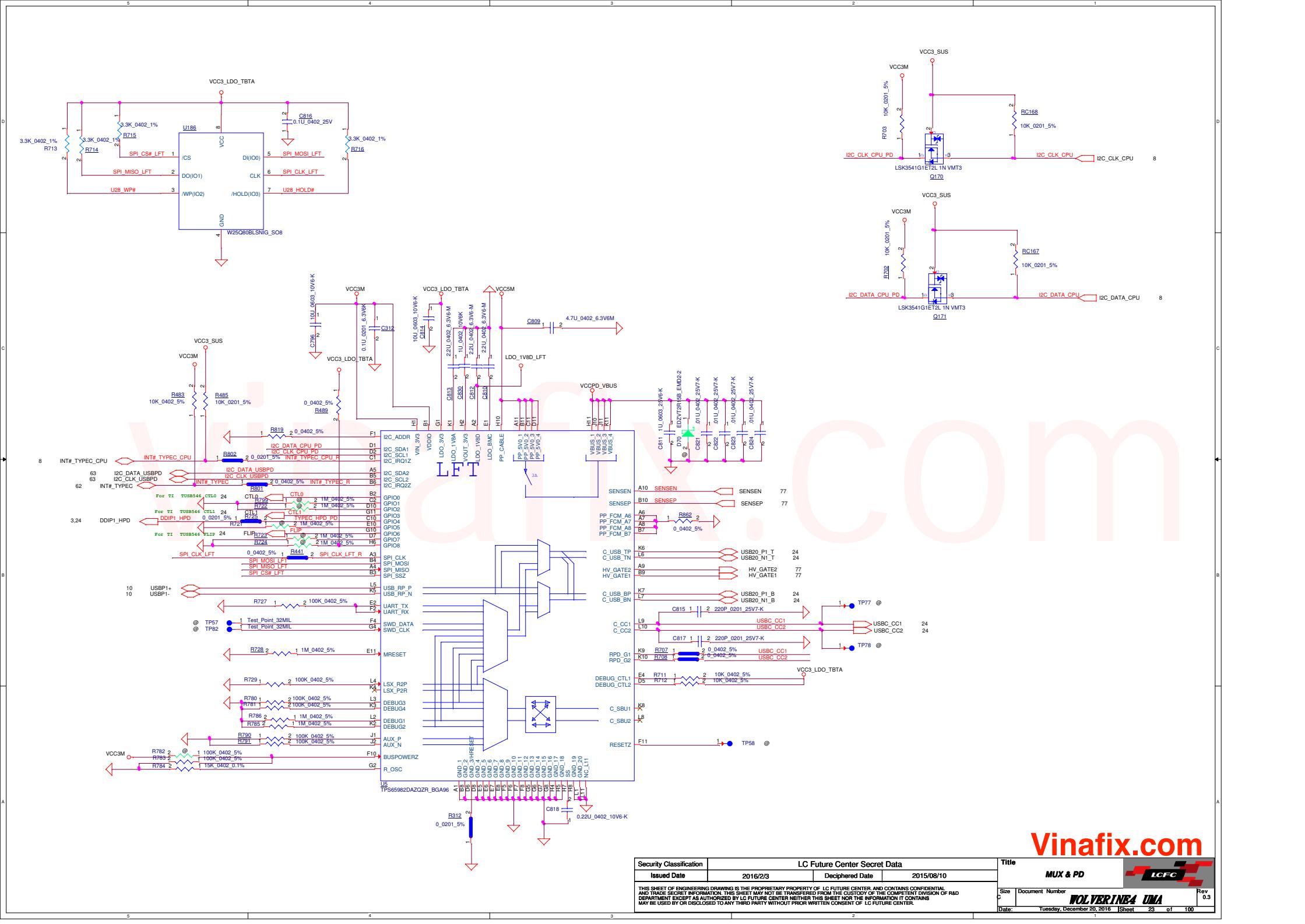
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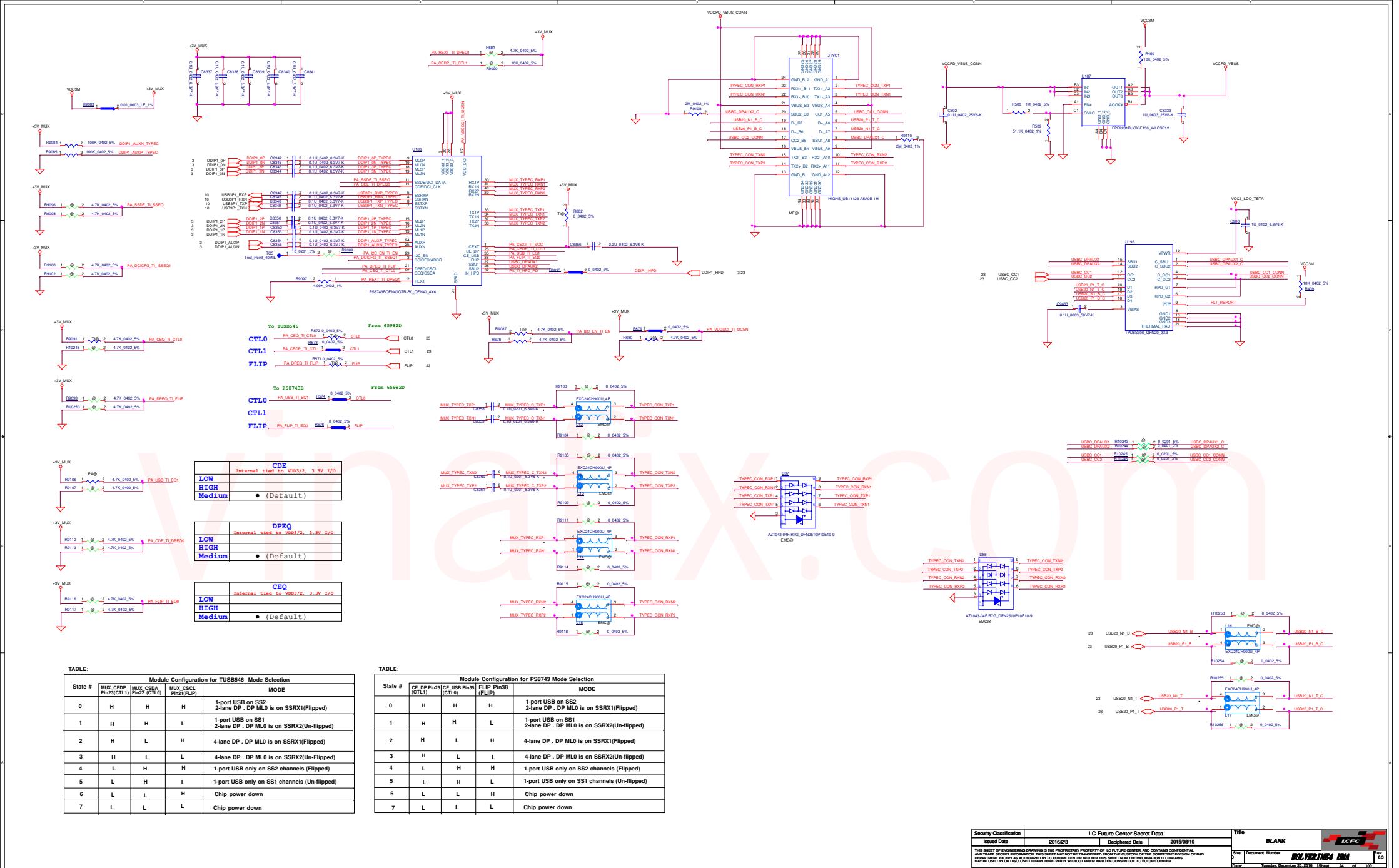
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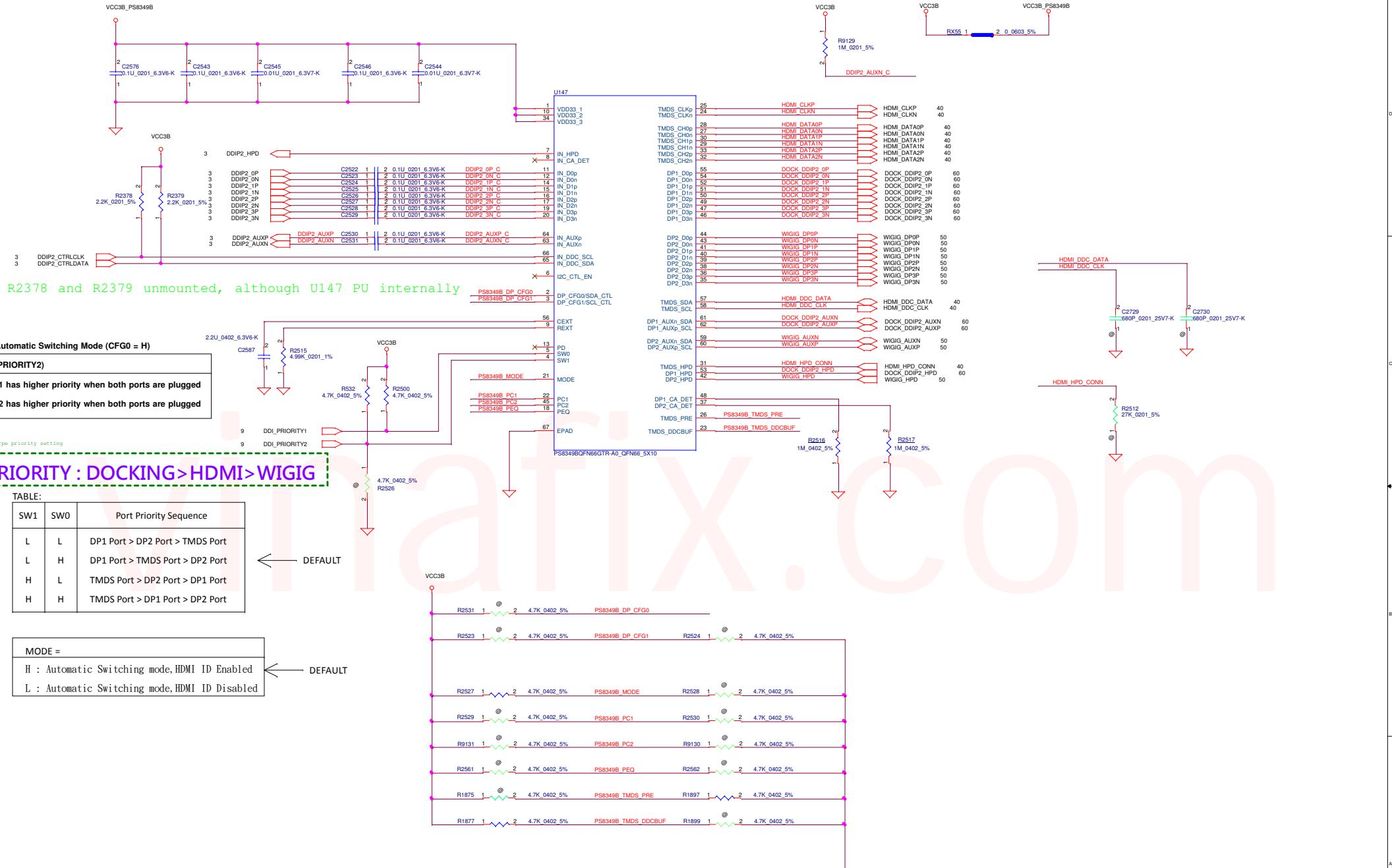
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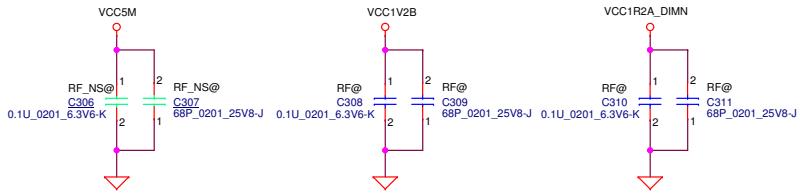
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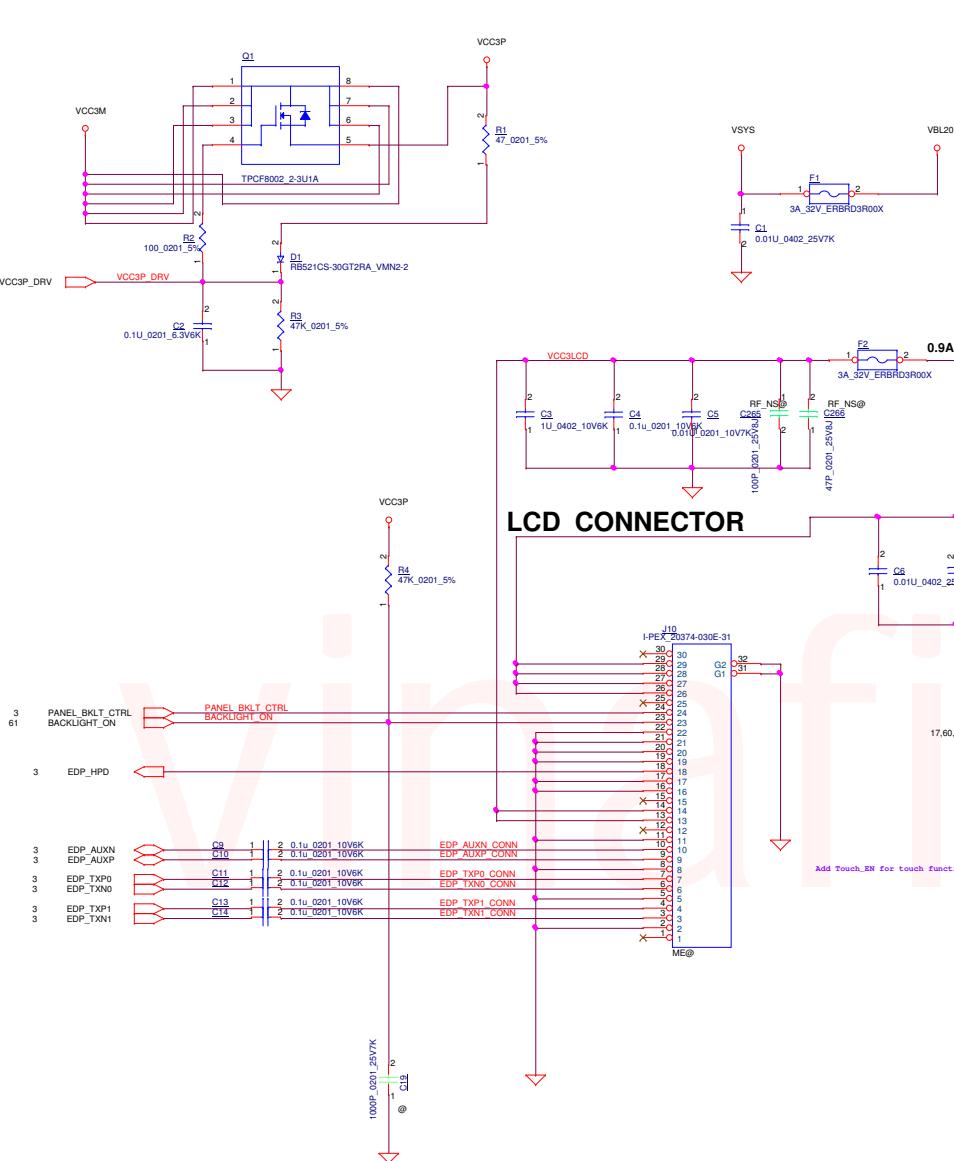
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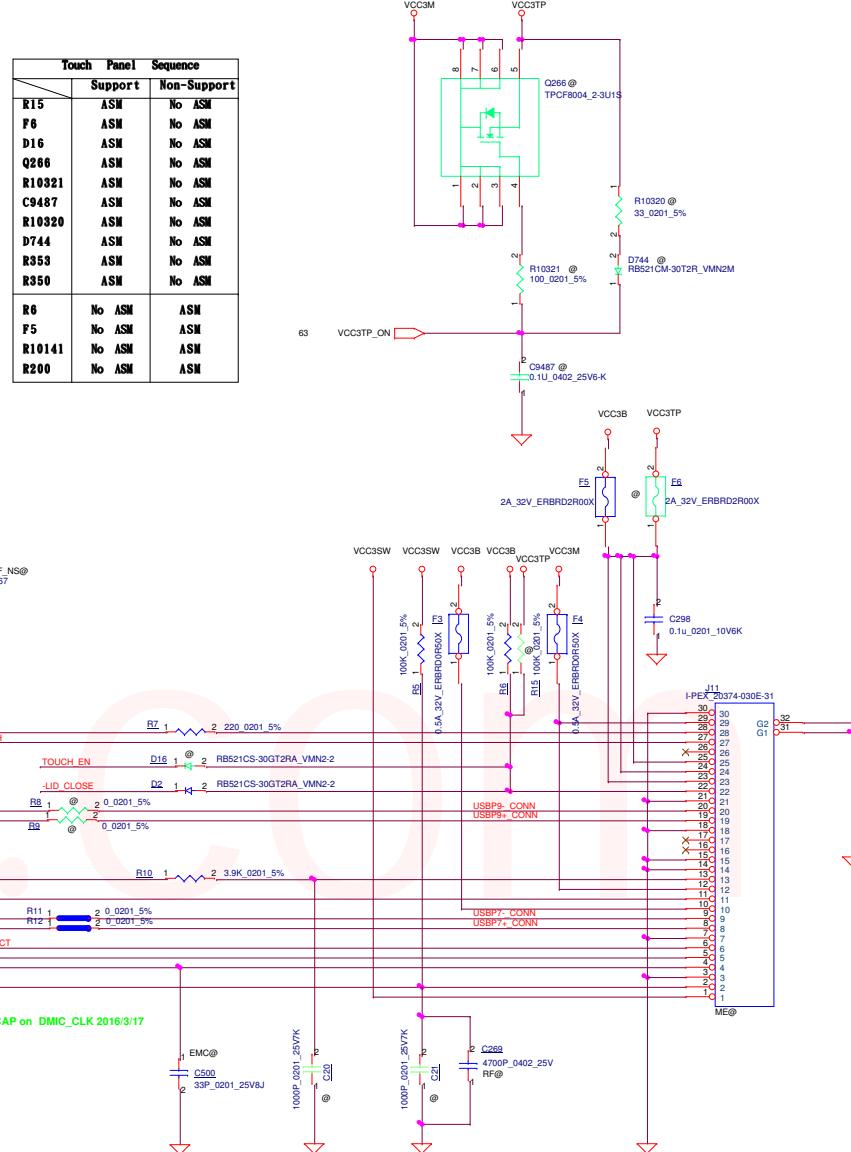


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Touch Panel Sequence	Support	Non-Support
R15	ASM	No ASM
F6	ASM	No ASM
D16	ASM	No ASM
Q266	ASM	No ASM
R10321	ASM	No ASM
C9487	ASM	No ASM
R10320	ASM	No ASM
D744	ASM	No ASM
R353	ASM	No ASM
R350	ASM	No ASM
R6	No ASM	ASM
F5	No ASM	ASM
R10141	No ASM	ASM
R200	No ASM	ASM

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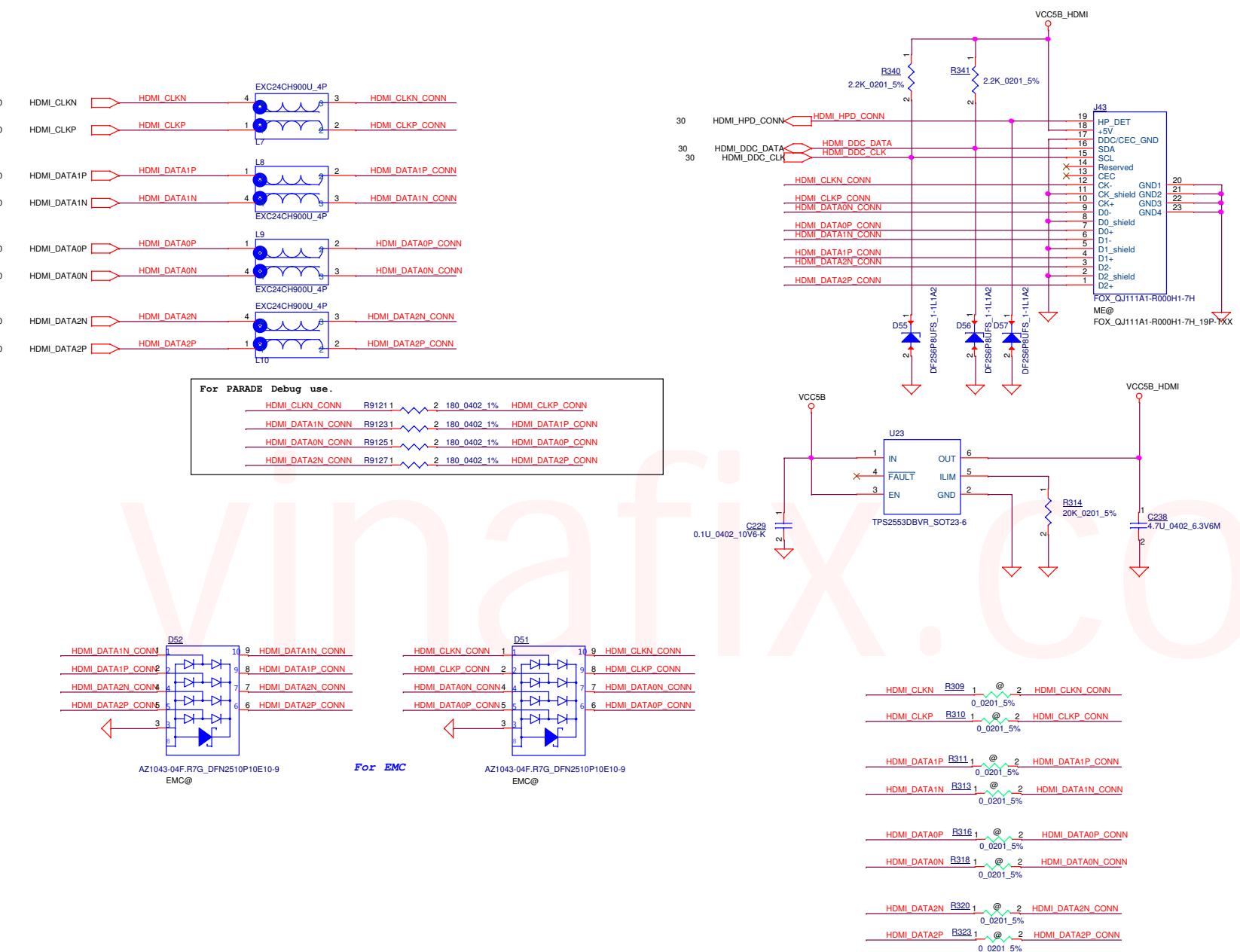


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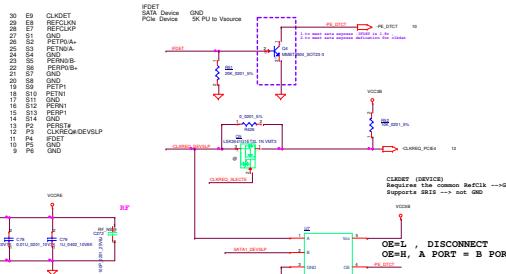
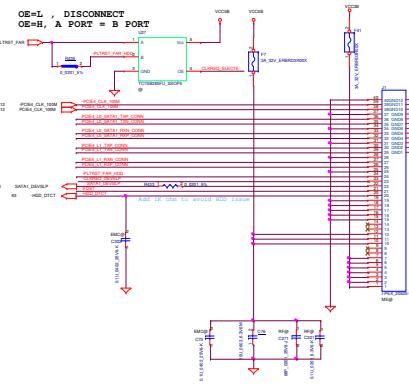
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EN	MODE	MODE
0	SATA Application	
1	PCIe Application	
1	X	Double

Equalization Setting:

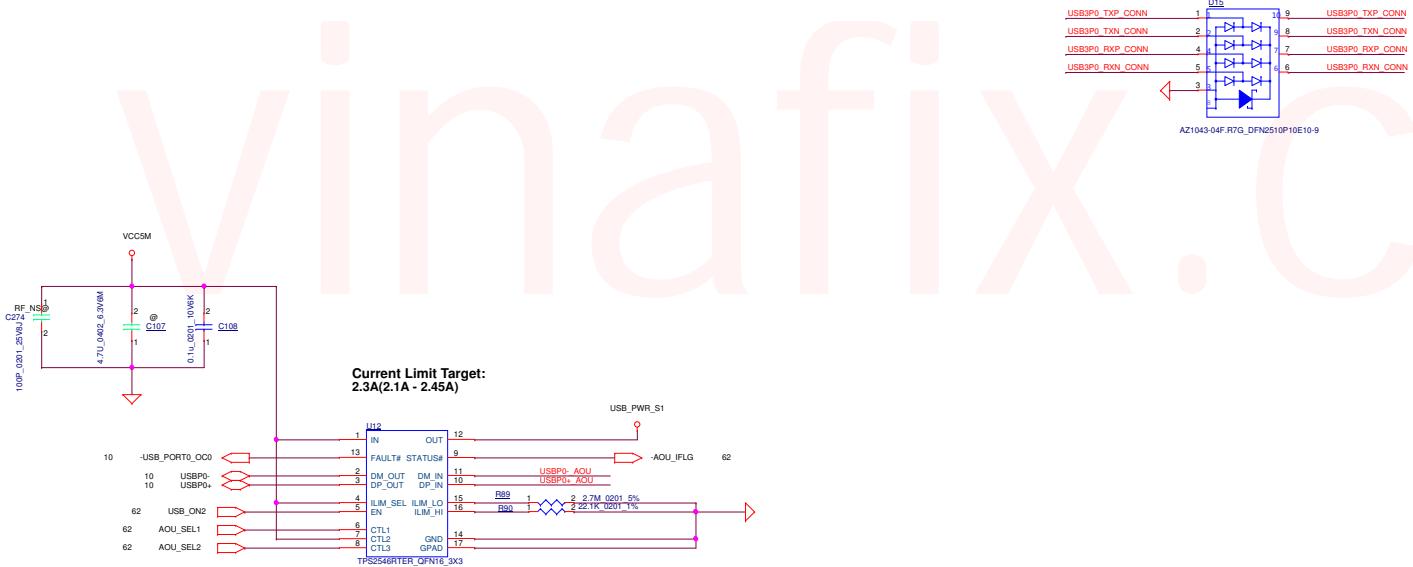
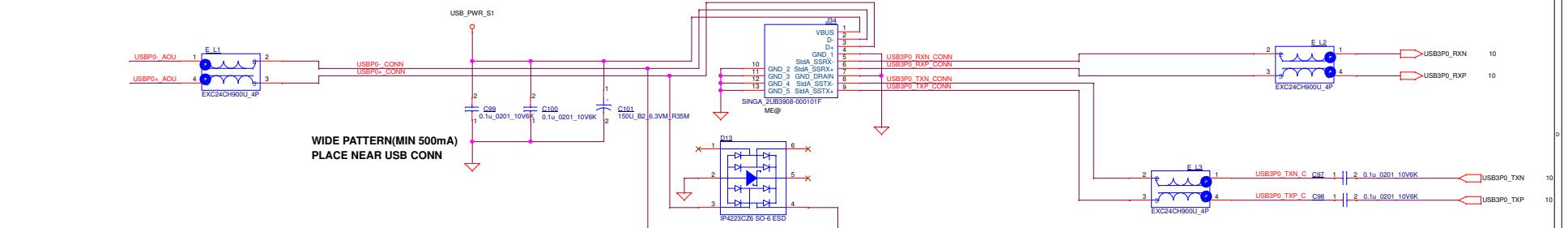
EQ_A/B are the selection pins for the equalization selection for each direction.

Equalizer setting	@0GHz	@4GHz
0	0dB	0dB
0	4dB (default)	4dB (default)
1	10dB	14dB

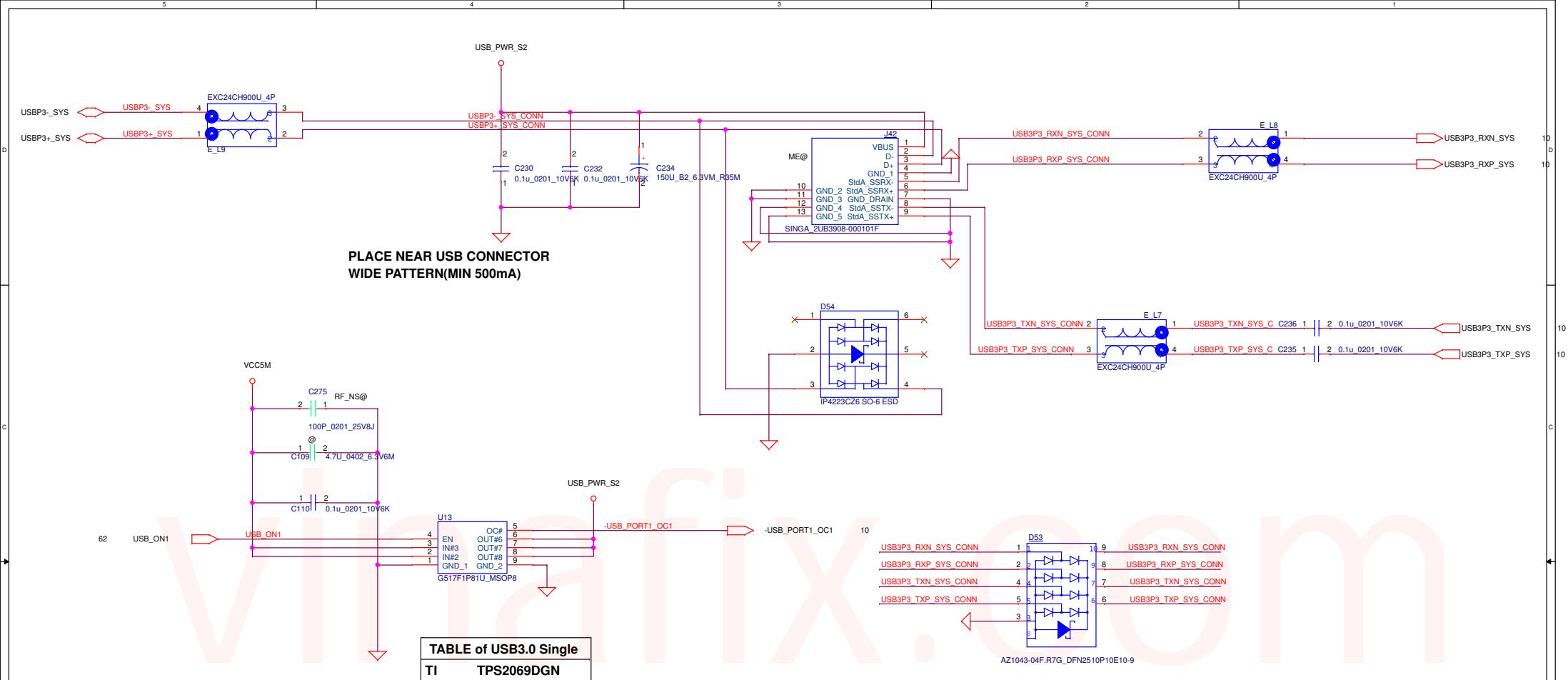
De-Emphasis Setting (for PCIe only):

Output DE Emphasis Setting:

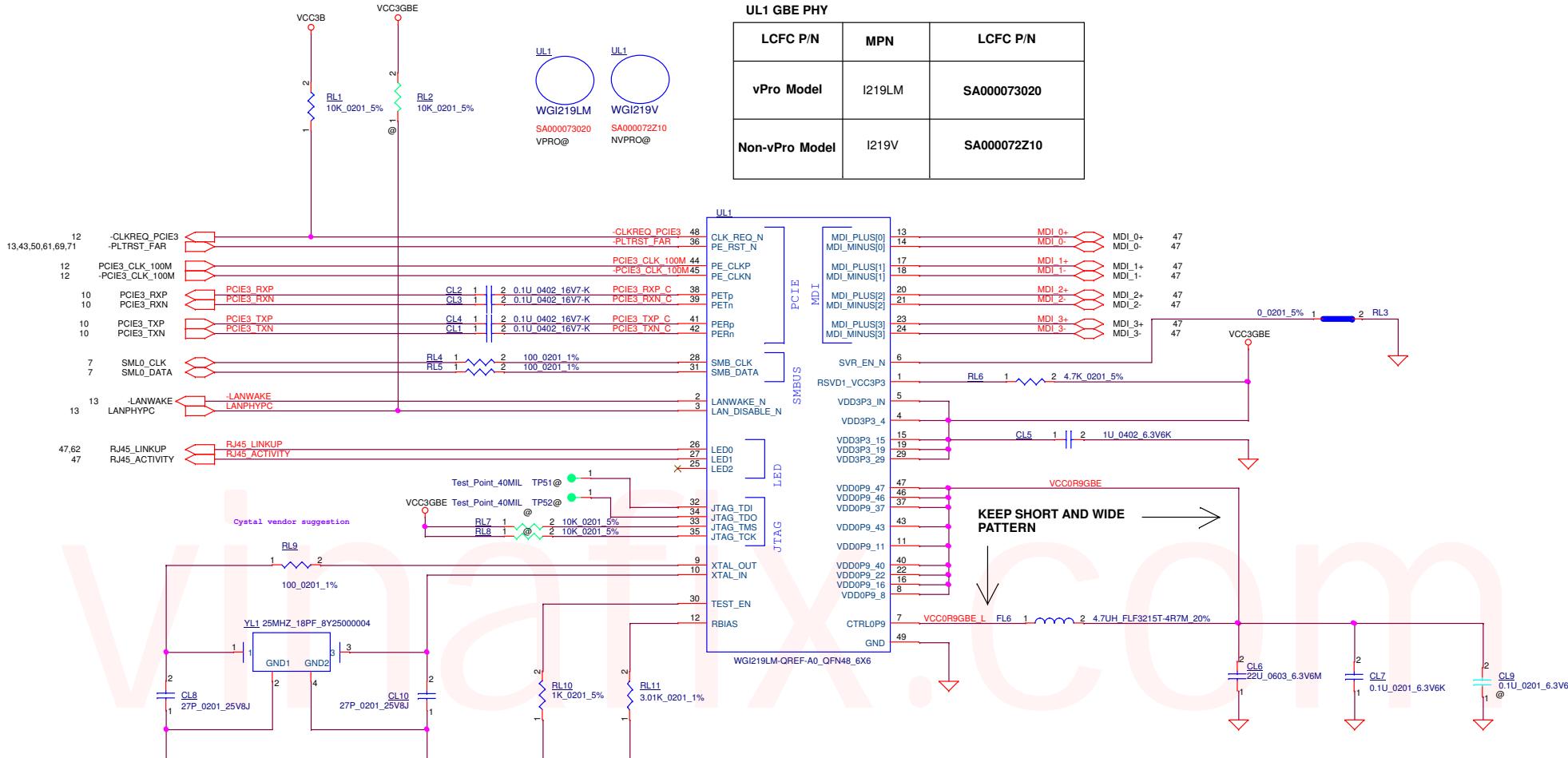
DE	DE Emphasis
0	2.5 dB
0	6dB (default)
1	4dB



Vendor	P/N
TI	TPS2546RTER

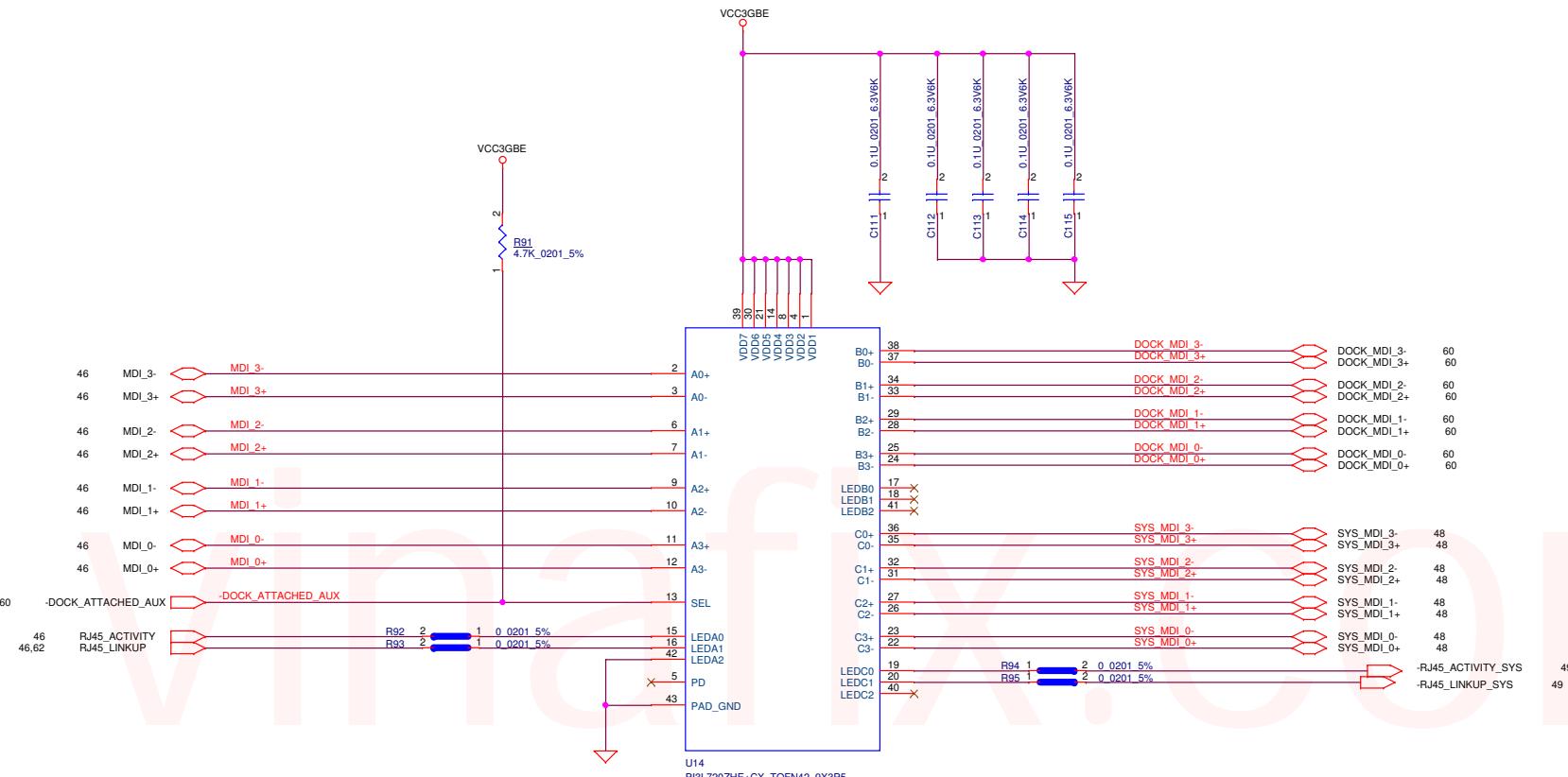


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						WOLVERINE4 UMA	
Date:	Tuesday, December 20, 2016	Sheet	45	of	100		



YL1 25Mhz

Vendor	Intel ESR spec	LCFC P/N	Vendor P/N	Vendor ESR spec
TXC	50 ohm Max	SJ1000H00J	8Y2500004	50 ohm Max
KDS	50 ohm Max	SJ1000P300	1ZZHAE25000CC0F	50 ohm Max



U14 GBE LAN SWITCH TABLE

LCFC P/N	VENDOR	MPN
SA00007E900	PERICOM	PI3L720ZHE+CX
SA000072400	TI	TS3L501ERUAR

Security Classification

Issued Date

2016/2/3

LC Future Center Secret Data

Deciphered Date

2015/08/10

Title

GBE LAN SWITCH



WOLVERINE4 UMA

Rev 0.3

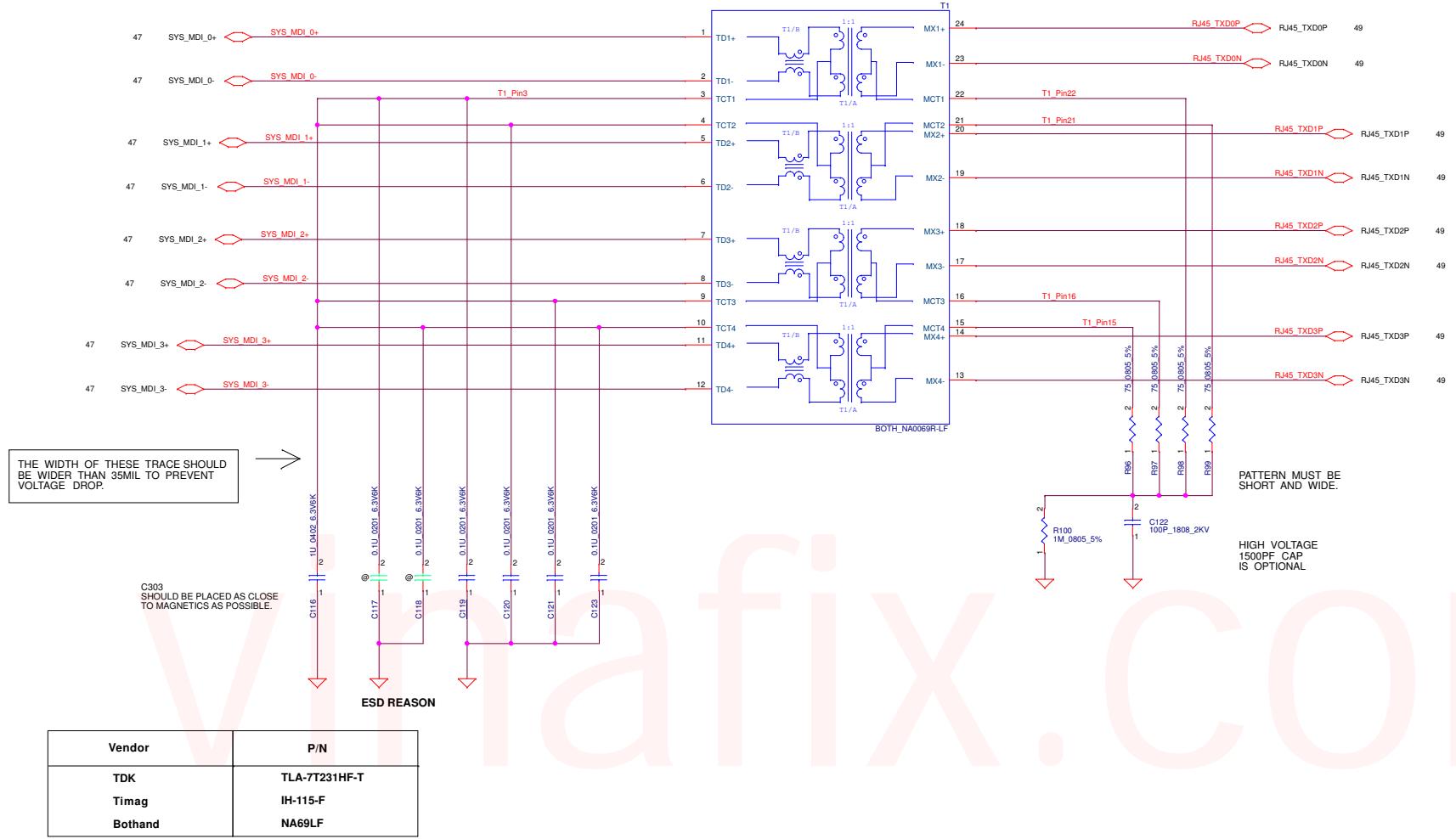
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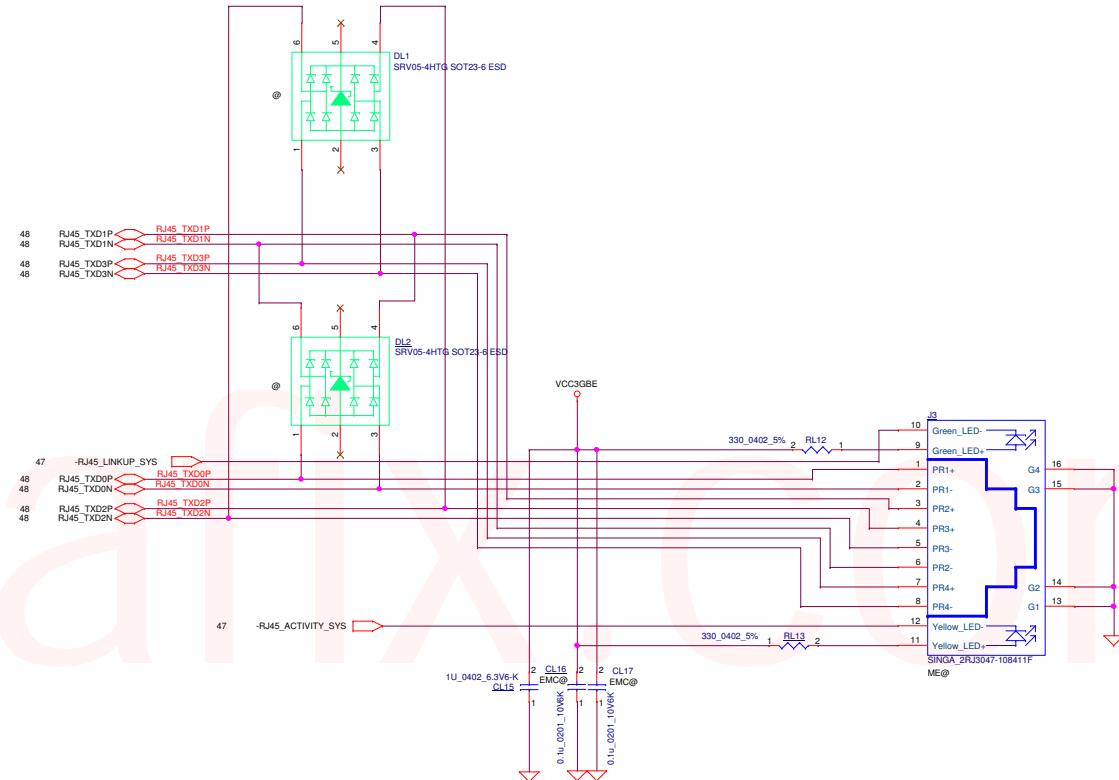
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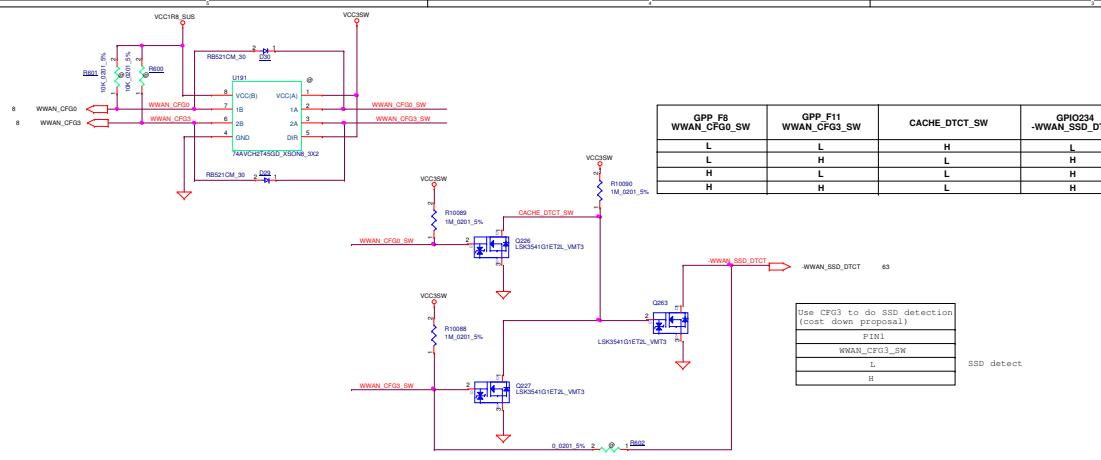




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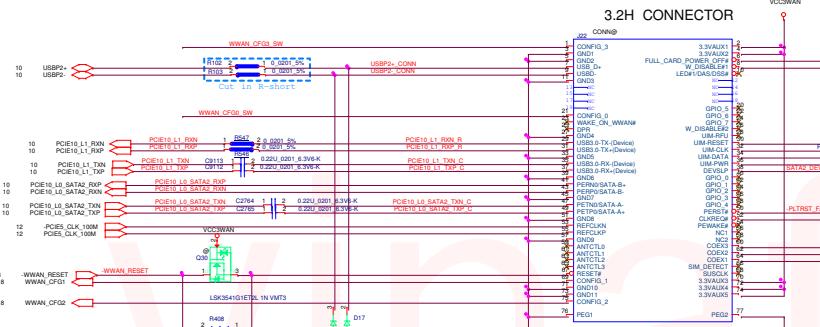
TABLE:

	WV4 KPL List	GPP_F8 CONFIG_0 (Pin 21)	GPP_F9 CONFIG_1 (Pin 69)	GPP_F10 CONFIG_2 (Pin 75)	GPP_F11 CONFIG_3 (Pin 1)
WWAN	Sierra (QC) EM7455 LTE-A WWAN	GND	GND	NC	NC
	Sierra (QC) EM7430 LTE-D WWAN	GND	GND	NC	NC
M.2 2242 SATA SSD	Lite-on 128GB SATA MLC M.2 2242-D3 / CVY-SB128 MLC	GND	GND	GND	GND
	SanDisk (Async) 128GB SATA MLC M.2 2242-D3 / Z500 TLC	GND	NC	NC	NC
M.2 2242 PCIe SSD	16GB Optane PCIe M.2 2242-S3	GND	NC	GND	GND



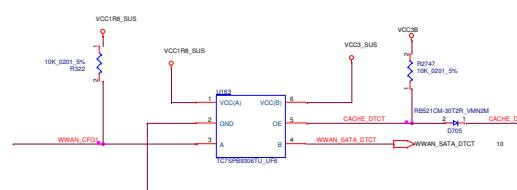
TYPE-B NGFF CCARD FOR WWAN

3.2H CONNECTOR



Use CFG3 to do SSD detection
(cost down proposal)
PIN1
WWAN_CFG3_SW
L H
H H

SSD detect

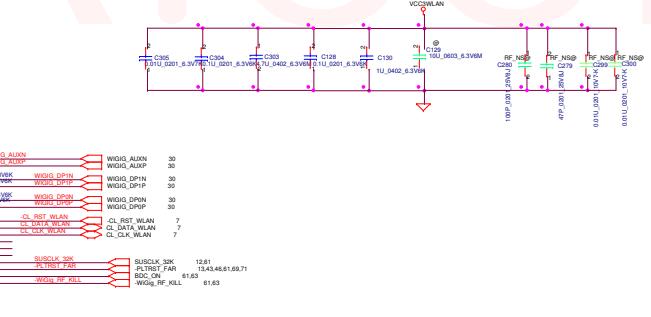
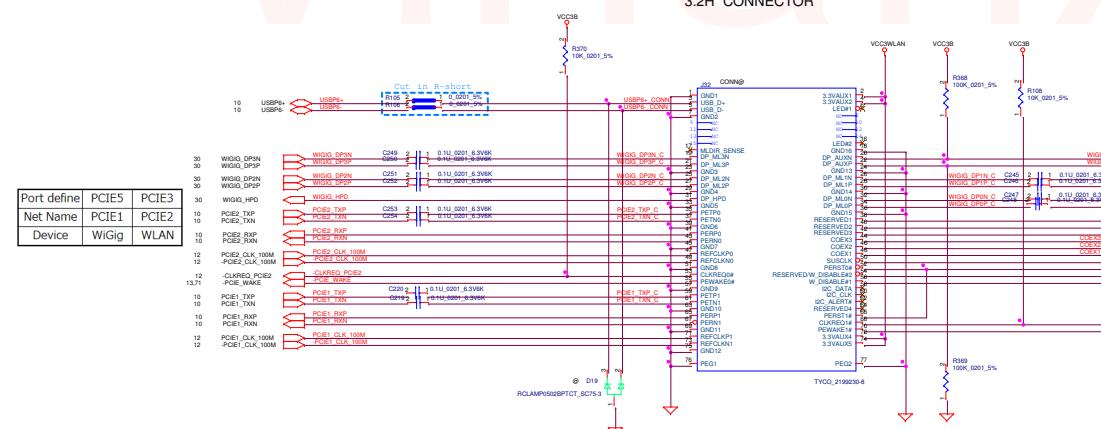


Use CFG1 to do PCIE SSD detection (cost down proposal)			
PIN1	WWAN_CFG3_SW	-WWAN_PE_DTCT	SATA SSD
L	H	OE	PCIE SSD
NC	L	DIO5	PCIE SSD

CACHE_DTCT_SW	WWAN_CFG1	-WWAN_PE_DTCT	PCIE SSD
H	L	L	SATA SSD
H	NC	H	WWAN USB2.0
L	L	H	WWAN USB2.0

TYPE-A NGFF CCARD FOR WLAN

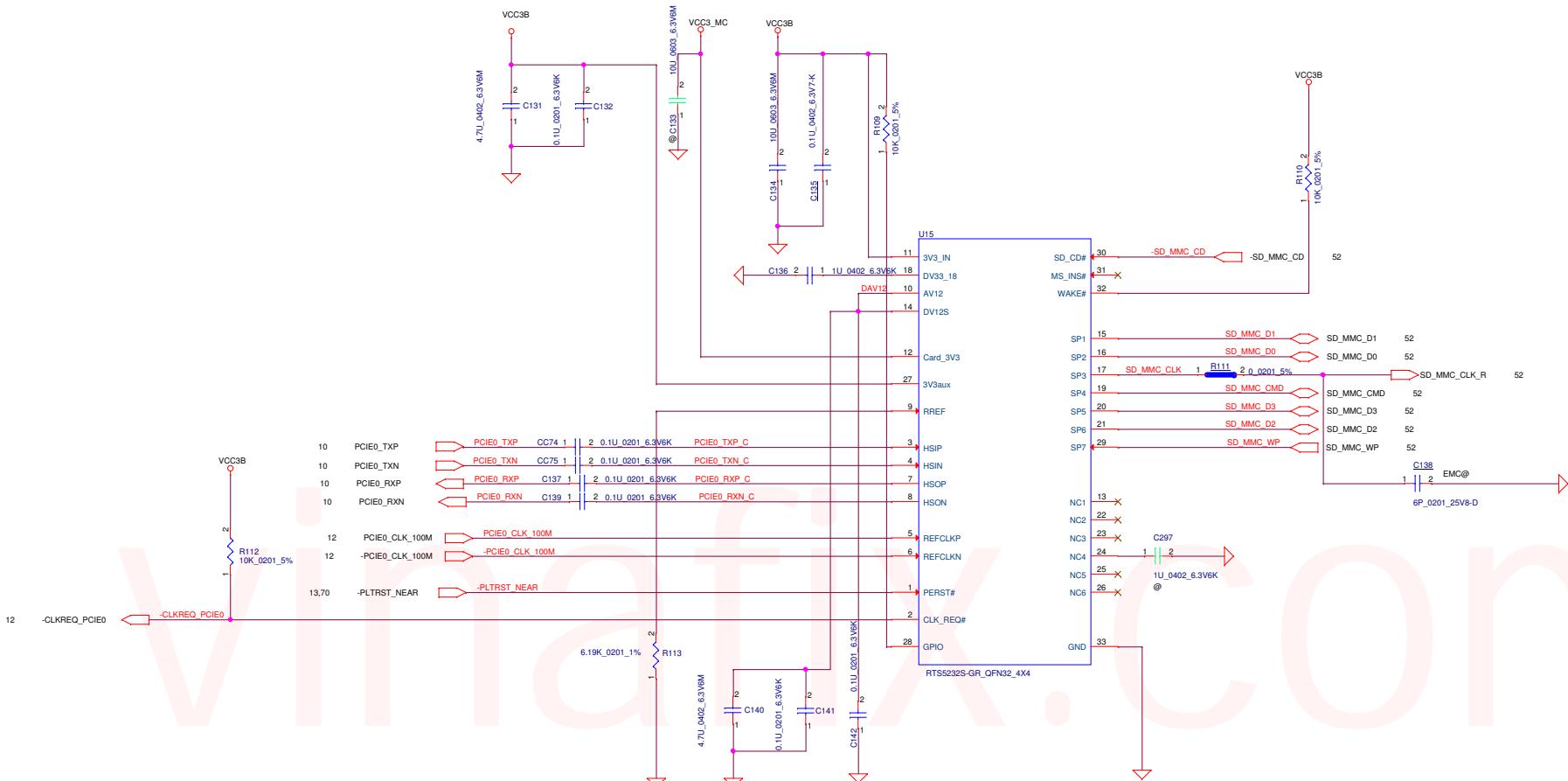
3.2H CONNECTOR



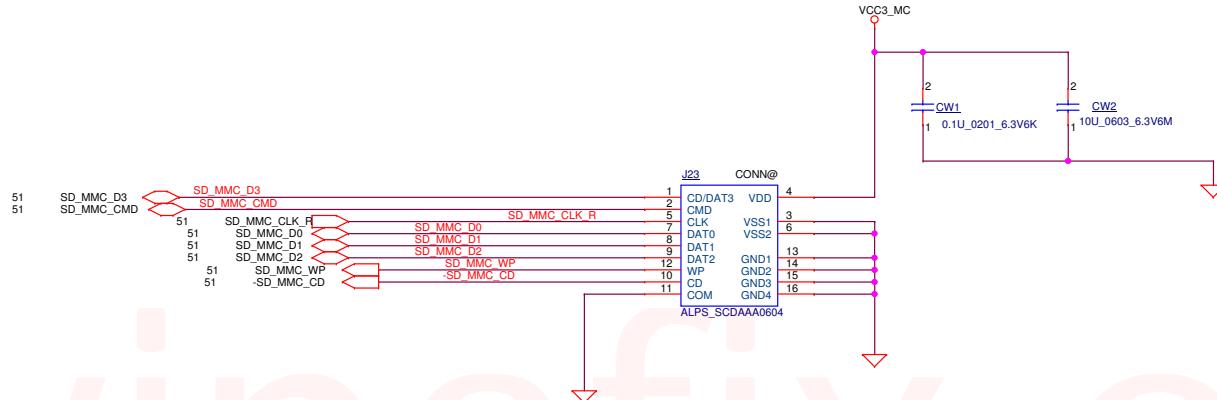
Port define	PCIE5	PCIE3
Net Name	PCIE1	PCIE2
Device	WiGig	WLAN

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		2015/08/10
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Security Classification	Issued Date	Deciphered Date	Rev	MEDIA CARD INTERFACE	LCFC	
	2016/2/3	2015/08/10	0.3			

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TABLE

Dock support		
	SUPPORT	NON-SUPPORT
R1235	NO ASM	NO ASM
R1236	ASM	NO ASM
R1237	ASM	NO ASM
R1238	ASM	NO ASM

LOGIC

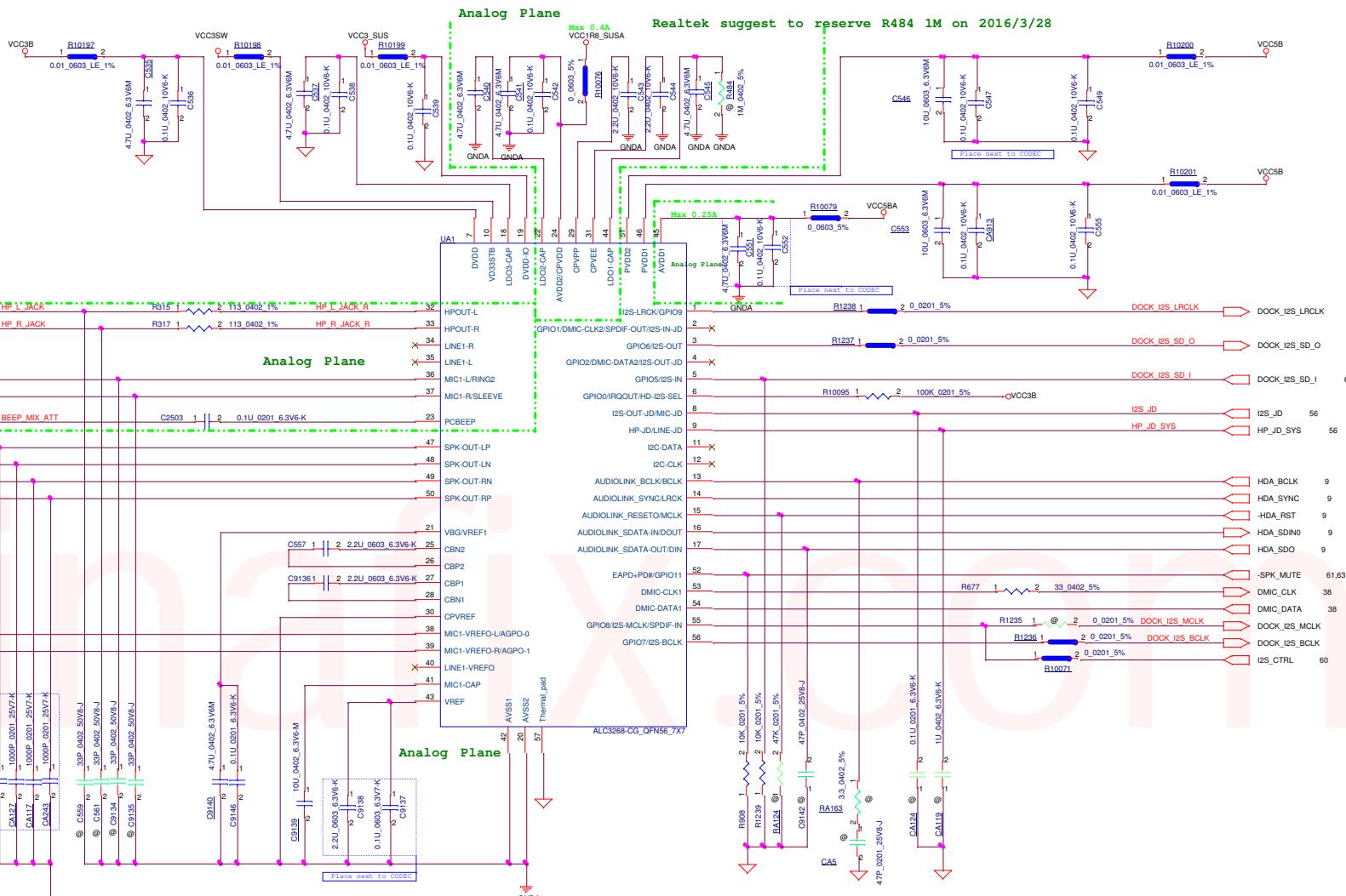
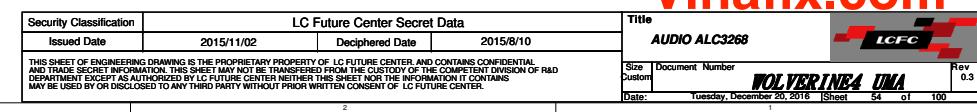
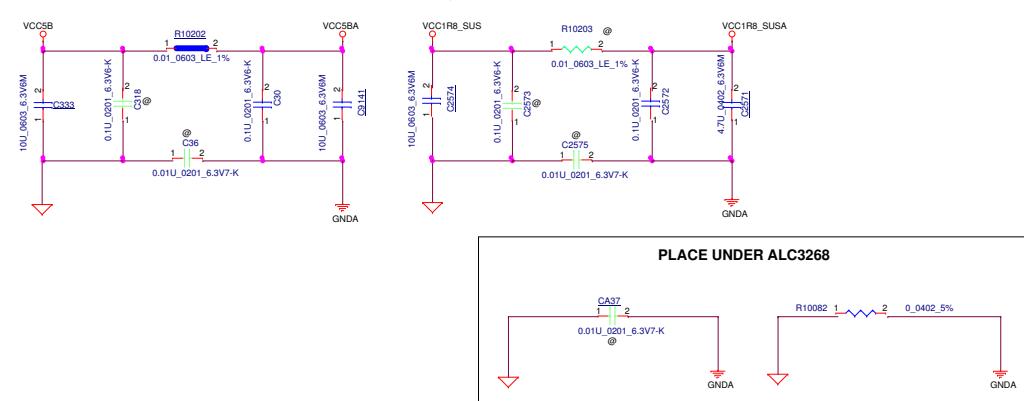


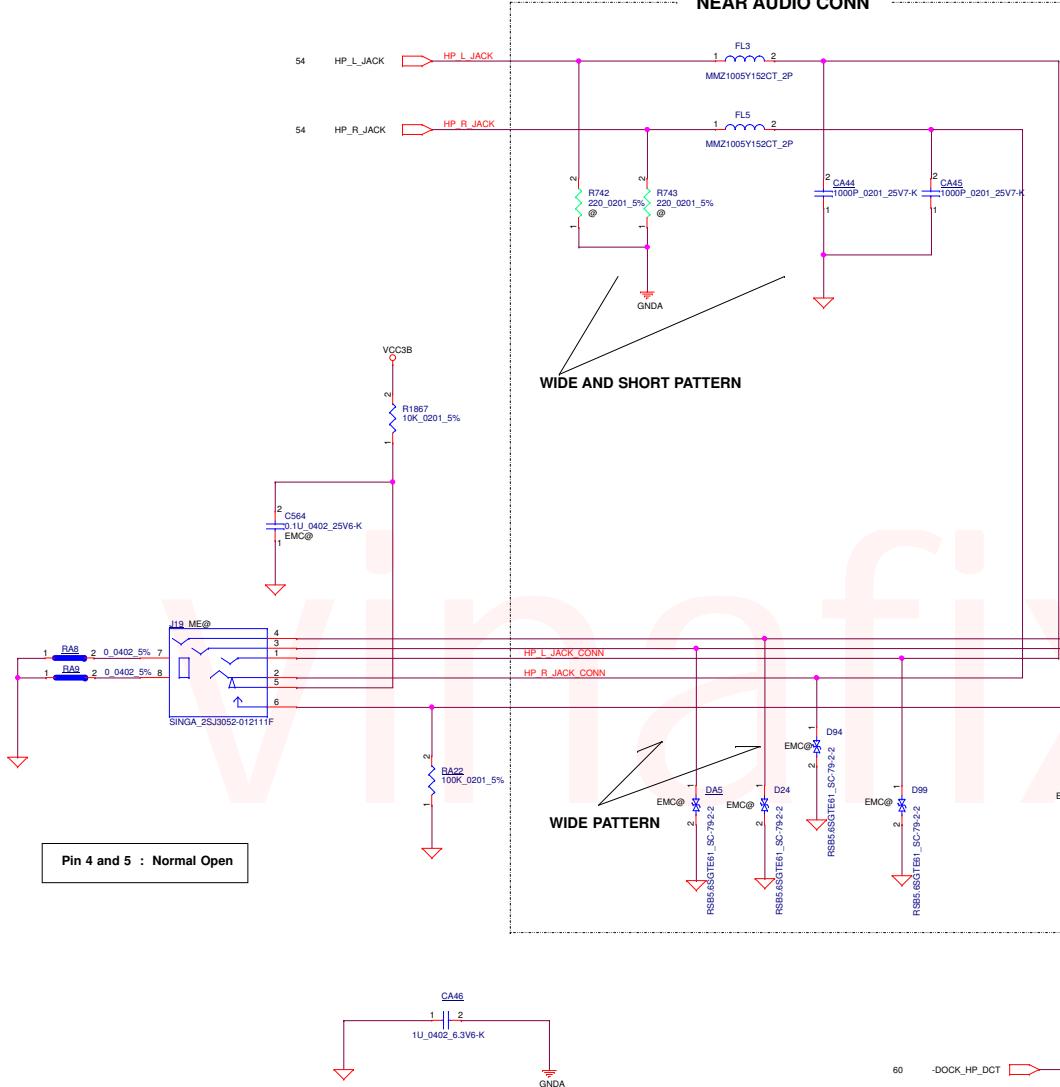
TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R961	ASM	NO ASM
R677	ASM	NO ASM

1



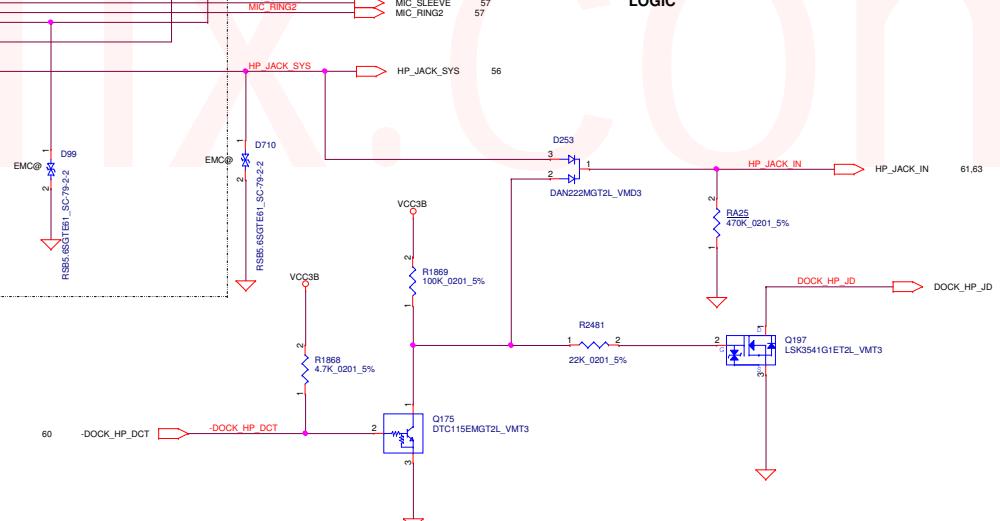
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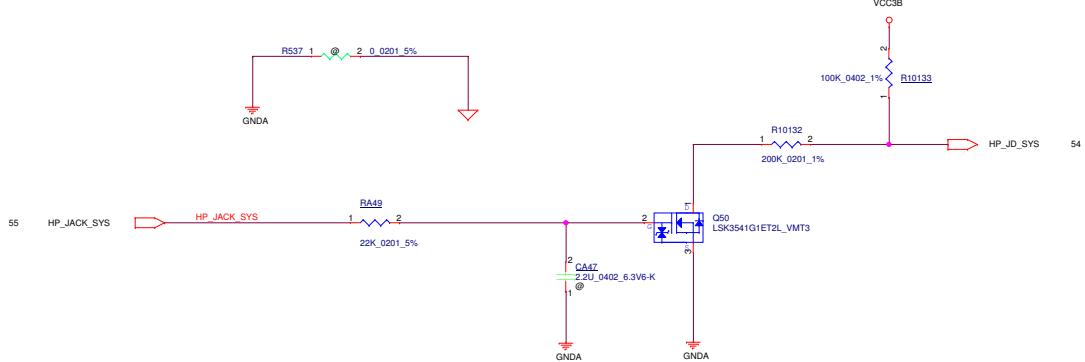


TABLE

DOCKING	SUPPORT	NON-SUPPORT
R1869	ASM	NO ASM
Q175	ASM	NO ASM
R2481	ASM	NO ASM
Q197	ASM	NO ASM

LOGIC

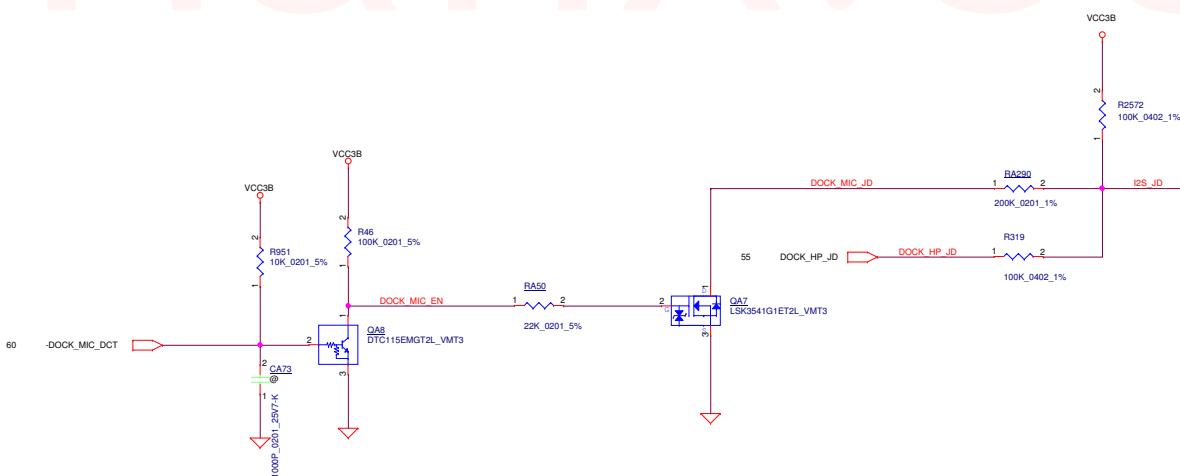




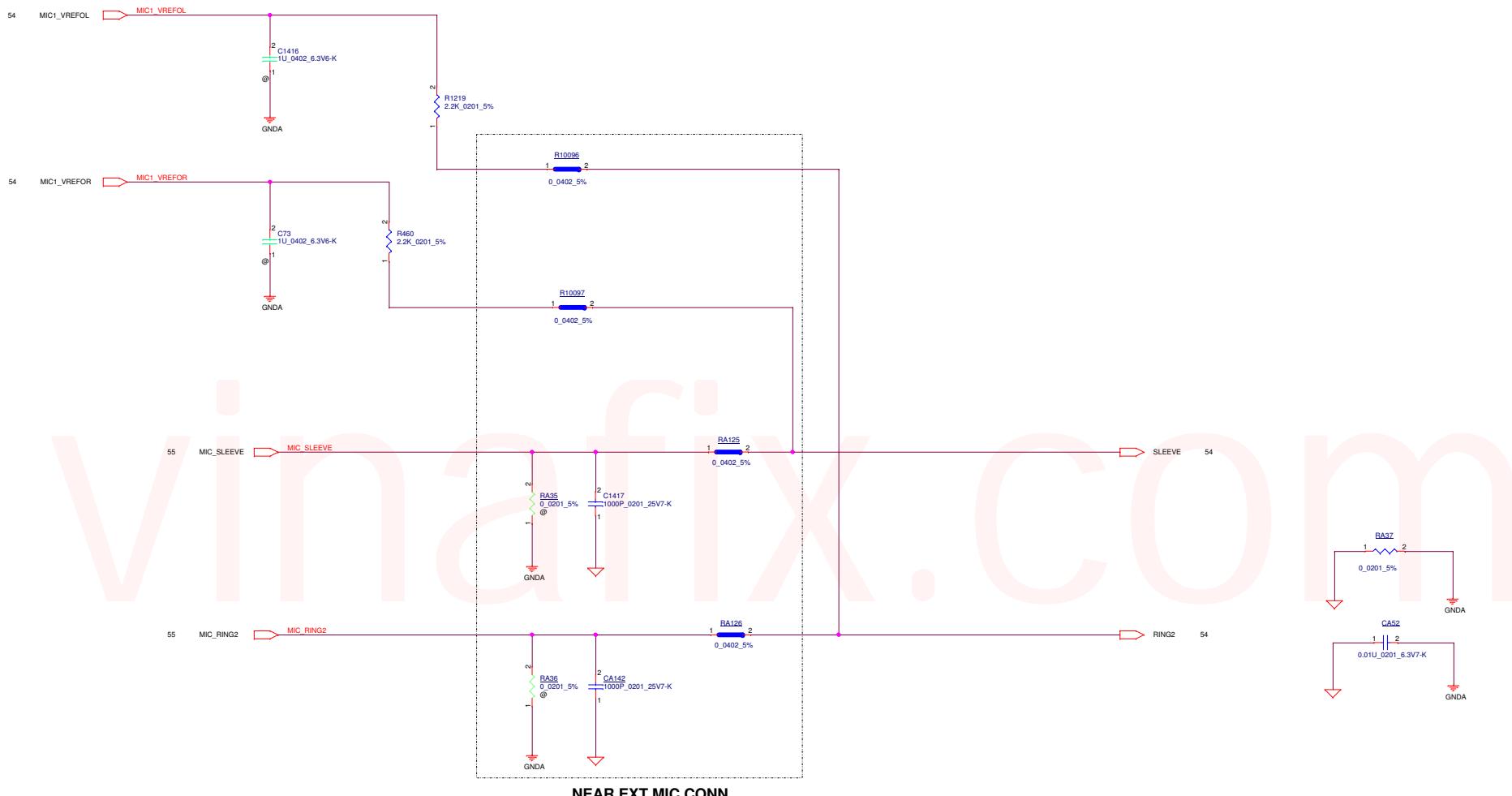
TABLE

DOCKING	SUPPORT		NON SUPPORT
MIC HW	ENABLE	DISABLE	
R951	ASM	NO ASM	NO ASM
R290	ASM	NO ASM	NO ASM
R46	ASM	NO ASM	NO ASM
Q5	ASM	NO ASM	NO ASM
R52	ASM	NO ASM	NO ASM
Q6	ASM	NO ASM	NO ASM
R319	ASM	ASM	NO ASM
R2572	ASM	ASM	NO ASM

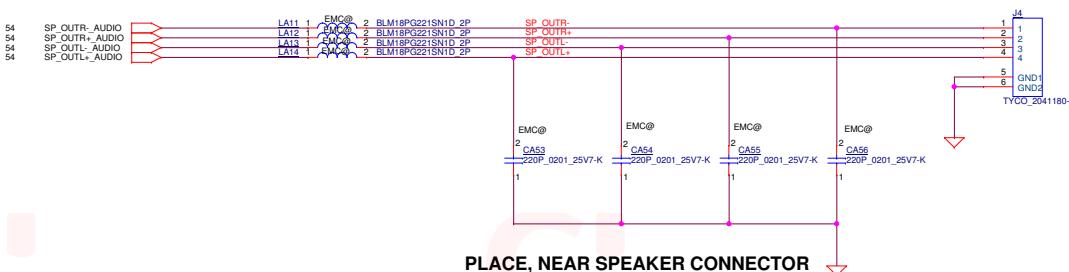
↑
LOGIC



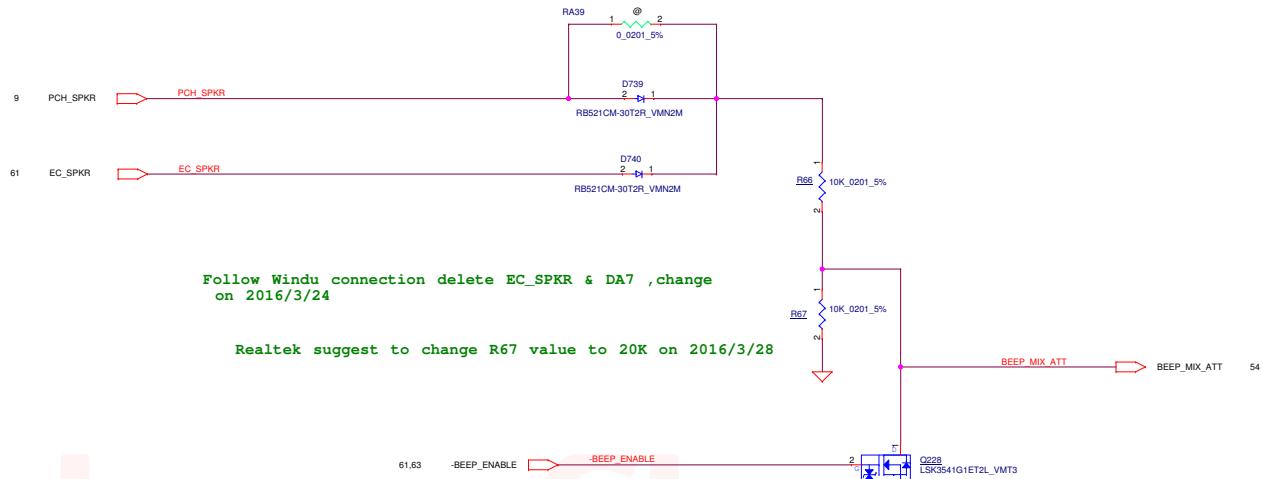
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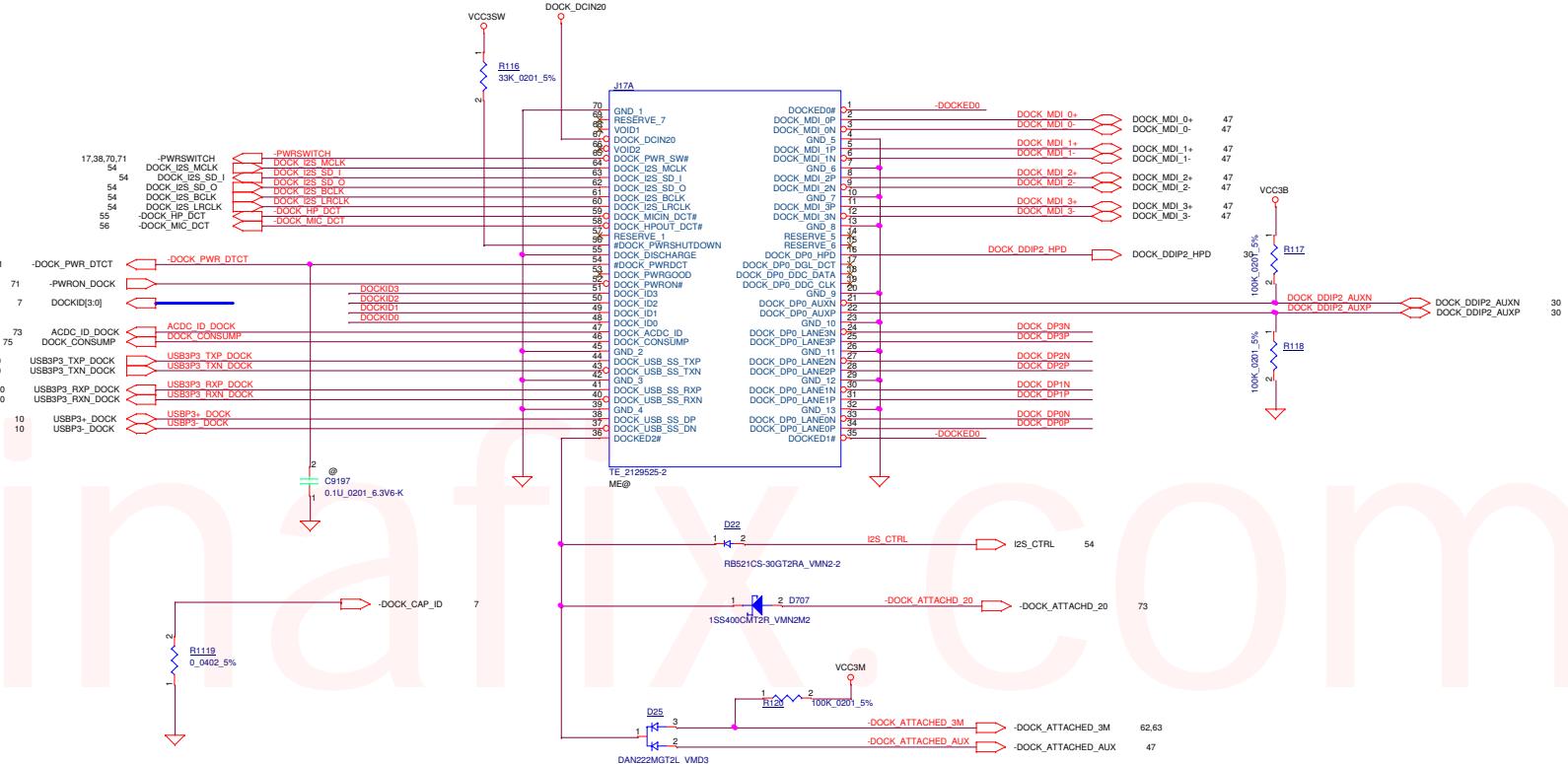
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Size	Document Number	Rev 0.3	
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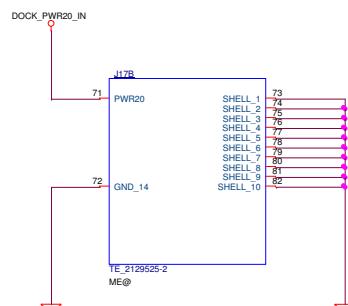


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20160222 change to reserved to avoid duplicated DOCK_PWR20_IN

Q6 & D23 delete on 2016/3/17, DOCK_PWR20_IN
power rail provided from PWR page



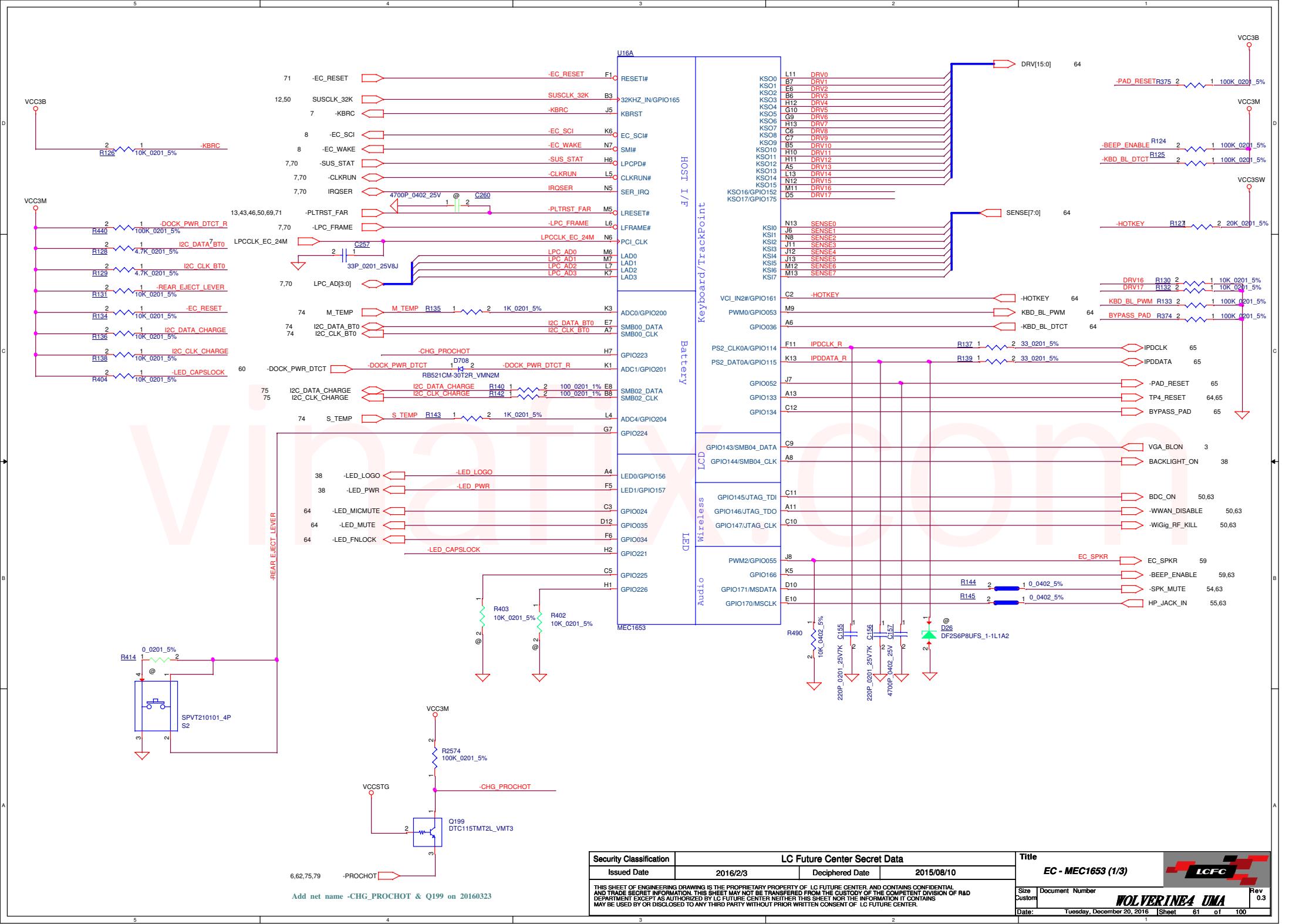
NEAR DOCK CONN

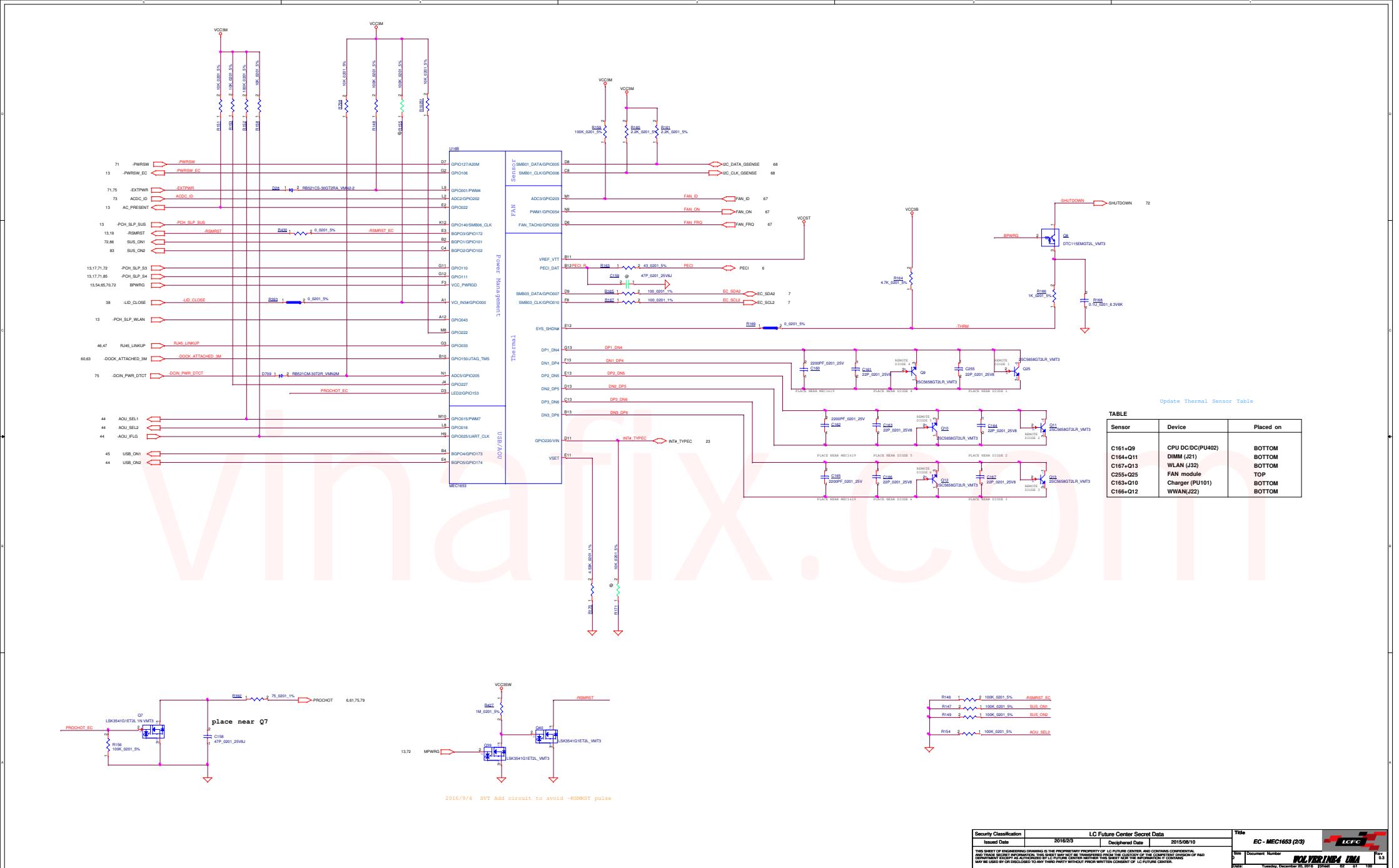
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30	DOCK_DDIP2_0N	C150_1 2 0.1u 0201 10V6K	DOCK_DDIP2_0N
30	DOCK_DDIP2_0P	C152_1 2 0.1u 0201 10V6K	DOCK_DDIP2_0P

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Issued Date	2016/2/3	Deciphered Date	2014/08/10

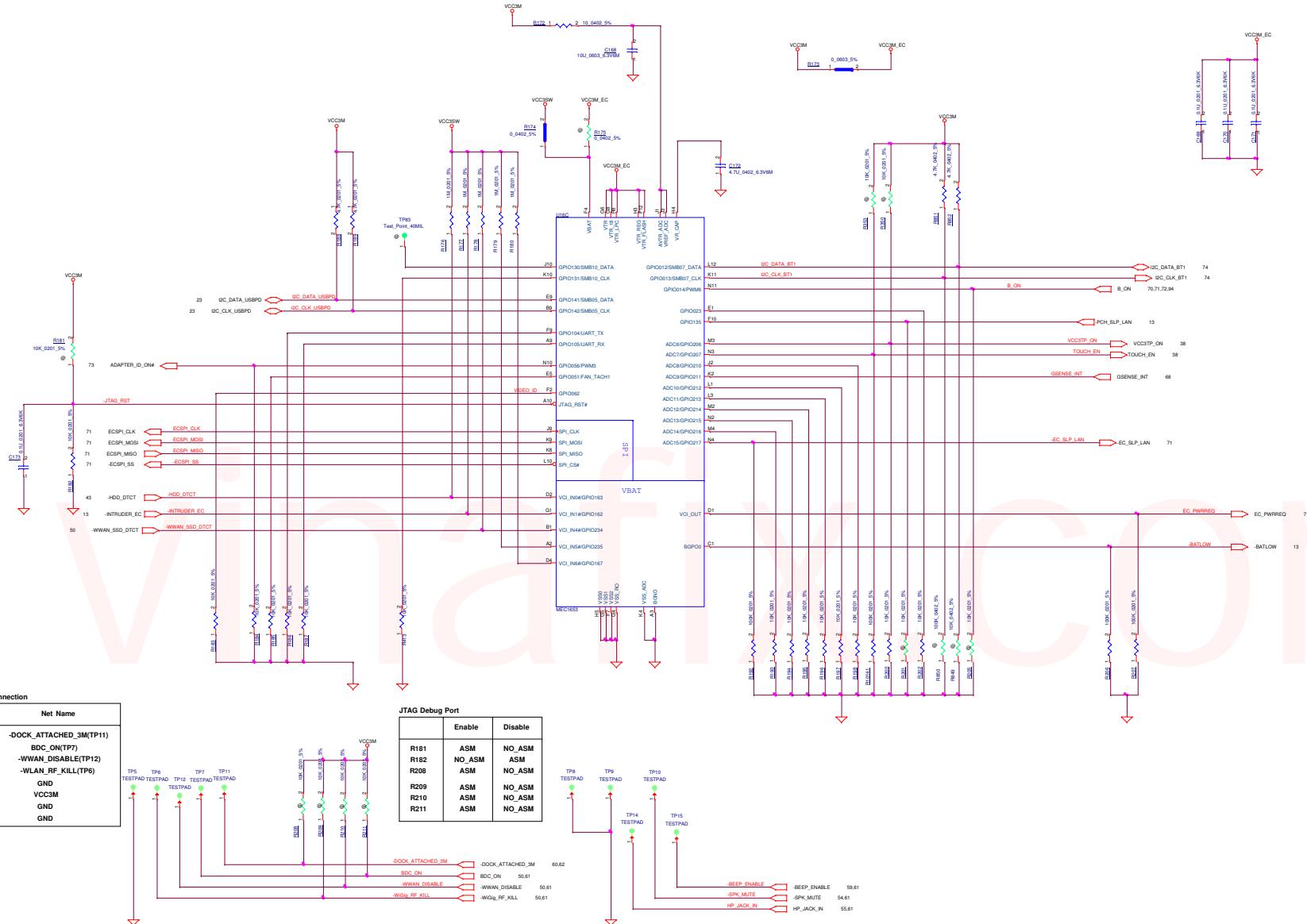
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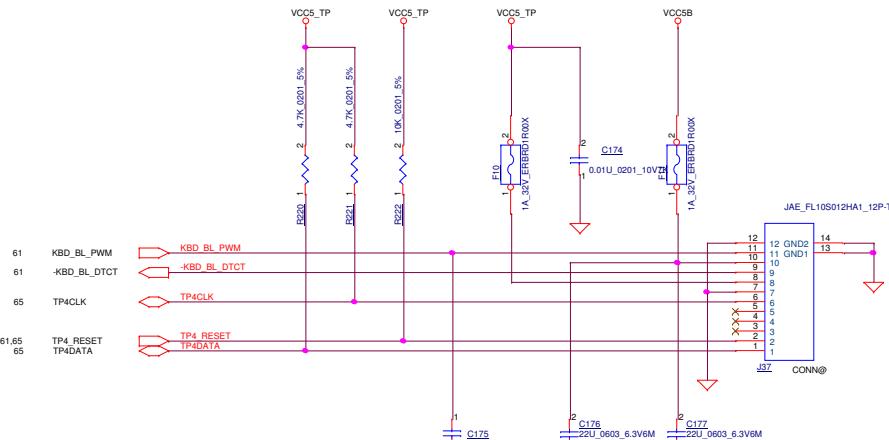
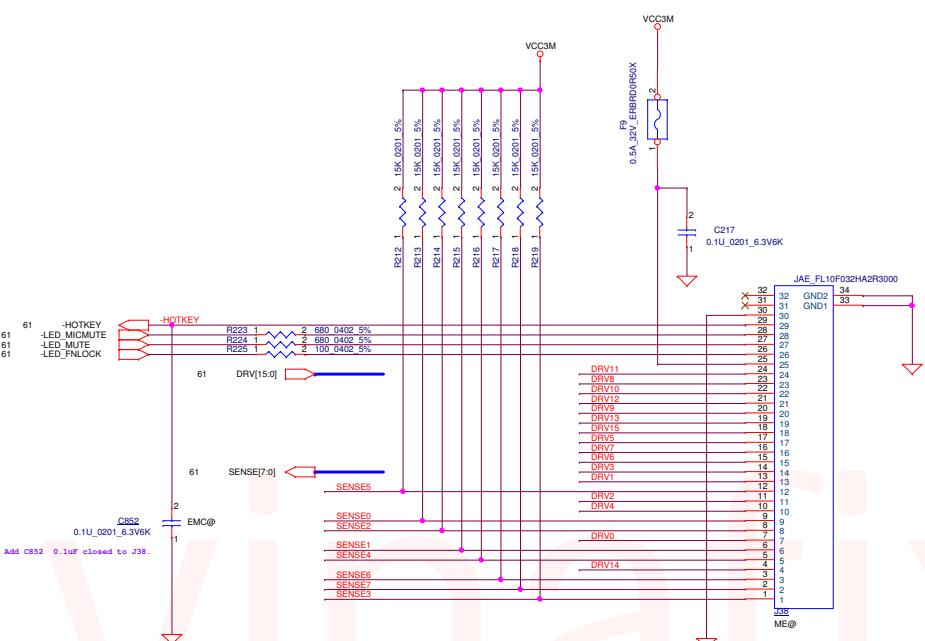
Title: DOCKING CONNECTOR
Document Number: WOLVERINE4 UMA
Rev: 0.3
Size: Custom
Date: Tuesday, December 20, 2016 | Sheet: 60 of 100

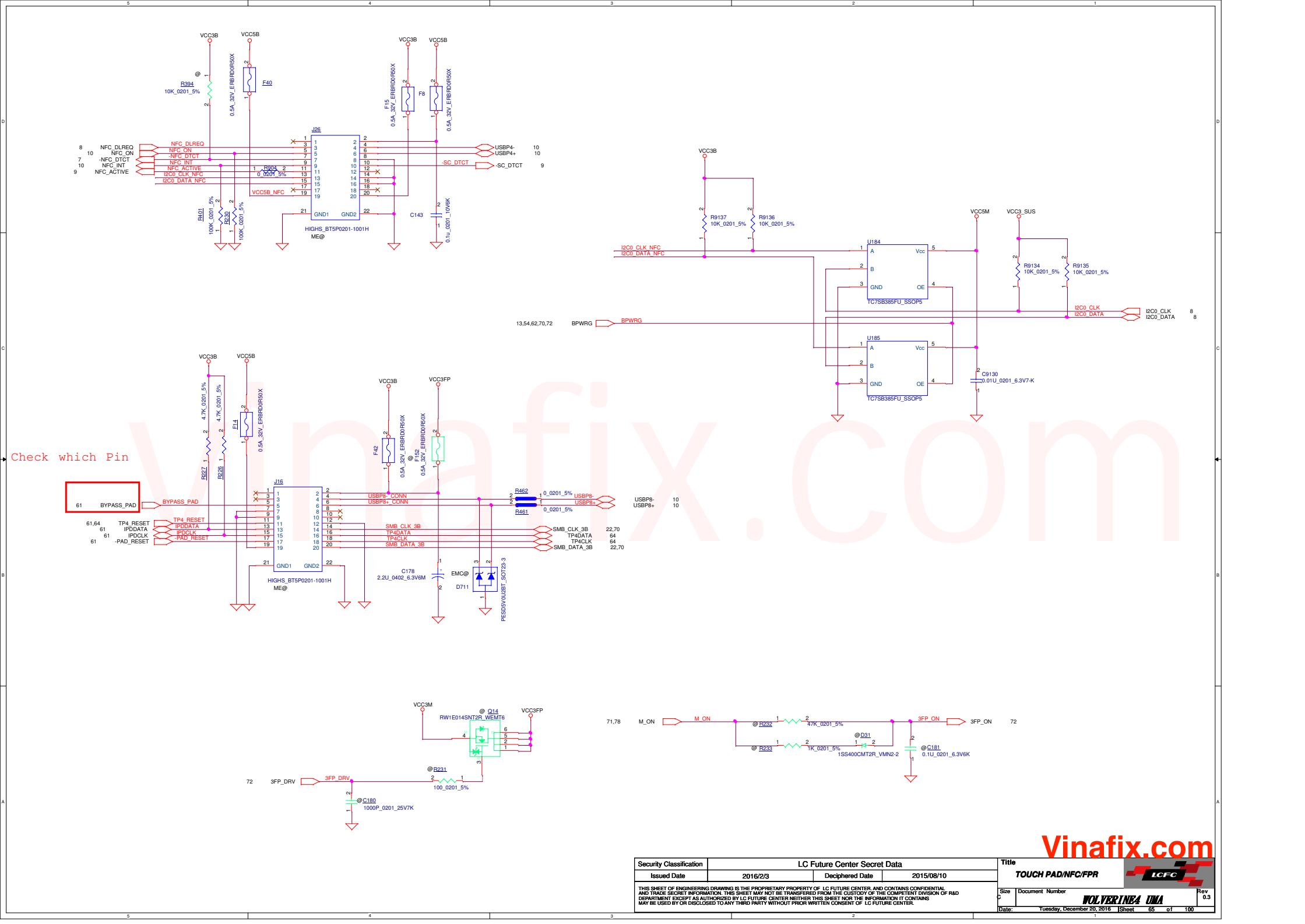




Sensor	Device	Placed on
C161+Q9	CPU DC/DC(PU402)	BOTTOM
C164+Q11	DIMM (J21)	BOTTOM
C167+Q13	WLAN (J32)	BOTTOM
C255+Q25	FAN module	TOP
C163+Q10	Charger (PU101)	BOTTOM
C166+Q12	WWAN(J22)	BOTTOM



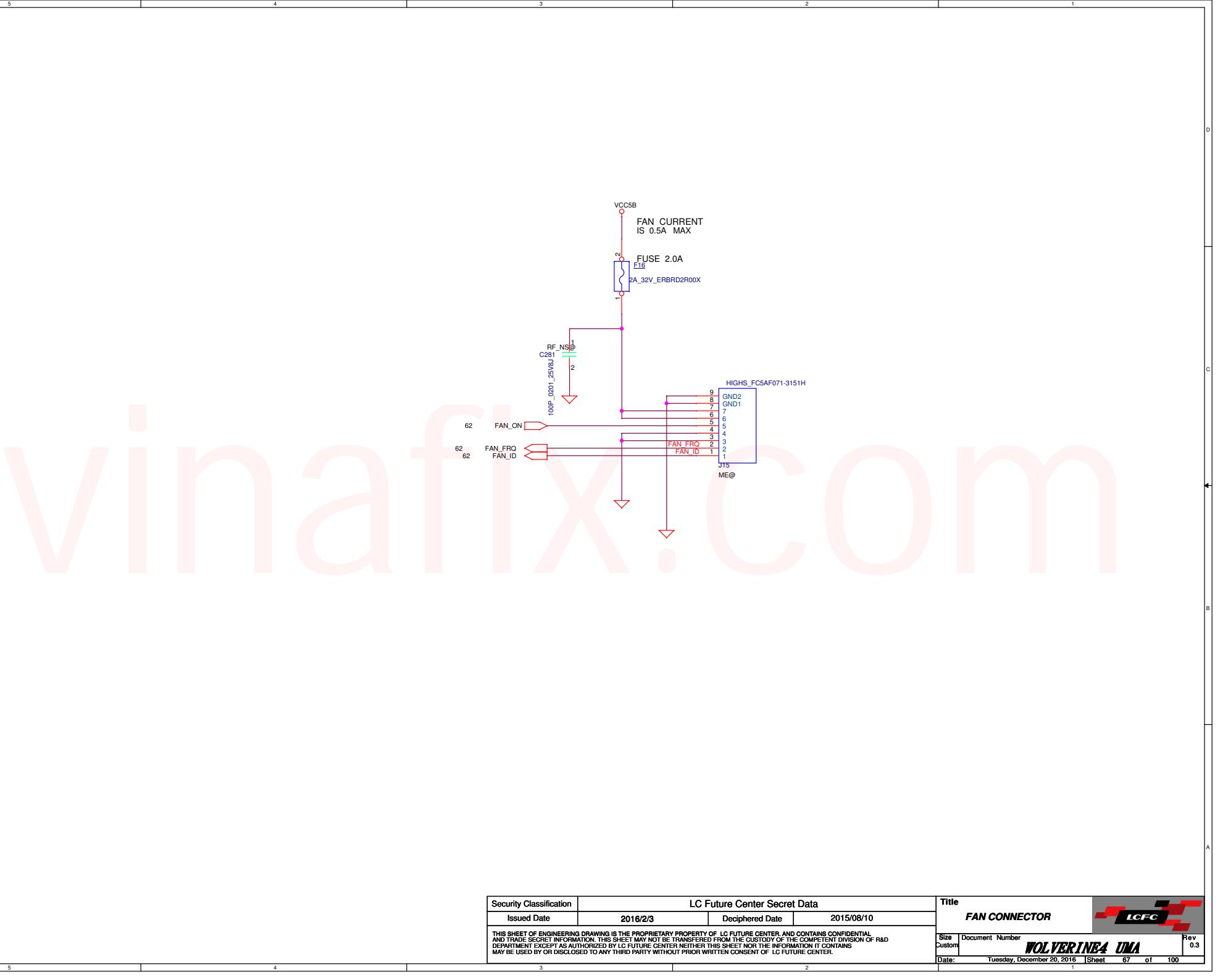




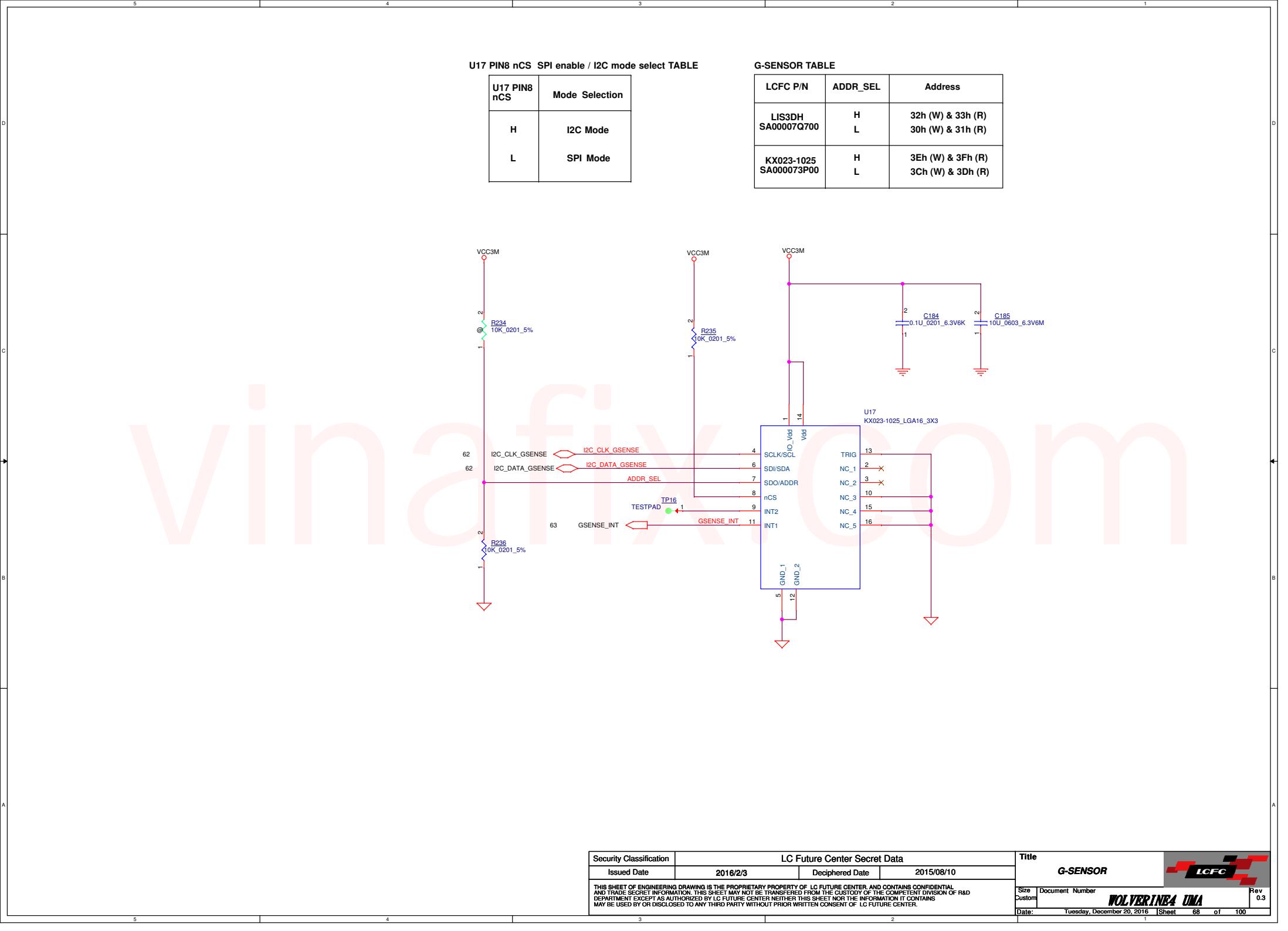
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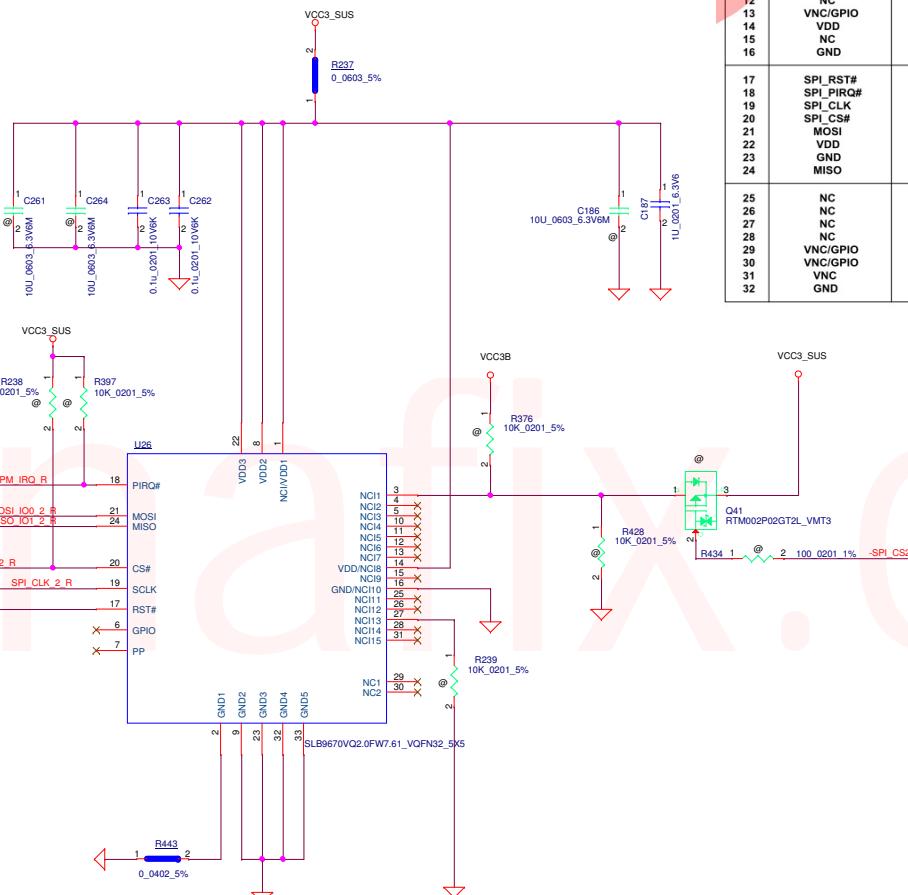


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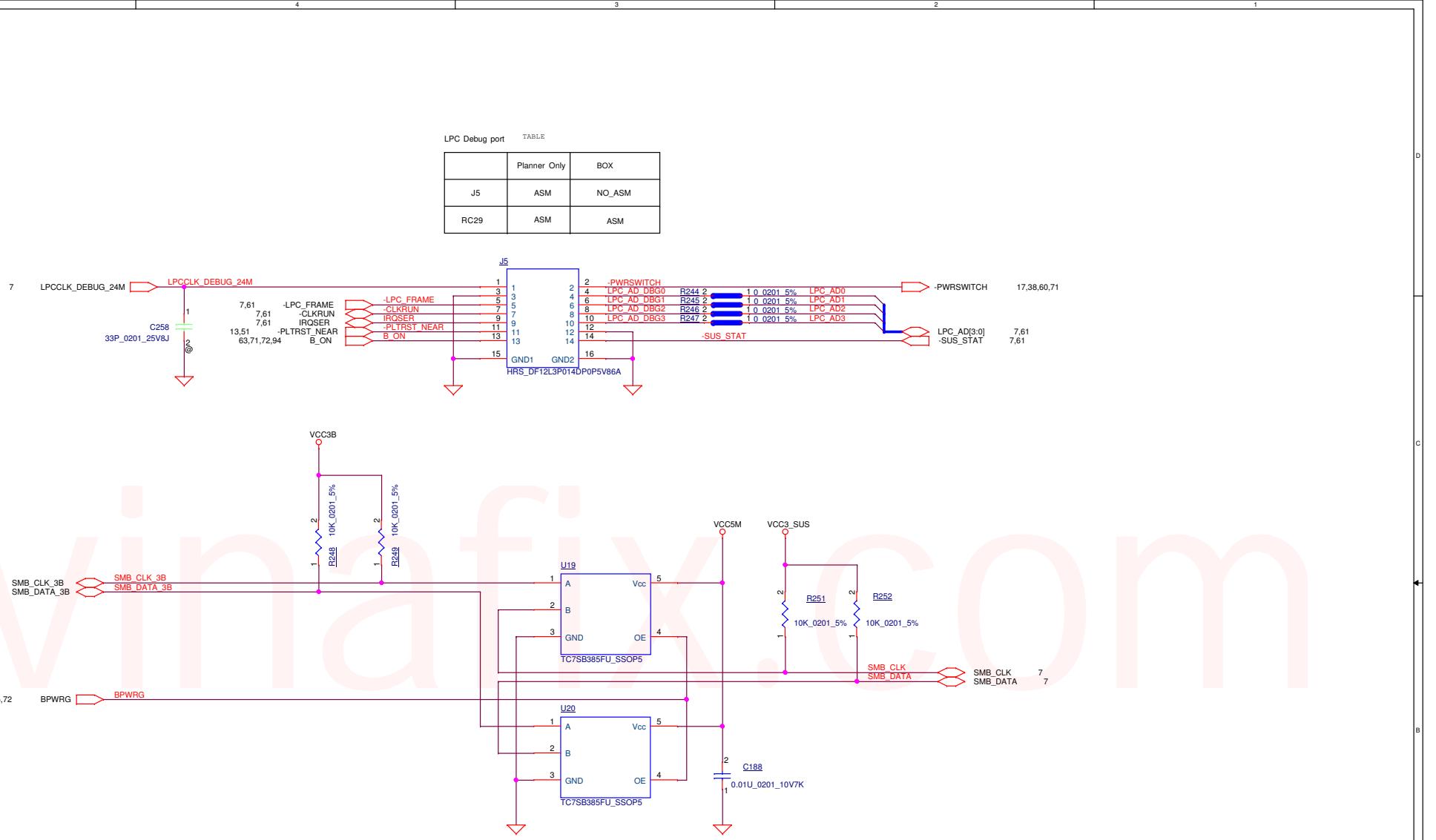


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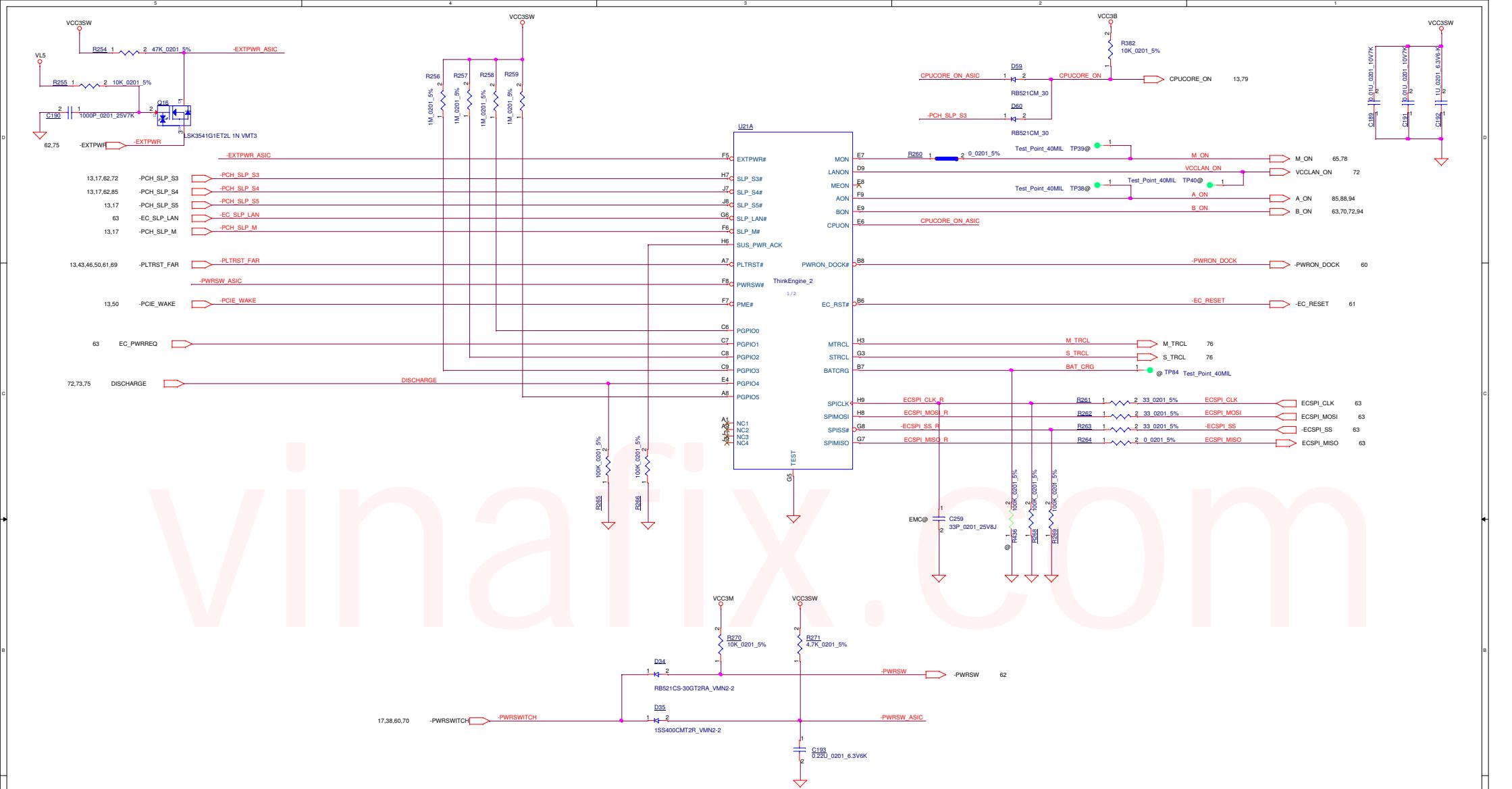
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2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	NC	NC
8	VDD	VDD	GPIO	VDD
9		GND	NC	GND
10		NC	NC	NC
11		NC	NC	NC
12		NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VPS	VDD	VDD
23	GND	NC	NC	GND
24	MISO	MISO	MISO	MISO
25		NC	NC	NC
26		NC	NC	NC
27		NC	NC	(SERIRQ)
28		NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND



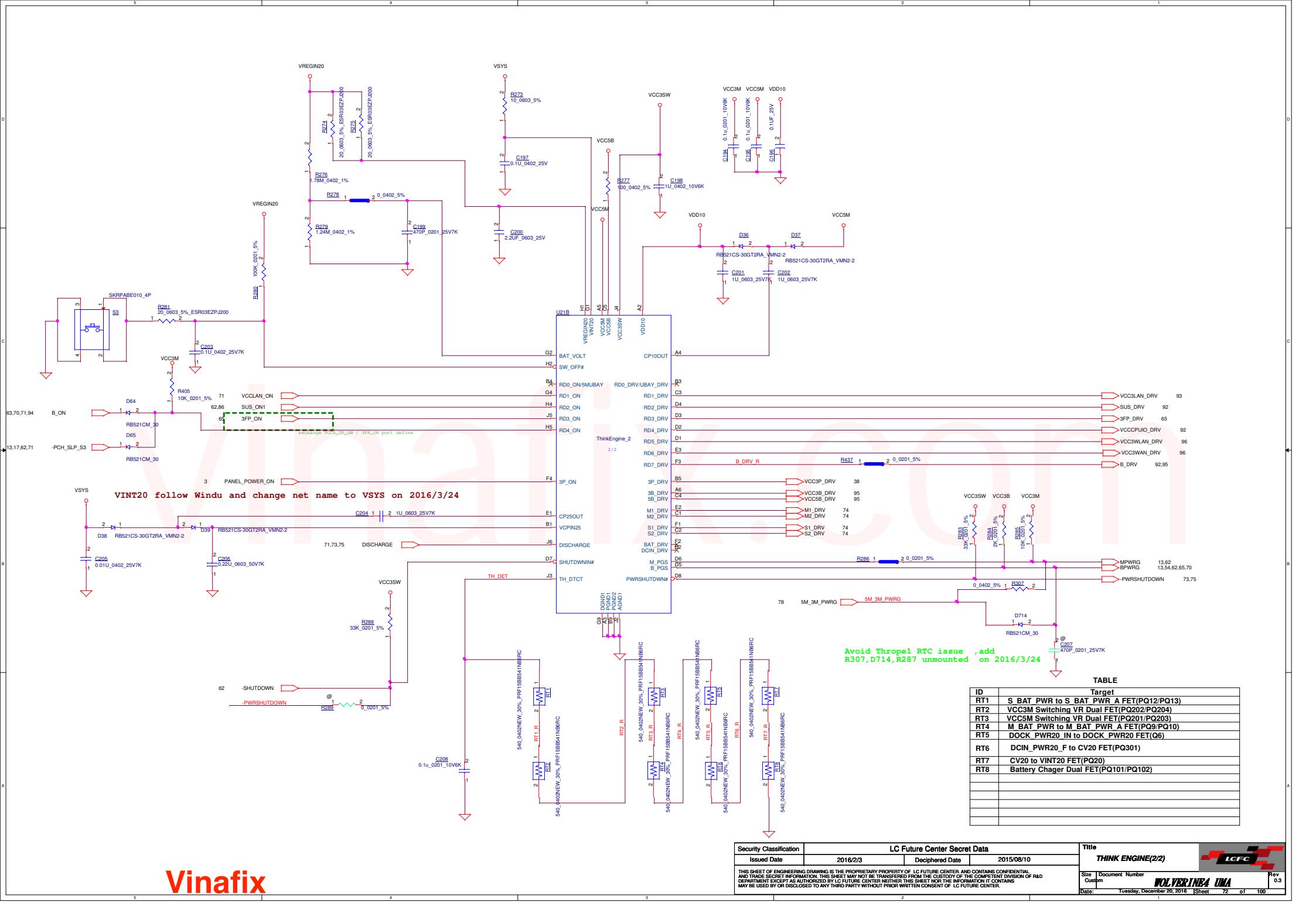
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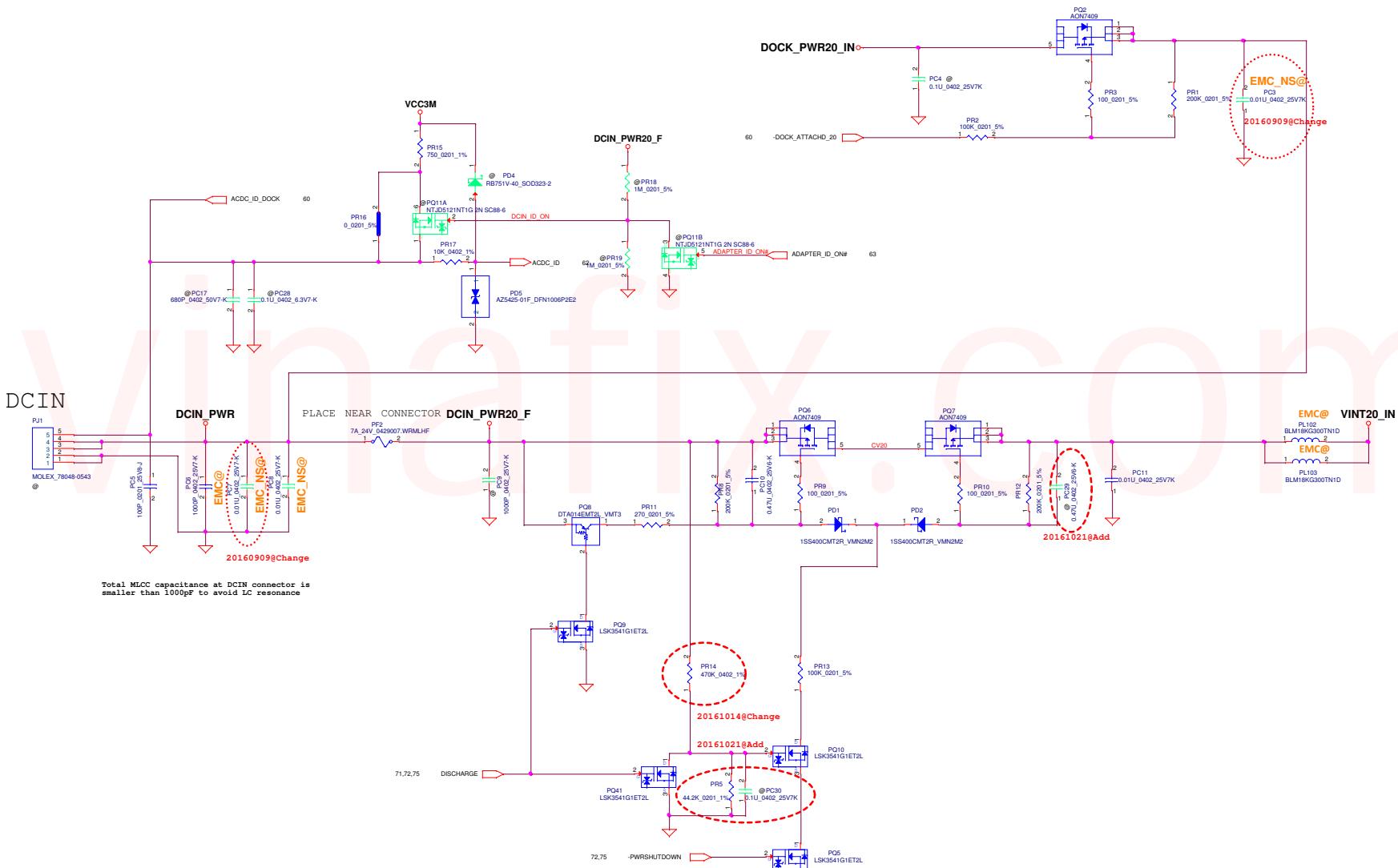


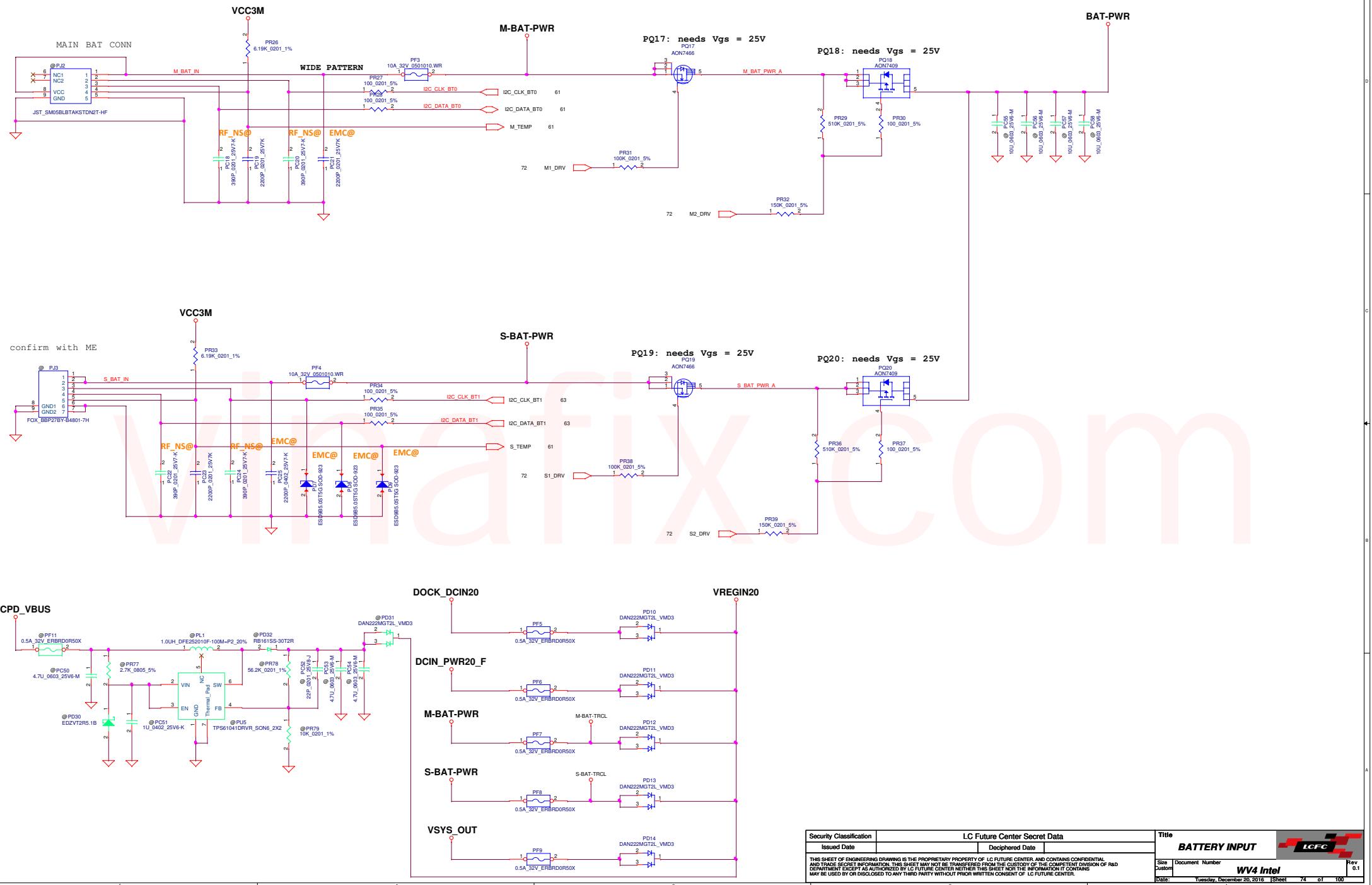
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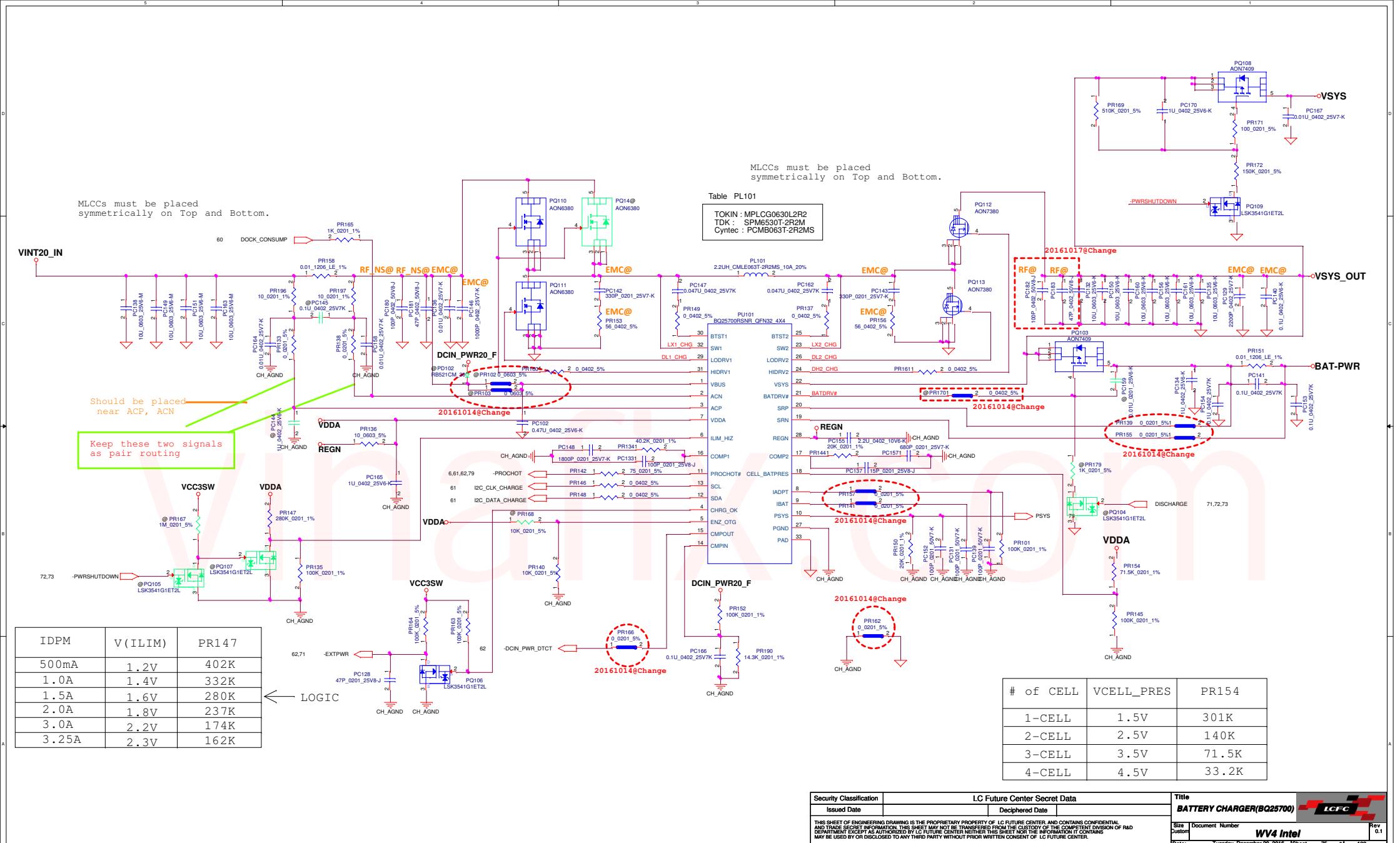
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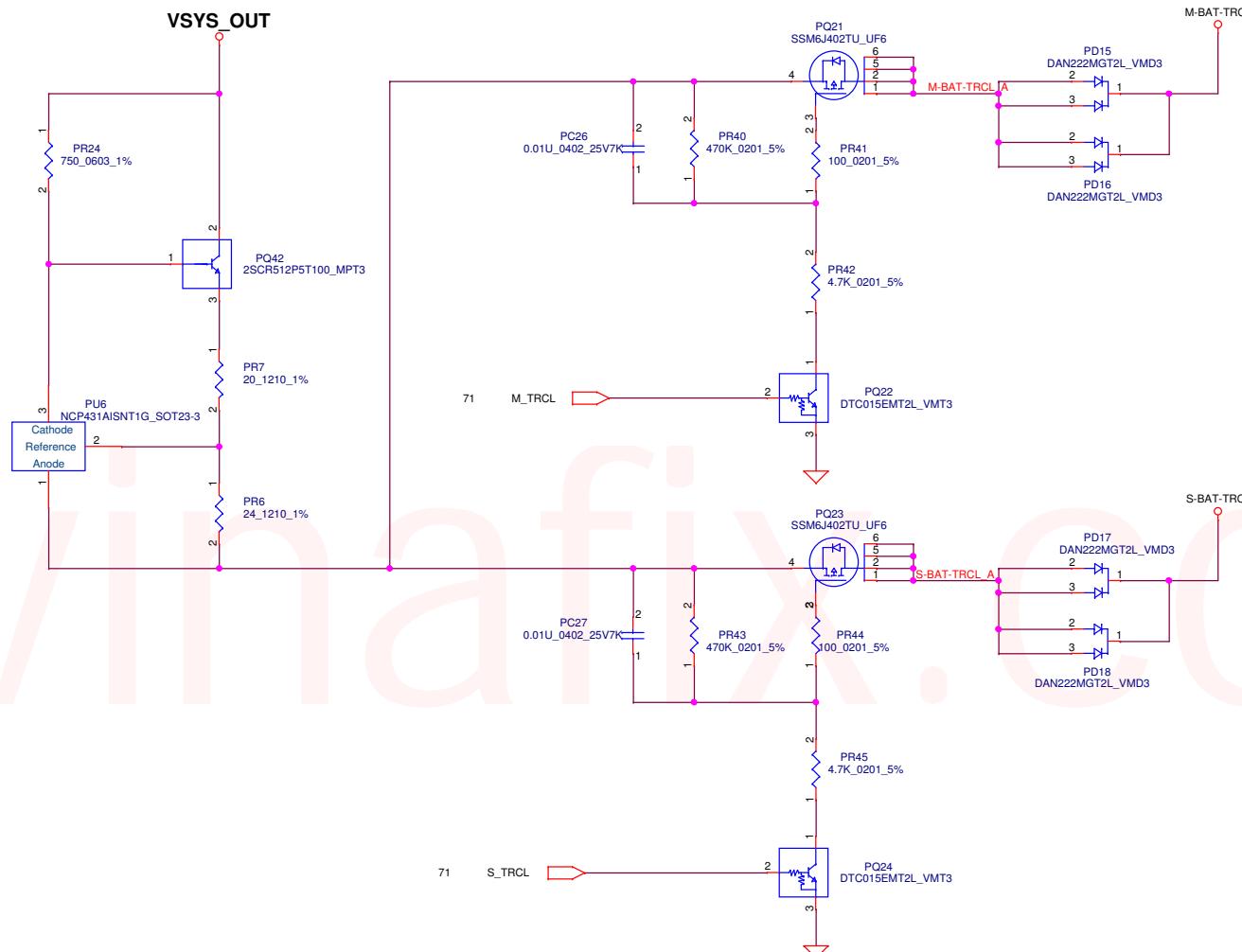






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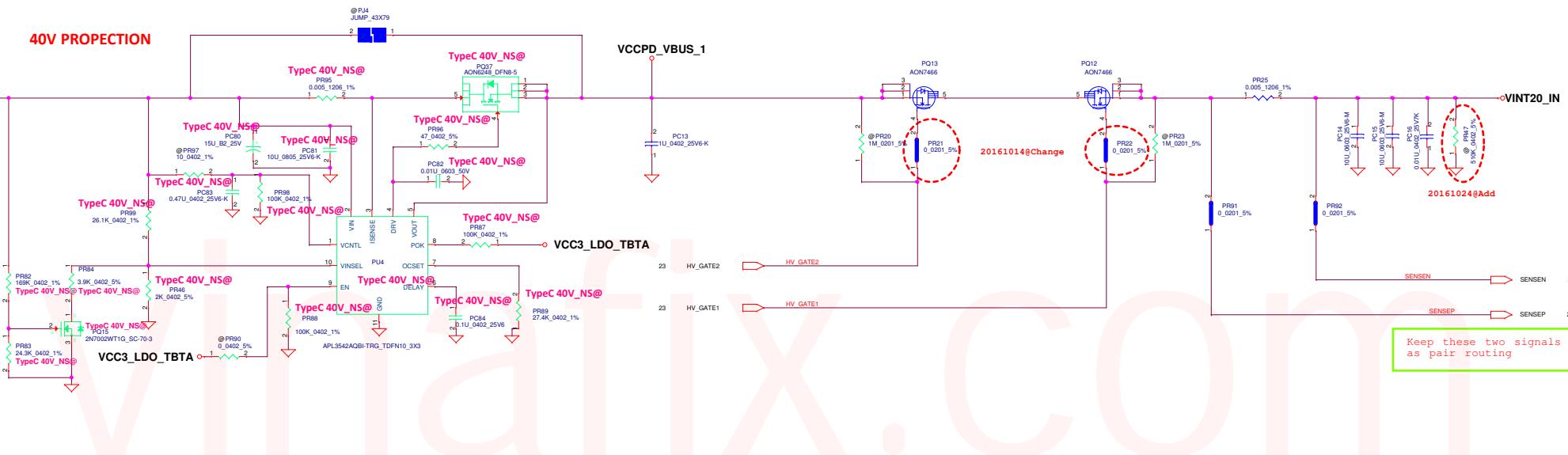
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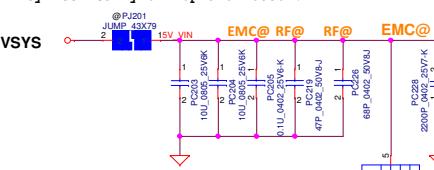


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OCP =12A

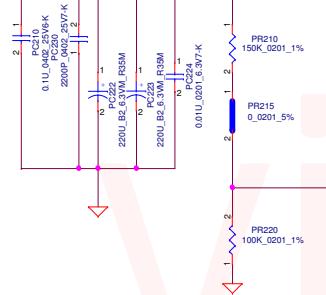
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VCC5MP
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OCP =12A



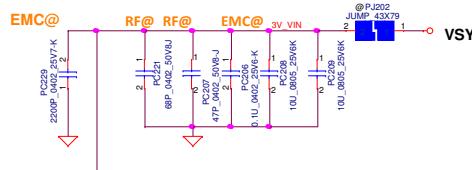
VCC5MP

EMC@ EMC@



VSY5
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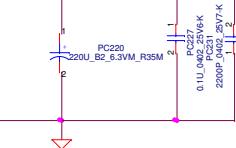
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VCC3MP

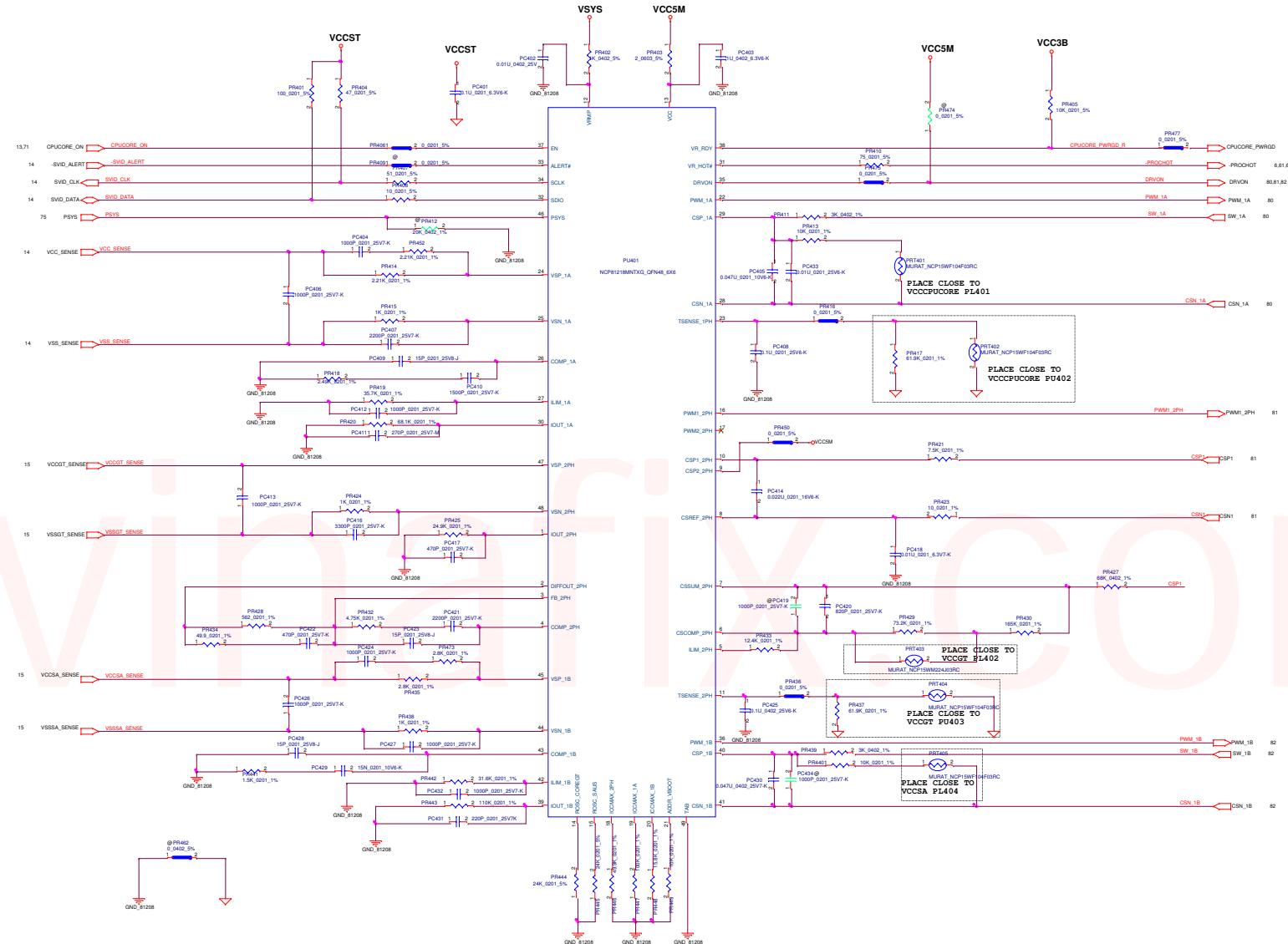
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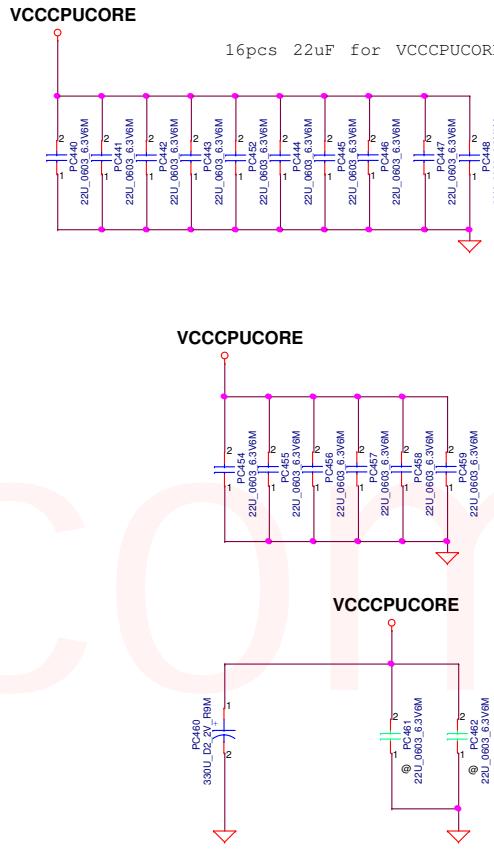
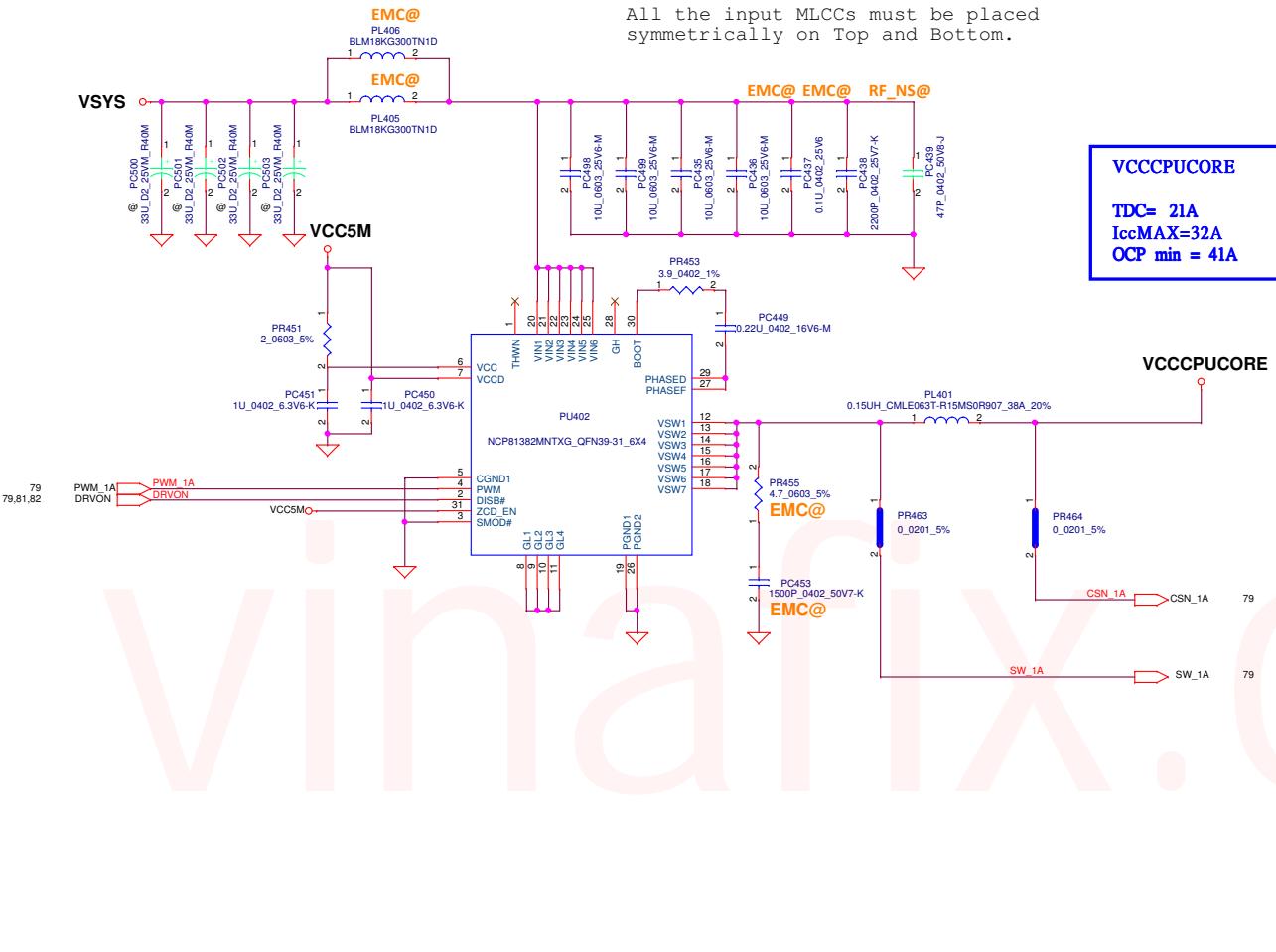
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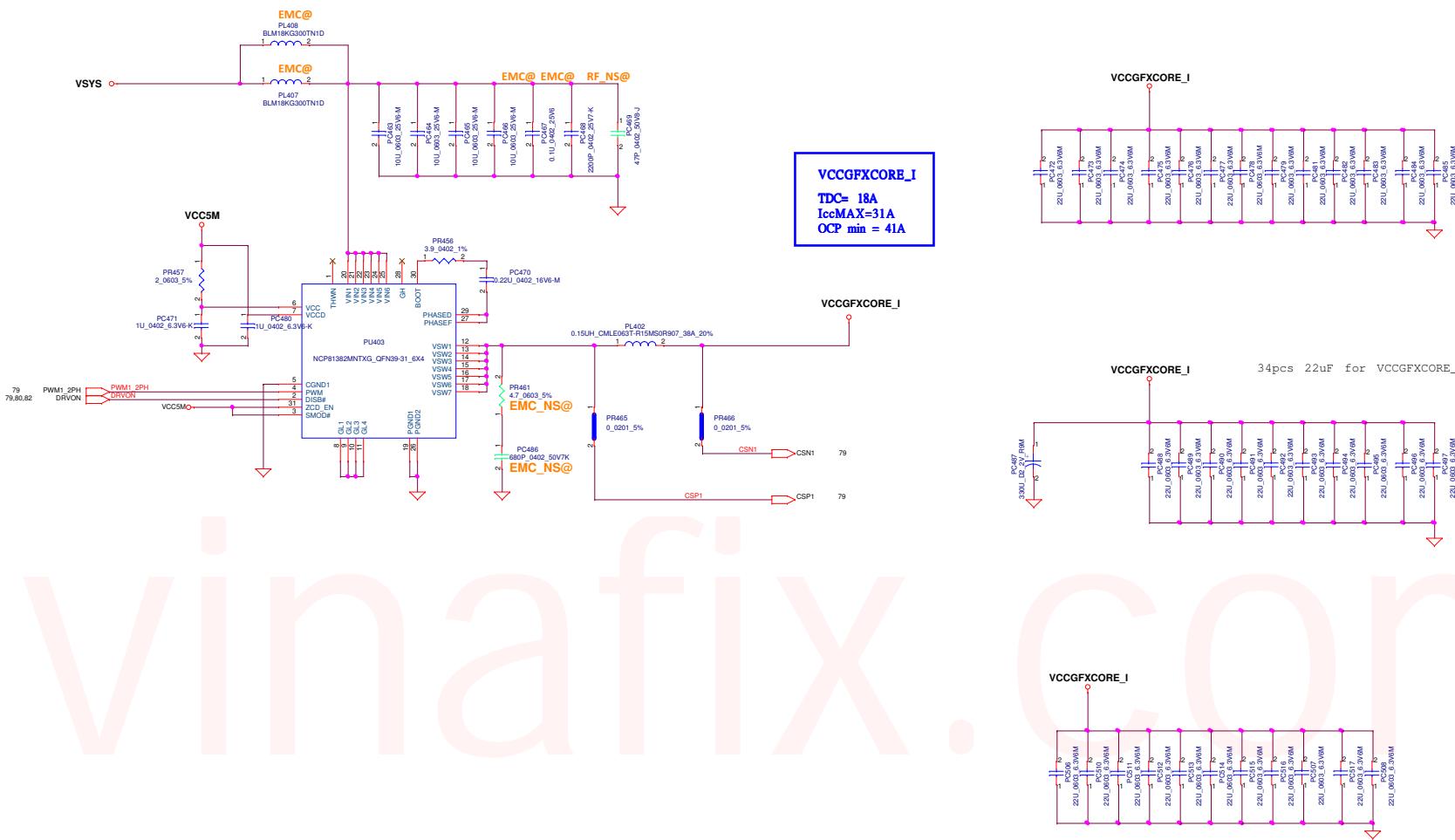
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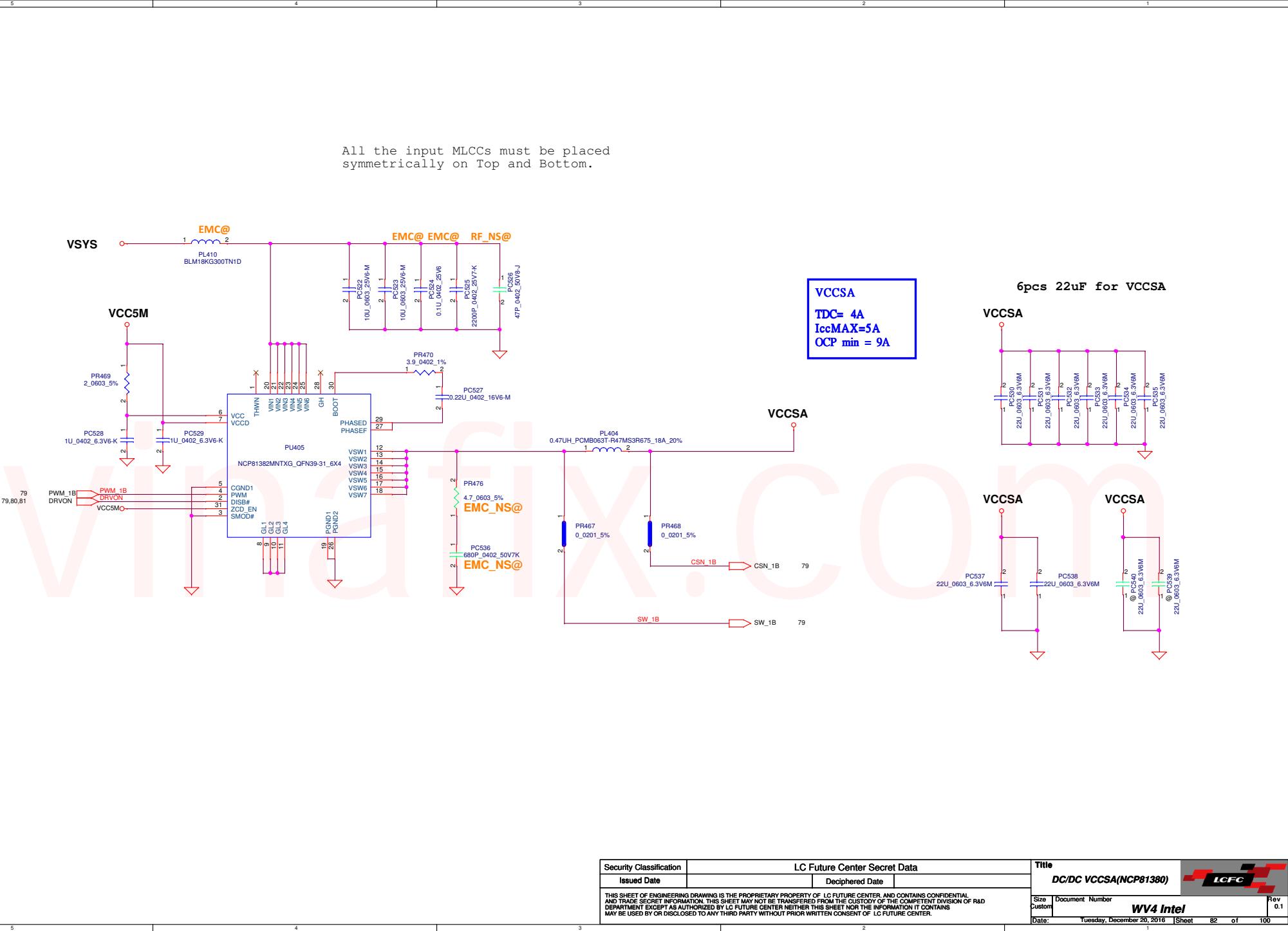
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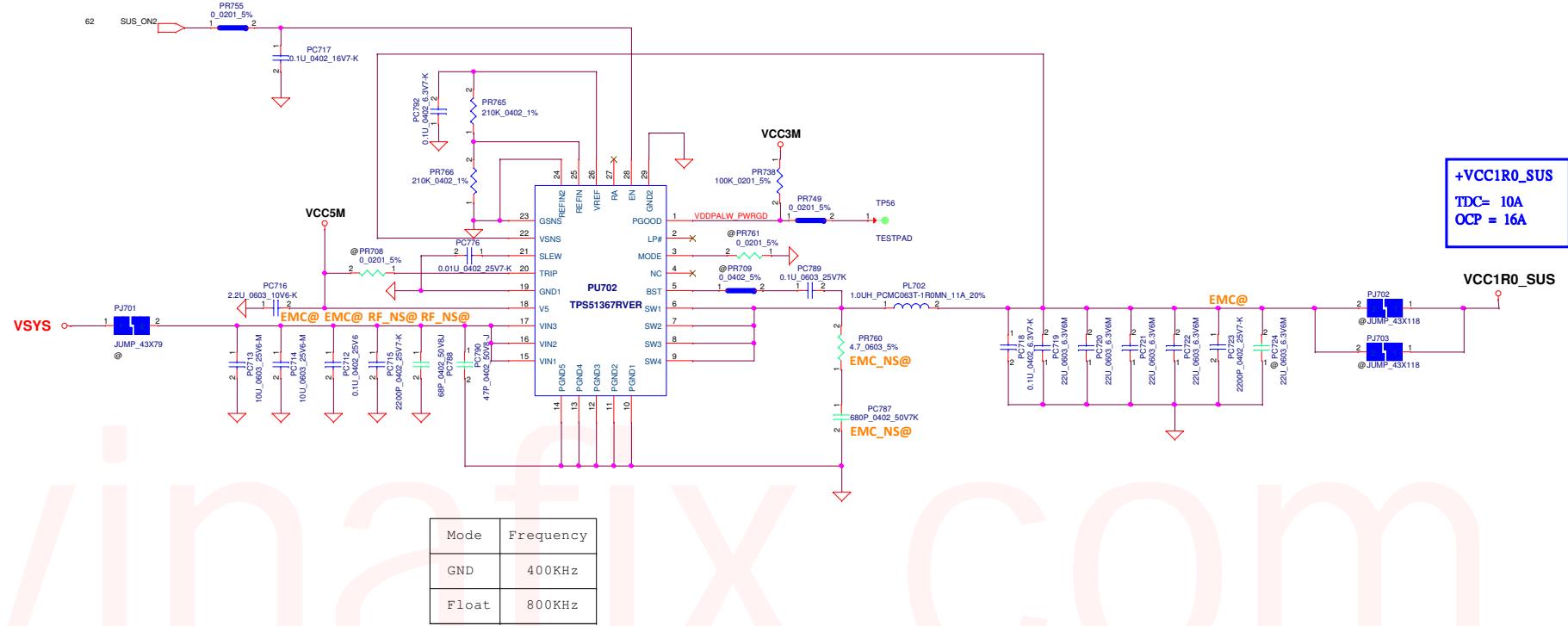


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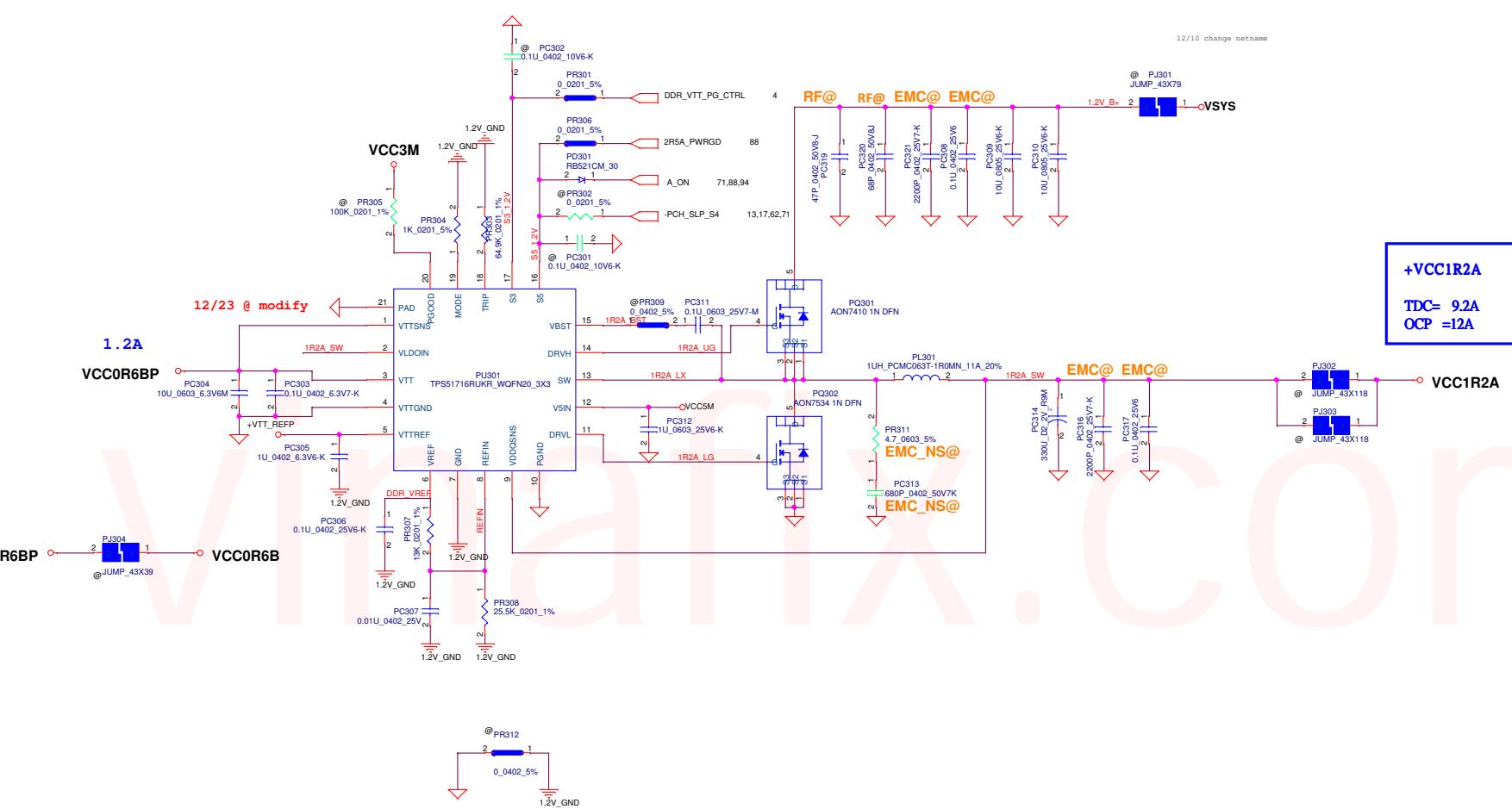


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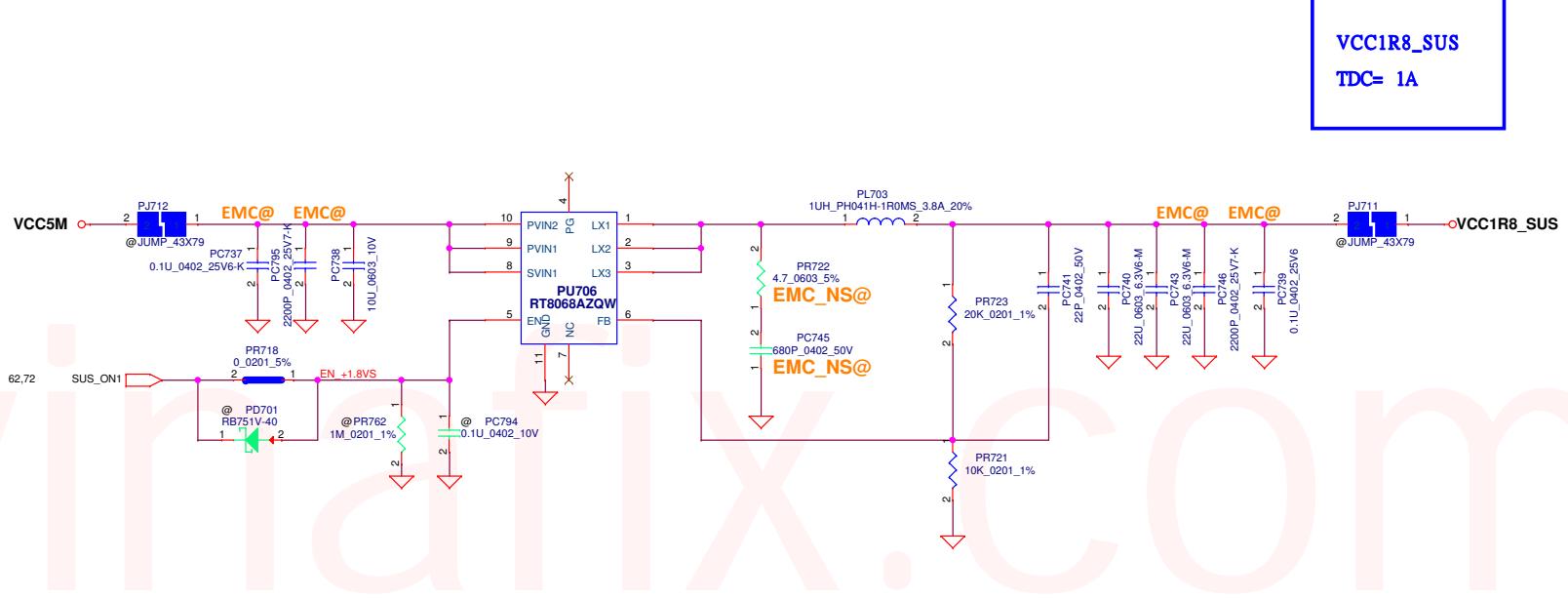
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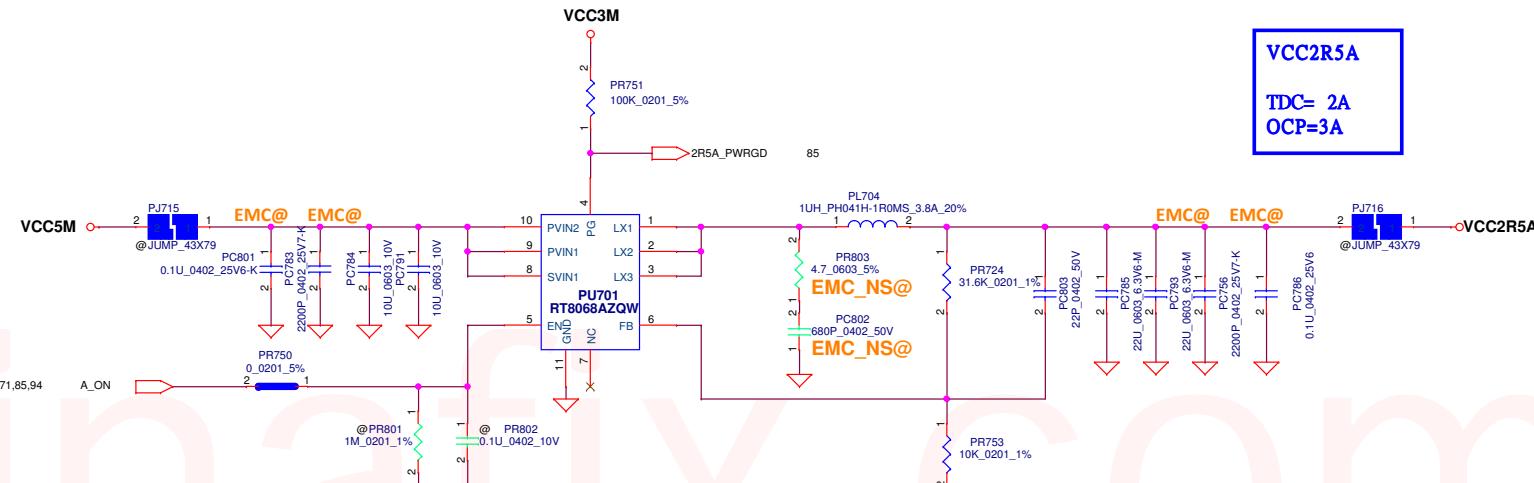
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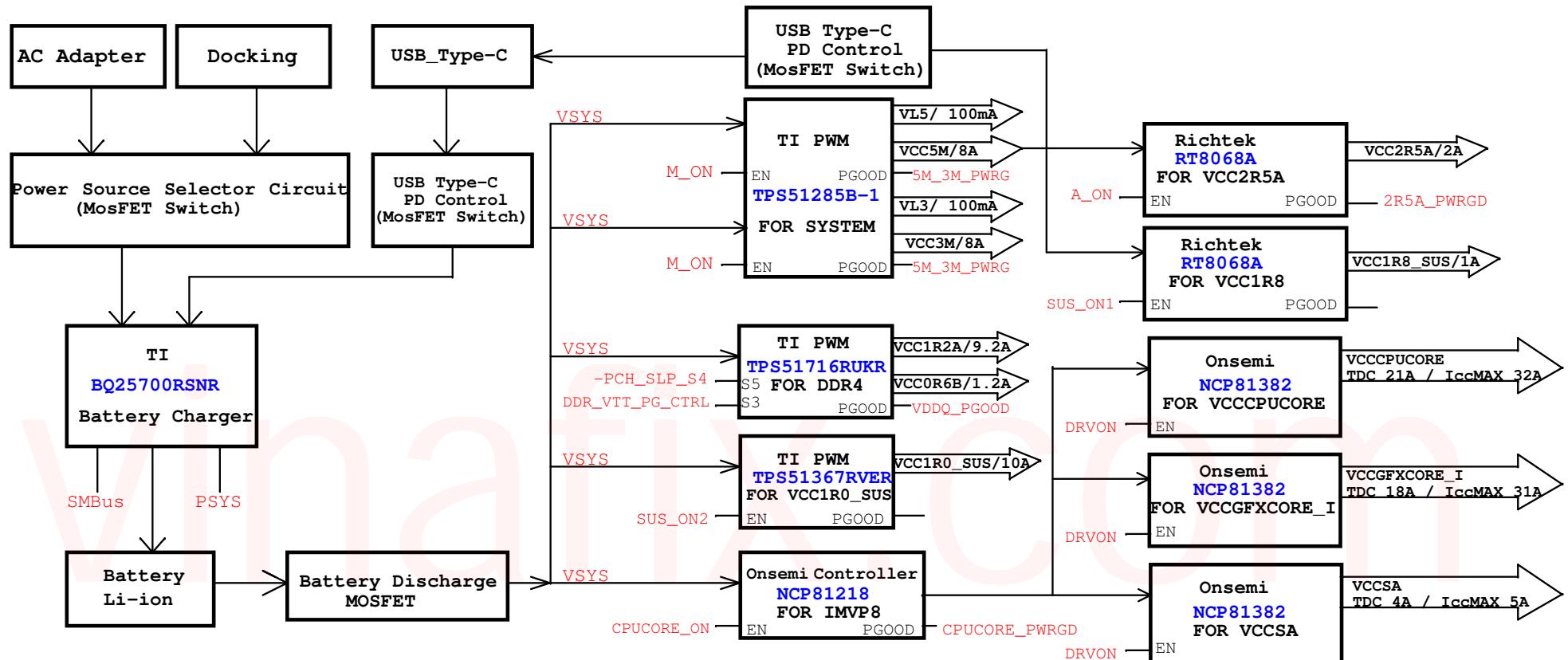
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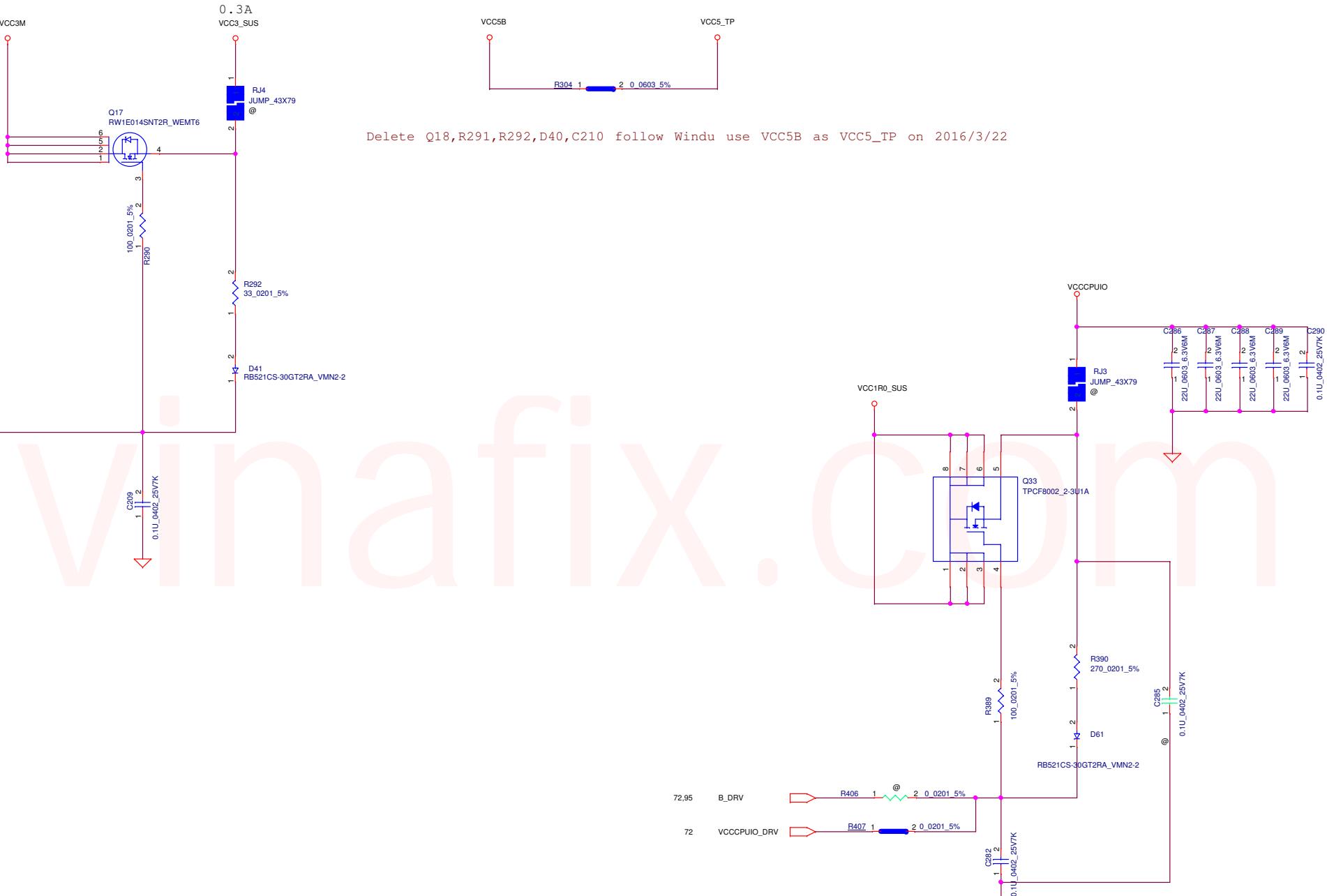
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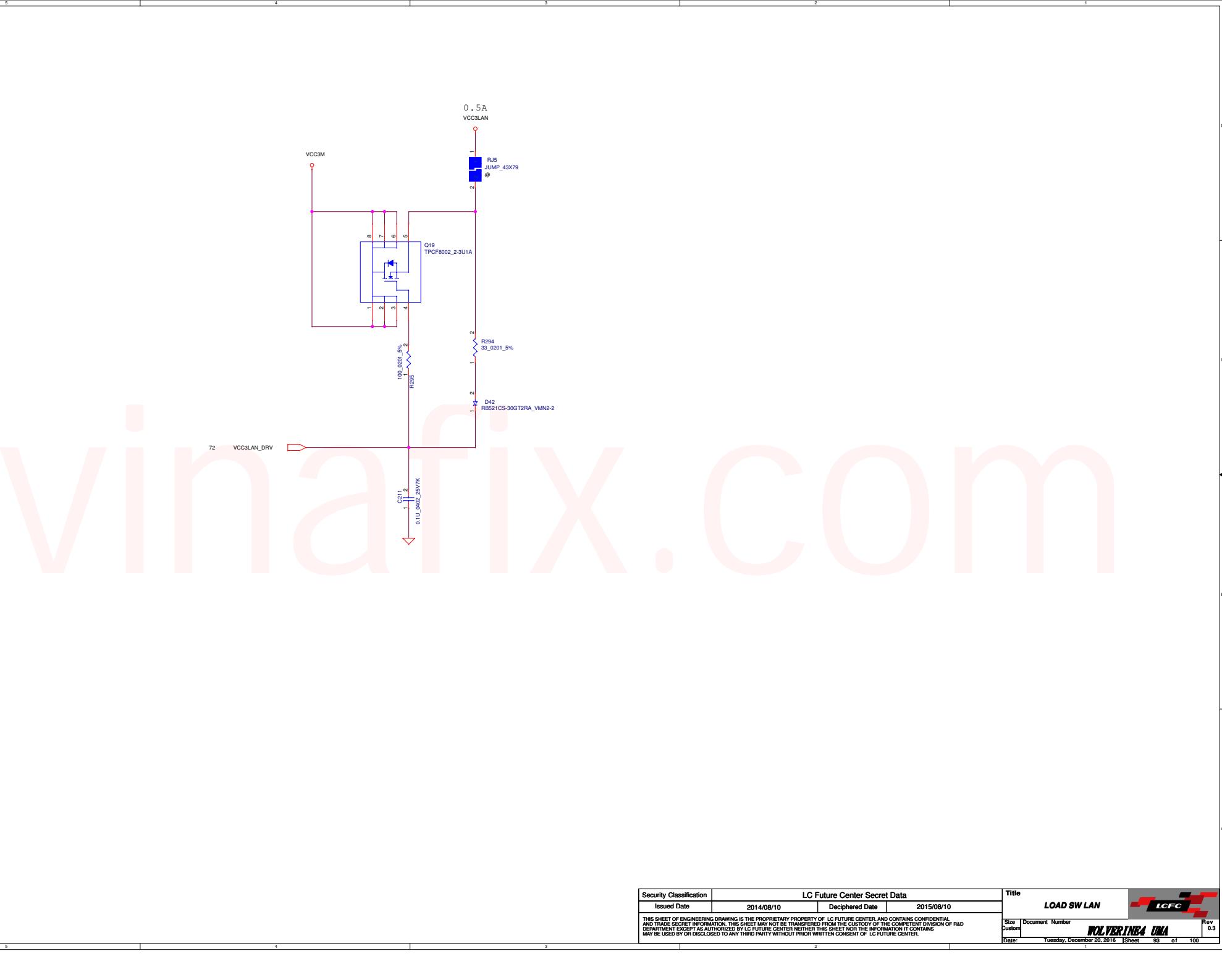
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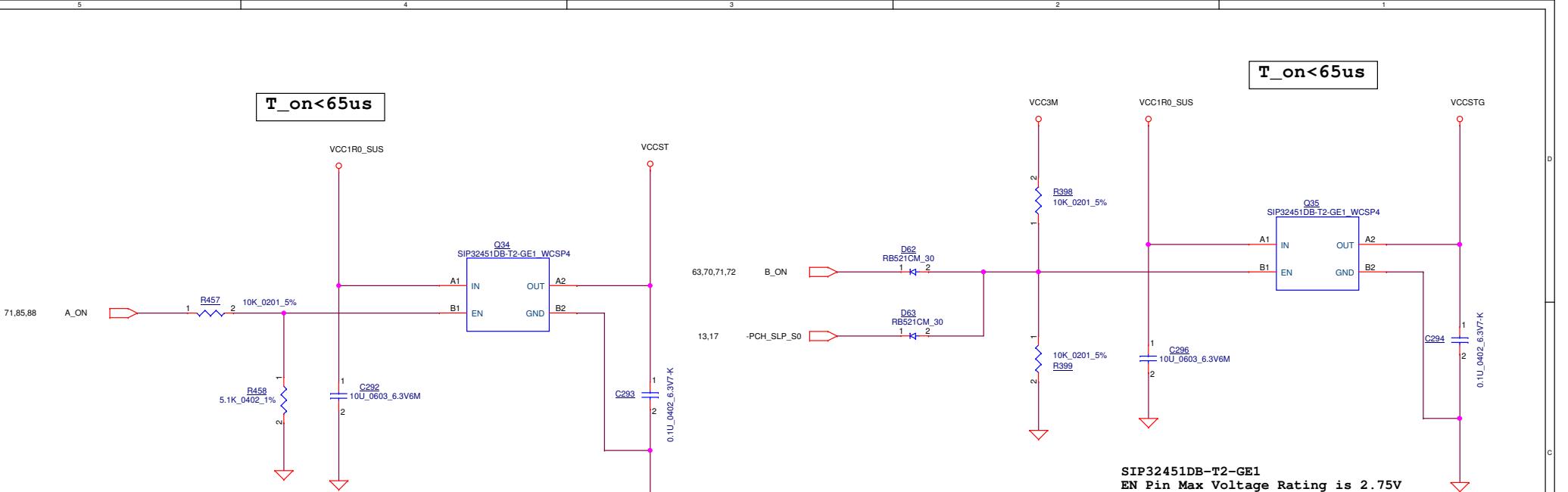
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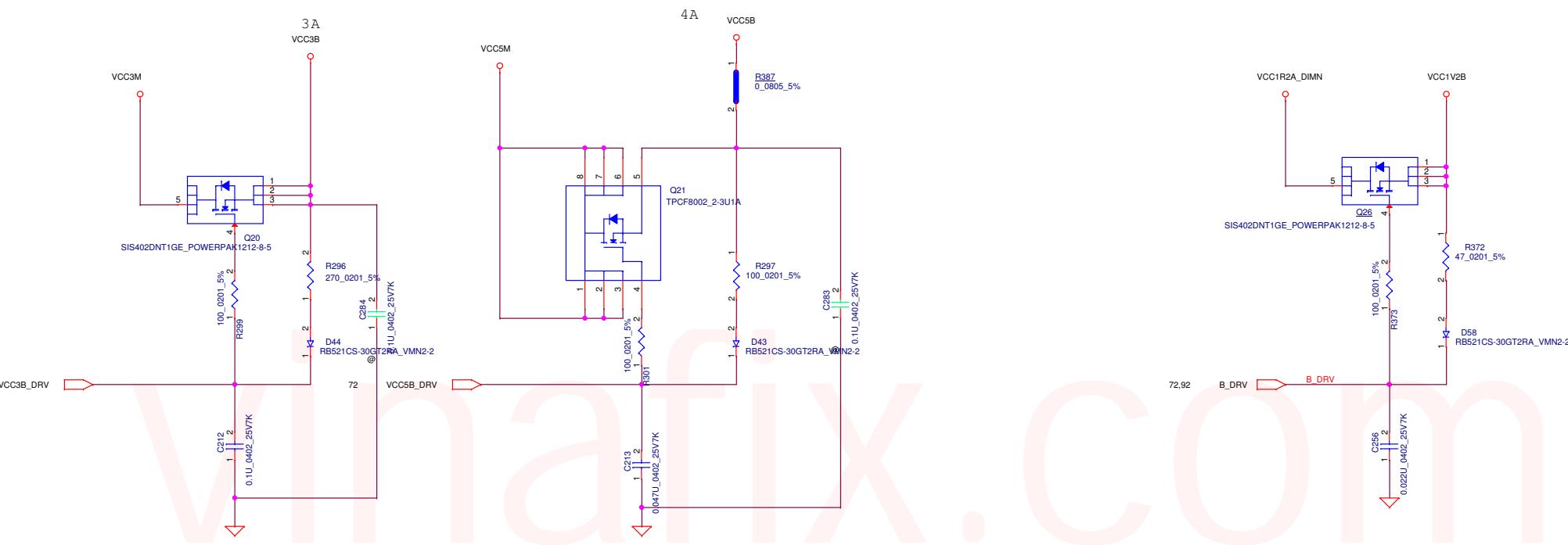
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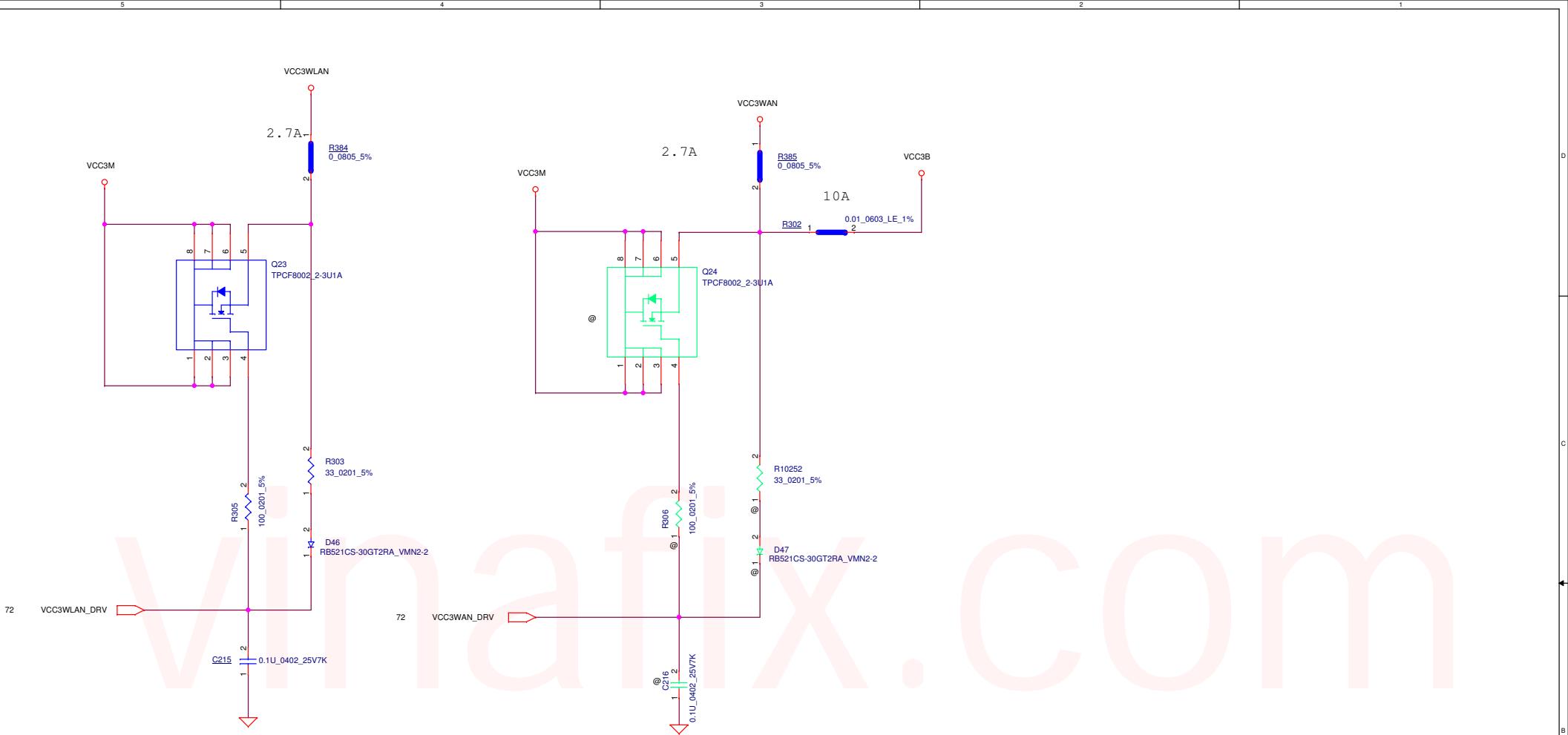
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TABLE

AOAC	YES	NO
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Q94	ASM	NO-ASM
R8924	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

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ST1 HOLEA PAD_C6P5D2P8 ST2 HOLEA PAD_C6P5D2P8 ST3 HOLEA PAD_C5P6D3P4 ST4 HOLEA PAD_CT5P6B6P6D3P4 ST5 HOLEA pad_ct6p5b7p5d3p4

c o b a
H1 HOLEA PAD_CT7P0B6P5D3P5 H2 HOLEA PAD_CT7P0B6P5D3P5 H3 HOLEA PAD_CT7P0B6P5D3P5 H4 HOLEA PAD_CT7P0B6P5D3P5

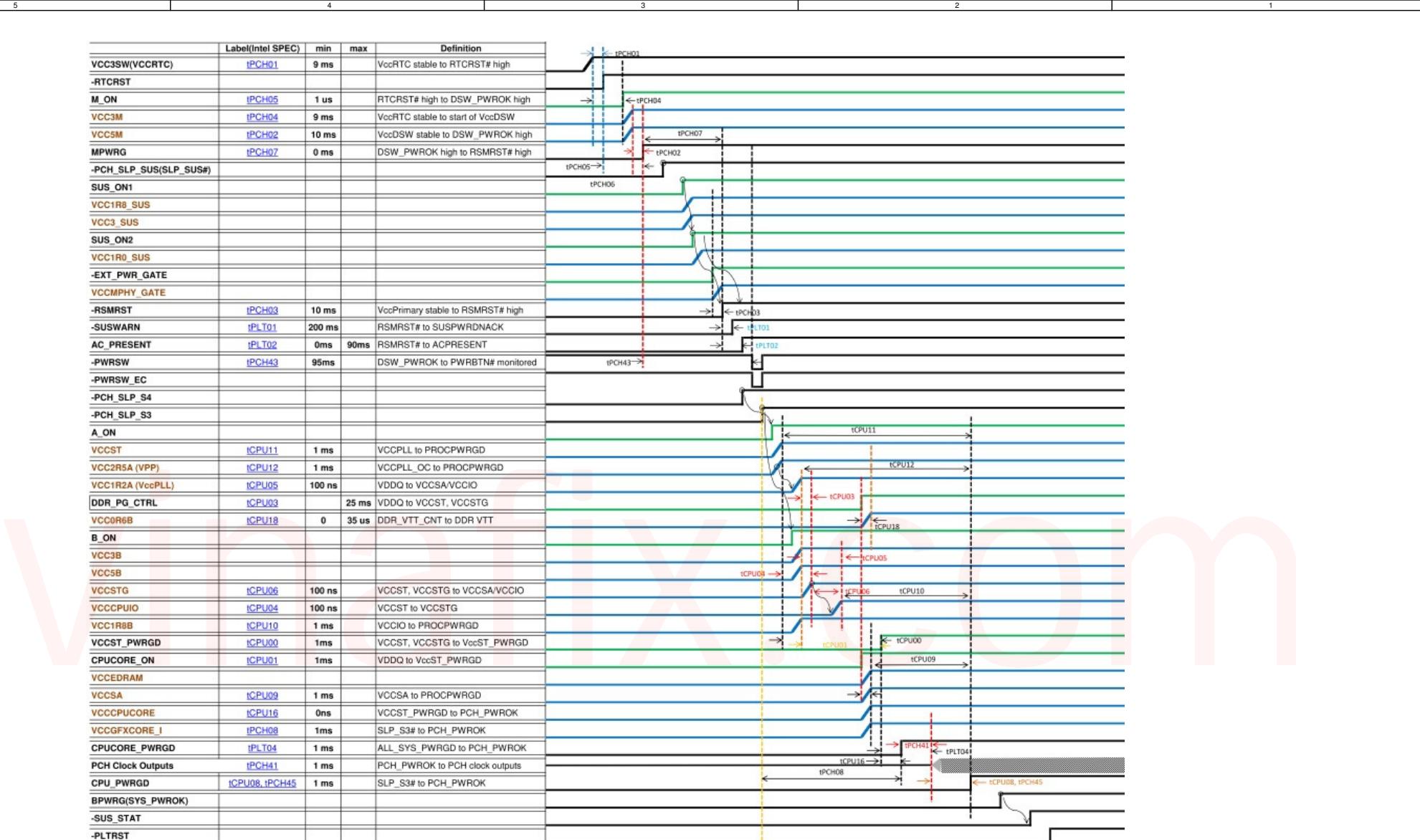
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H5 HOLEA PAD_C6P5D2P8 H6 HOLEA PAD_CT6P5D1P9 H7 HOLEA PAD_CT9P6D6P7 H8 HOLEA PAD_CT7P0B8P4D2P8

H13 HOLEA PAD_CT5P0D1P8X2P6 H14 HOLEA pad_ct6p5b8p0d2p5 H15 HOLEA PAD_CT4P0B2P7D1P7

H16 HOLEA PAD_C6P5D2P5

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