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CAD Note:
Default component footprint is SMD 0201, X5R, 1% resistors.

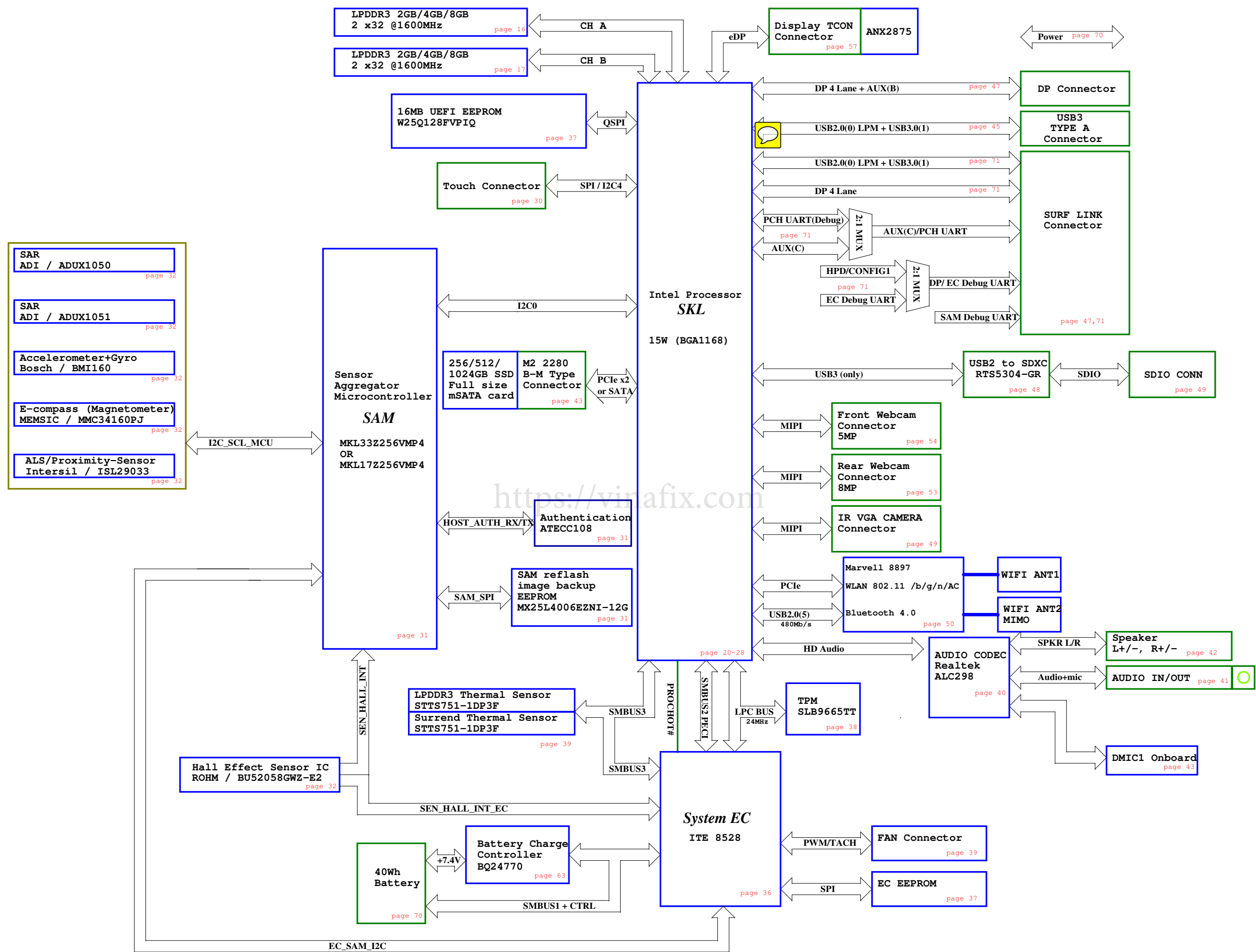
Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

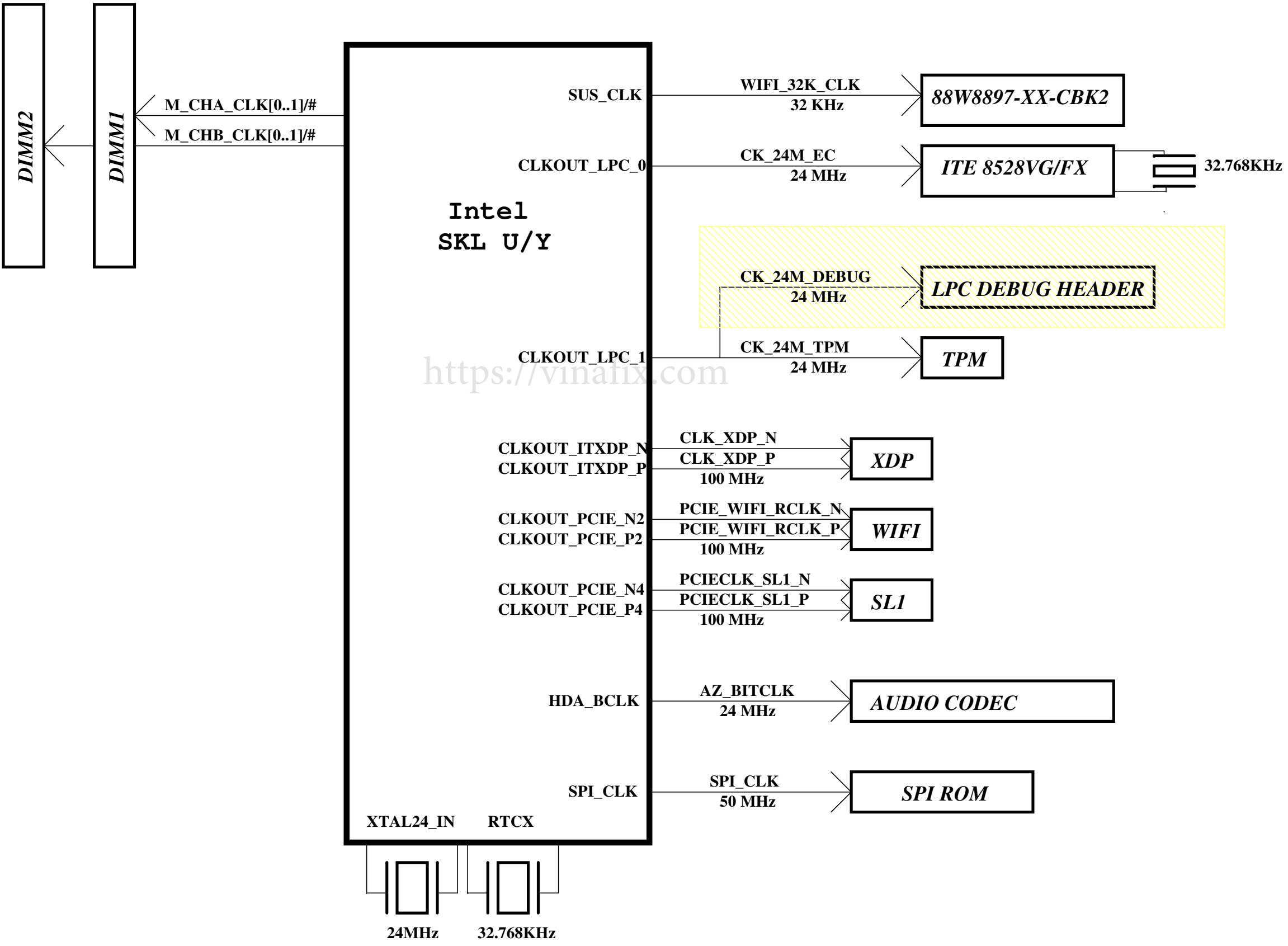
Schematics Change History

Rev.	Date	Comments
Op9	28 Oct 2014	1. Starting with G_EV1_1021-1630.DSN 2. Added SL schematic from page 72 ...\\T\\MB\\DV_RELEASED\\Schematic\\CASTLE2_DV_2014_1021_1100.DSN 3. Added External USB3 schematic from ...\\T\\MB\\DV_RELEASED\\Schematic\\CASTLE2_DV_2014_1021_1100.DSN 4. Added external DP ...\\T\\MB\\DV_RELEASED\\Schematic\\CASTLE2_DV_2014_1021_1100.DSN 5. Added IR_CAMERA from Front Camera...put in page 49 6. Removed page 73 PCIe GPU 7. Added Blade from T 8. Removed P72 T2B Pwr Transistors
Op10	3 Nov 2014	1. Changing to NVDC 2. Replaced GTX with GT, kept bypass caps 3. Replaced Charger with BQ24770
Op11	3 Nov 2014	1. Replace SKL-U with SKL-Y
Op12	11 Nov 2014	1. Model DDR connection from Intel SDS
Op13	18 Nov 2014	1. Added FUB information to all components 2. Changed Decretes.. sizing caps
Op14	20 Nov 2014	1. Added +5VA_SHA 2. Added T Cost Down/XCN's 3. Added SL +5V load Switch & Caps 4. Added Blade +5V load Switch & Caps
Op15	26 Nov 2014	1. Removed Boost 2. Re-adjusted usb ports on CPU 3. Removed Audio DSP
Op16	03 Dec 2014	1. changed +1VSB regulator 2. changed IR Camera/added diode 3. added power numbers from 0.91 PDG, Oct14 4. changed BLADE connector 5. cpu decoupling caps changed 6. changed +5V/+3V inductors (place holder)
Op17	05 Dec 2014	1. swapped M_A_CAA with MA_CAB on U1601/U1602 2. added two SAR chips, P32 3. remove tp's from csi lines on (p23) 4. change from 10 ceramic to 3 tantalum-poly on usb3 typeA (p45) 5. remove the RSENSE from output of +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) 6. change RSENSE input to 0402 from 0603 for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) input regulator 7. change inductor for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58) to HMLE20161B-1R0MDR-01 8. change RSENSE input to 0402 from 0603 for +5V_TS,+5V_SDXC,+5V_AUDIO,+5V, +5V_FAN(p64) 9. change RSENSE input to 0402 from 0603 for +3P3V_PANEL,+3P3V,+3P3V_SENSOR,+1P8V_DMIC (p65) 10. Replacing the SL connector with X908351-001 11. Replace PL5901 and PL5902 with CMLE042T-2R2MS-01 12. Replace 0402 1uF 6.3V with 0201 1uF 6.3V X5R 13. Replace L7201 with TOKO #A919CY-100M 14. Added VSYS -> BLADE FANG supply (p73)
Op18	09 Dec 2014	1. Reduced sizes of parts for Cameras (Resistors/Caps/Regulators)
Op19	12 Dec 2014	1. All 47uF caps become 0805/1mmZ 2. All 10uF caps become 0402...4V/6.3V
Op20	15 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x4 2. Shui Changes 3. more Shui Changes
Op21	16 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x5 2. changes from EV_schematic_issue_check_1216_JDM1.xlsx 3. changed name of +6_12 to +V_ALWAYS_ON 4. Removed 2 Mikes & Front Mike & added FPC conn 5. Added 2nd BLADE connector
Op22	17 Dec 2014	1. Replaced SD connector with AY531465T 2. changes from EV_schematic_issue_check_viola_1217_JDM1.xlsx
Op23 current		1. See apexUfixes_revXpXX.xlsx

CAD Note:
Default component footprint is SMD 0201, X5R, 1% resistors S = Short after design fixed
Property: BUILD-OPT
DNP = Not Installed Part.

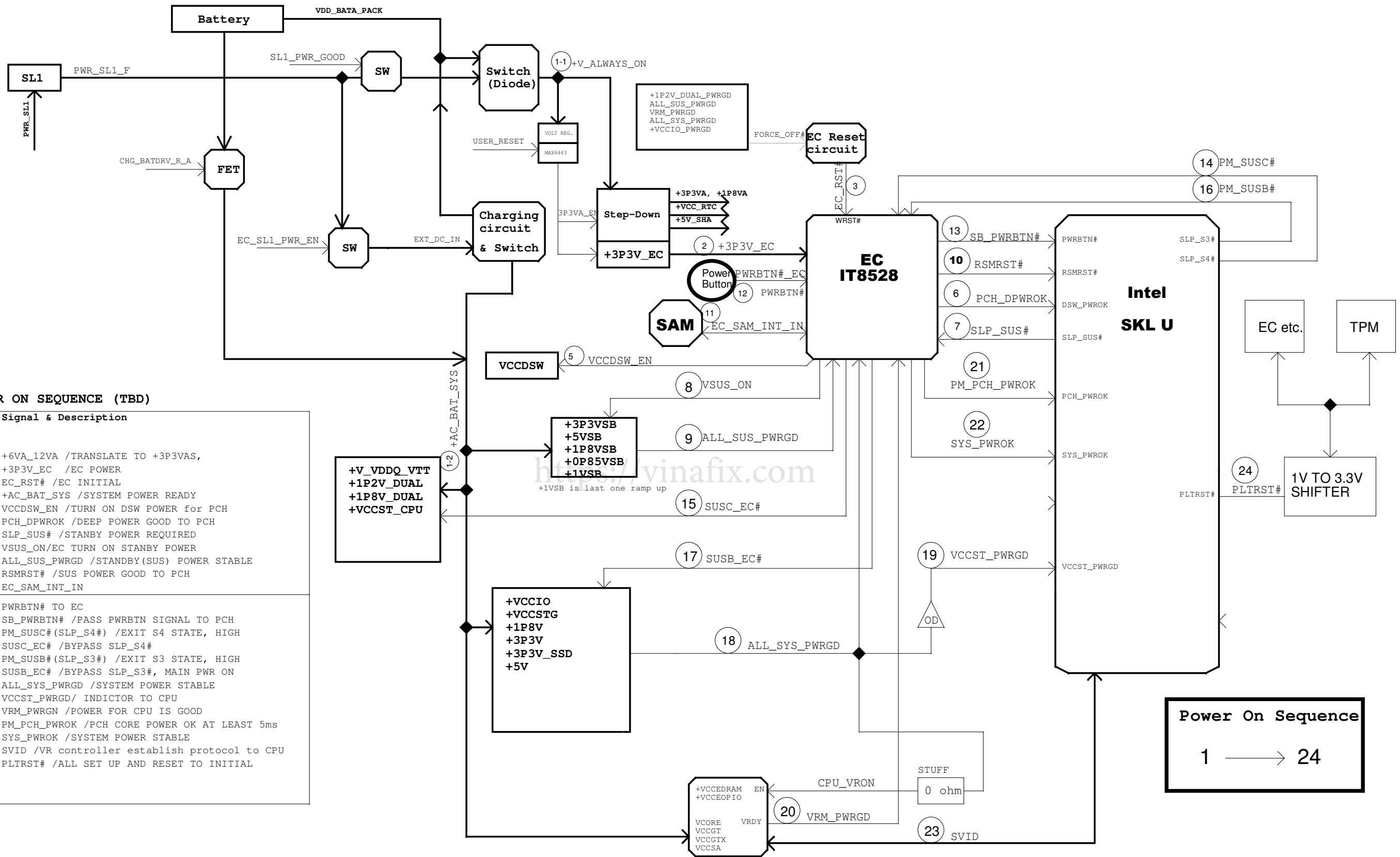


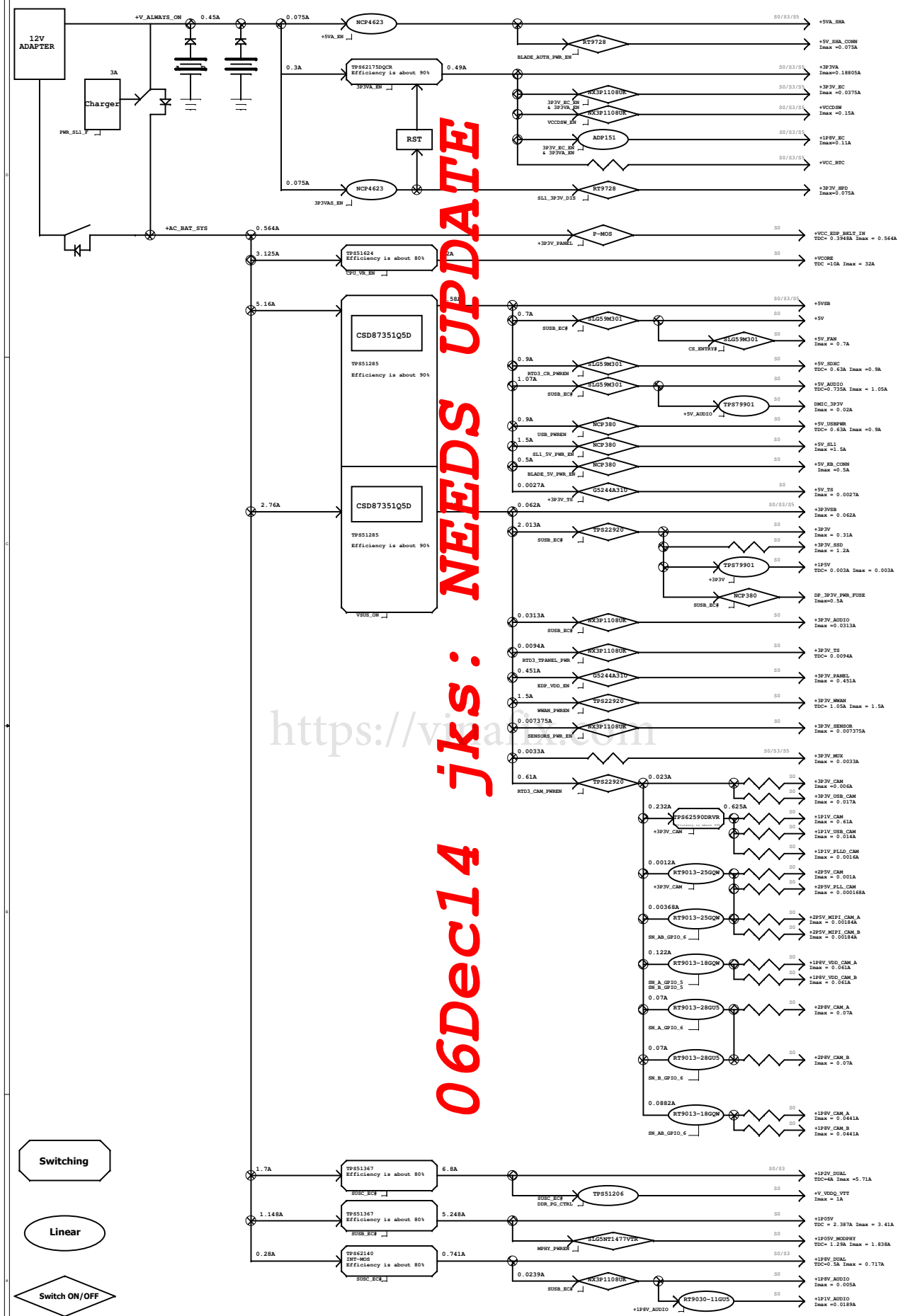
HSW Buffer Through Mode for Pre-Silicon



POWER ON SEQUENCE (TBD)

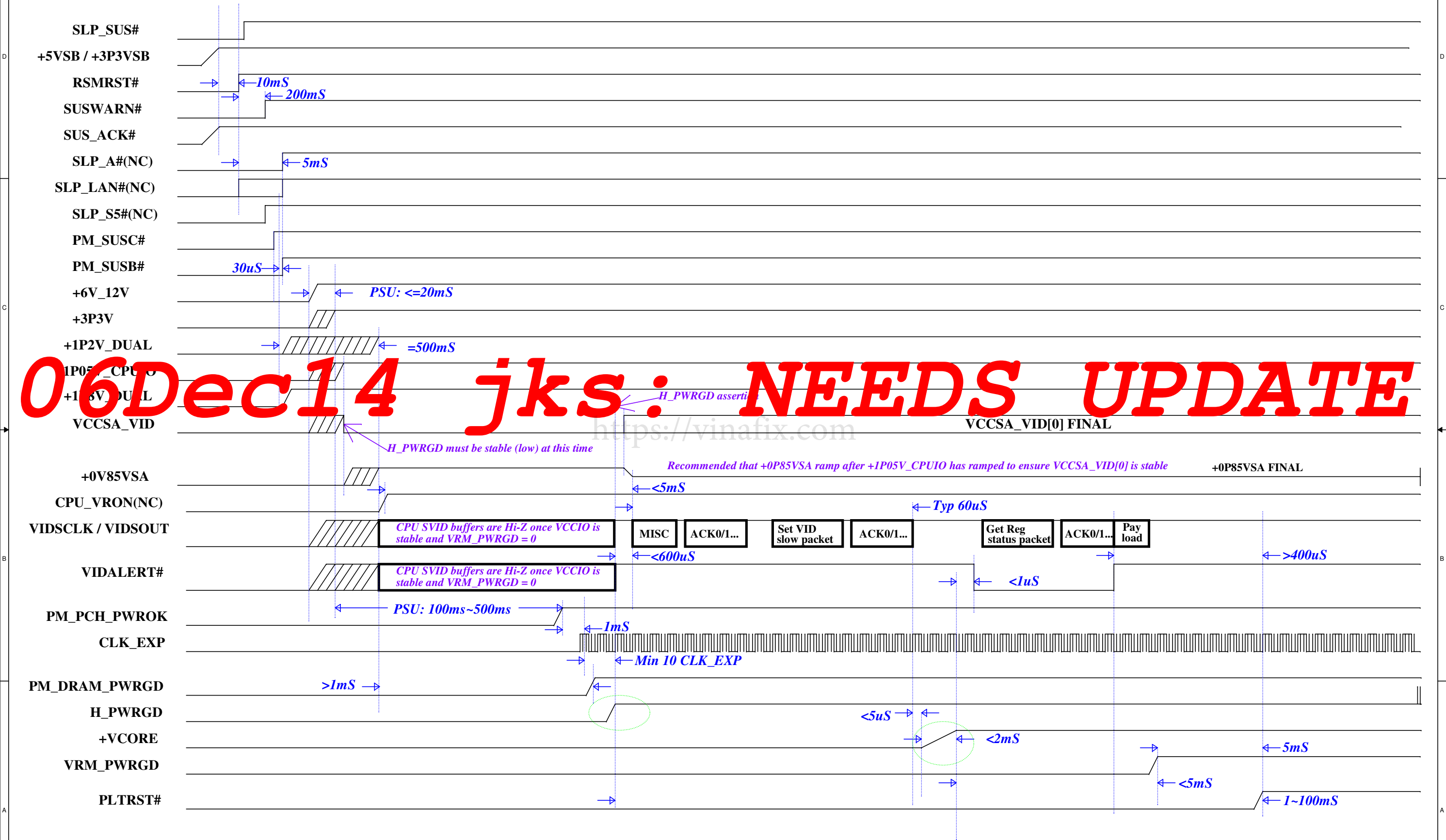
STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4	+AC_BAT_SYS /SYSTEM POWER READY
5	VCCDSW_EN /TURN ON DSW POWER for PCH
6	PCH_DPWROK /DEEP POWER GOOD TO PCH
7	SLP_SUS# /STANBY POWER REQUIRED
8	VSUS_ON/EC TURN ON STANBY POWER
9	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10	RSMRST# /SUS POWER GOOD TO PCH
11	EC_SAM_INT_IN
12	PWRBTN# TO EC
13	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15	SUSC_EC# /BYPASS SLP_S4#
16	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19	VCCST_PWRGD/ INDICATOR TO CPU
20	VRM_PWRGN /POWER FOR CPU IS GOOD
21	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
22	SYS_PWROK /SYSTEM POWER STABLE
23	SVID /VR controller establish protocol to CPU
24	PLTRST# /ALL SET UP AND RESET TO INITIAL





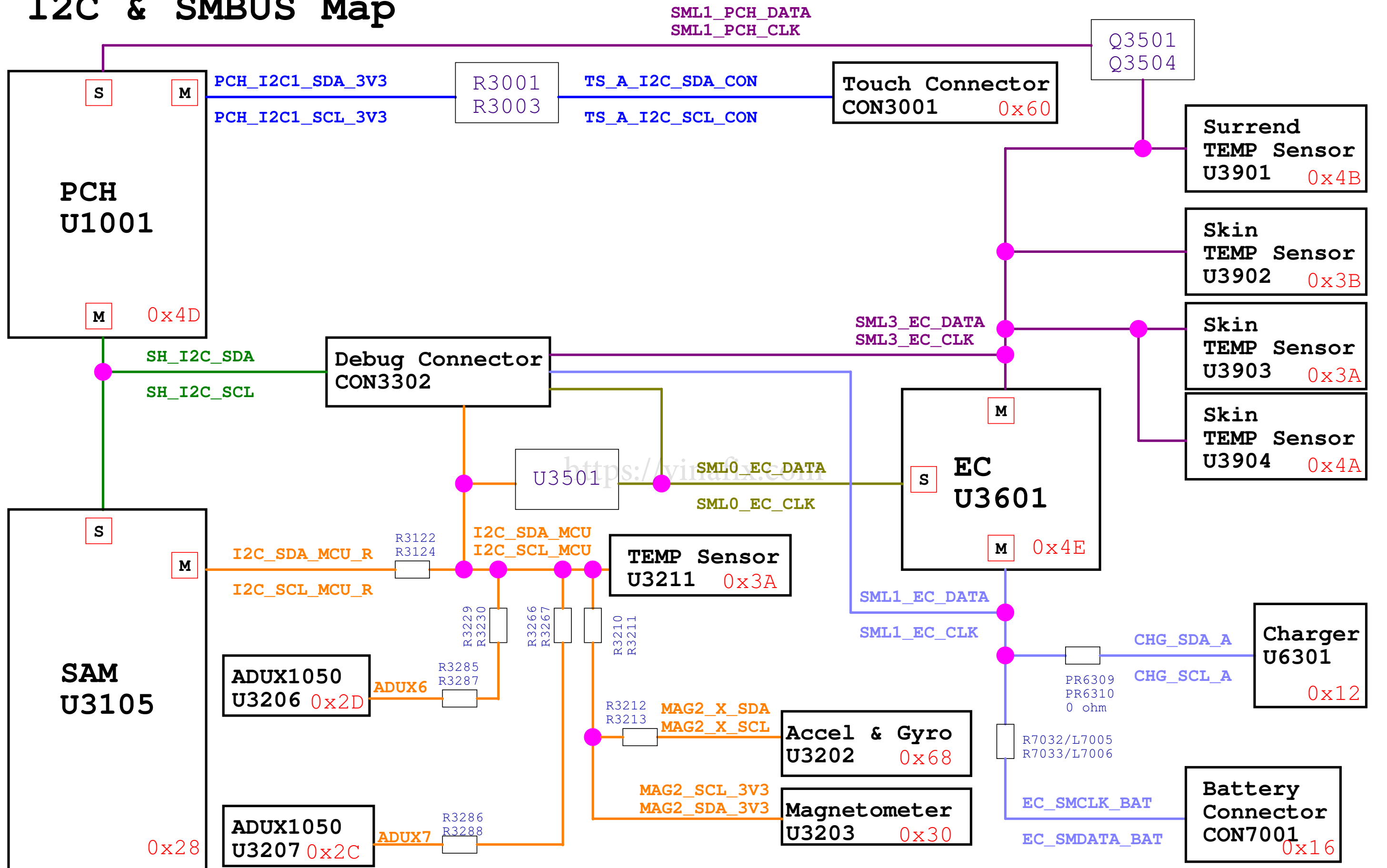
[illegible]

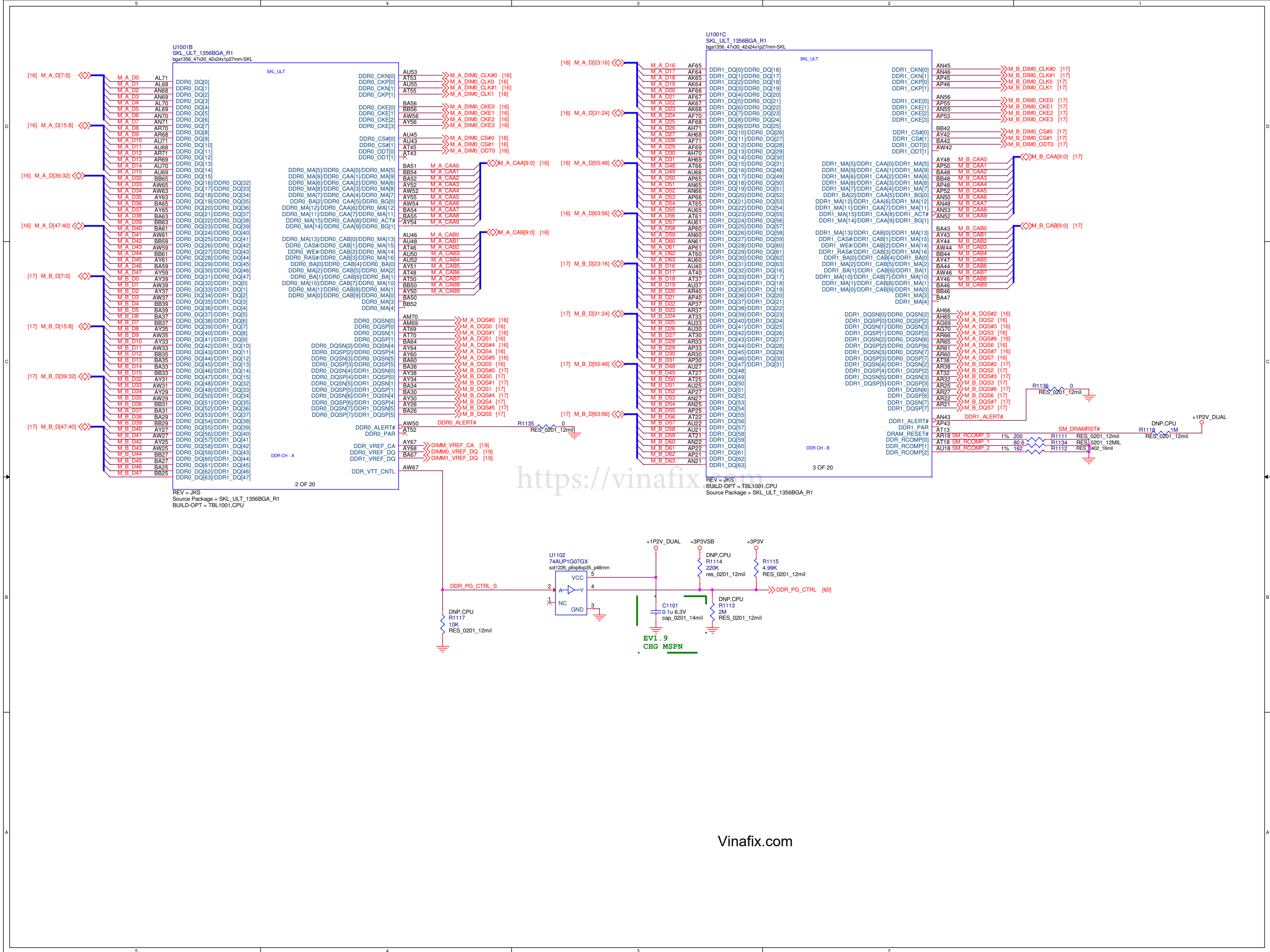
S5 to S0 Power Sequence

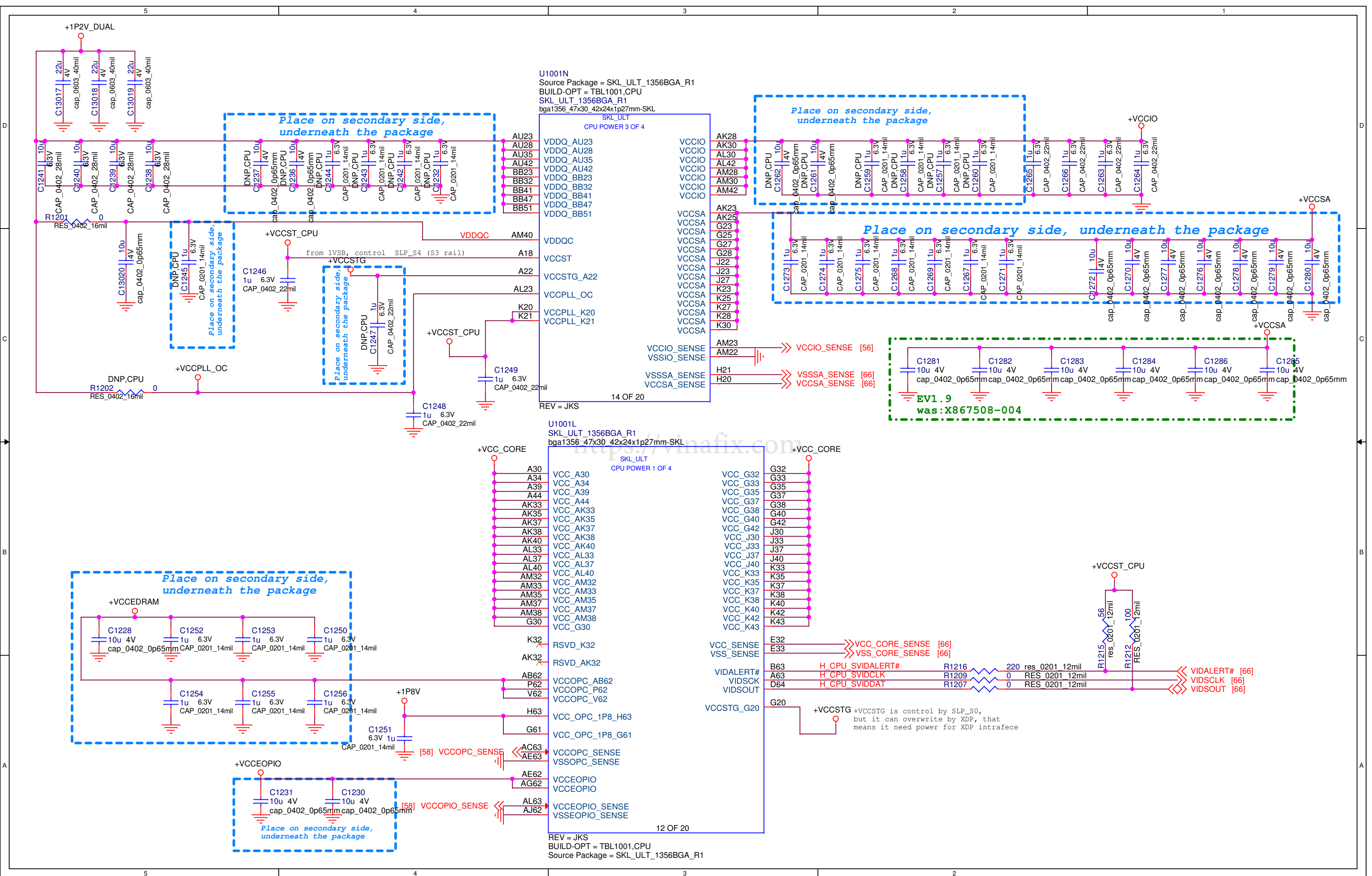


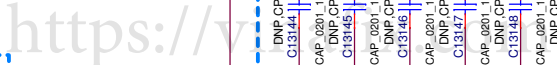
06Dec14 jks: **NEEDS UPDATE**

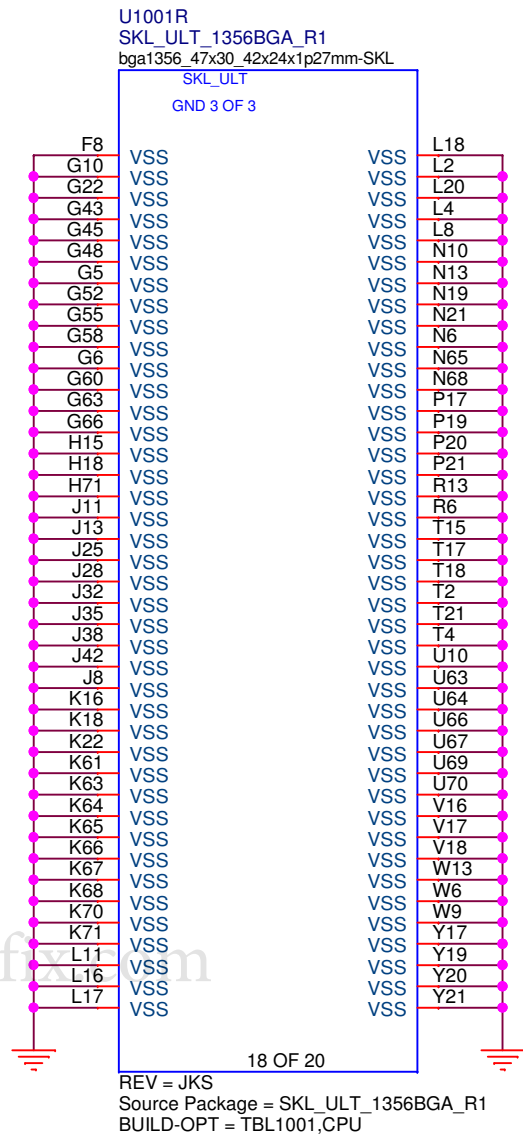
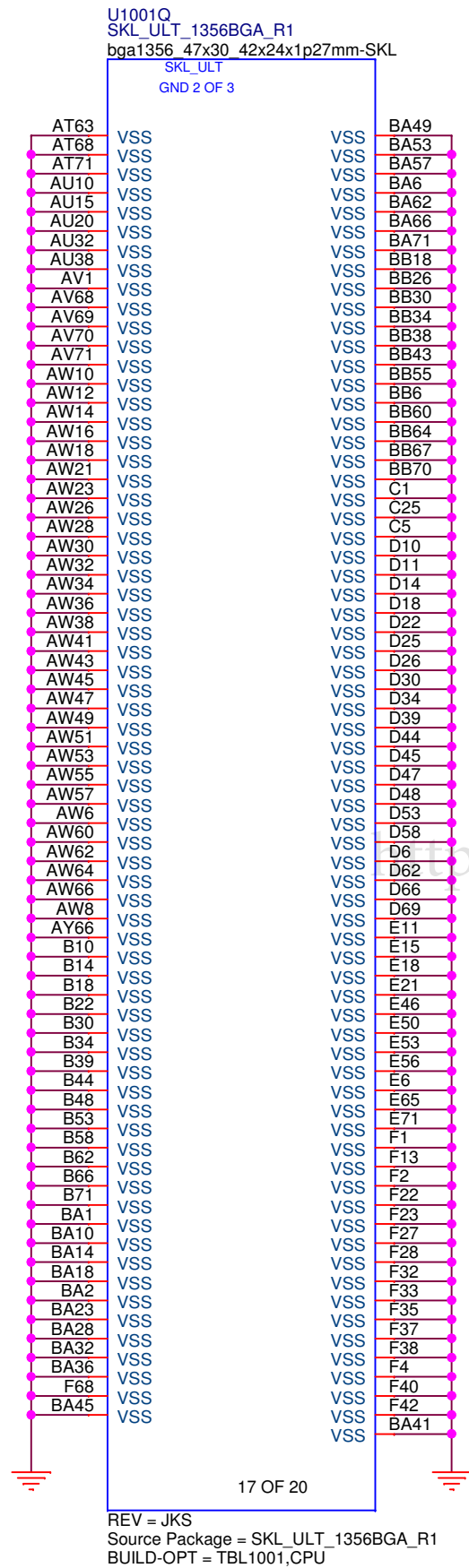
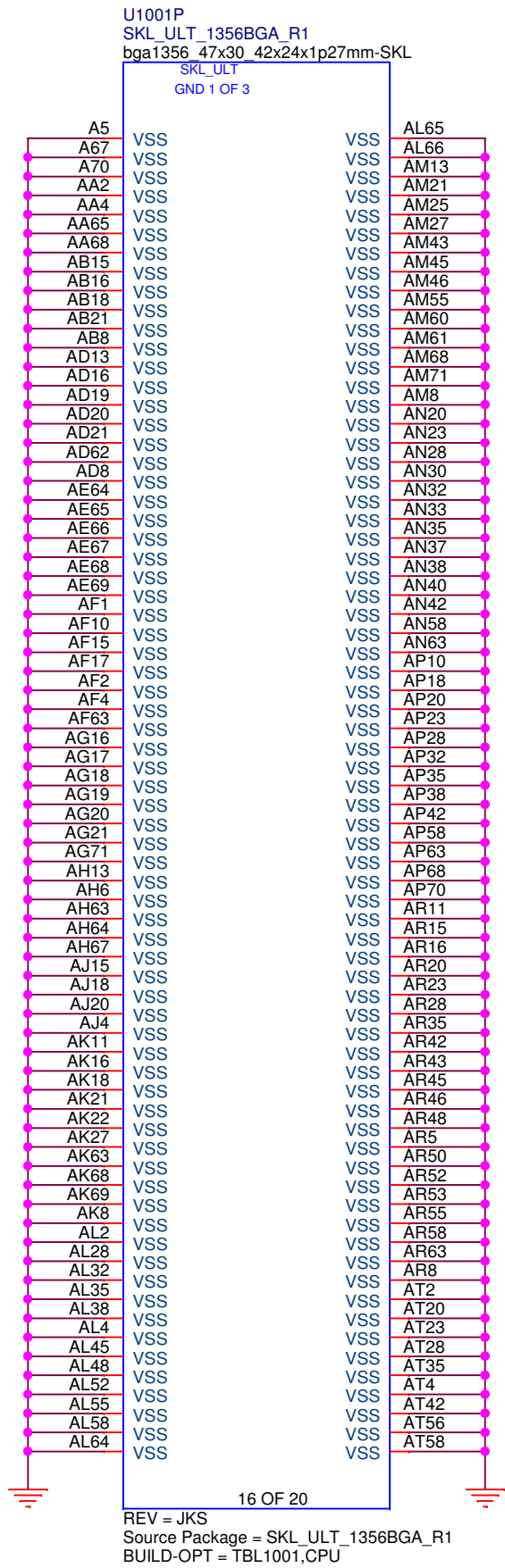
I2C & SMBUS Map





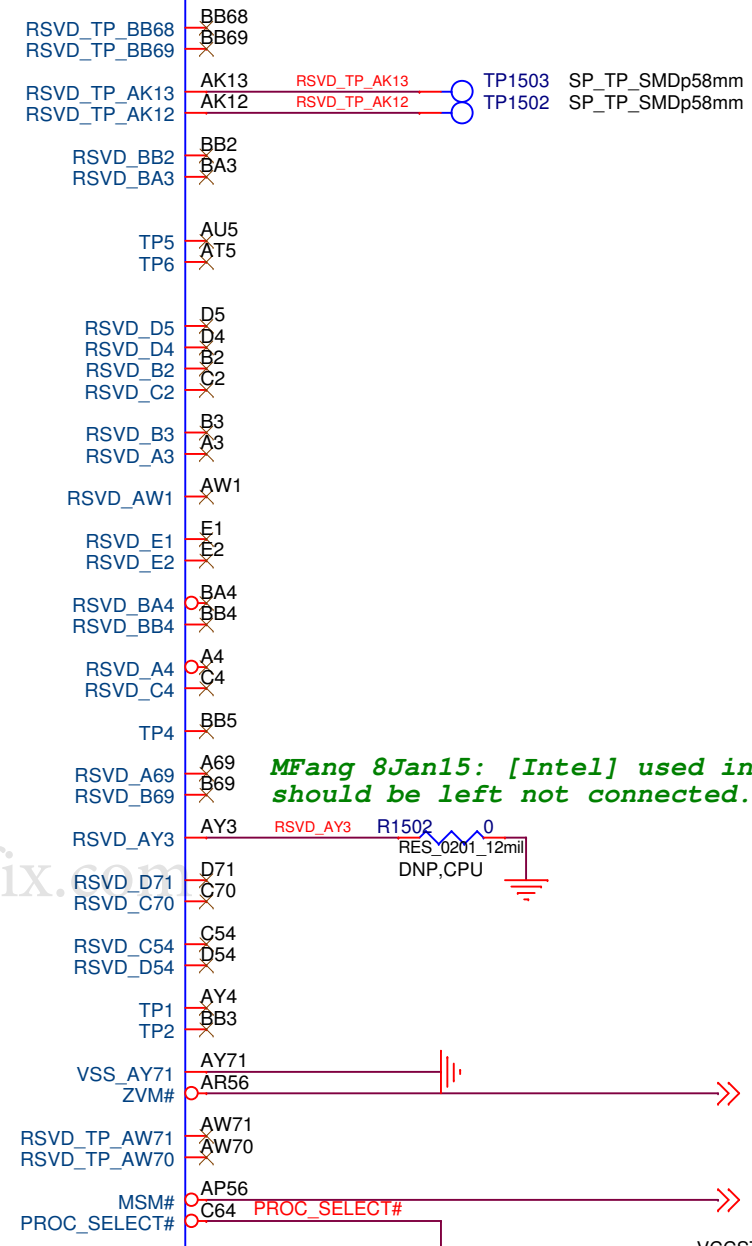
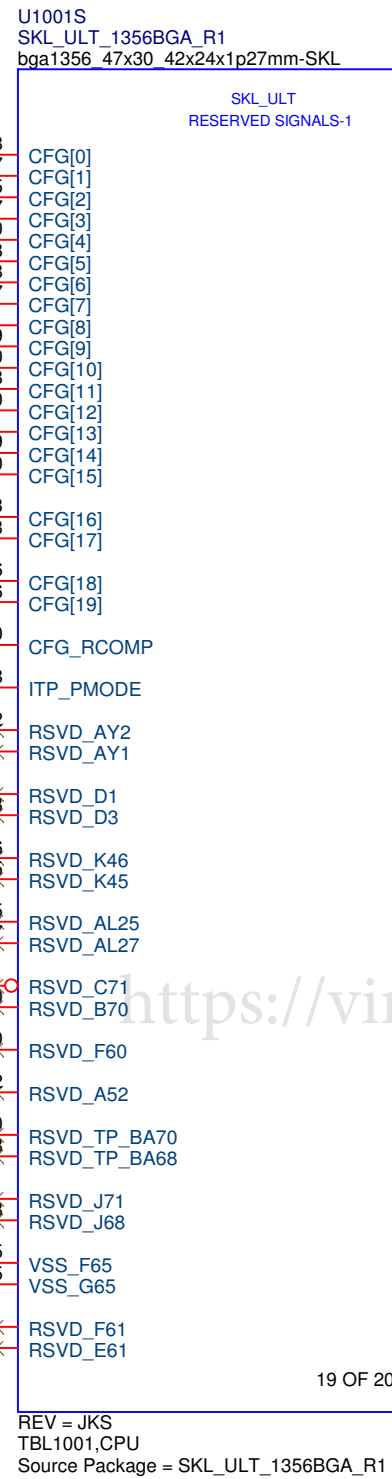
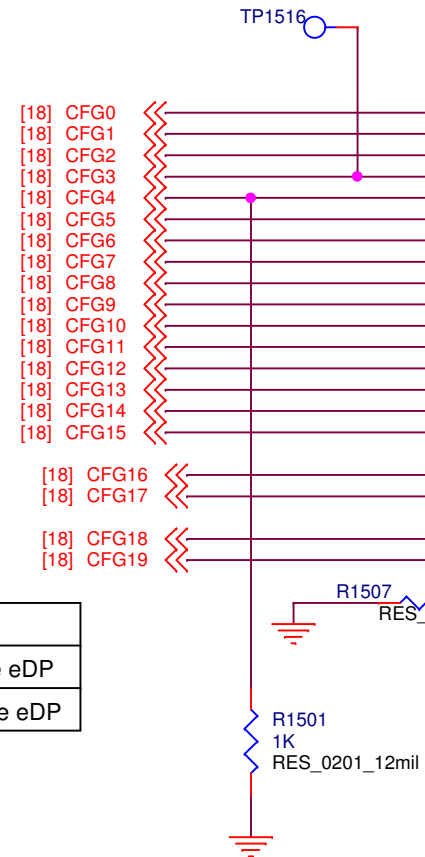






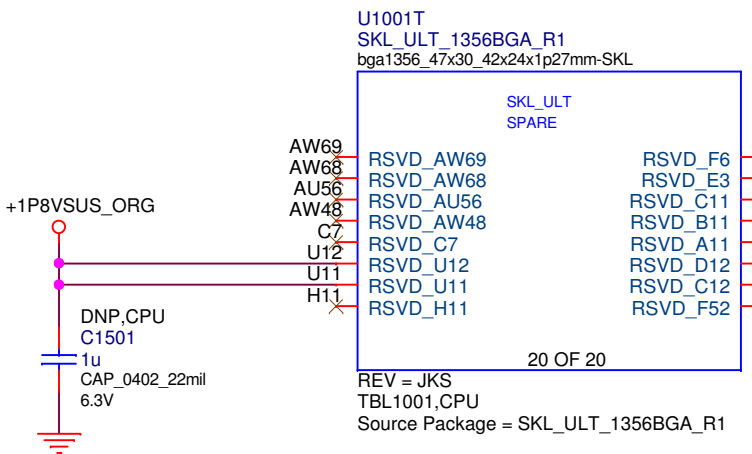
- [18] CFG0
- [18] CFG1
- [18] CFG2
- [18] CFG3
- [18] CFG4
- [18] CFG5
- [18] CFG6
- [18] CFG7
- [18] CFG8
- [18] CFG9
- [18] CFG10
- [18] CFG11
- [18] CFG12
- [18] CFG13
- [18] CFG14
- [18] CFG15
- [18] CFG16
- [18] CFG17
- [18] CFG18
- [18] CFG19

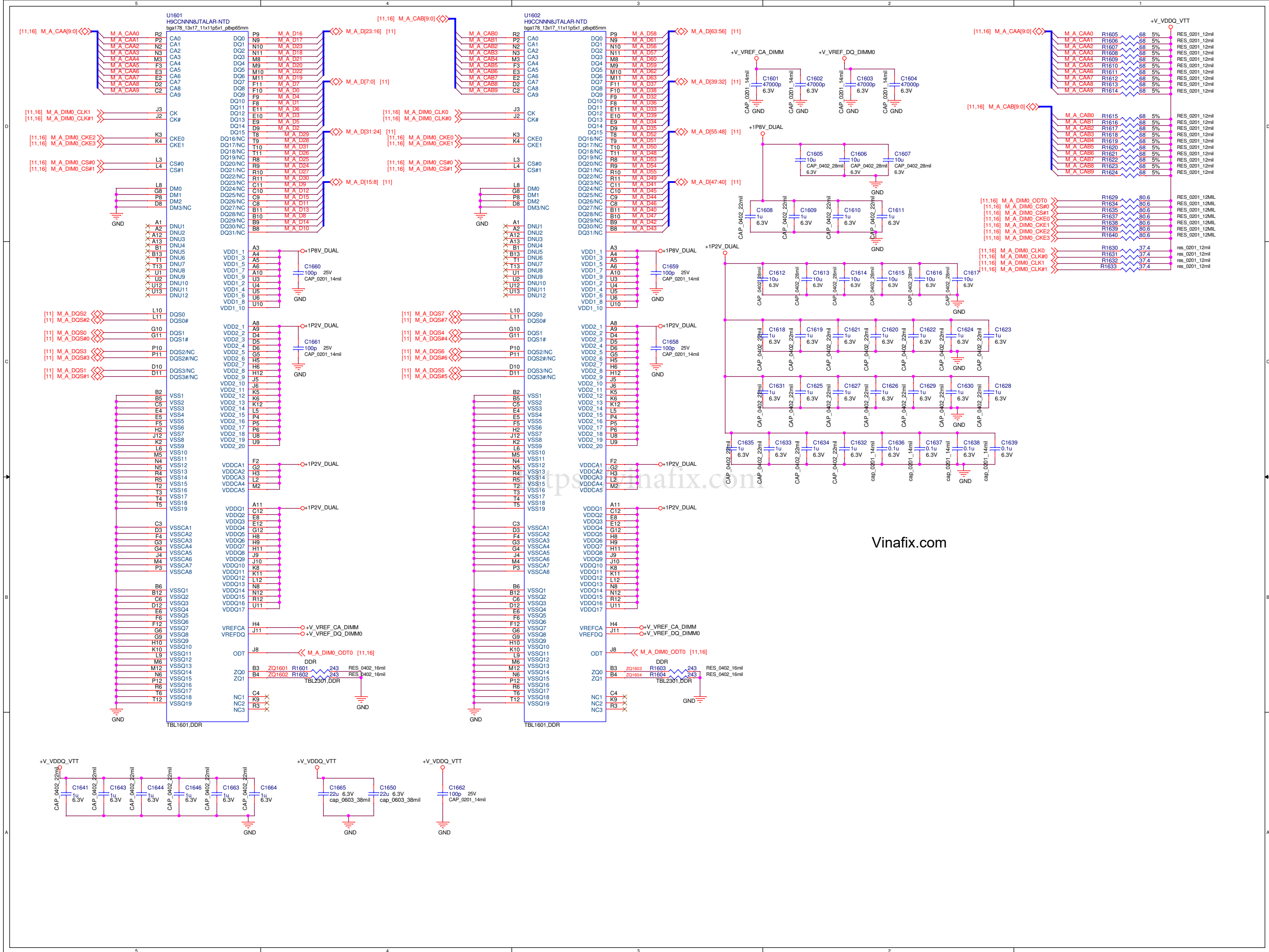
CFG4	
0 Default	enable eDP
1	Disable eDP



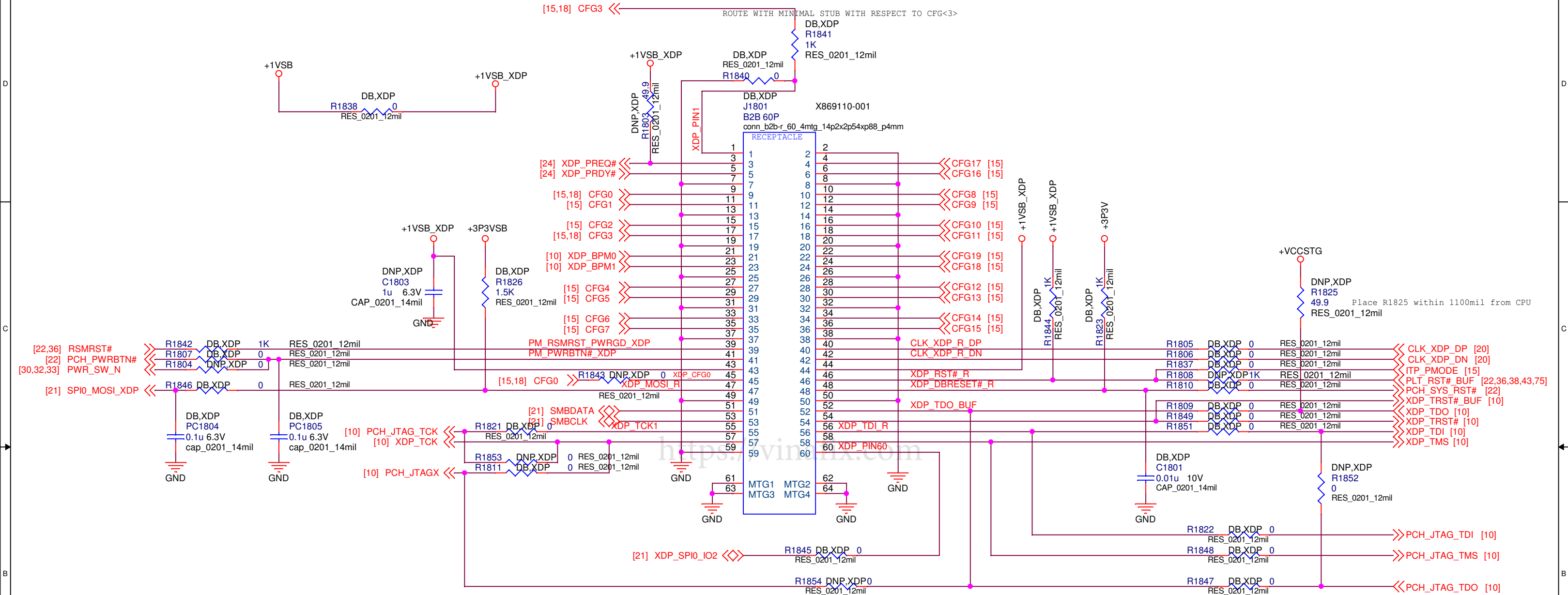
MFang 8Jan15: [Intel] used in the HVM testing should be left not connected.

ZVM# and MSM# may need to control the VCCOCP and VCCEPIO





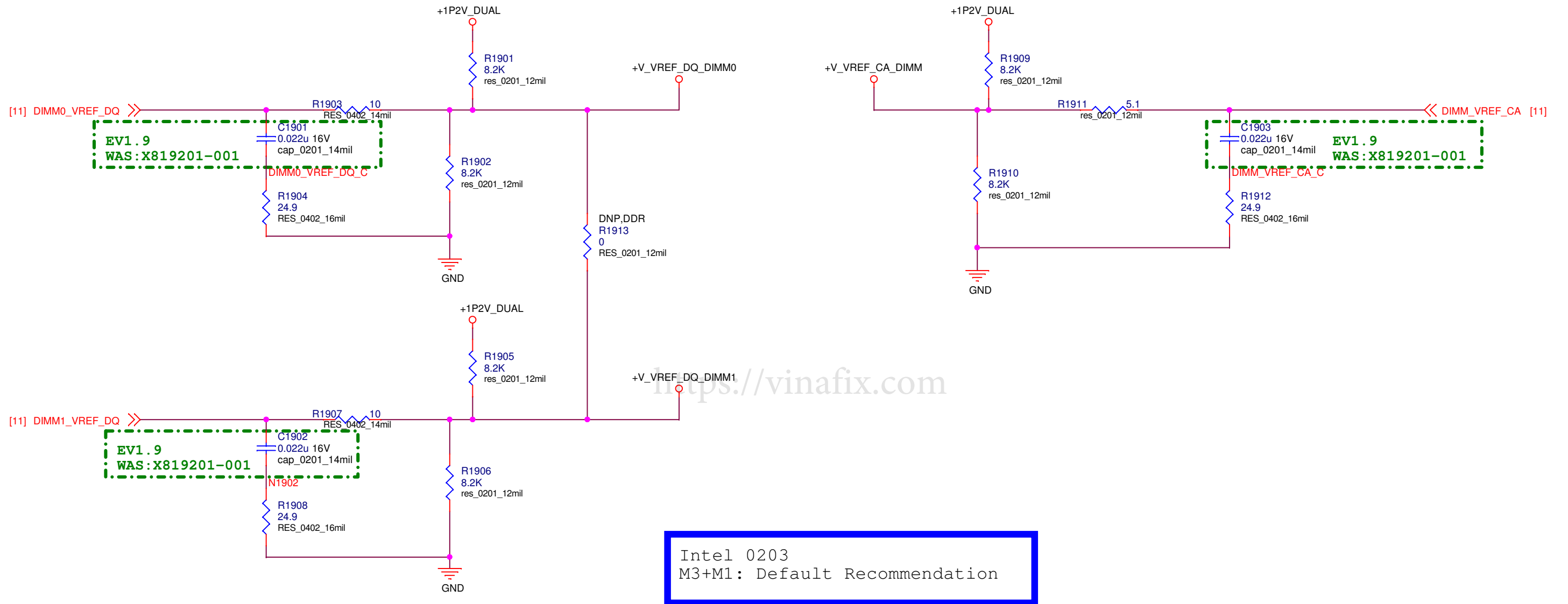
PRIMARY XDP connector



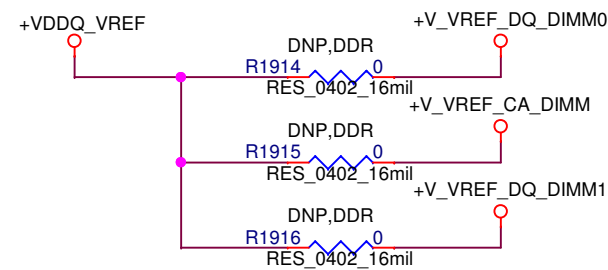
For the signals only go to XDP, the OR should be close to XDP connector.
For the signals to both XDP and target circuit, the option resistor location should follow the target signal routing.

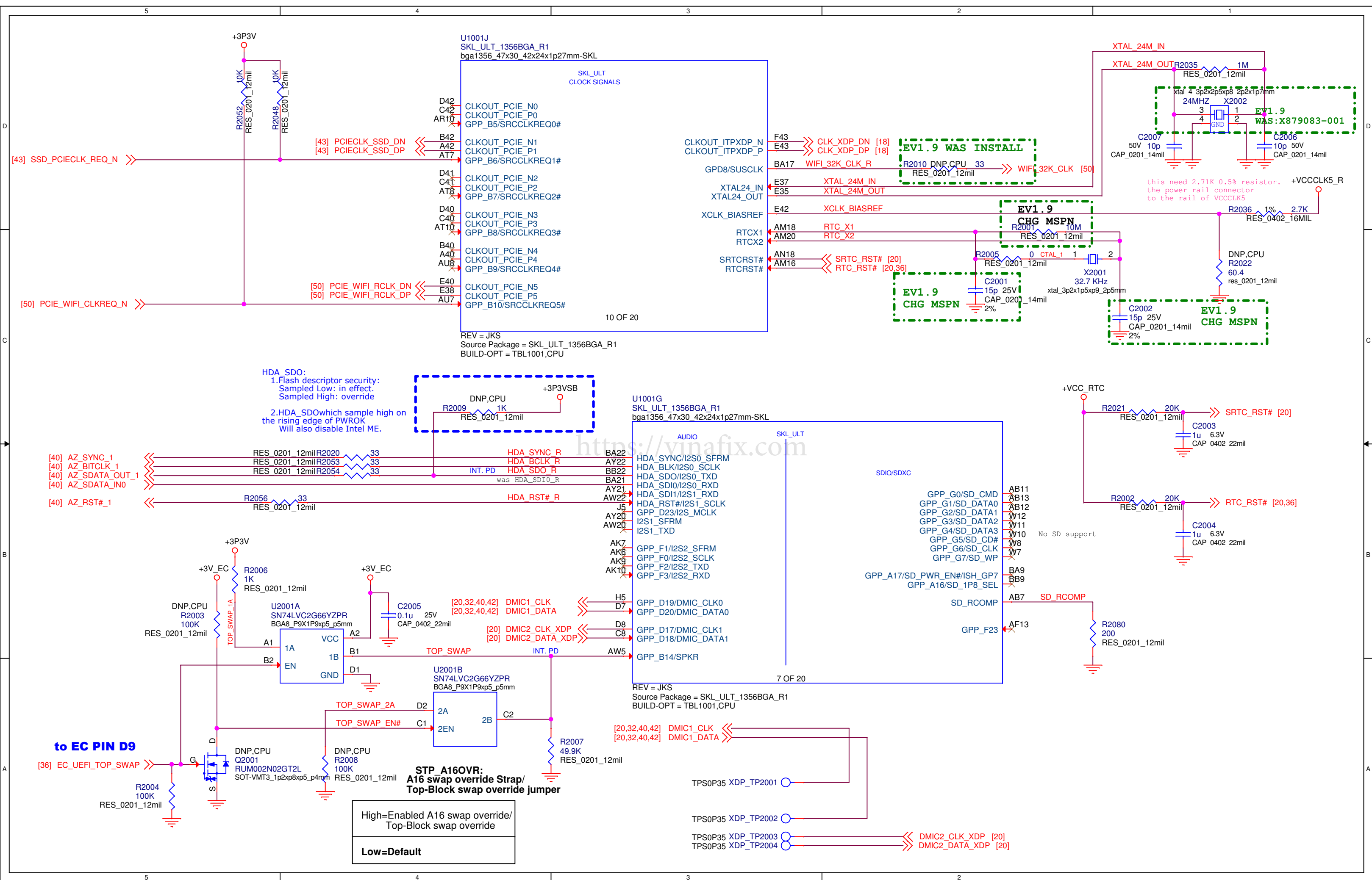
LPDDR3 Vref

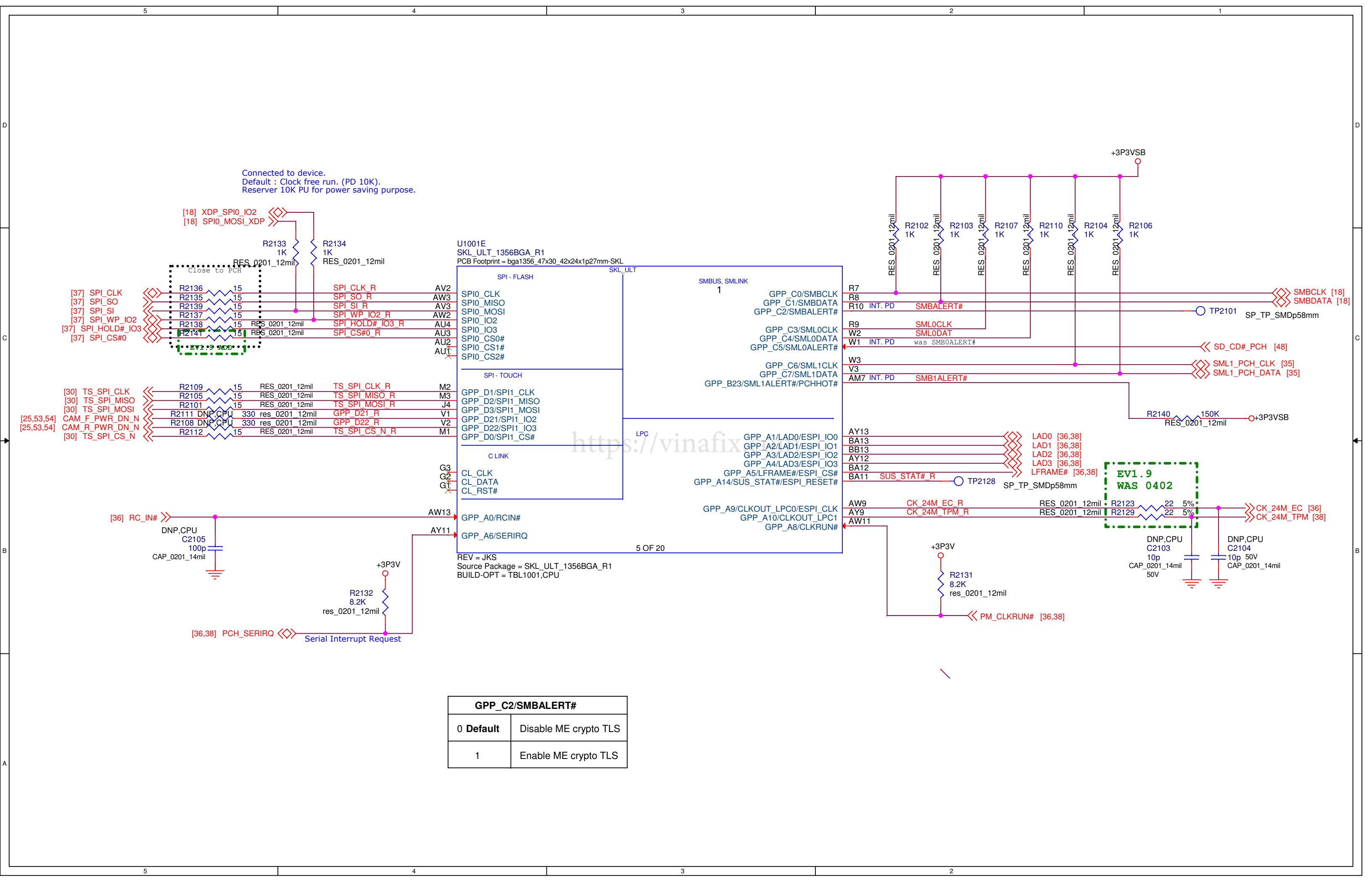
M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

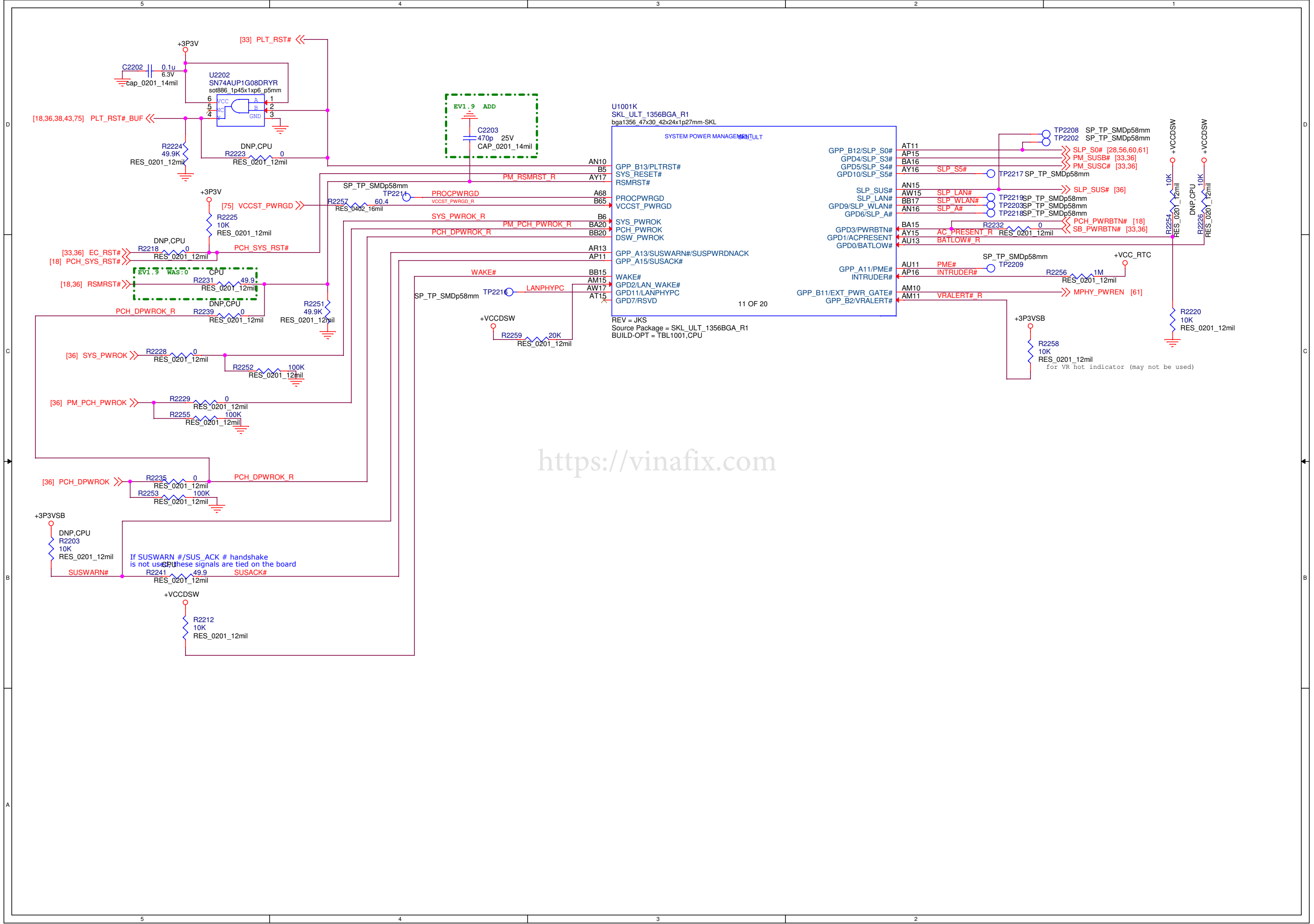


Intel 0203
M3+M1: Default Recommendation







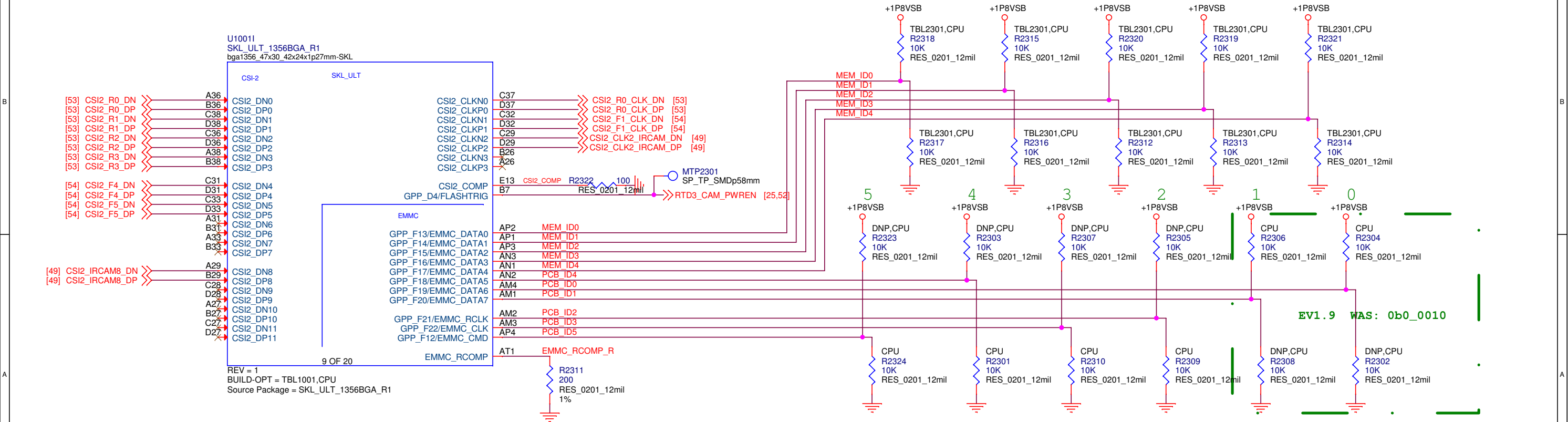


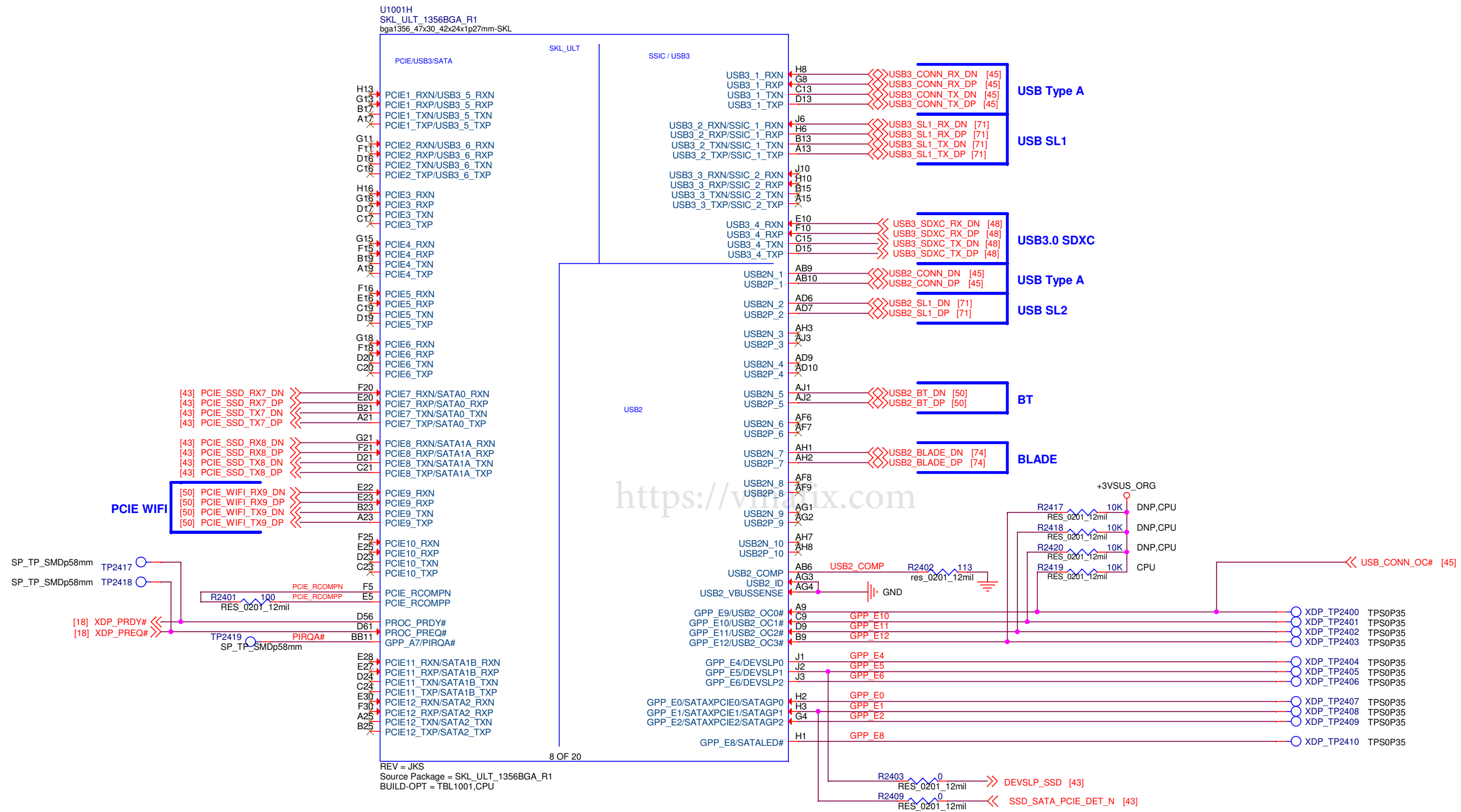
Rev 4	EC Processor ID		PCH ID	TPM			EC Board Rev	PCH Board ID[3:0]				DRAM Manufacturer		RAM Speed	RAM Size & Calibration		
Signal	EC_ID1	ED_ID0	PCB_ID5	PCB_ID4			R3619	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0	MEM_ID1	MEM_ID0	MEM_ID4	MEM_ID3	MEM_ID2	ZQ1
	1 = R3642 0 = R3643	1 = R3640 0 = R3641	1 = R2323 0 = R2324	1 = R2303 0 = R2301	R3813 R3815 R3816	R3814		1 = R2307 0 = R2310	1 = R2305 0 = R2309	1 = R2306 0 = R2308	1 = R2304 0 = R2302	1 = R2315 0 = R2316	1 = R2318 0 = R2317	1 = R2321 0 = R2314	1 = R2319 0 = R2313	1 = R2320 0 = R2312	R1602 R1604 R1702 R1704
	U22=0 U23E=1 Y=0 S=1	U22=0 U23E=0 Y=1 S=1	U=0 Y=1	Infineon =0 Nation Z =1	Infineon =DNP NationZ =POP	Infineon =POP NationZ =DNP						Hynix =0 Samsung =0	Hynix =0 Samsung =1	1600 LPDDR3=0 1866 LPDDR3=1	4GB=0 8GB=0 16GB=1	4GB=0 8GB=1 16GB=0	4GB =DNP 8GB =POP 16GB =POP
EV 0.9							80.6Ω	0	0	0	0						
EV 1.0							169Ω	0	0	0	1						
EV 1.5							698Ω	0	0	1	0						
EV 1.9							909Ω	0	0	1	1						

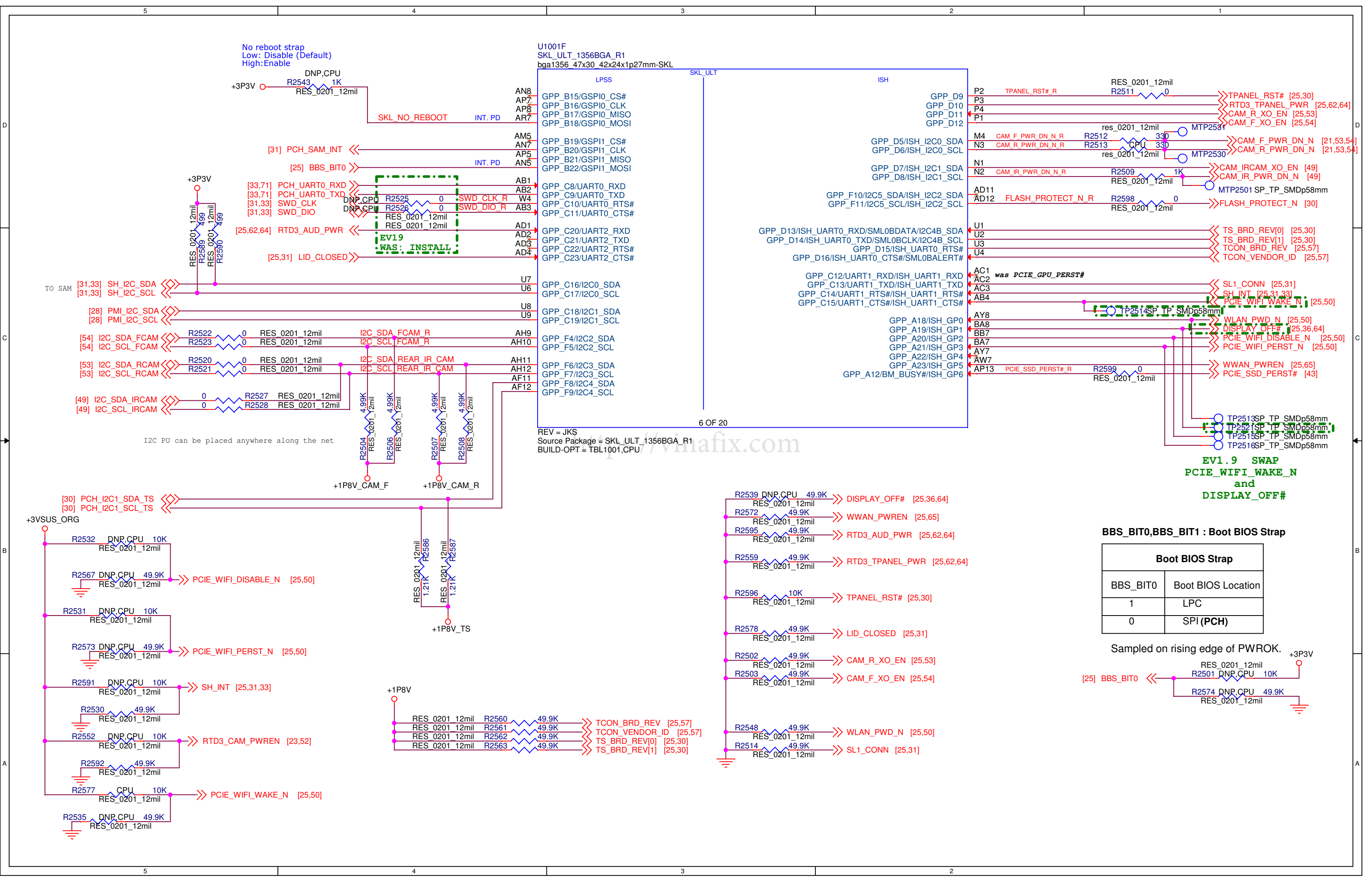
TBL2301

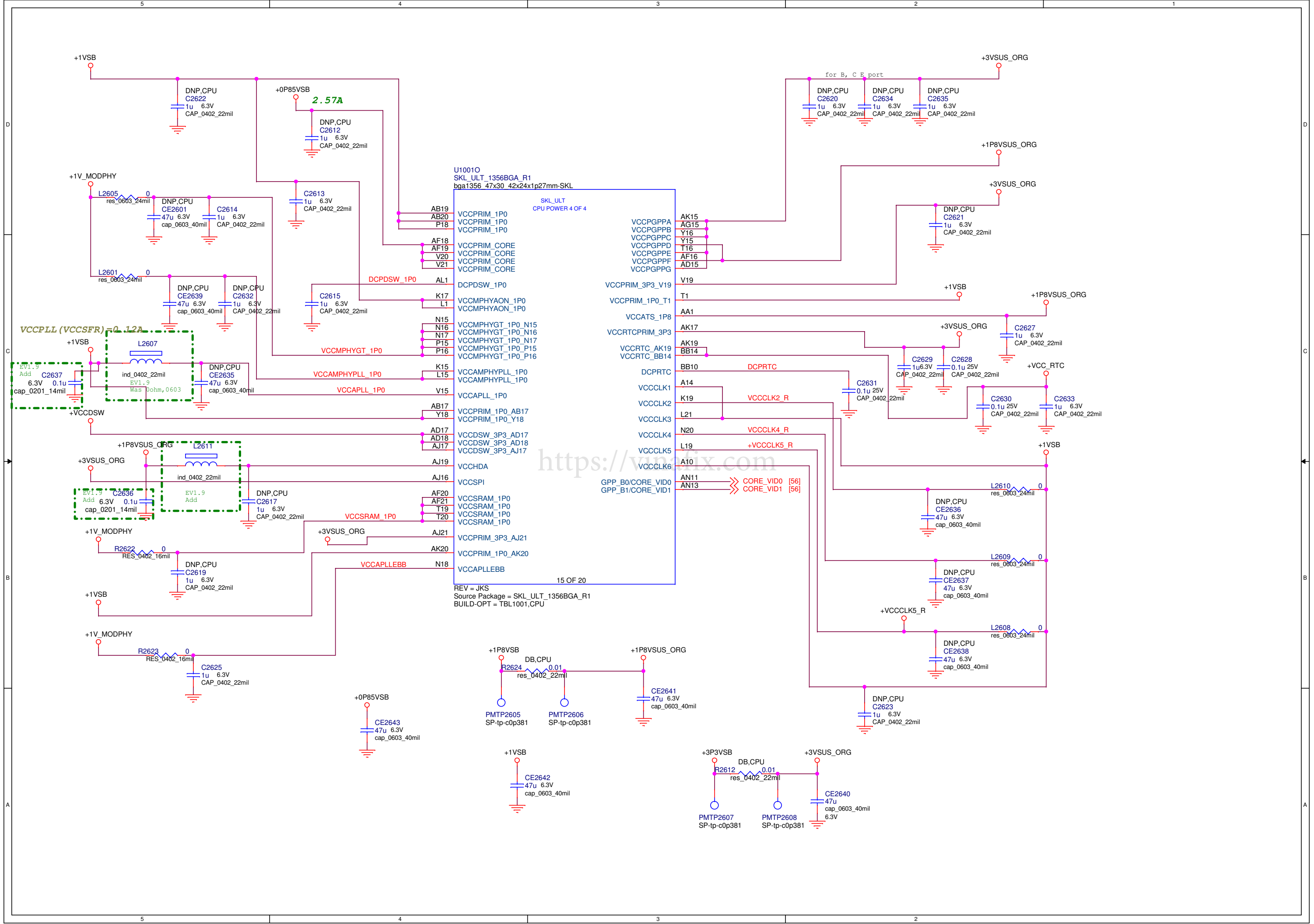
https://vinafix.com

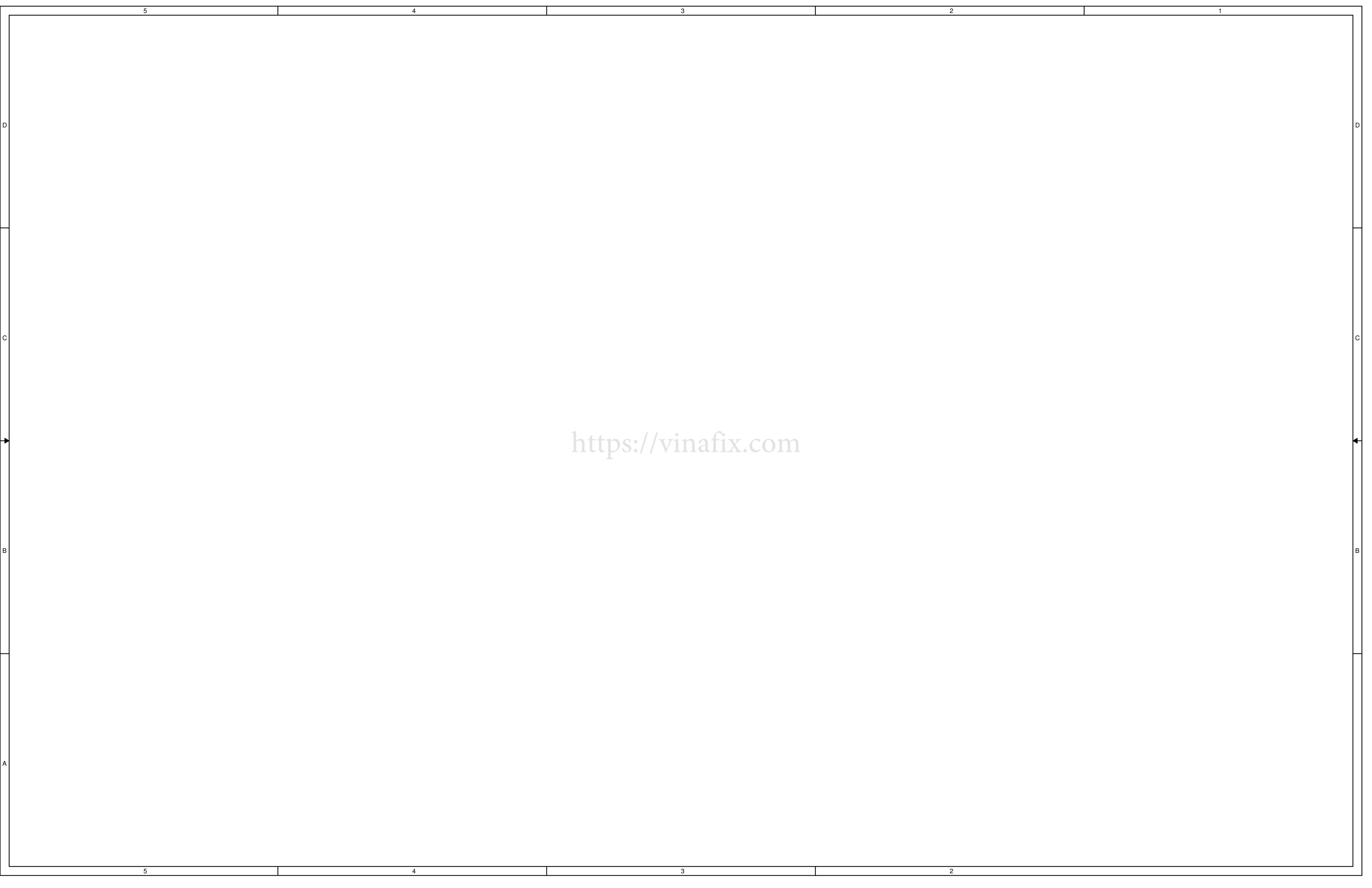
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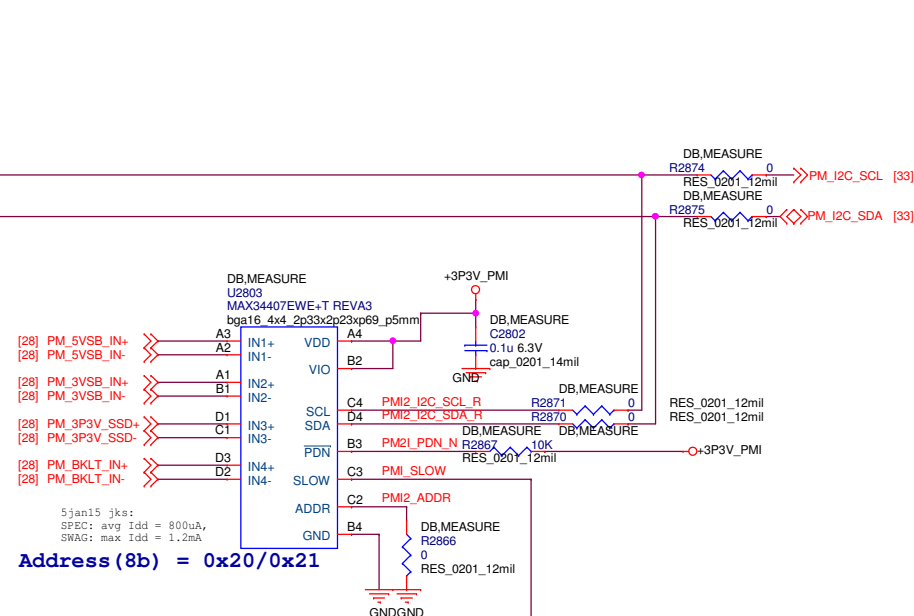
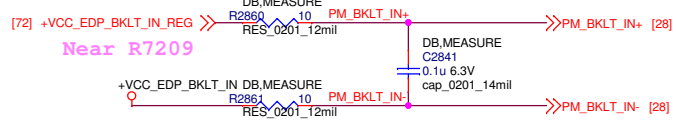
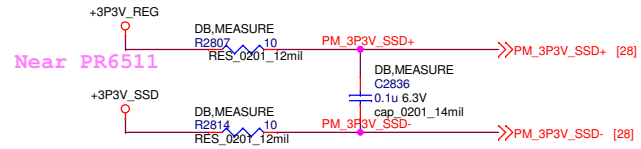
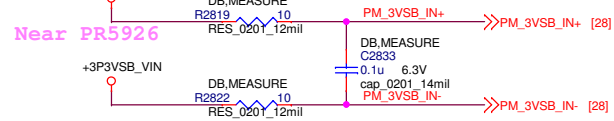
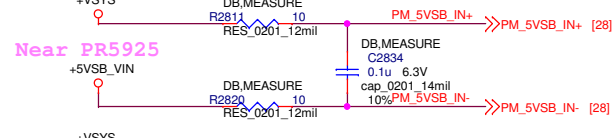
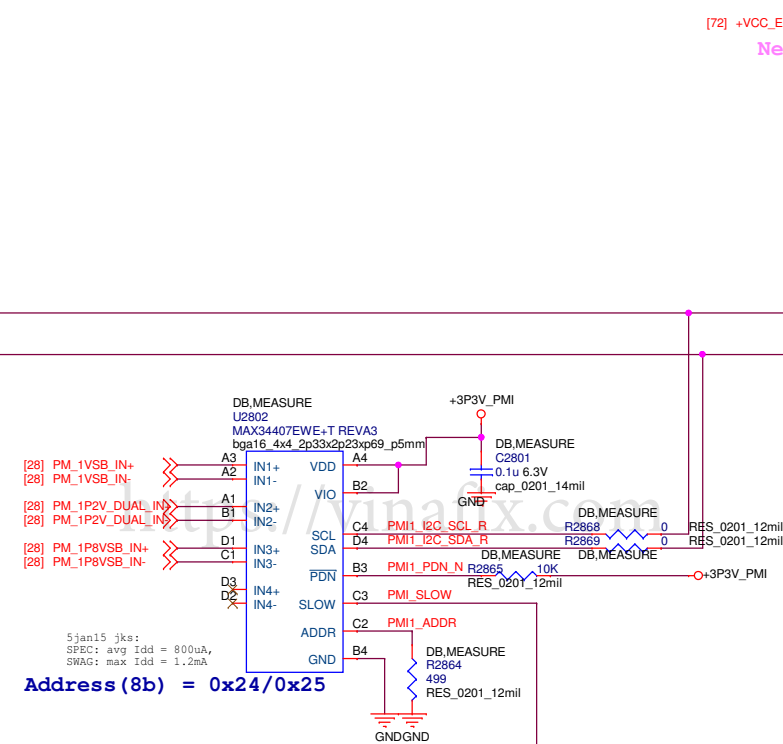
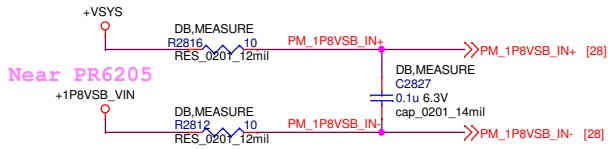
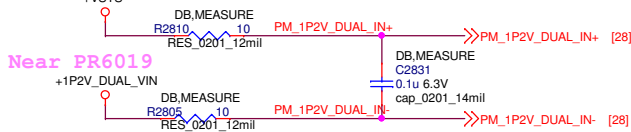
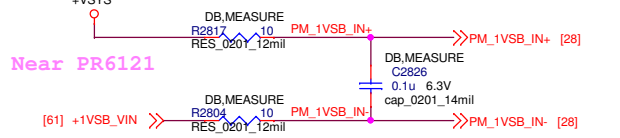
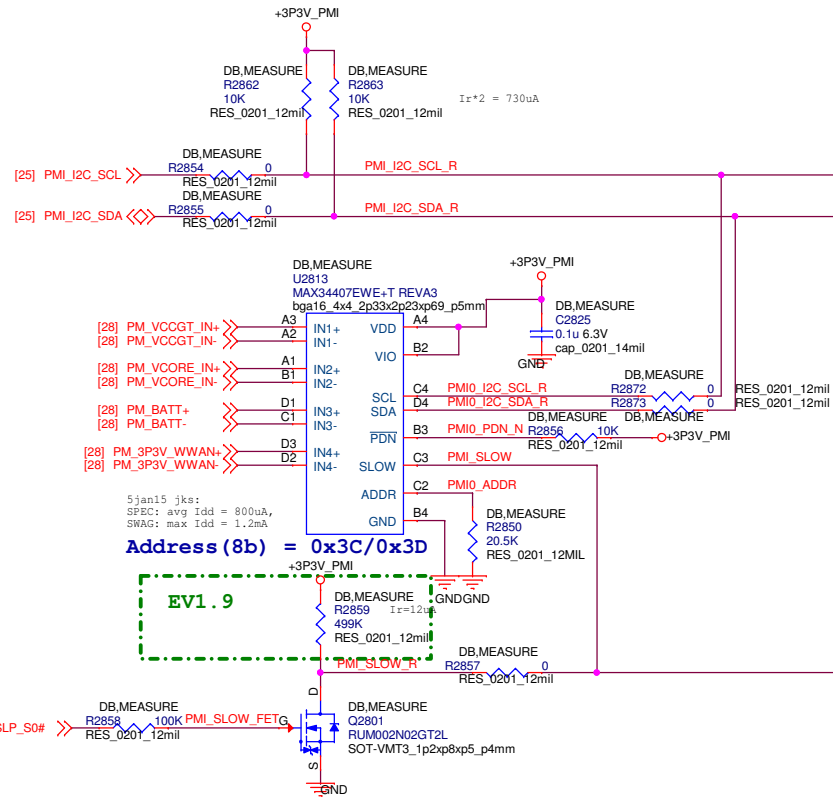
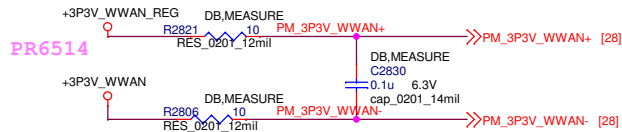
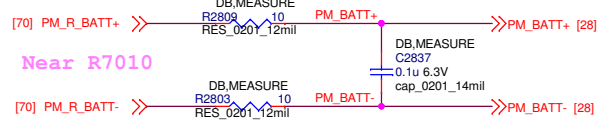
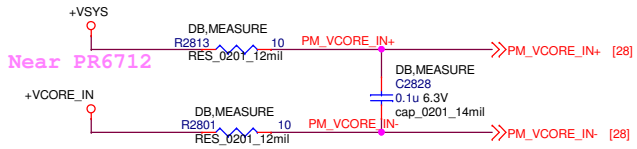
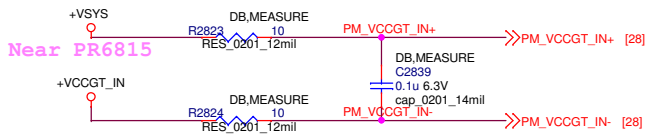






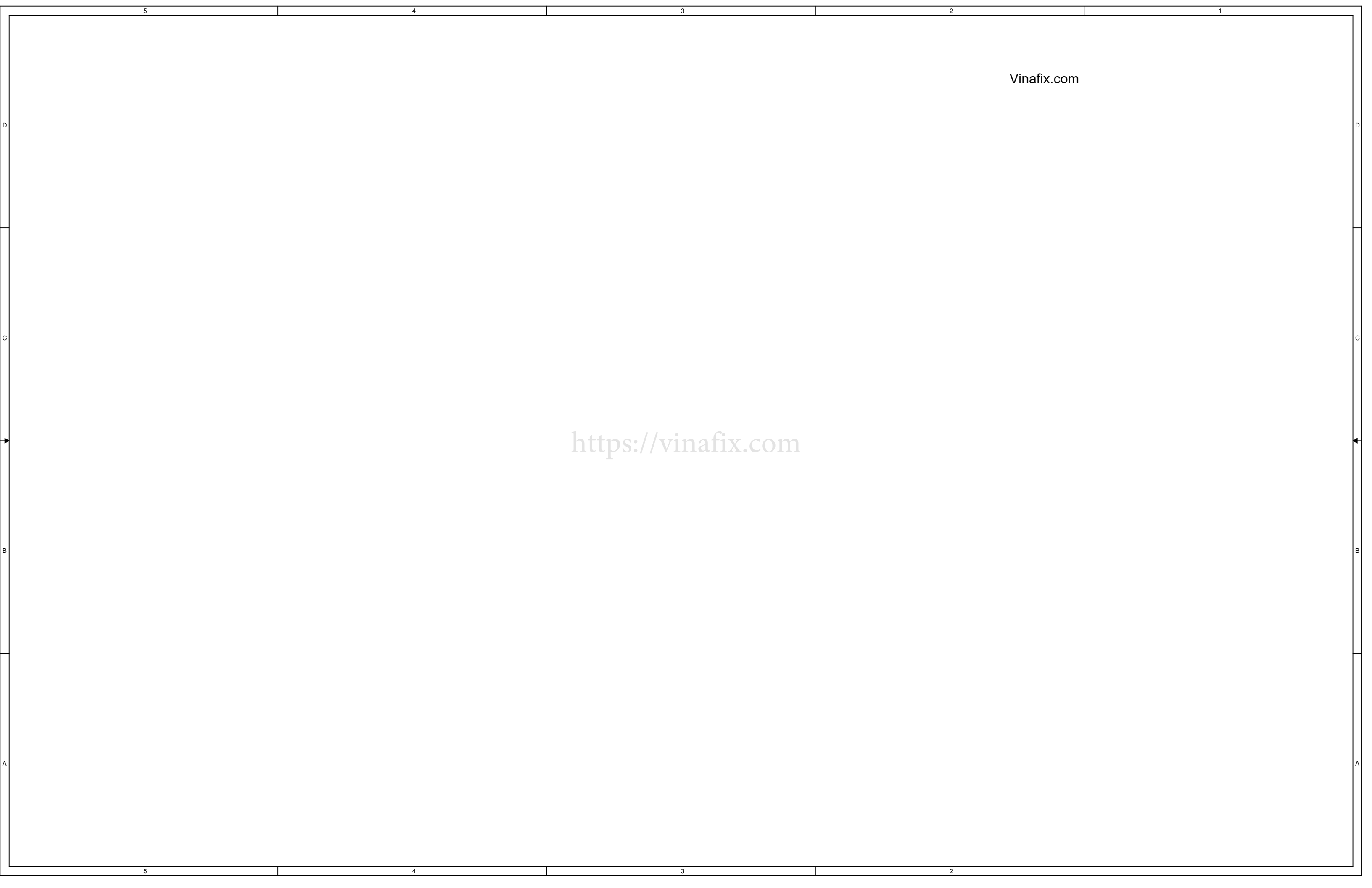






Resistor Address for MAX3440

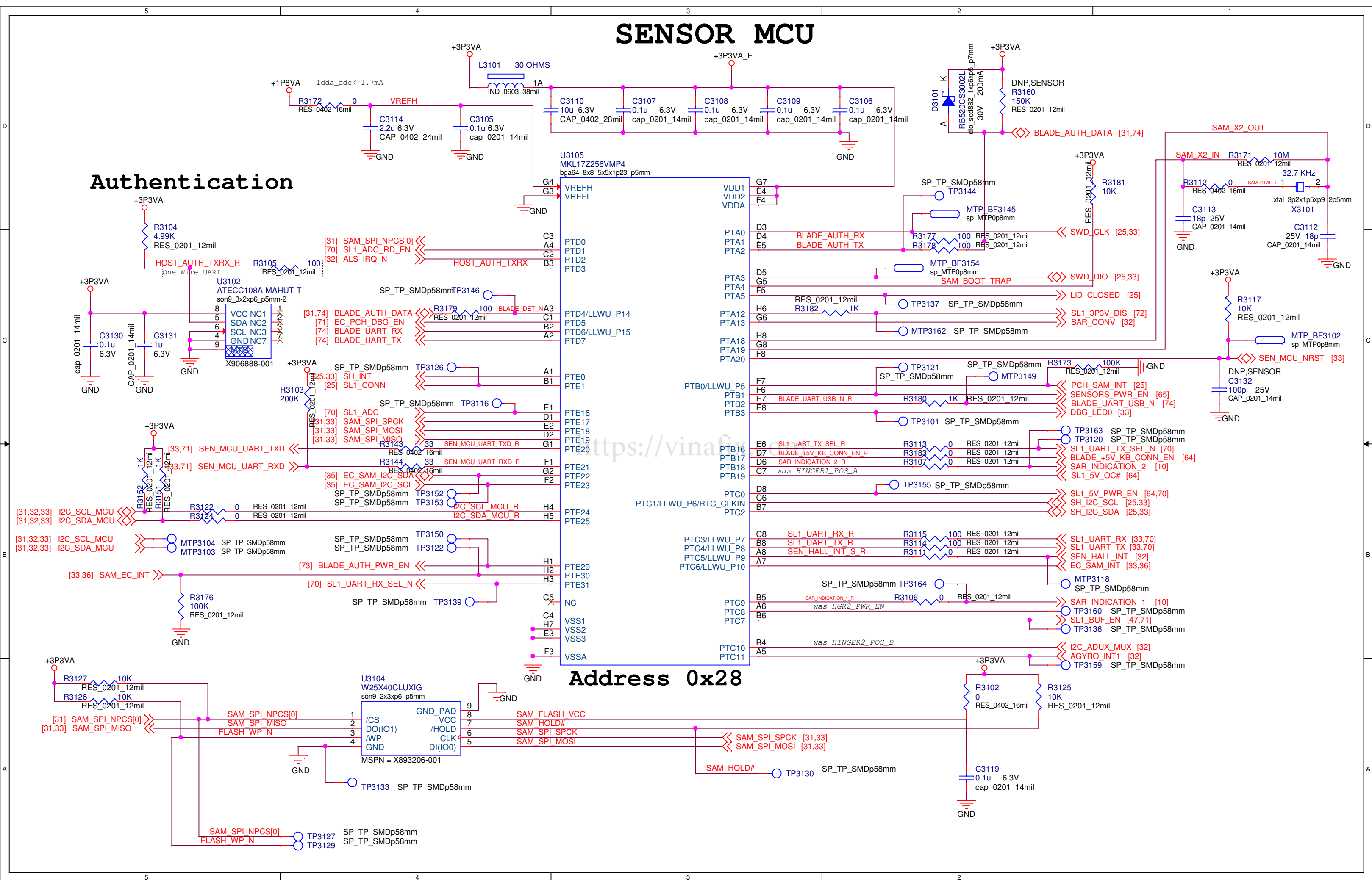
20.5K	=>	2x3C/2x3D
11.0K	=>	2x38/2x39
5.90K	=>	2x34/2x35
3.16K	=>	2x30/2x31
1.74K	=>	2x2C/2x2D
931K	=>	2x28/2x29
499	=>	2x24/2x25
GND	=>	2x20/2x21



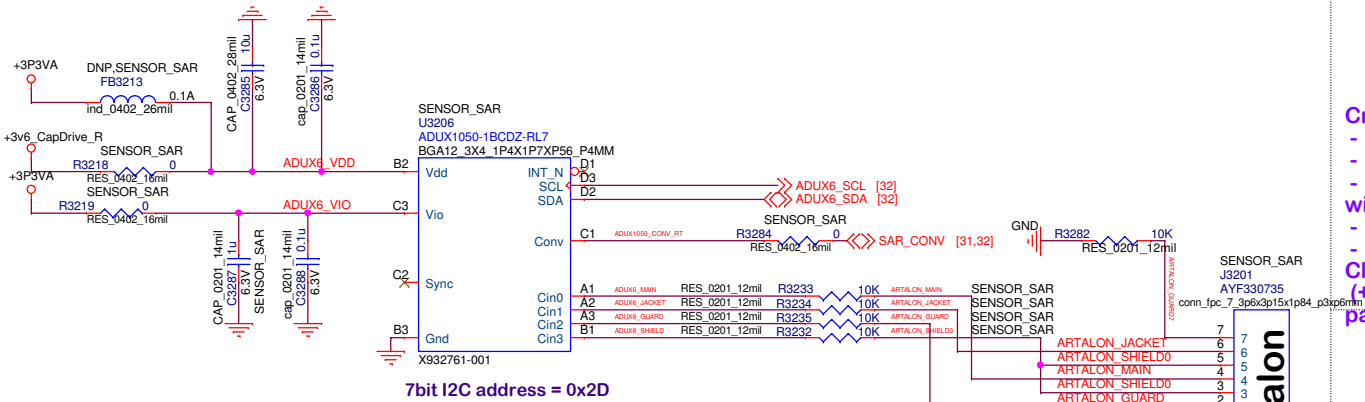
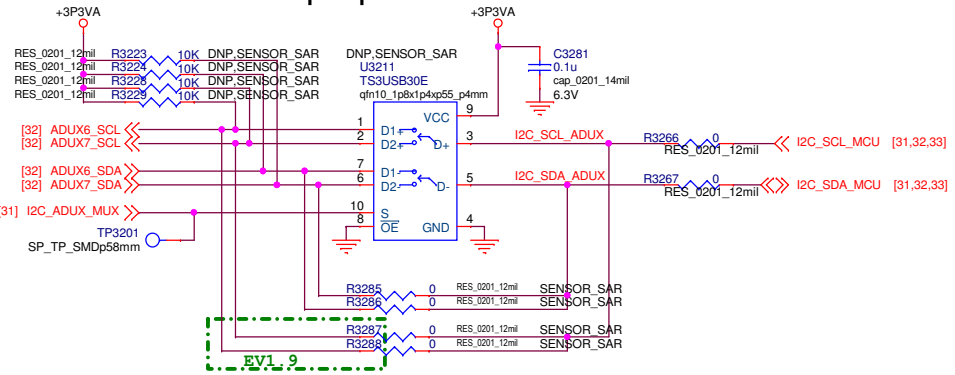
SENSOR MCU

Authentication

Address 0x28

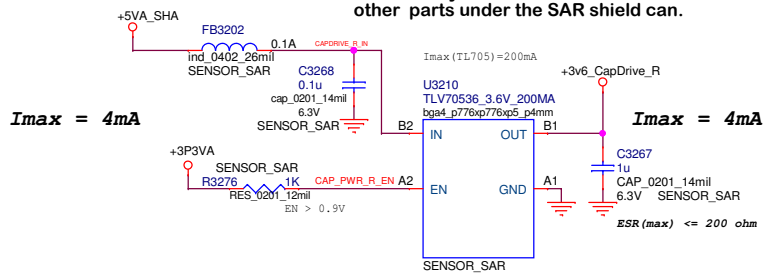
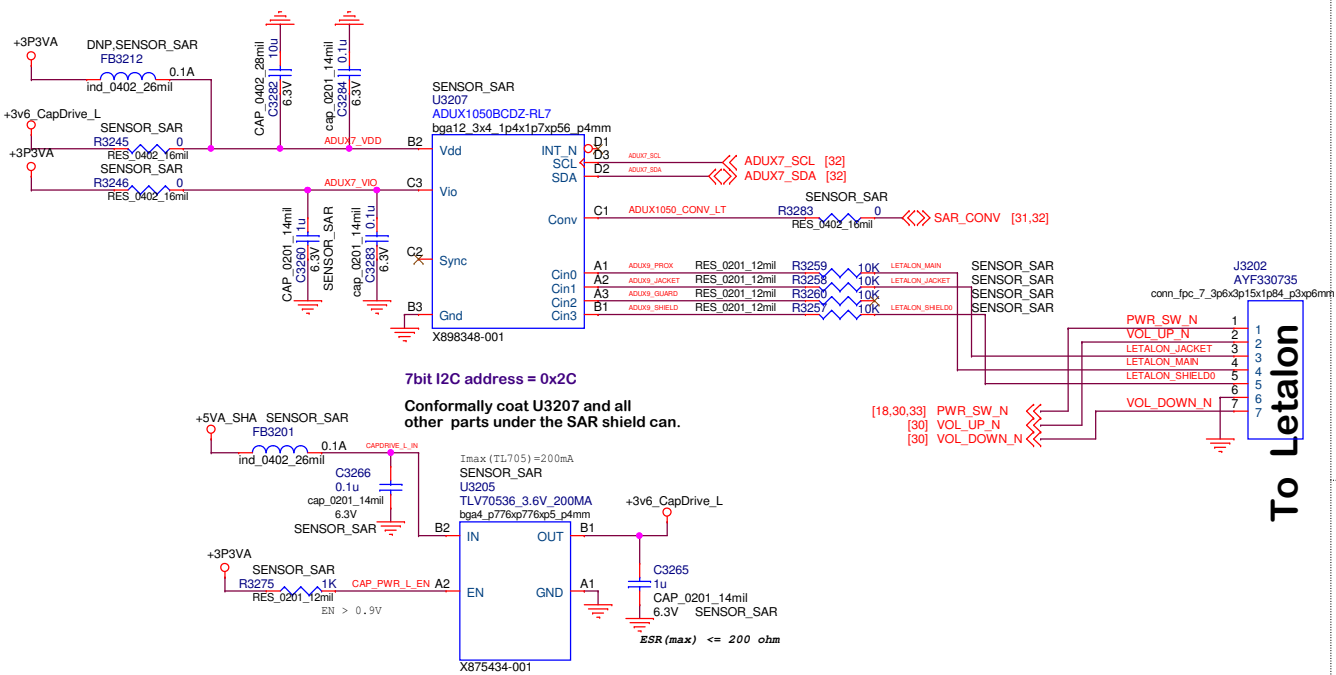


WiFi envelope protection drivers



7bit I2C address = 0x2D

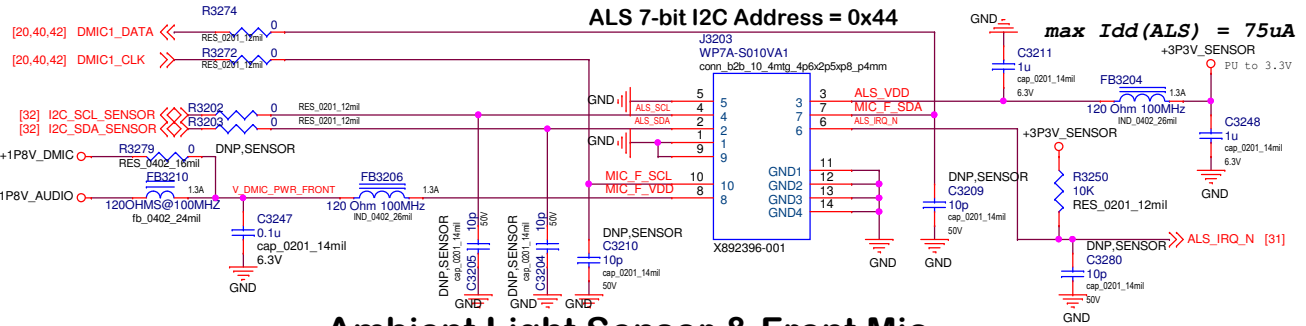
Conformally coat U3206 and all other parts under the SAR shield can.


$$I_{max} = 4mA$$
$$I_{max} = 4mA$$
$$SR(\max) \leq 200 \text{ ohm}$$


7bit I2C address = 0x2C

Conformally coat U3207 and all other parts under the SAR shield can.

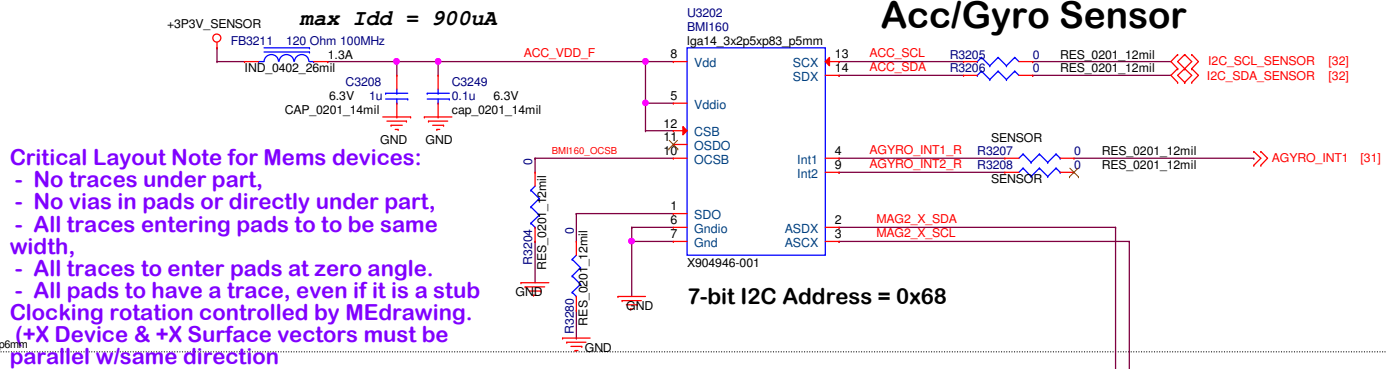
SR (max) <= 200 ohm



ALS 7-bit I2C Address = 0x44

$$\max I_{dd}(ALS) = 75\mu A$$

Ambient Light Sensor & Front Mic



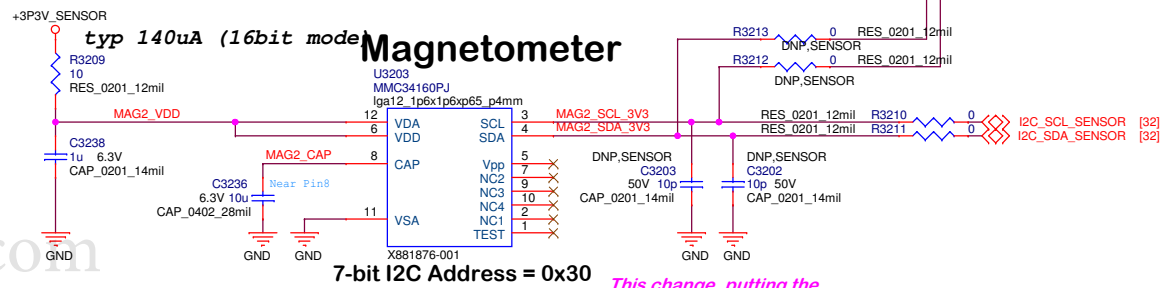
Critical Layout Note for Mems devices:

- No traces under part,
 - No vias in pads or directly under part,
 - All traces entering pads to be same width,
 - All traces to enter pads at zero angle.
 - All pads to have a trace, even if it is a stub
- Clocking rotation controlled by MEdrawing.
- (+X Device & +X Surface vectors must be parallel w/same direction)

Acc/Gyro Sensor

$$\max I_{dd} = 900\mu A$$

7-bit I2C Address = 0x68



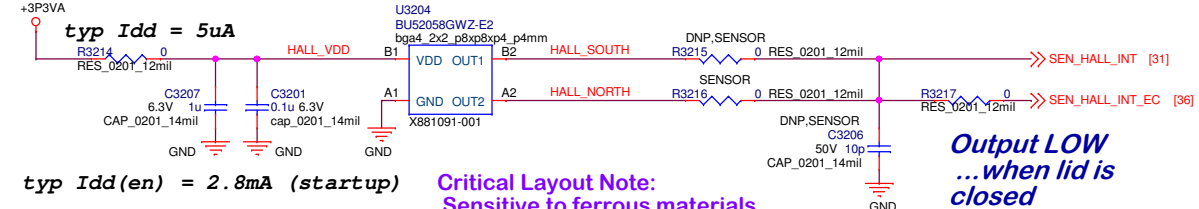
eMagnetometer

7-bit I2C Address = 0x30

Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm
... on any layer.
Clocking rotation controlled by
MEDrawing.

This change, putting the MAG behind the Agyro allows us to take advantage of the time-stamped FIFO in the Agyro to reduce power consumption and address load on the I2C bus -- in addition to improving jitter filtering in post processing. Eventually this will enable IR range camera frame syncing.

Hall Effect Sensor

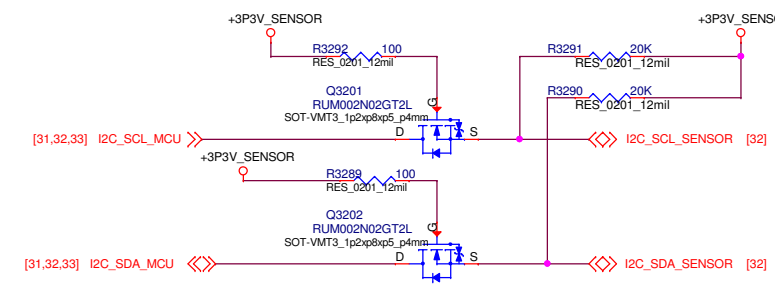


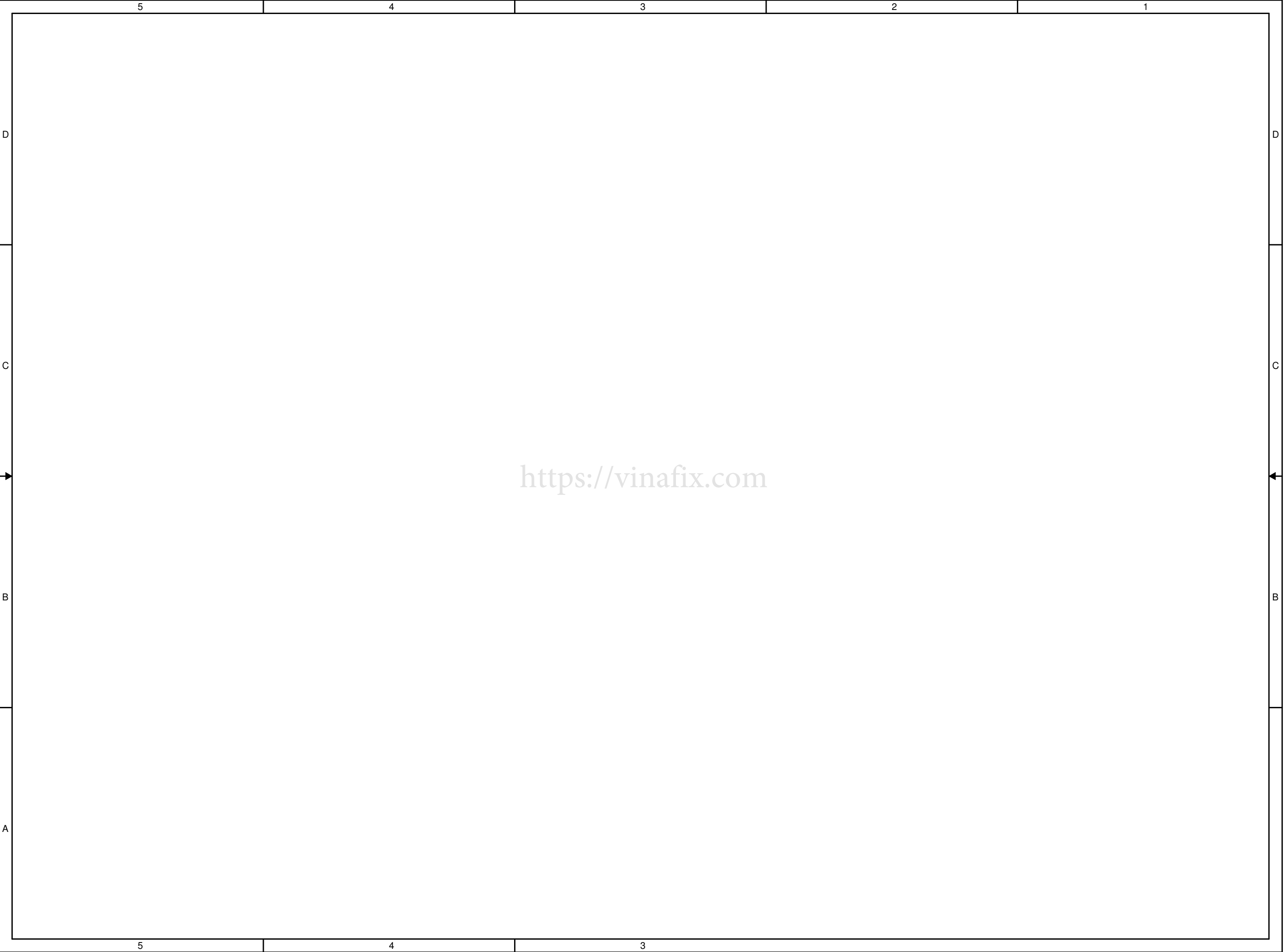
```
typ Idd = 5uA
```

$$typ\ I_{dd}(en) = 2.8mA\ (startup)$$

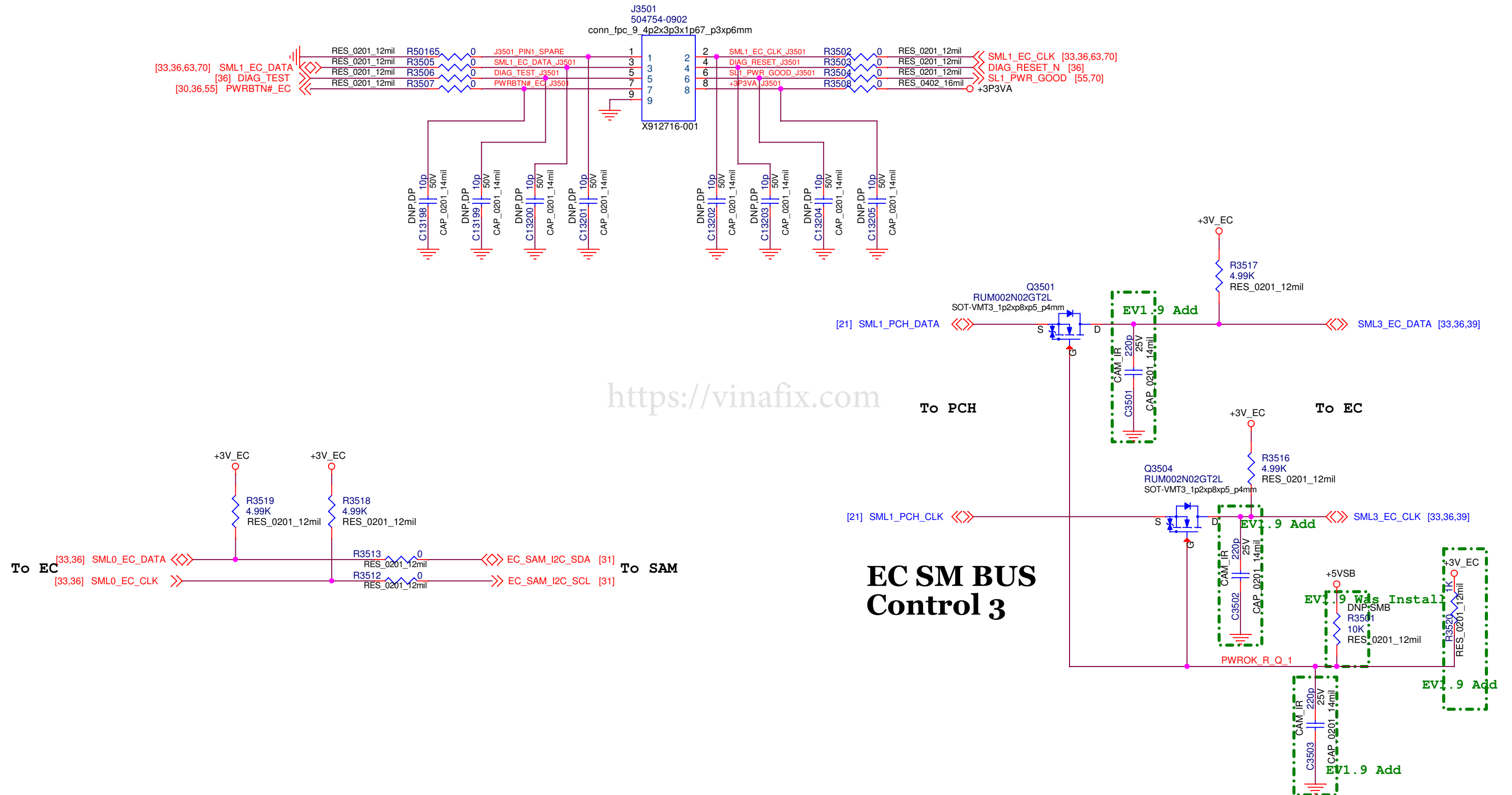
*Output LOW
...when lid is
closed*

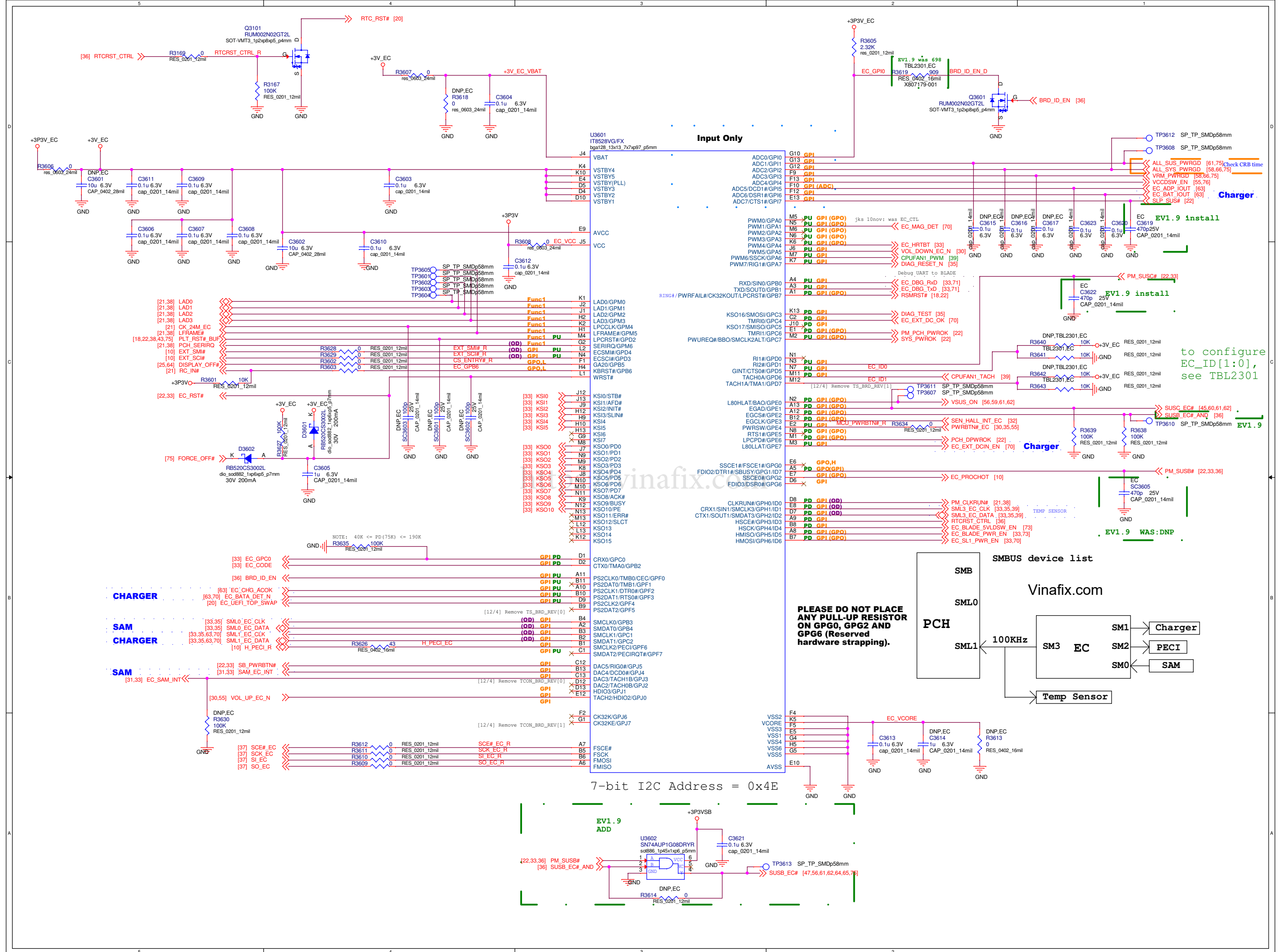
Critical Layout Note:
Sensitive to ferrous materials
Do not mount under a steel shield can
If mounted on Glass side of board,
Trigger may occur
as early as 30Gauss North B-field
or as late as 50Gauss North B-field
Be careful not to mount within 15mm
of speaker autofocus camera or other
magnet.
X-Y location controlled by MEdrawing.





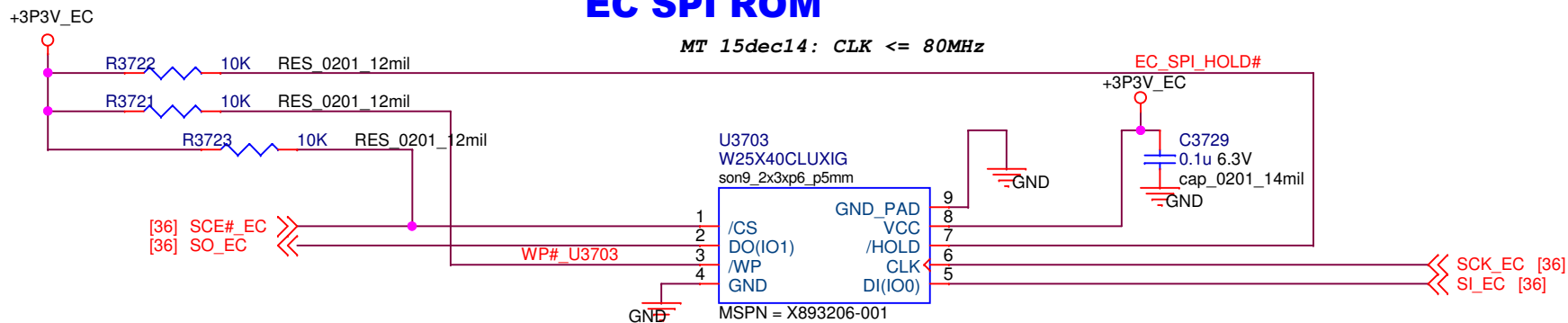
DIAGNOSTIC CONNECTOR





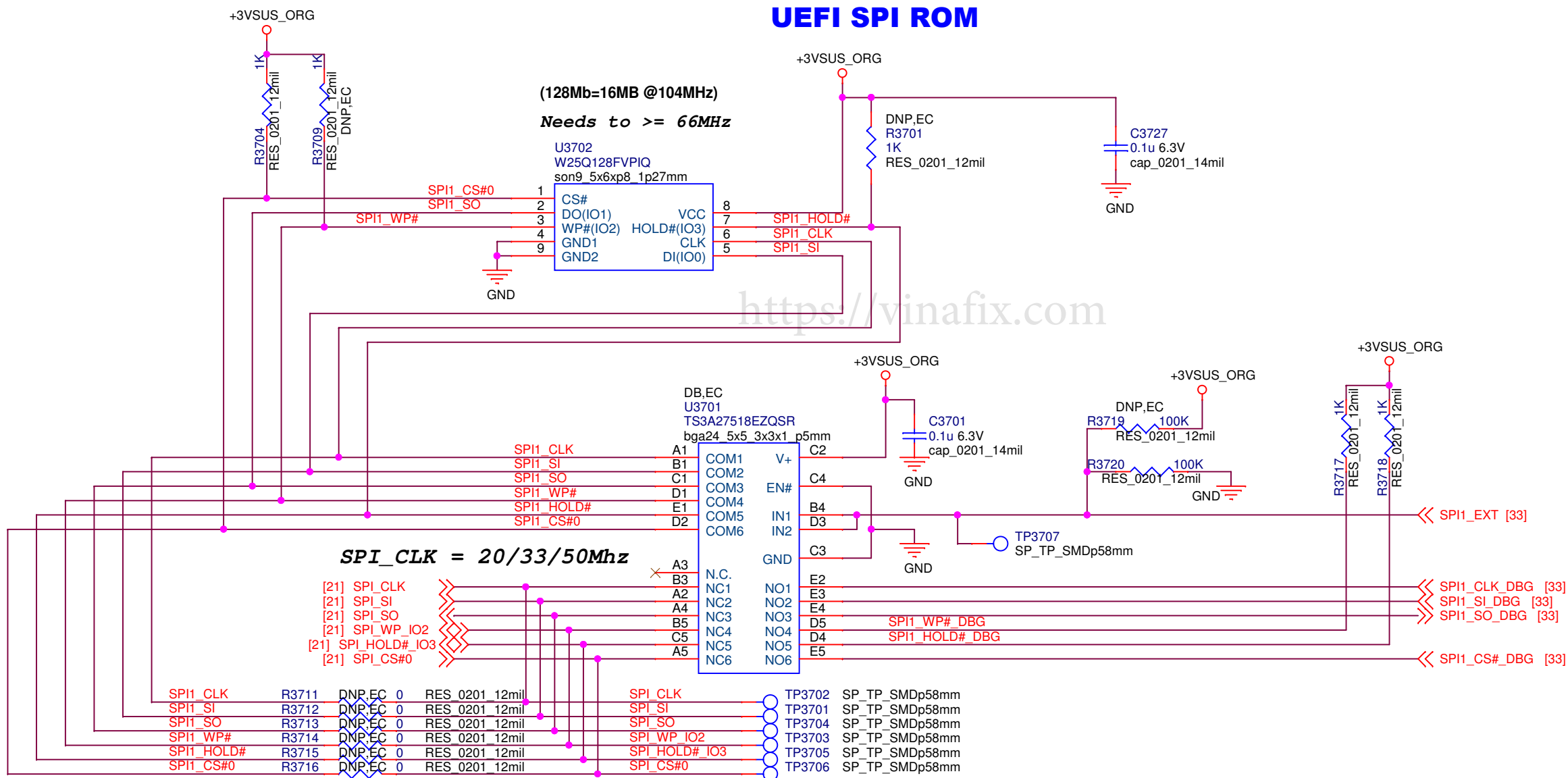
EC SPI ROM

MT 15dec14: CLK <= 80MHz



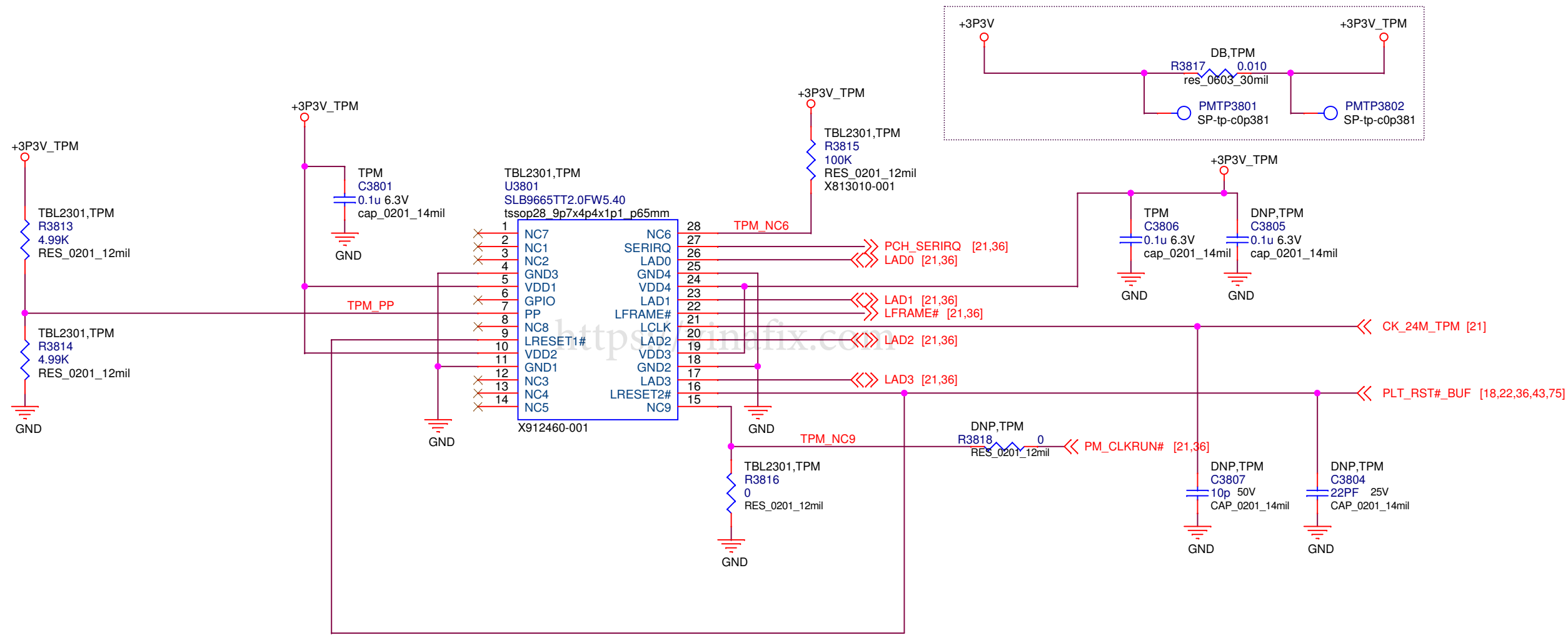
UEFI SPI ROM

(128Mb=16MB @104MHz)
Needs to >= 66MHz



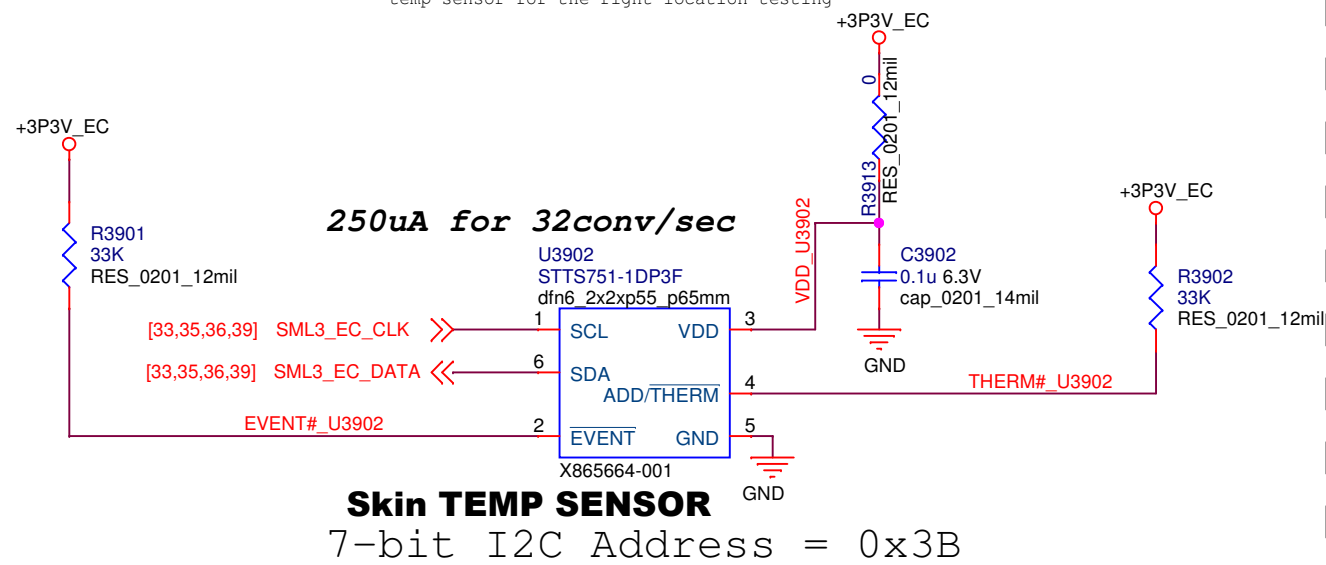
IN1/IN2 = L => COM to NC
IN1/IN2 = H => NC to COM

Trusted Platform Module

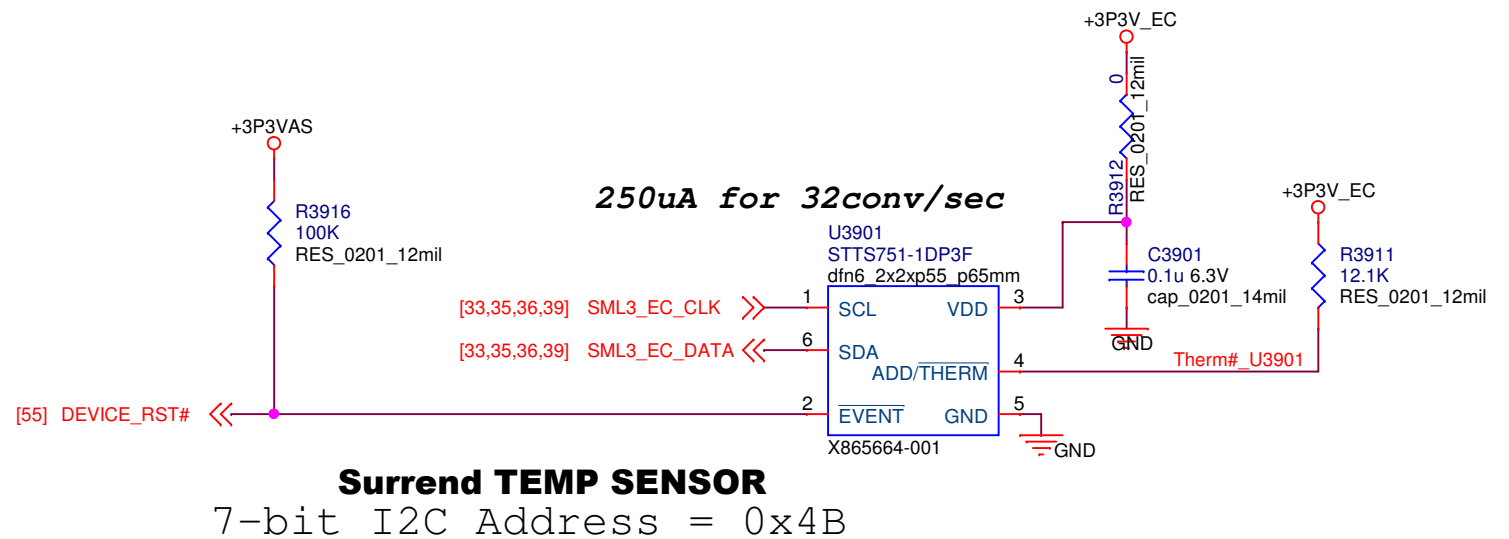
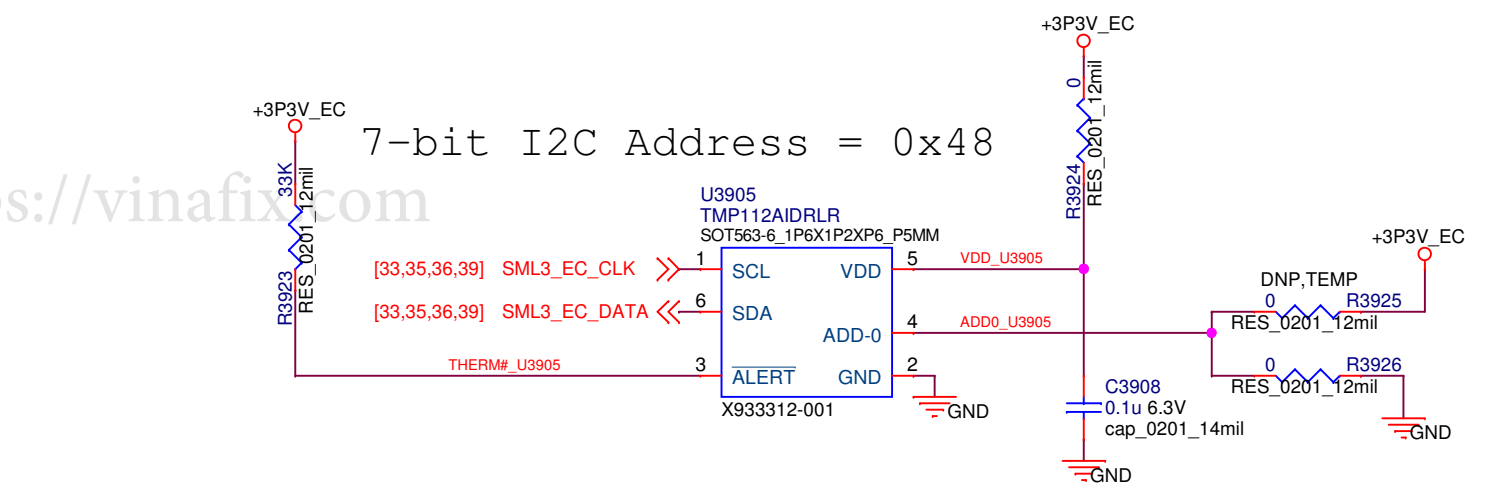
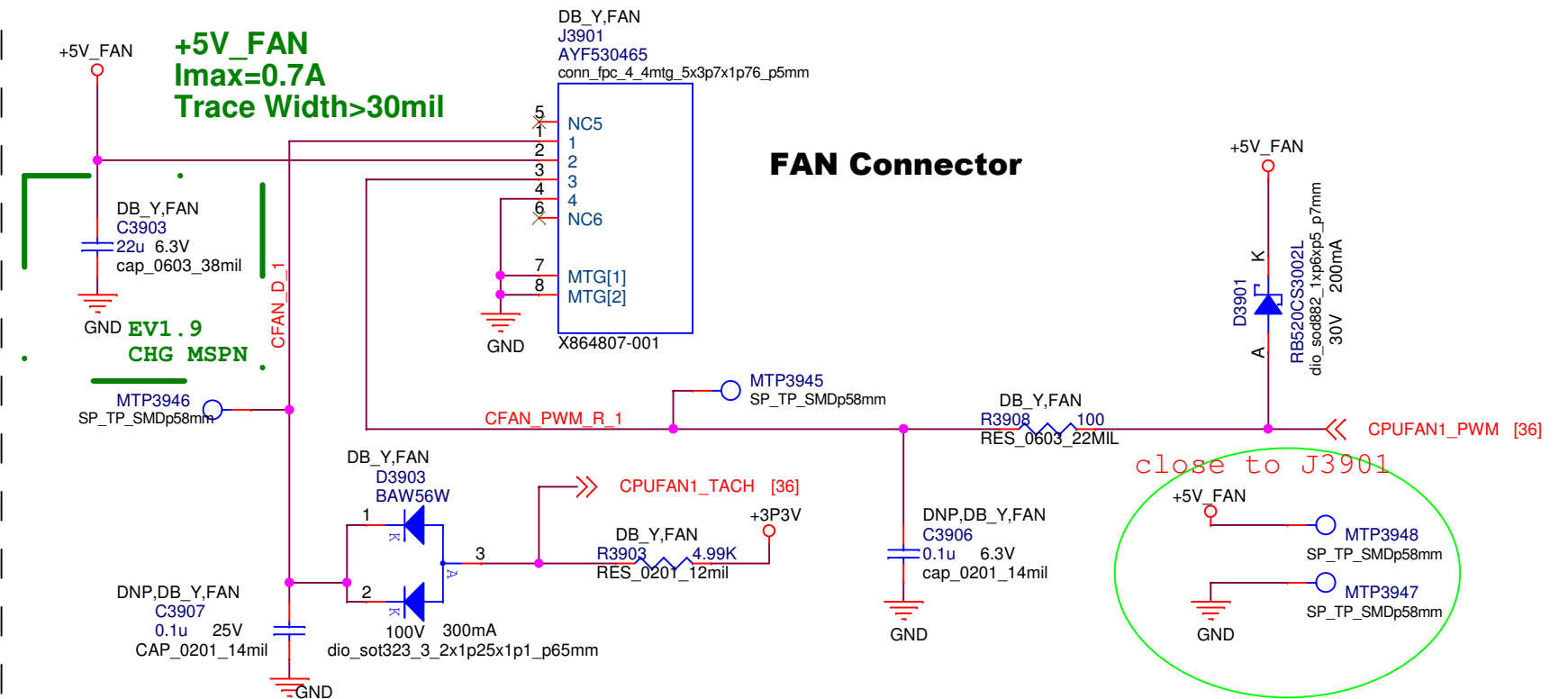
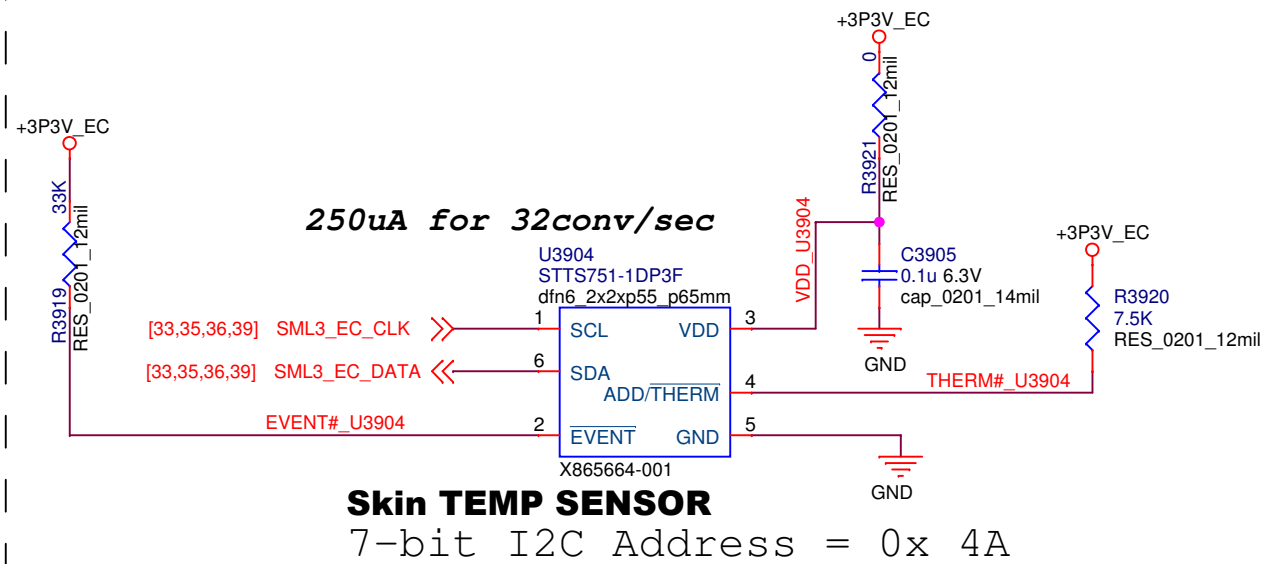
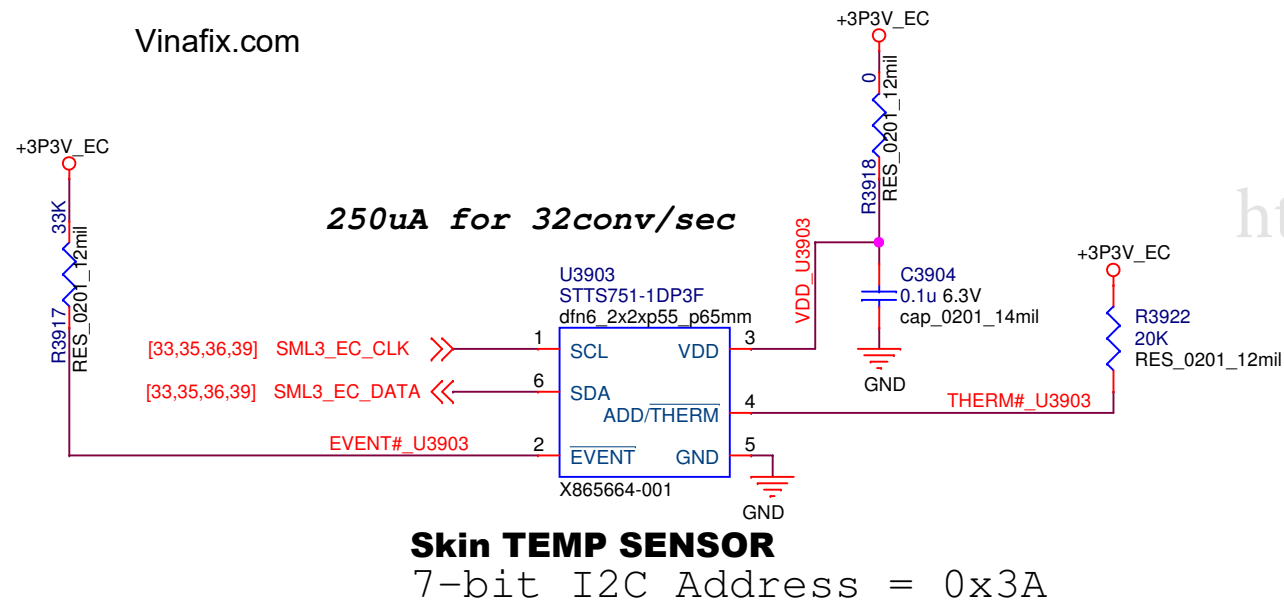


jks 6dec14: Only one sensor will be used for final product

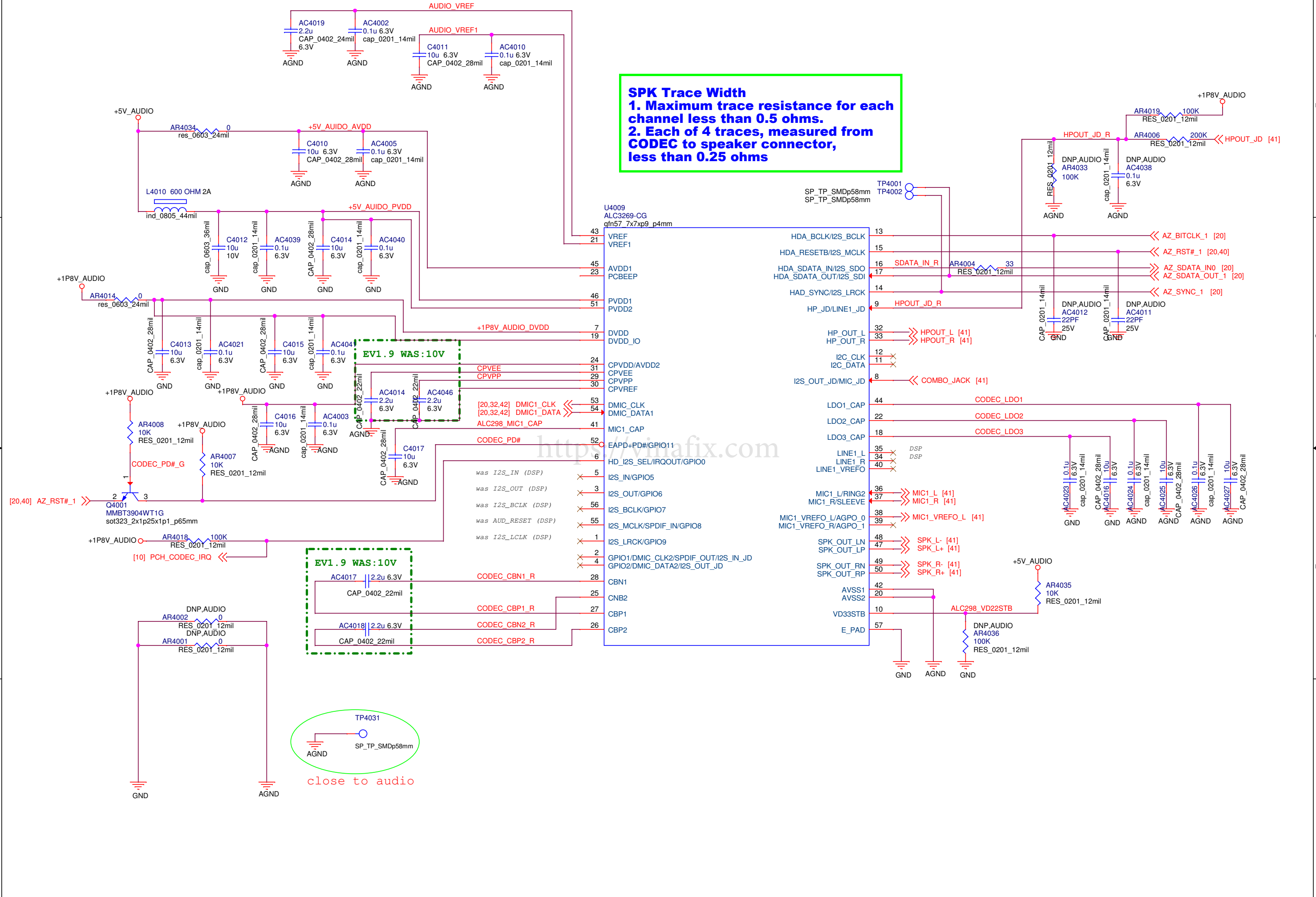
temp sensor for the right location testing



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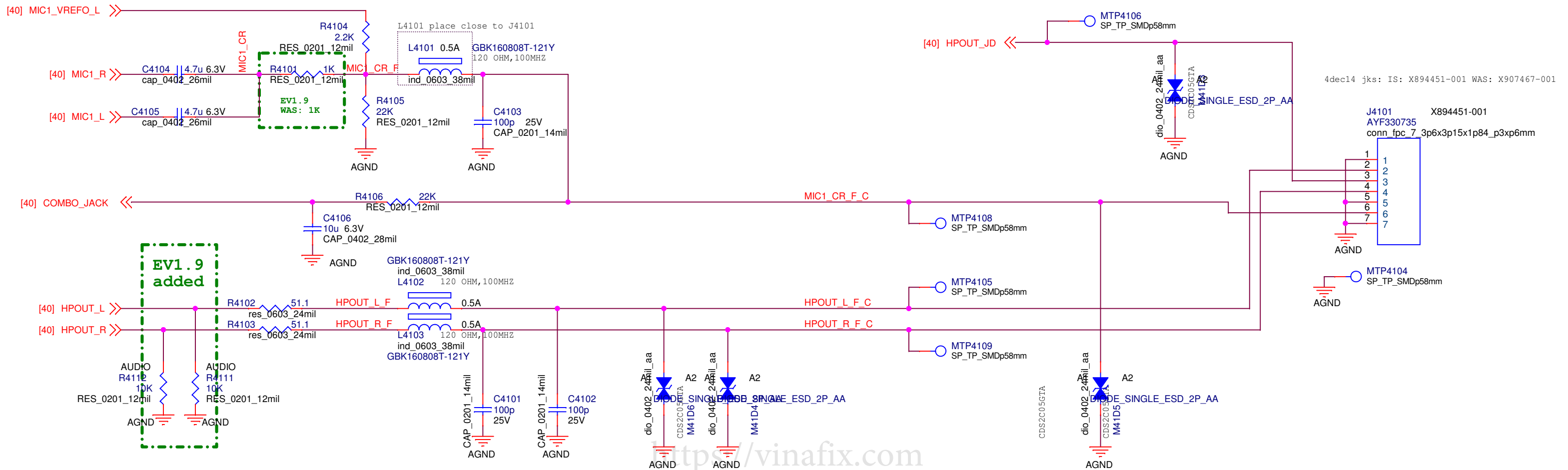


D
C
B
A

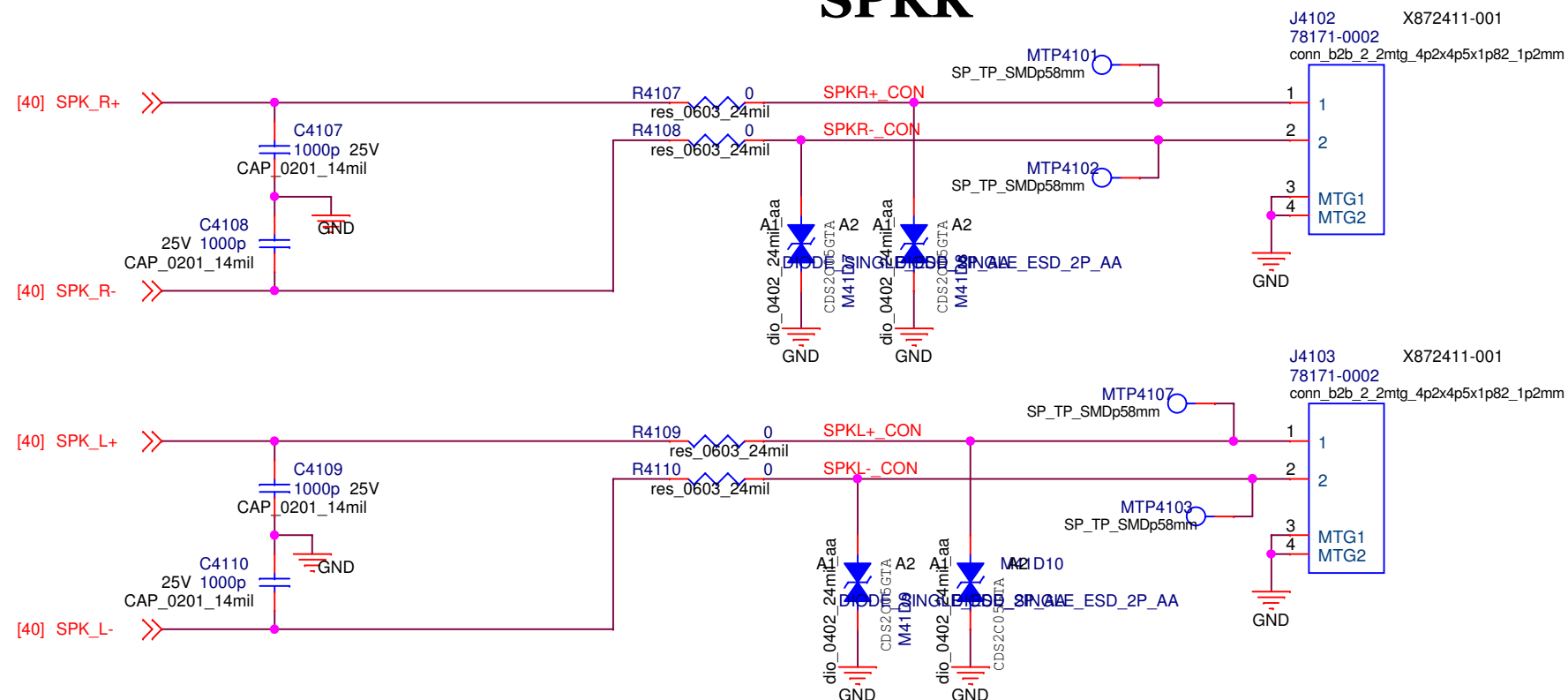


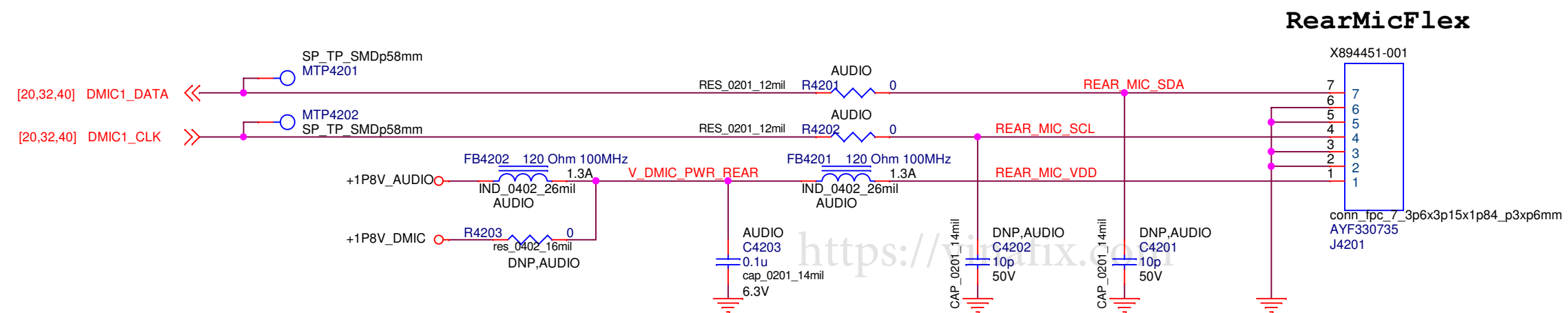
D
C
B
A

Audio Jack/MIC1 Combo Jack



SPKR

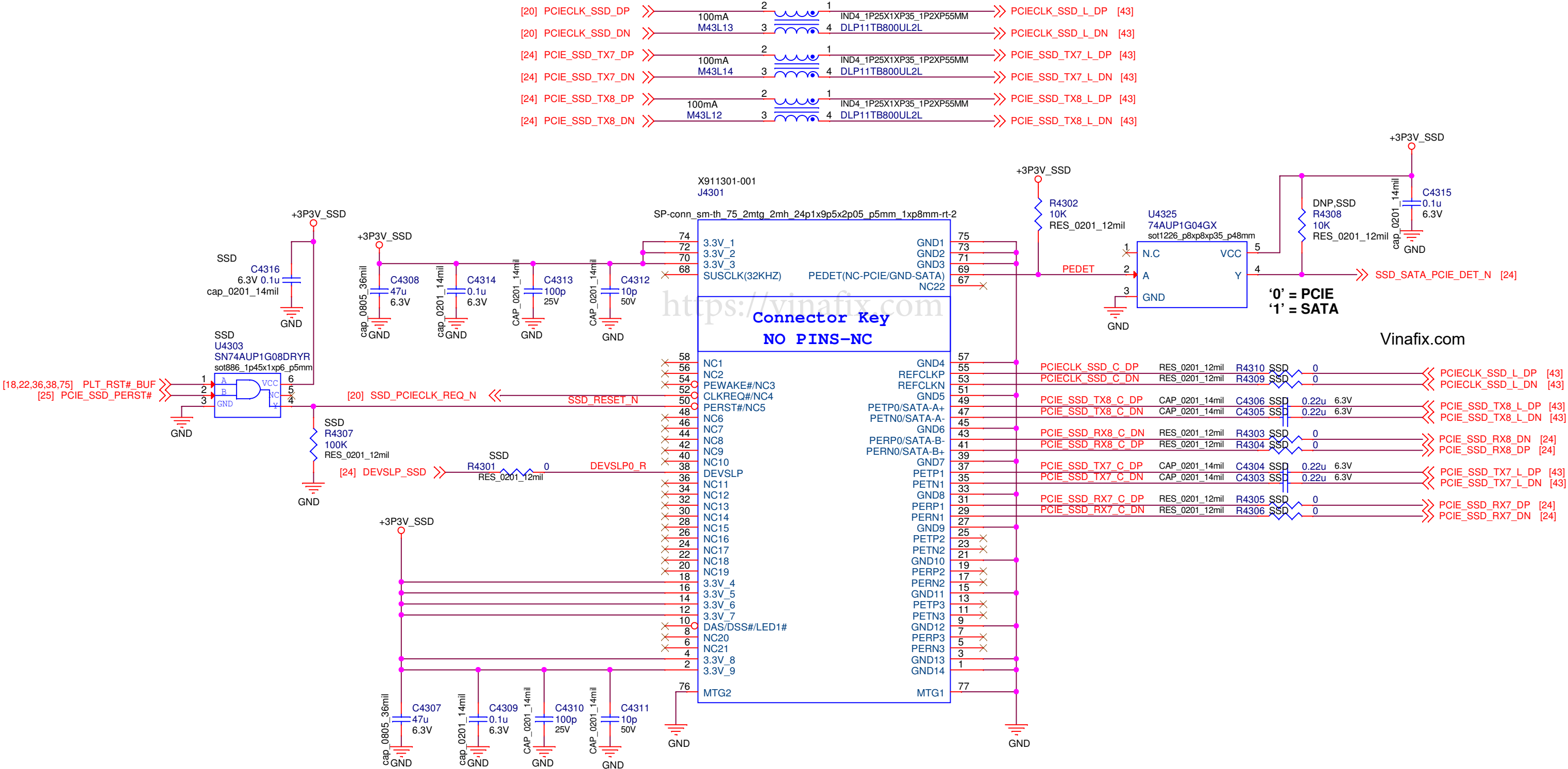


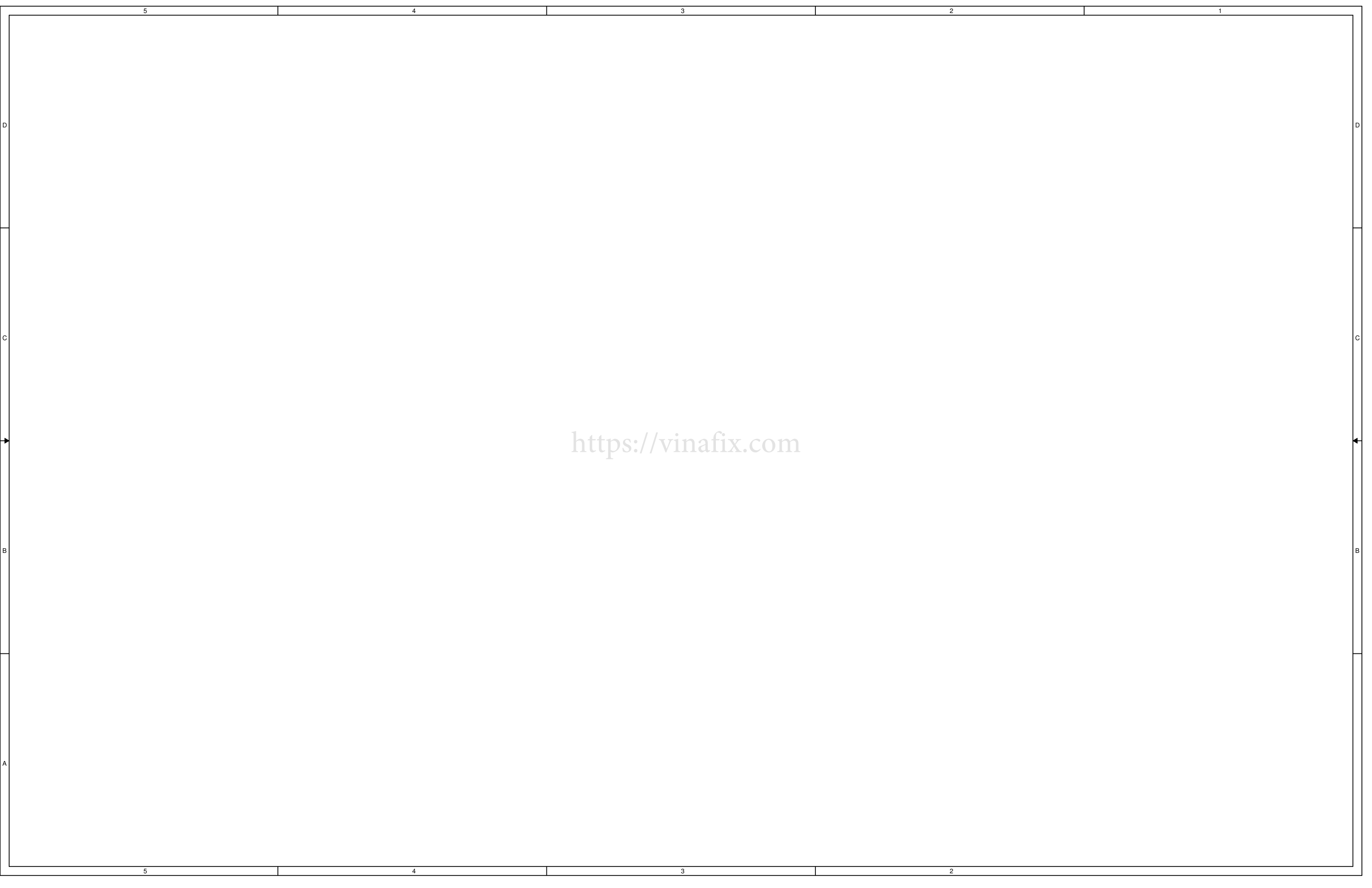


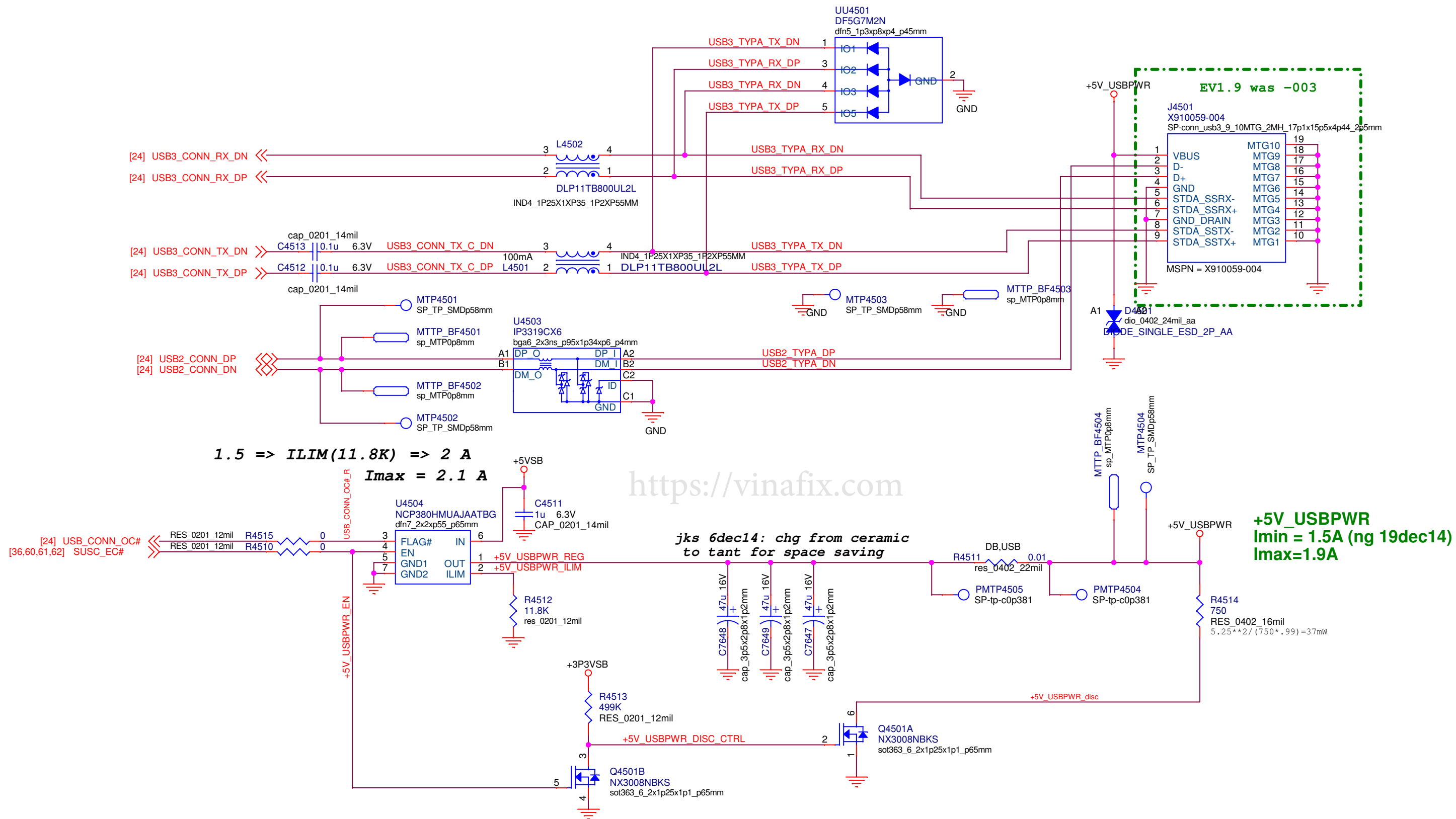
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen2/SATA	PCI Express* Gen3/SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.

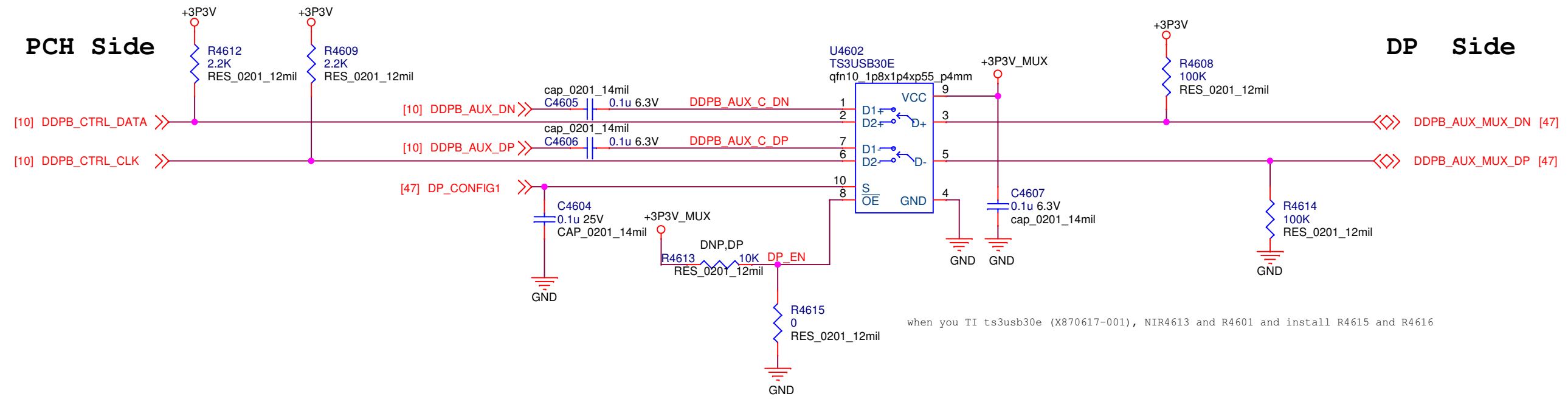
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.



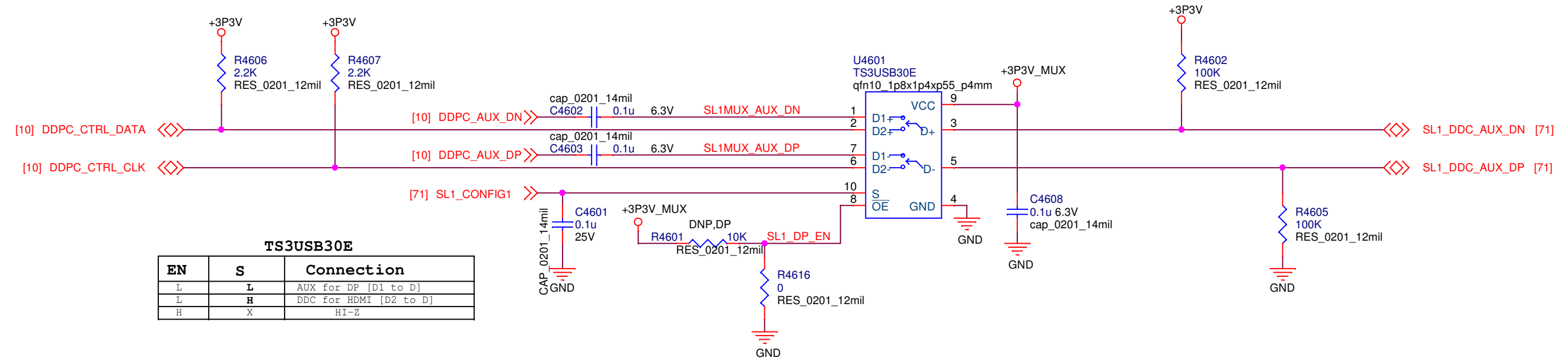




mDP mux to HDMI/DVI Dongle control



SL1 DP mux to HDMI/DVI Dongle control



NOTE:
Pass gate to prevent back-drive when sink device is on and PCH is powered down.

NOTE:
Place D4701 near to DP connector

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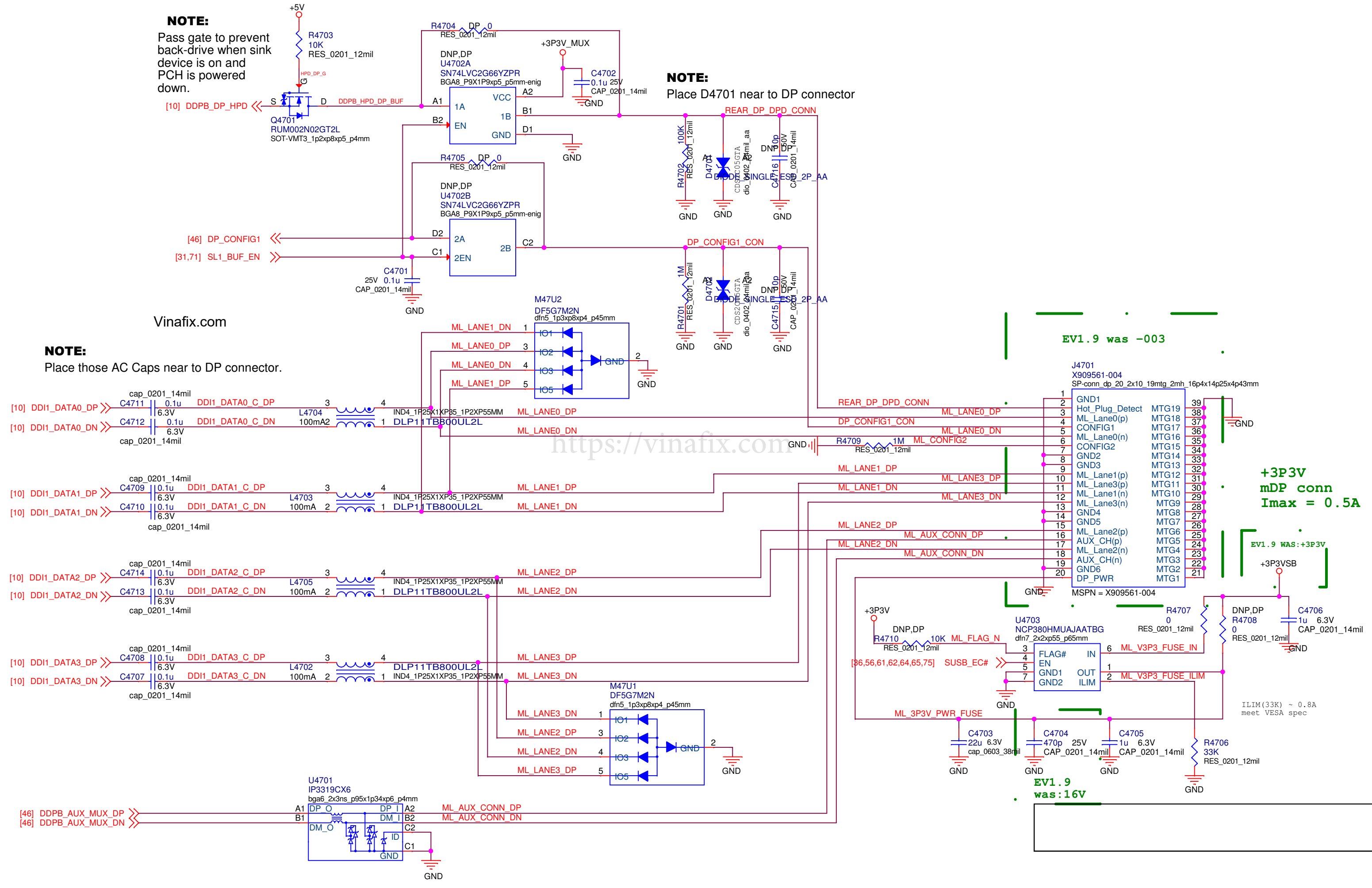
NOTE:
Place those AC Caps near to DP connector.

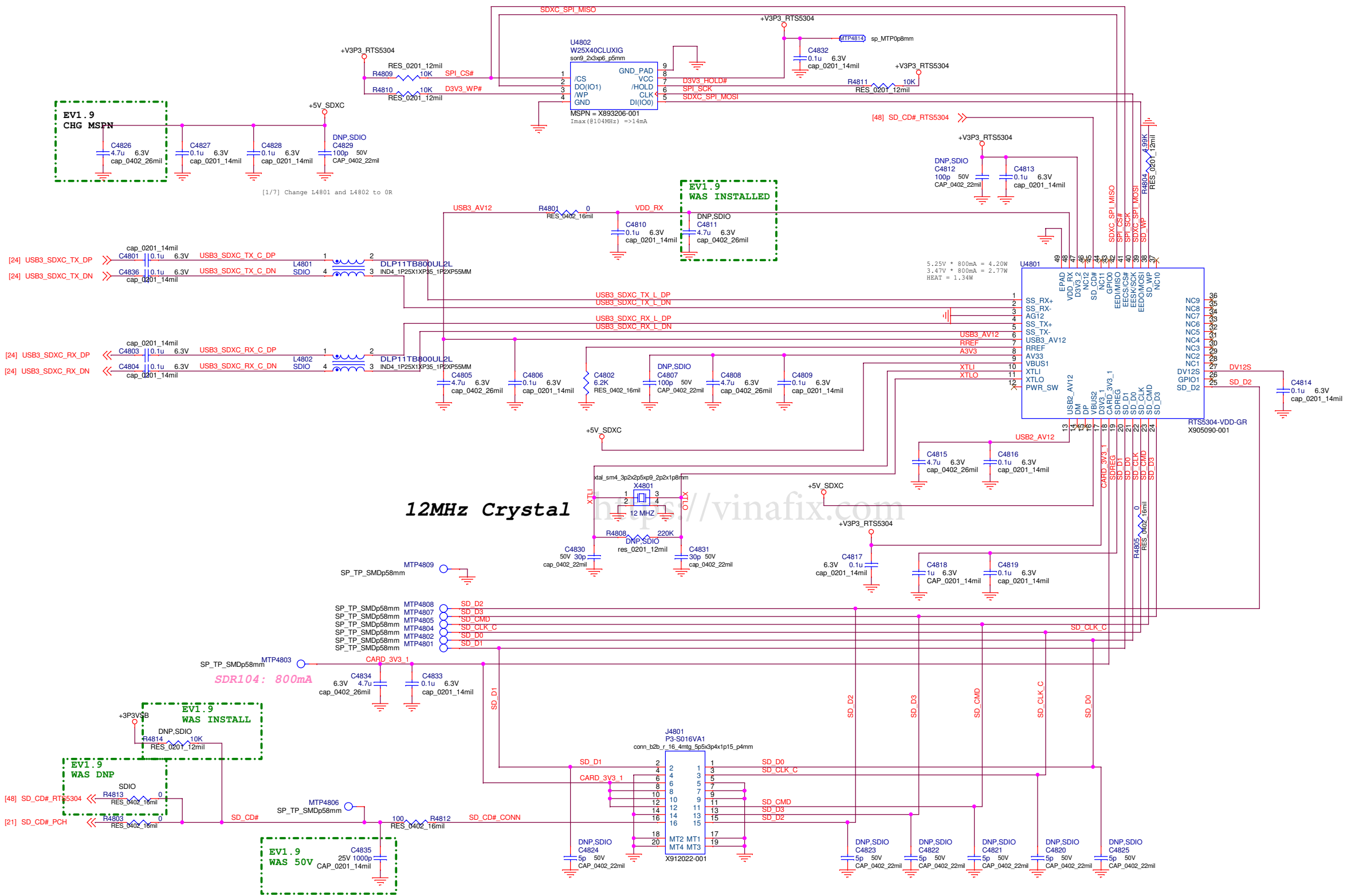
EV1.9 was -003

+3P3V
mDP conn
I_{max} = 0.5A

EV1.9 WAS: +3P3V

EV1.9 was: 16V



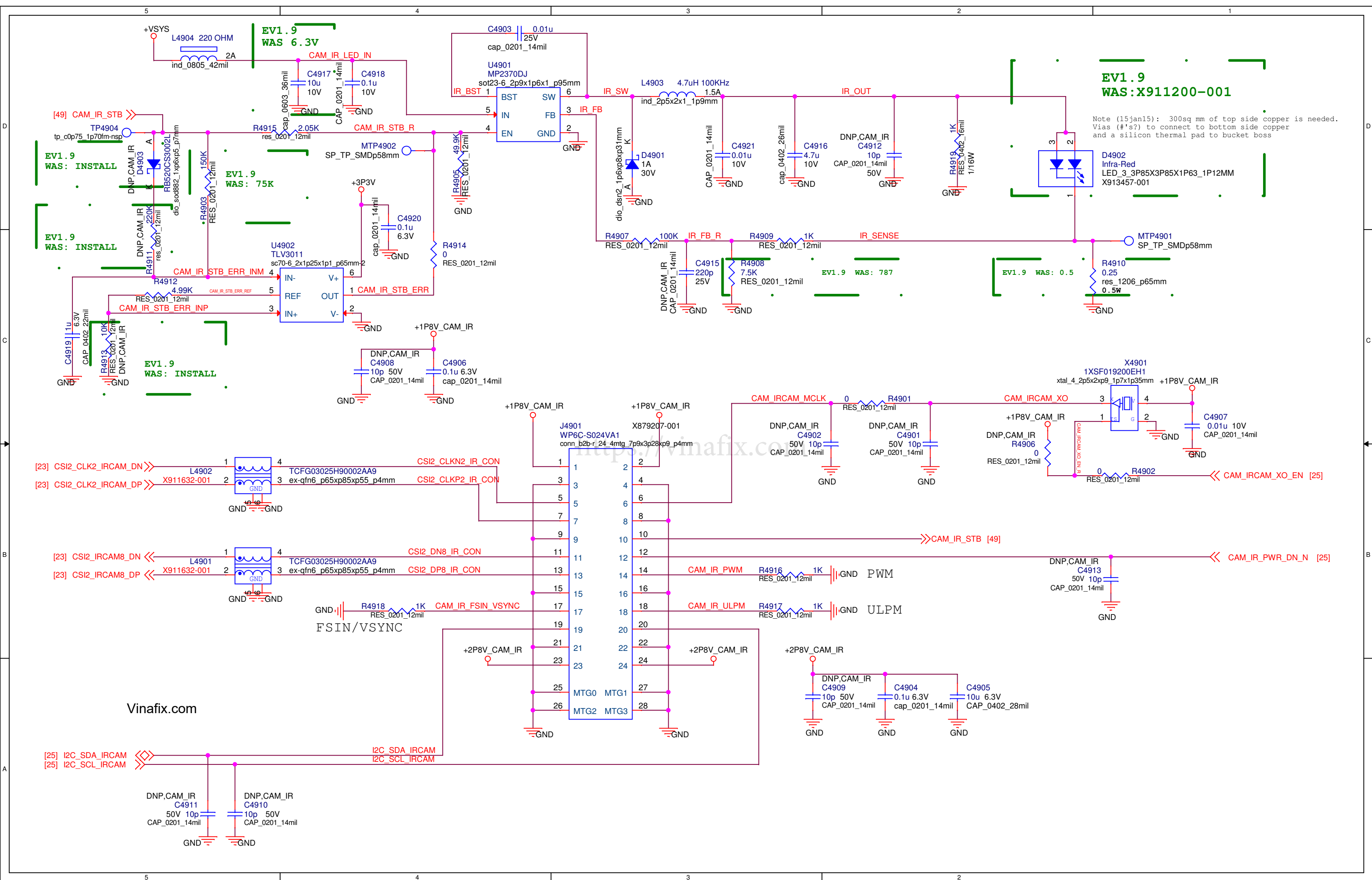


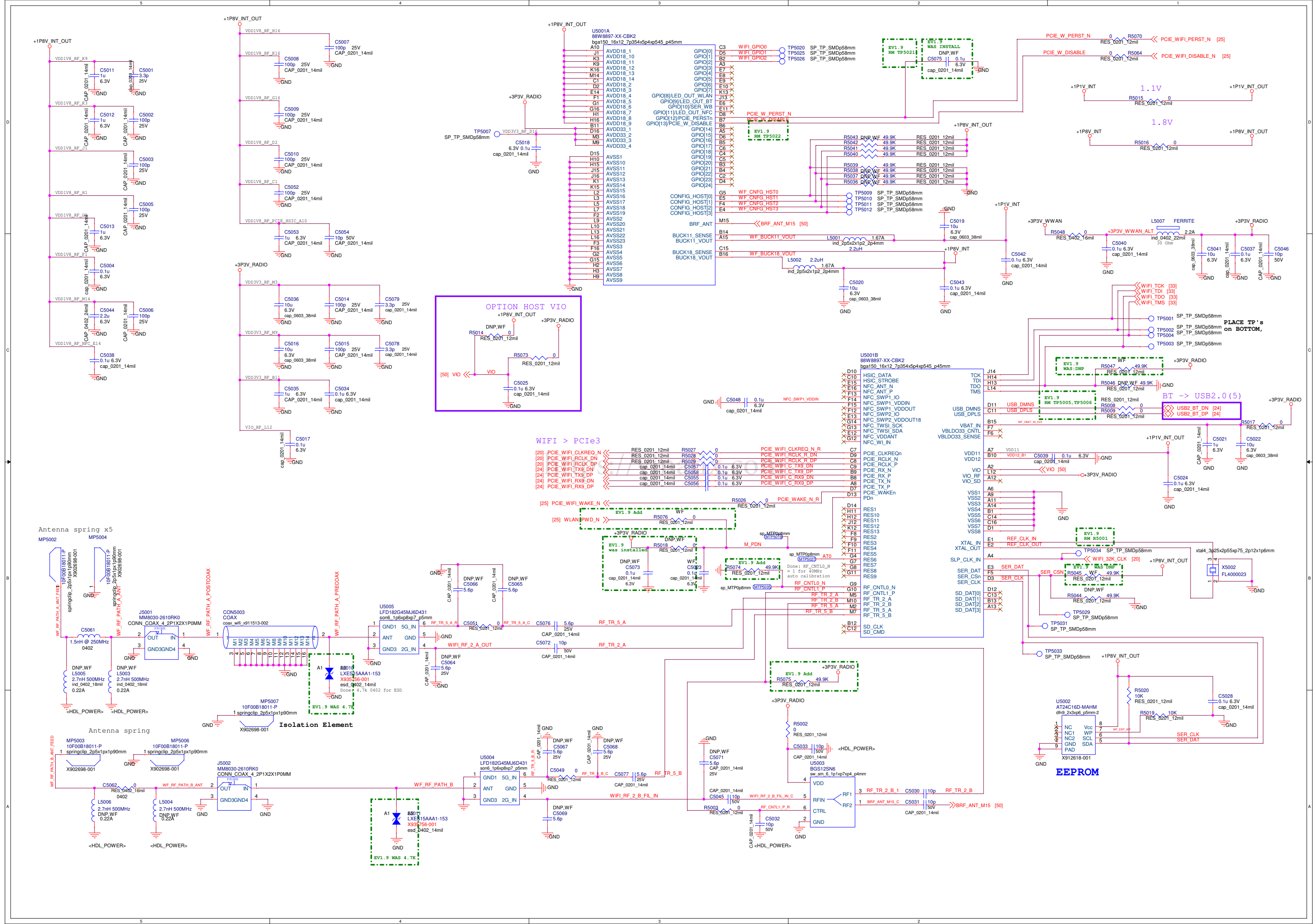
12MHz Crystal

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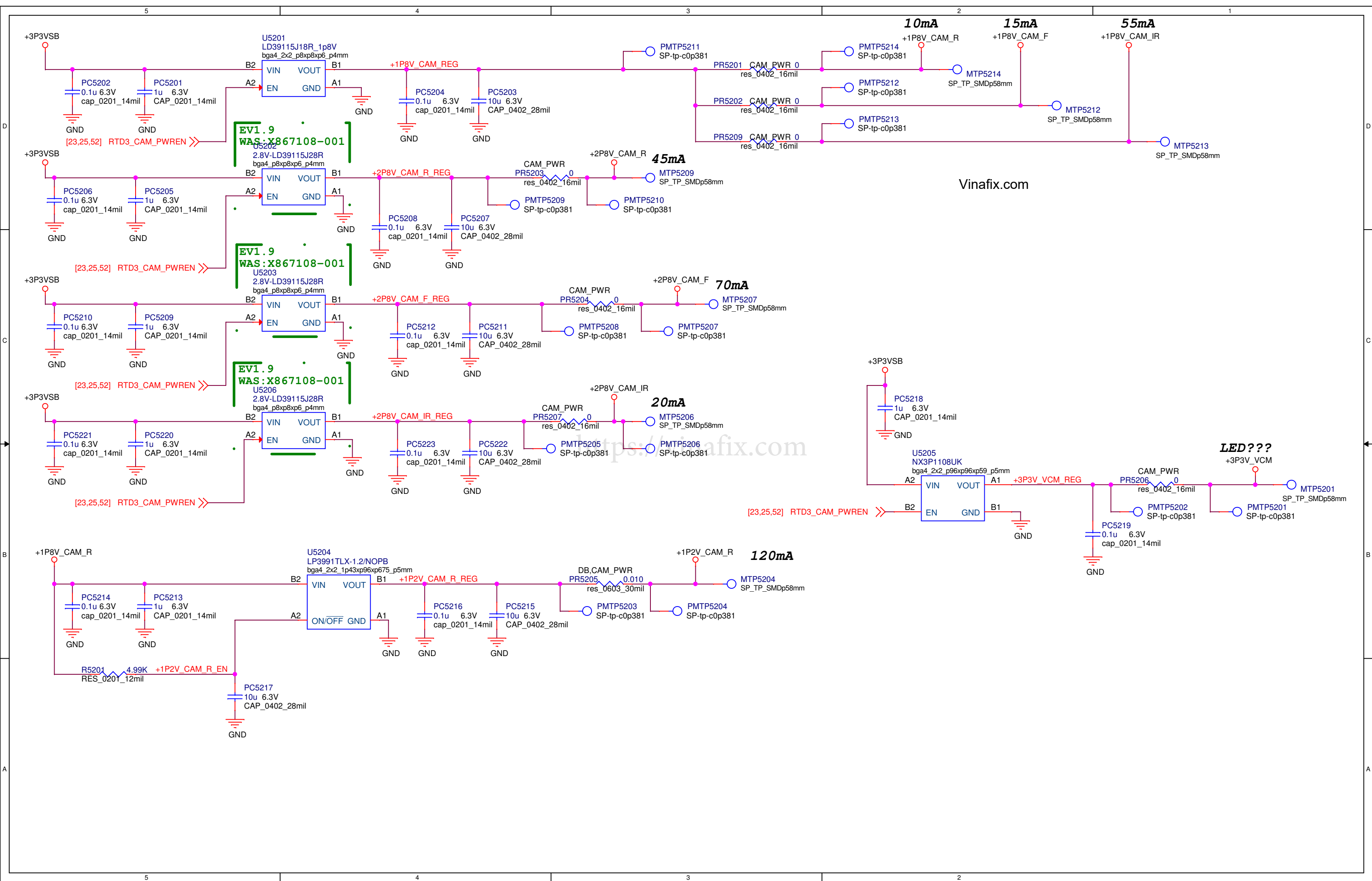
SDR104: 800ma

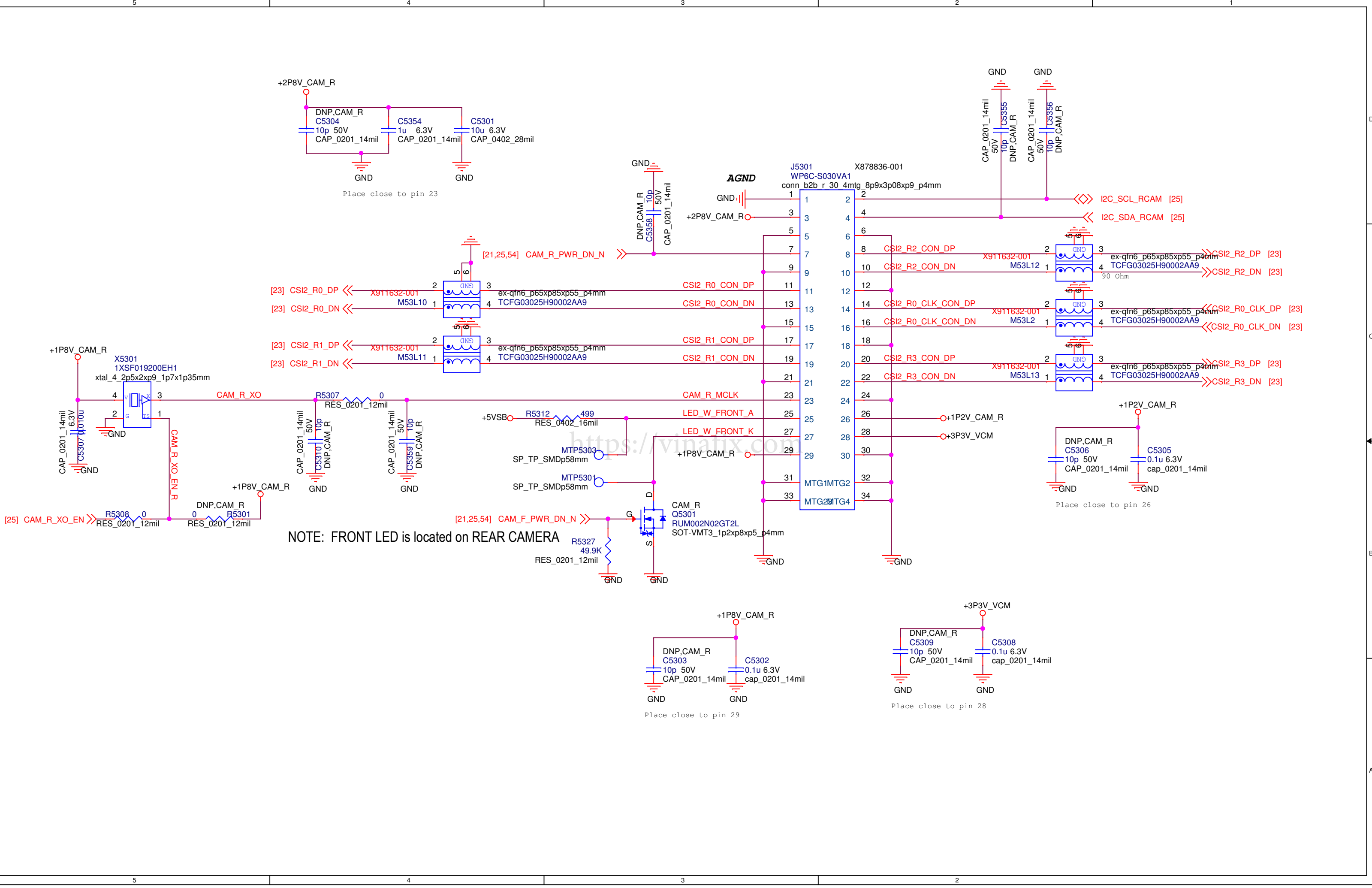
EV1.9 WAS 50V



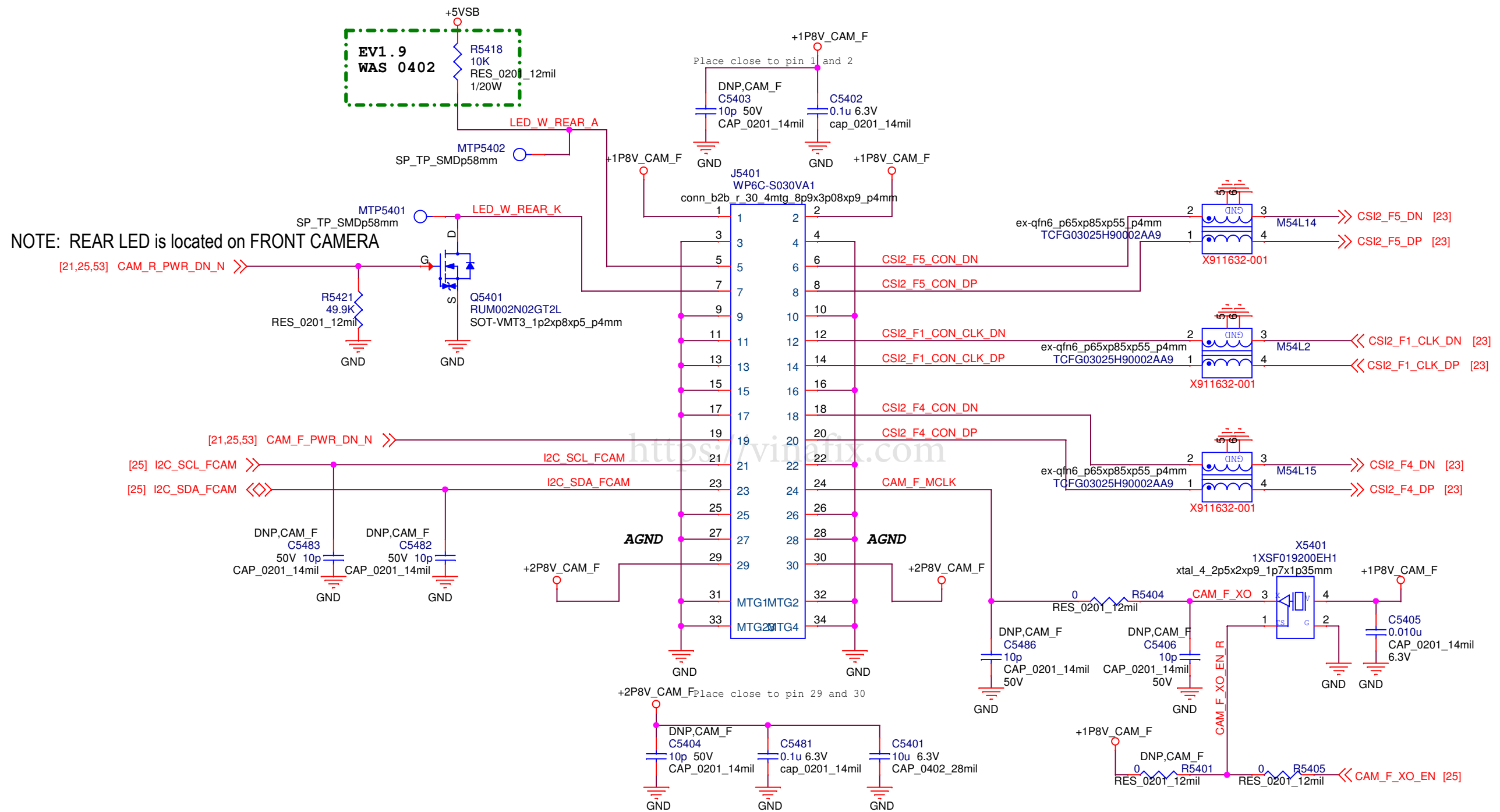


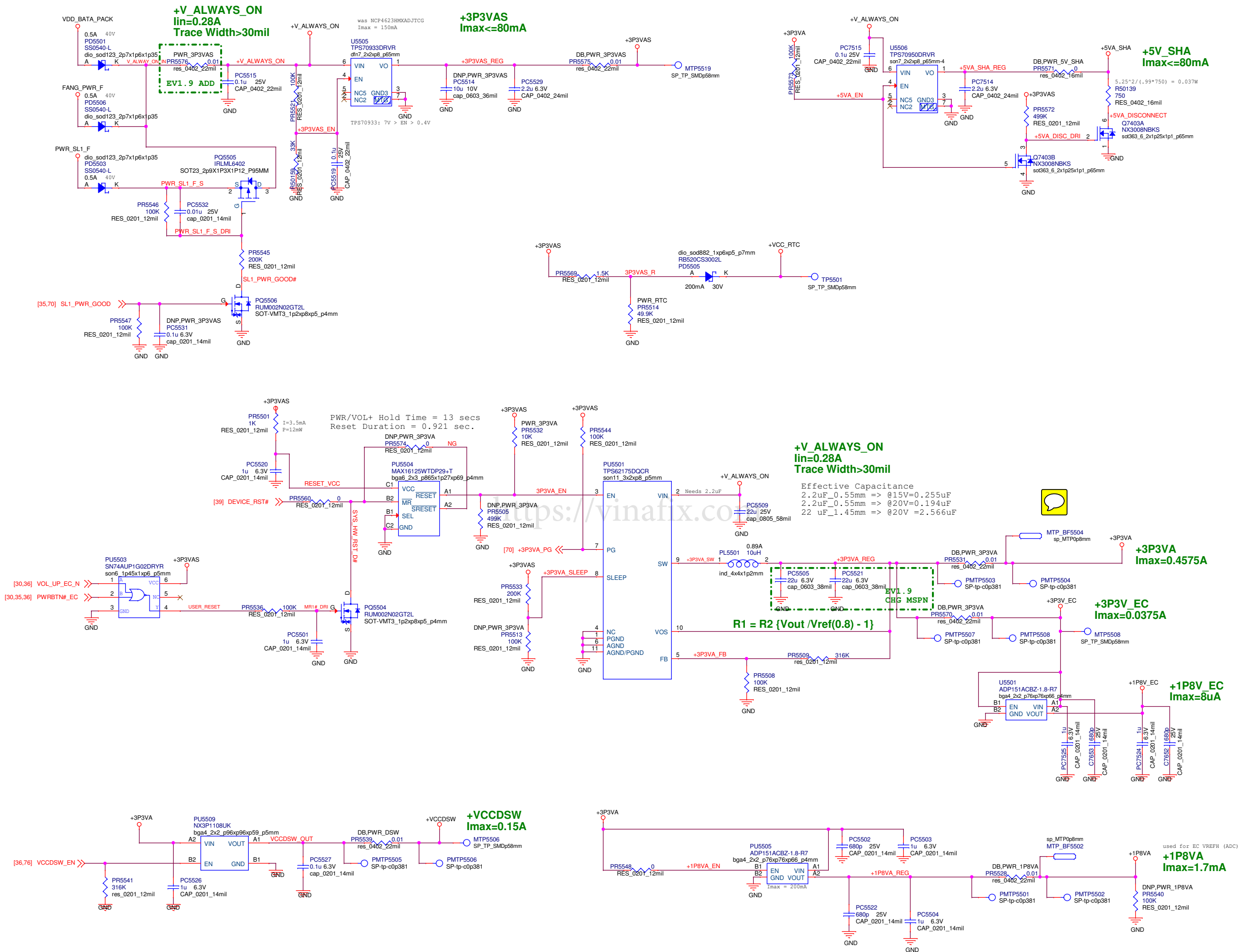
EMPTY
https://vinafix.com

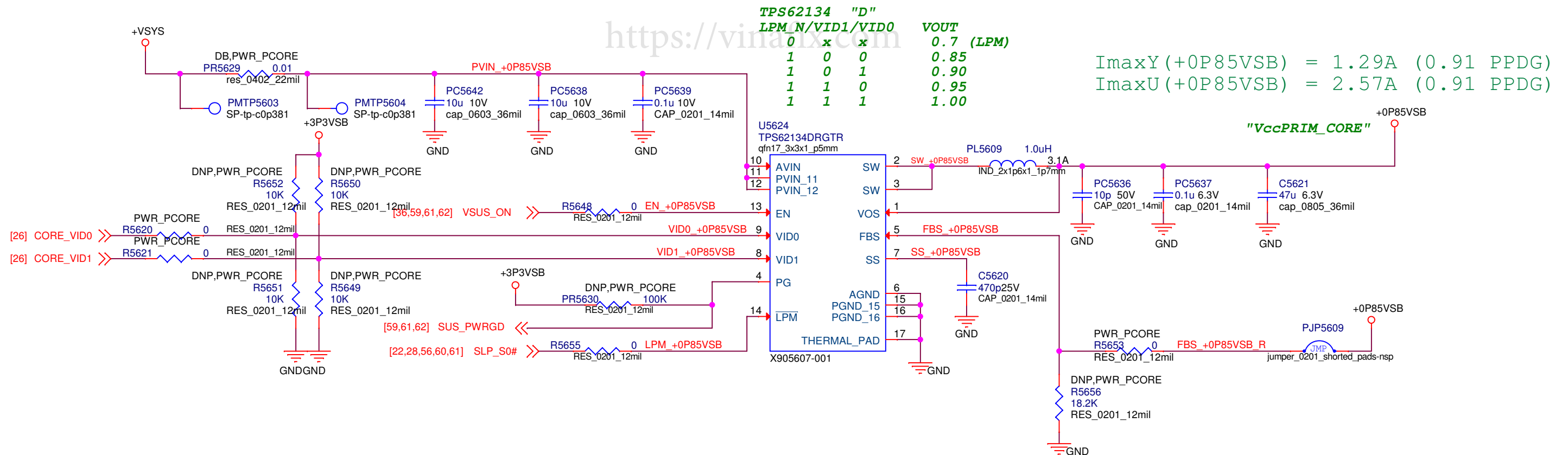
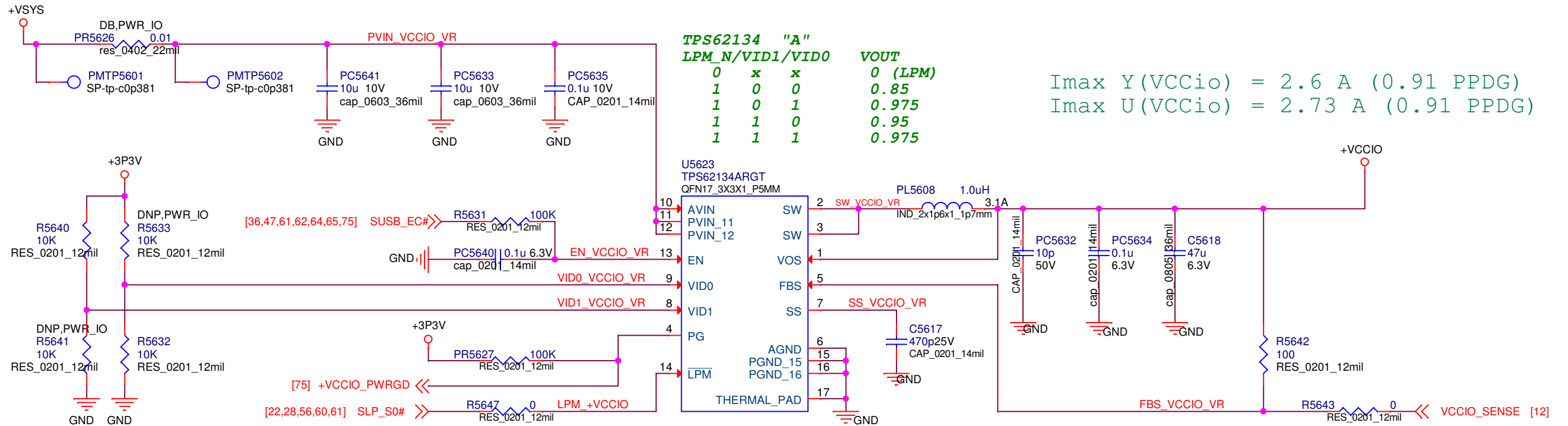


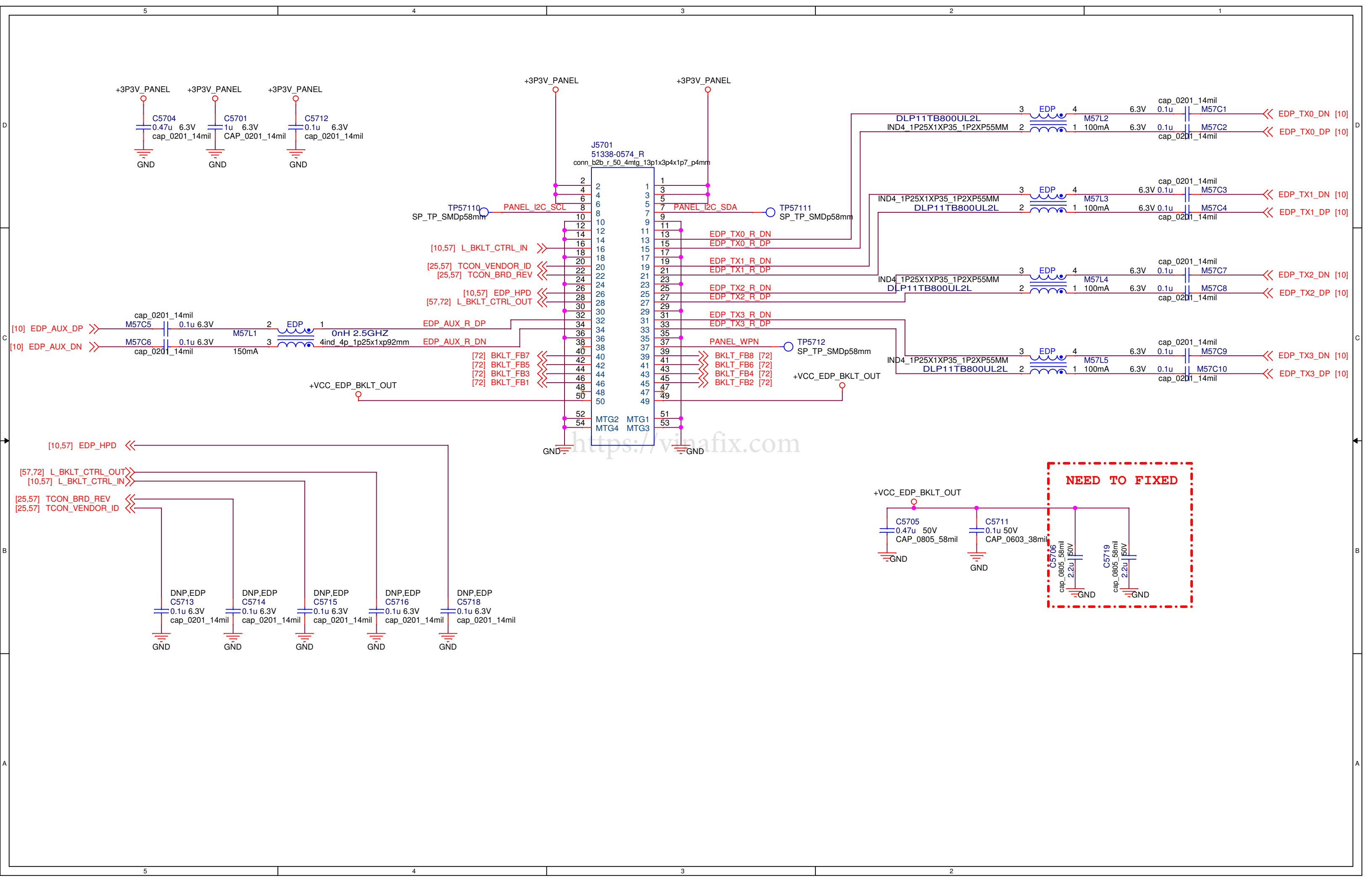


NOTE: FRONT LED is located on REAR CAMERA

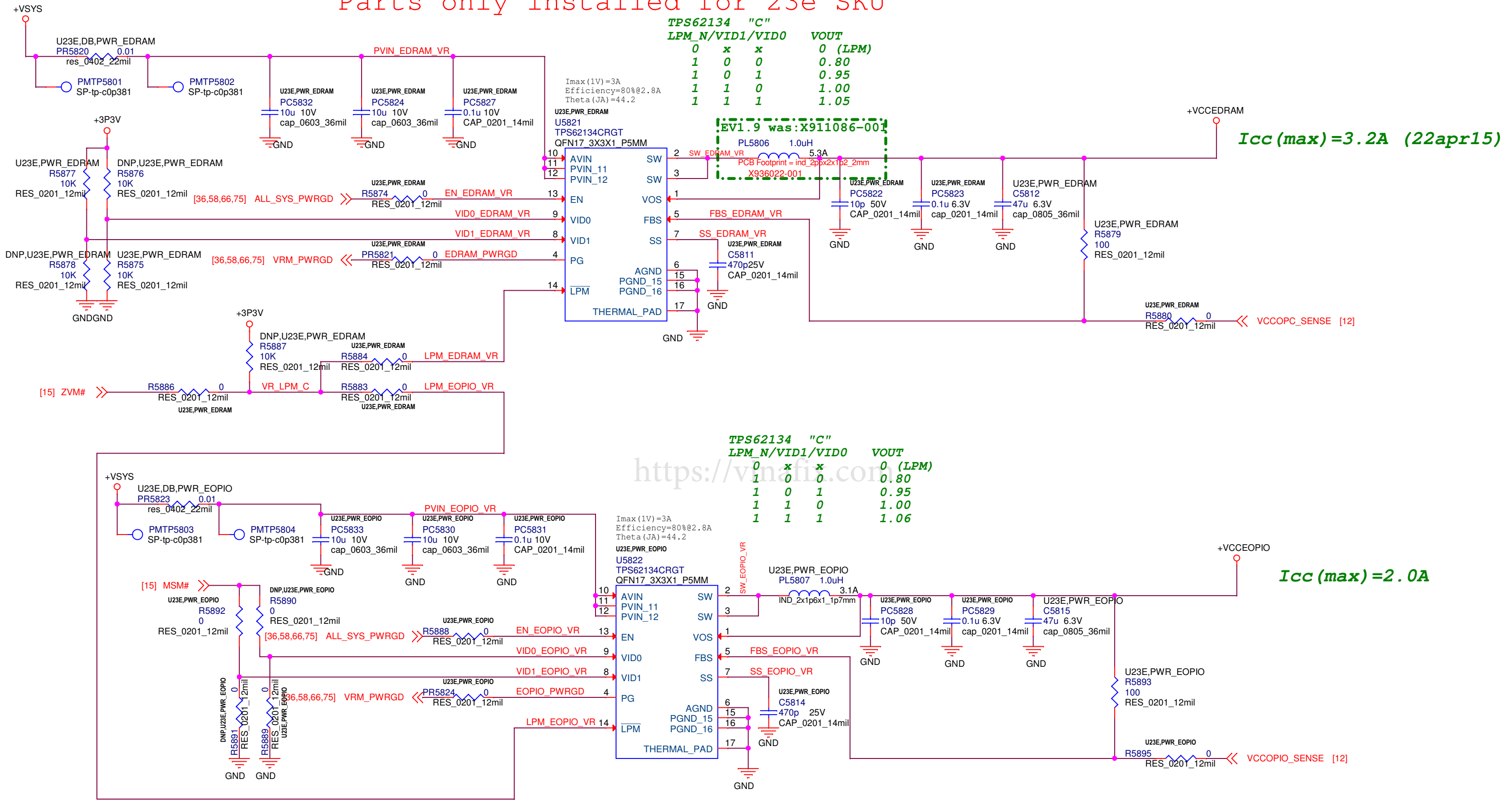


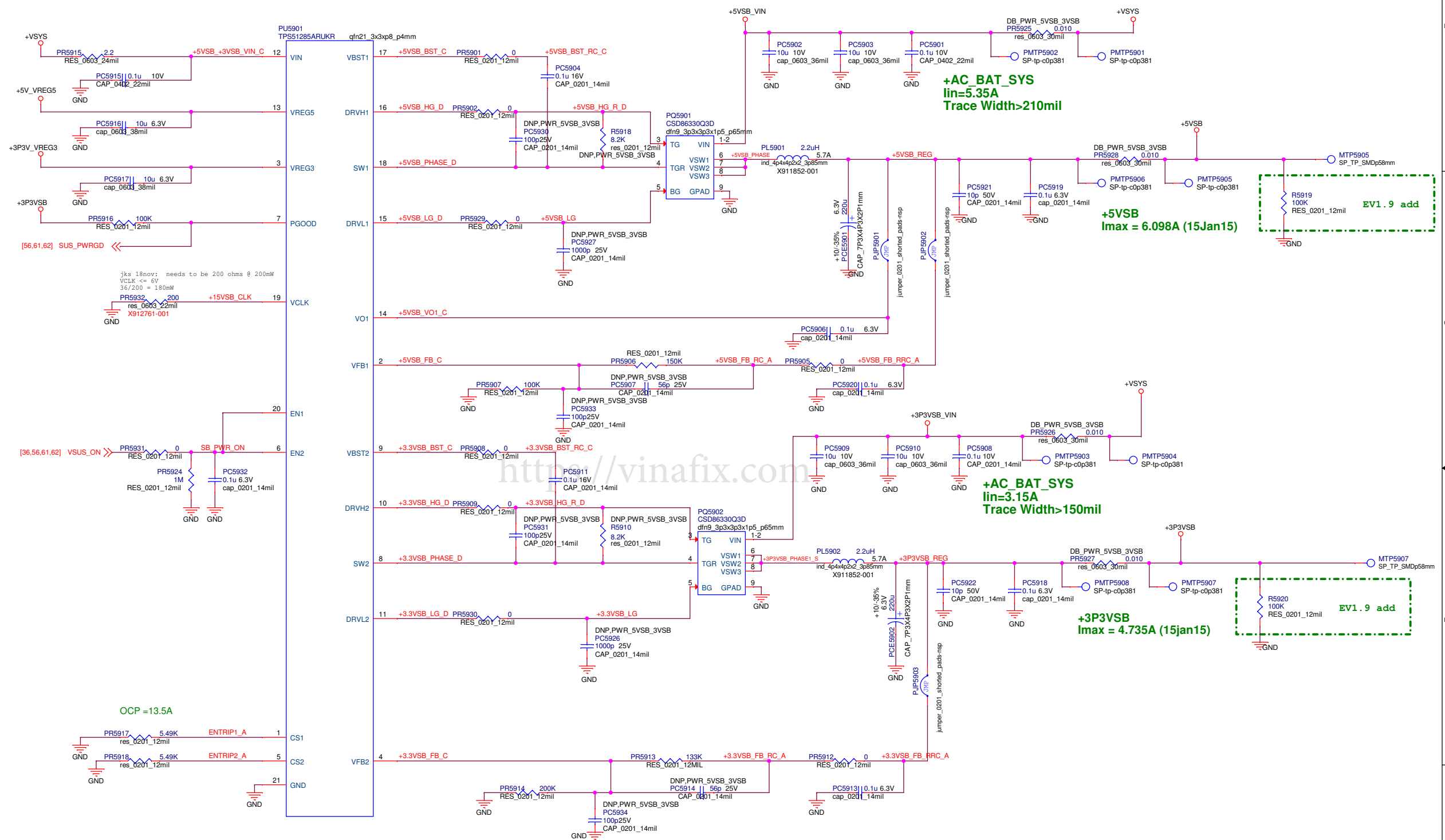


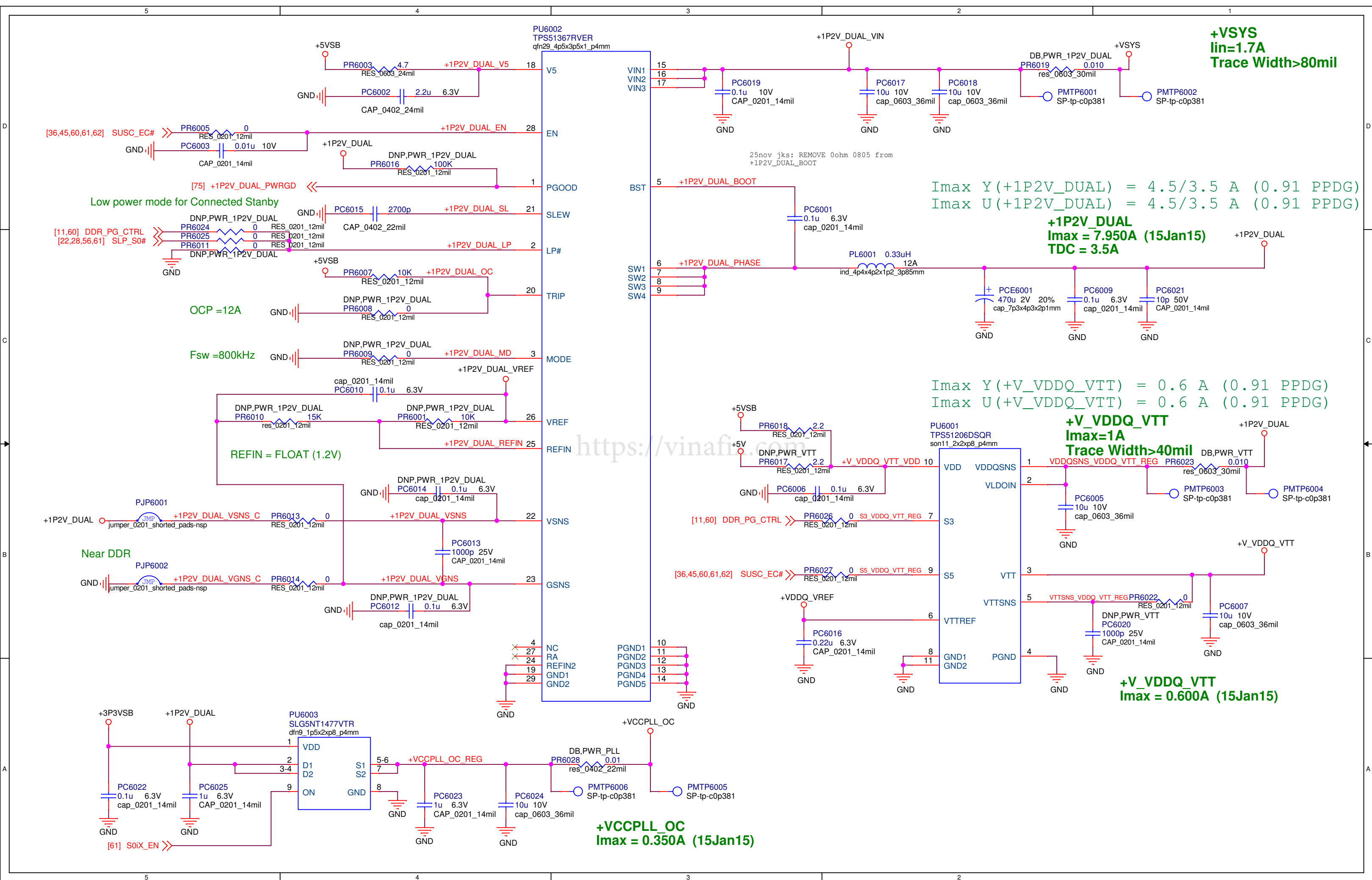


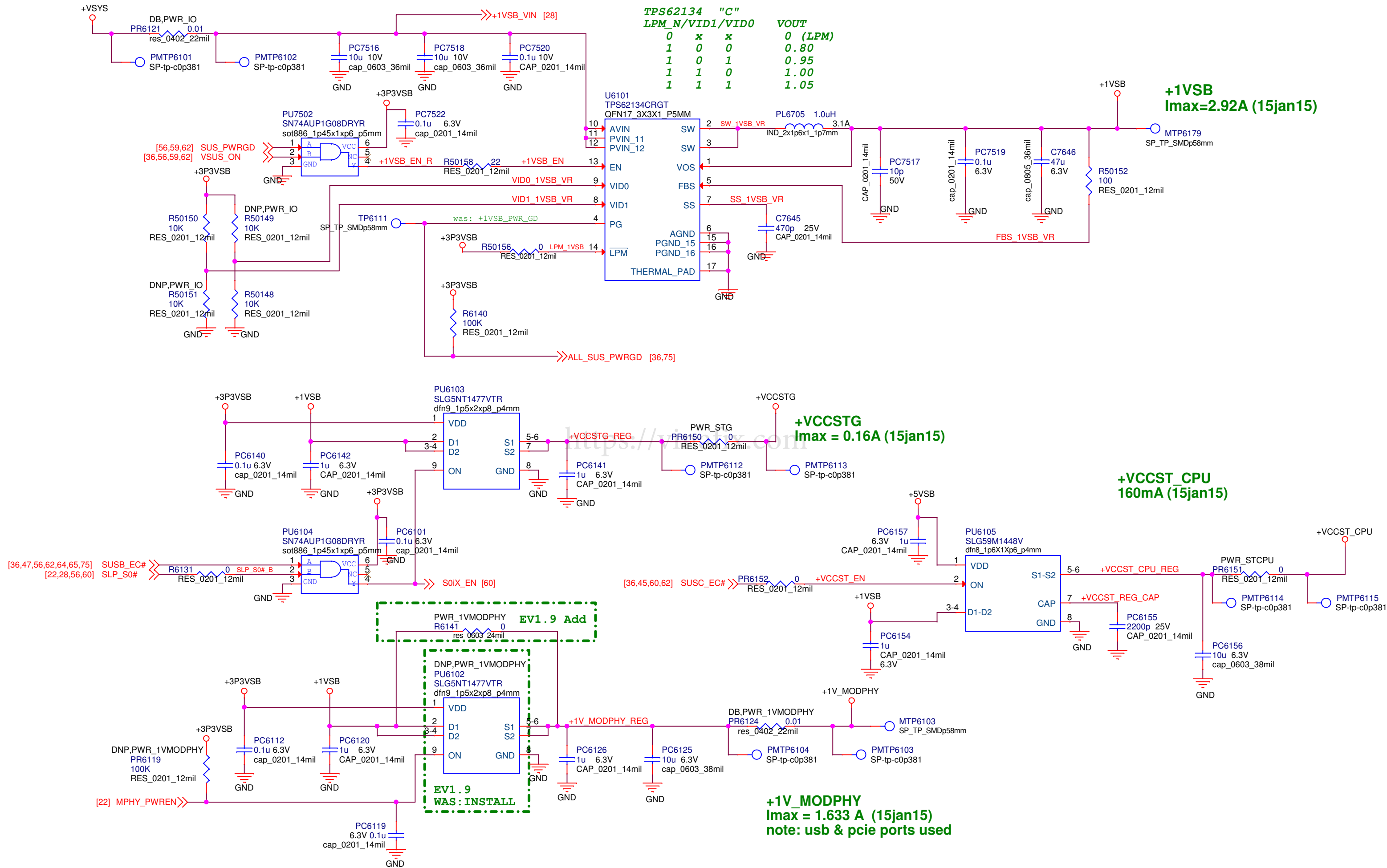


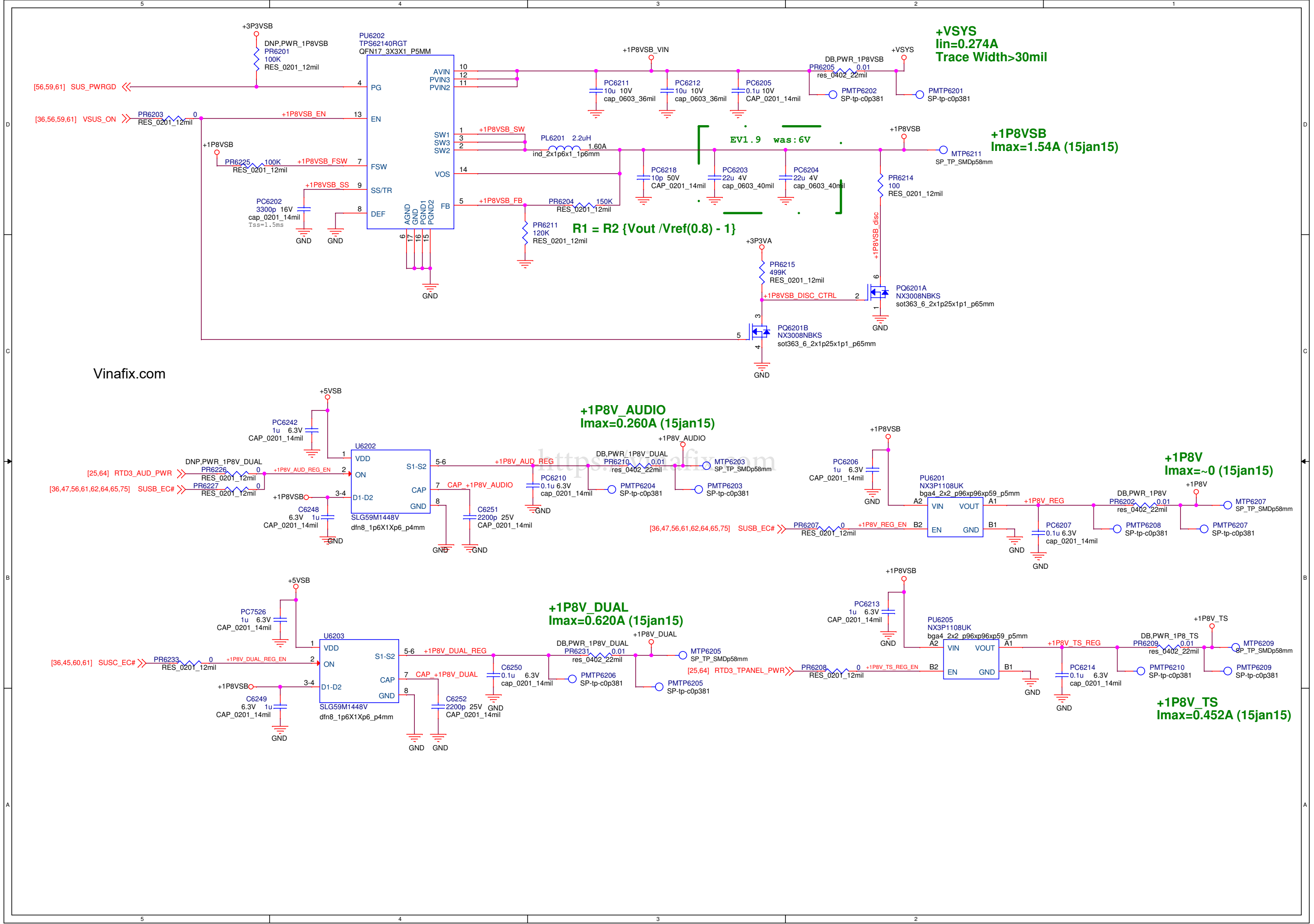
Parts only installed for 23e SKU











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+1P8V AUDIO
Imax=0.260A (15jan15)

+1P8V DUAL
Imax=0.620A (15jan15)

+1P8V
Imax=~0 (15jan15)

+1P8V TS
Imax=0.452A (15jan15)

+VSYS
Iin=0.274A
Trace Width>30mil

+1P8VSB
Imax=1.54A (15jan15)

$$R1 = R2 \{V_{out} / V_{ref}(0.8) - 1\}$$

EV1.9 was: 6V

CHGR_VIN
lin=9.731A
Trace Width>389mil

+SYS
lin=8A
Trace Width>320mil

+SYS
Imax = 12.0A
TDC = 10.0A

CHGR needs 200uF for loop stability
{2*f*pi = 1/sqrt(L*C)}

EffCap@20V=3.22uF*3=9.66uF

$I(\text{ripple}) = V_{in} \cdot \text{DutyCycle} \cdot (1 - \text{DutyCycle}) / (\text{FreqSwitch} \cdot L)$
 $I(\text{ripple}) = 20\% - 40\% I(\text{charge})$
 $V_{in}(12.6V \pm 10\%) \Rightarrow I(\text{ripple})@2.2uH \Rightarrow 1.93A, 40.5\%$
 $V_{in}(12.6V \pm 10\%) \Rightarrow I(\text{ripple})@3.3uH \Rightarrow 1.29A, 27.0\%$
assuming 60W, DutyCycle=0.5, Freq=1020KHz

EV1.9
CHGR MSPN
EV1.9
CHGR MSPN

7-bit I2C Address = 0x12

$C_{gs} \geq 40 \cdot C_{gd}$
 $C_{gs} \cdot 0.9 \geq 40 \cdot C_{gd} \cdot 1.1$
 $C_{gs} \geq (1.1/0.9) \cdot 40 \cdot 1nF$
 $C_{gs} \geq 49nF$

[33,35,36,70] SML1_EC_CLK

[33,35,36,70] SML1_EC_DATA

[36] EC_CHG_ACOK

[36] EC_ADP_IOUT

[66] PMON

[10,66] H_PROCHOT#

[36] EC_BAT_IOUT

[63] CHG_REGN_D

PC6327 100p 25V
CAP_0201_14mil

PC6319 100p 25V
CAP_0201_14mil

C6336 100p 25V
CAP_0201_14mil

RES_0201_12mil
PR6312 499K

DNP,PWR_CHGR
PR6313 150K
RES_0201_12mil

7-bit I2C Address = 0x12

EV1.9
CHGR MSPN
EV1.9
CHGR MSPN

$C_{gs} \geq 40 \cdot C_{gd}$
 $C_{gs} \cdot 0.9 \geq 40 \cdot C_{gd} \cdot 1.1$
 $C_{gs} \geq (1.1/0.9) \cdot 40 \cdot 1nF$
 $C_{gs} \geq 49nF$

[33,35,36,70] SML1_EC_CLK

[33,35,36,70] SML1_EC_DATA

[36] EC_CHG_ACOK

[36] EC_ADP_IOUT

[66] PMON

[10,66] H_PROCHOT#

[36] EC_BAT_IOUT

[63] CHG_REGN_D

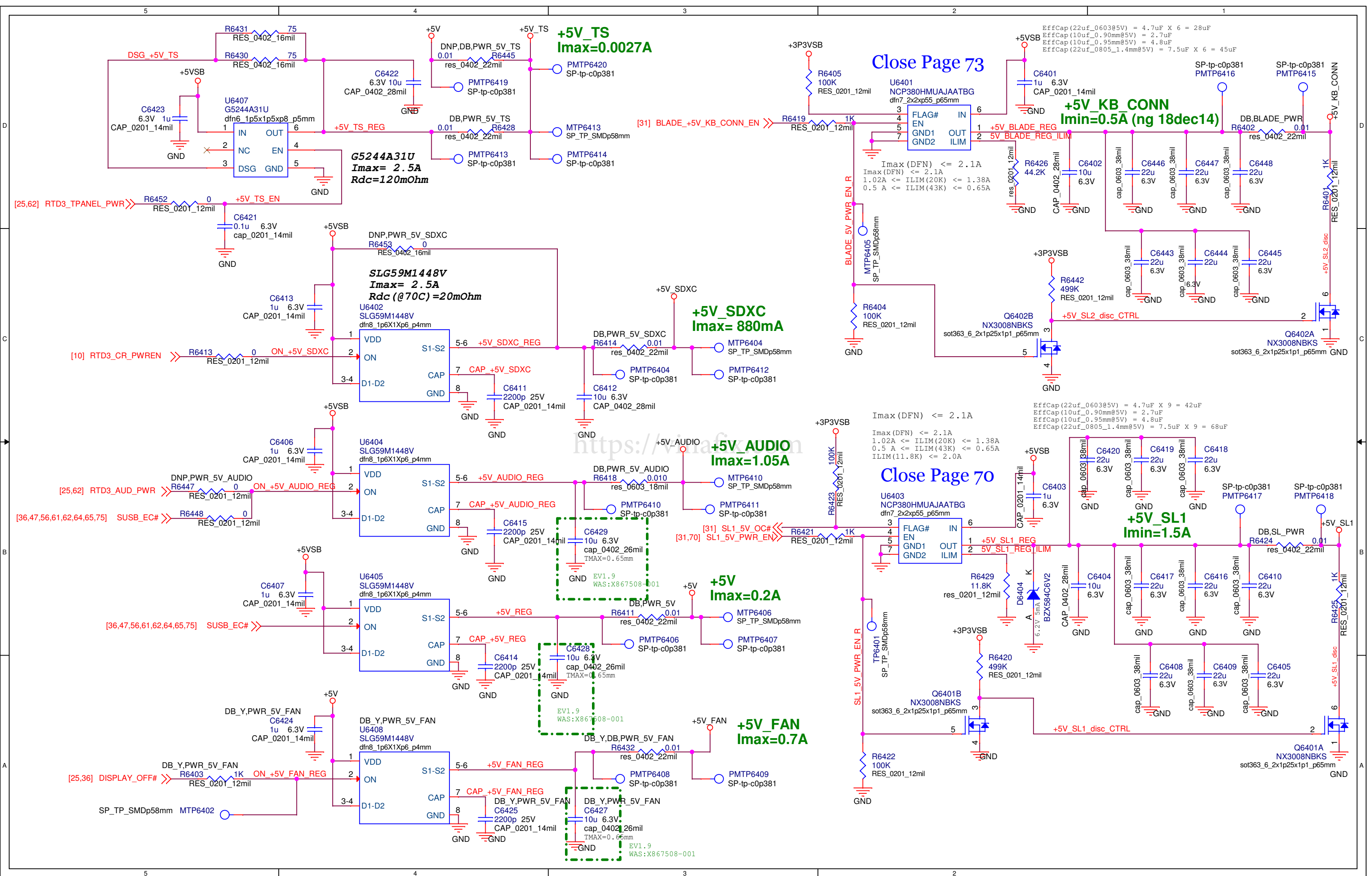
PC6327 100p 25V
CAP_0201_14mil

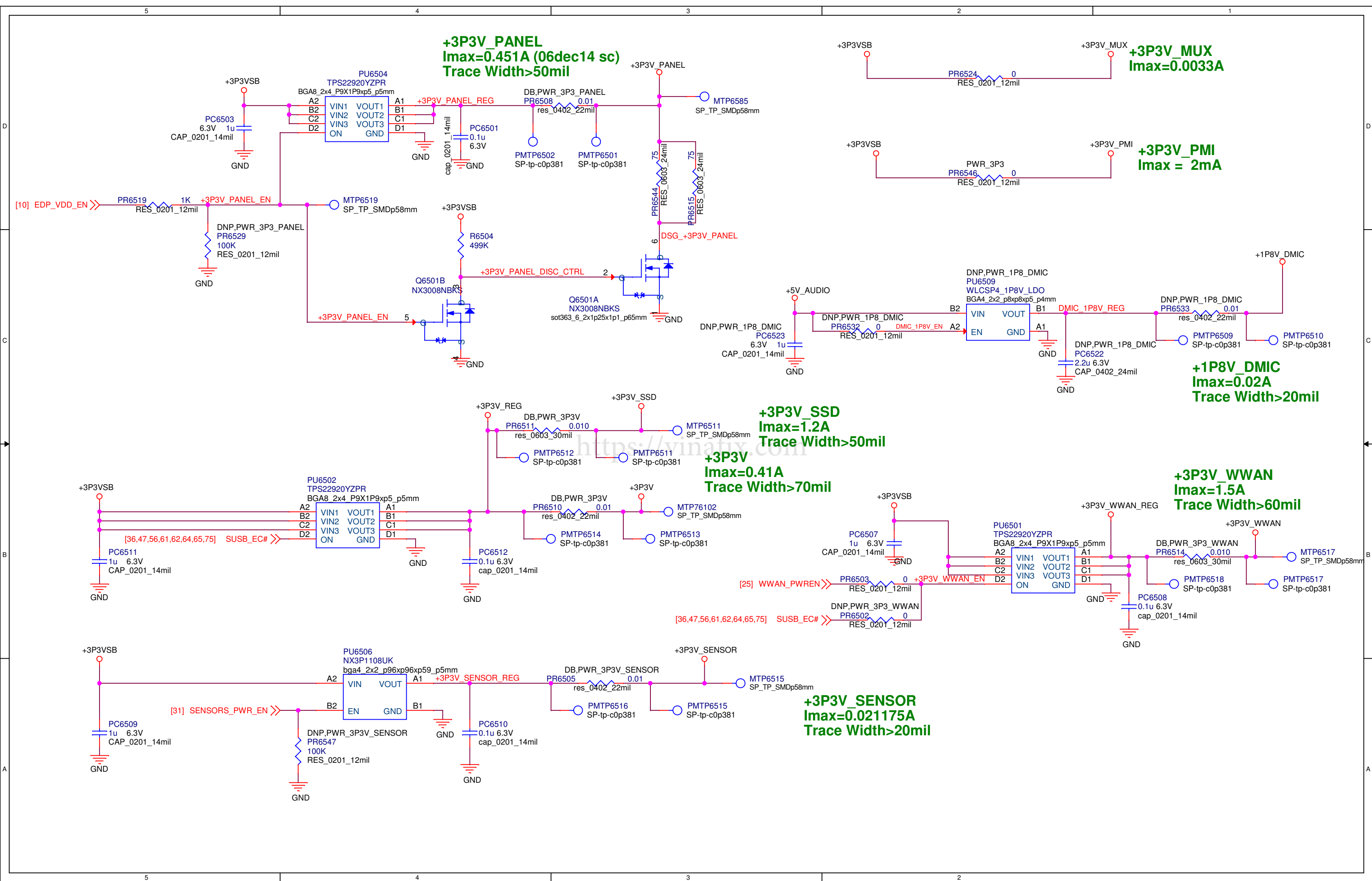
PC6319 100p 25V
CAP_0201_14mil

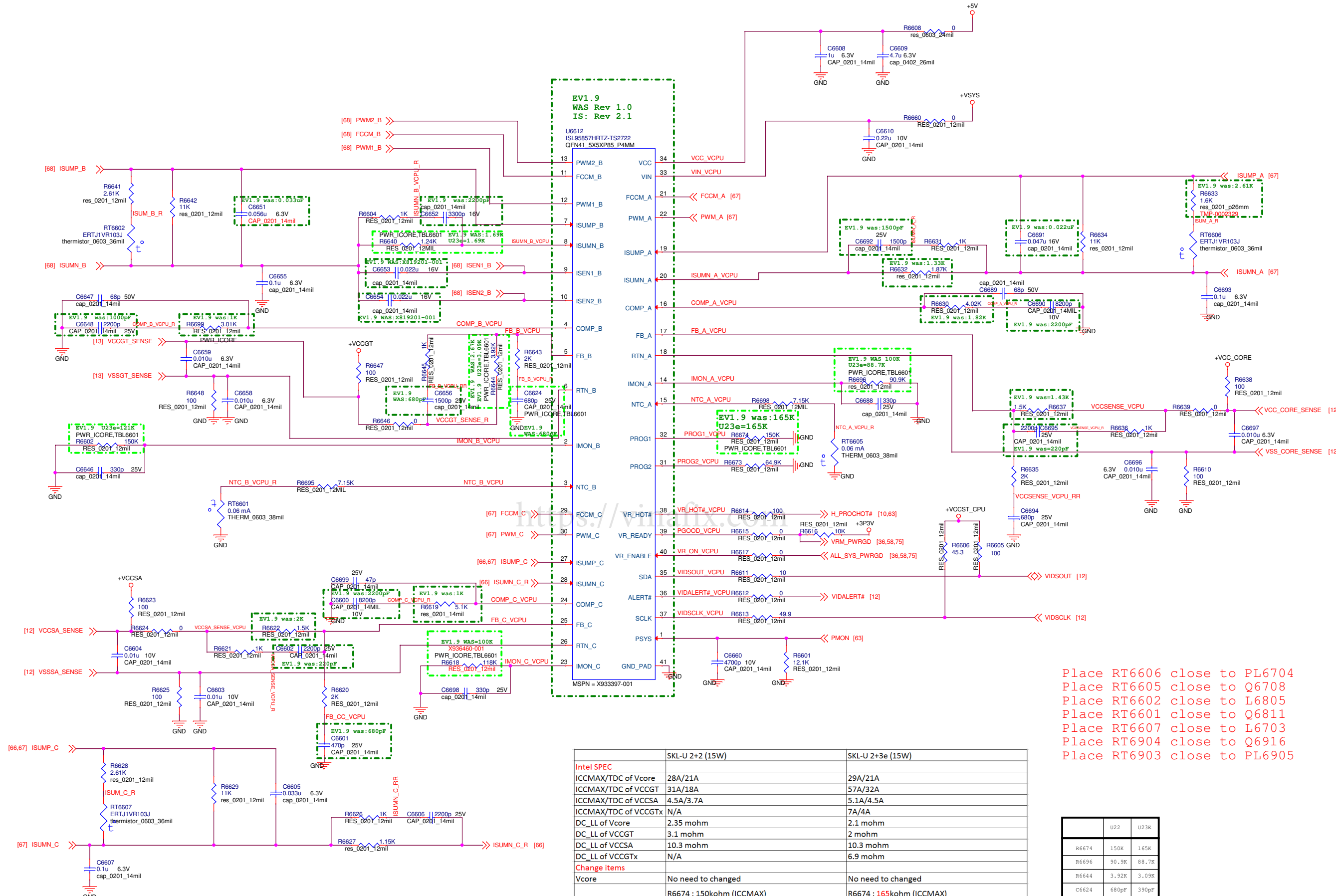
C6336 100p 25V
CAP_0201_14mil

RES_0201_12mil
PR6312 499K

DNP,PWR_CHGR
PR6313 150K
RES_0201_12mil



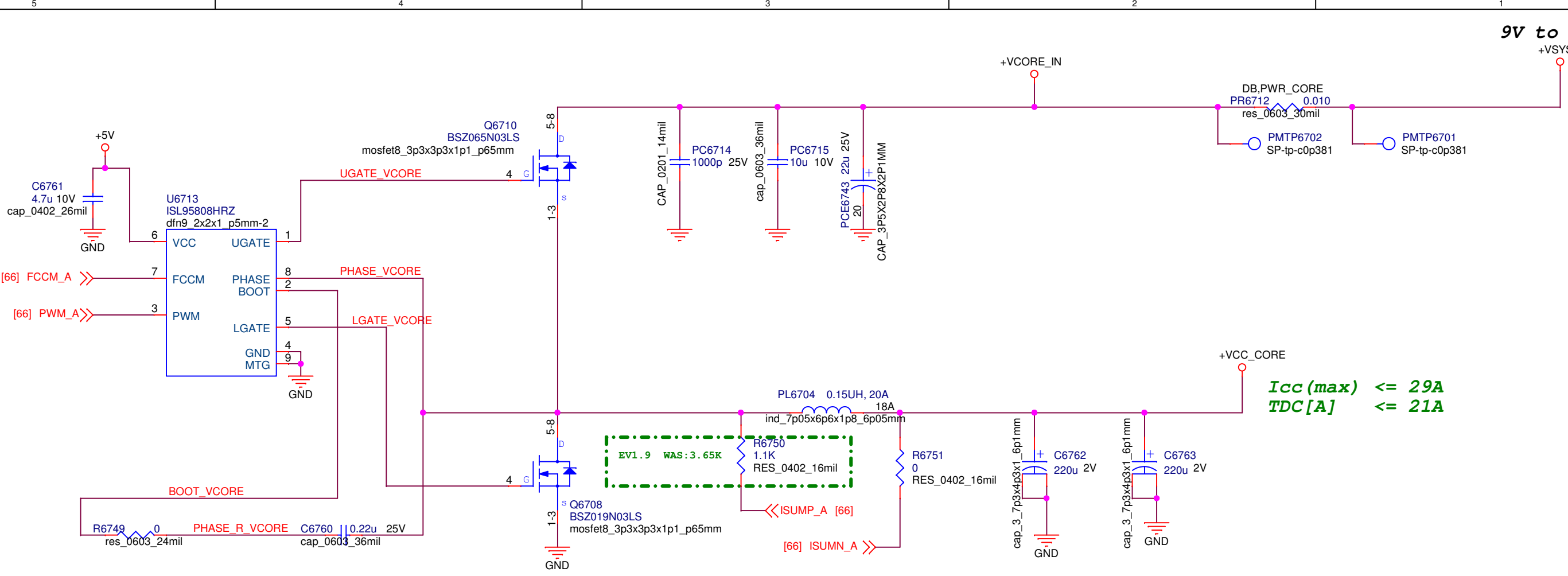




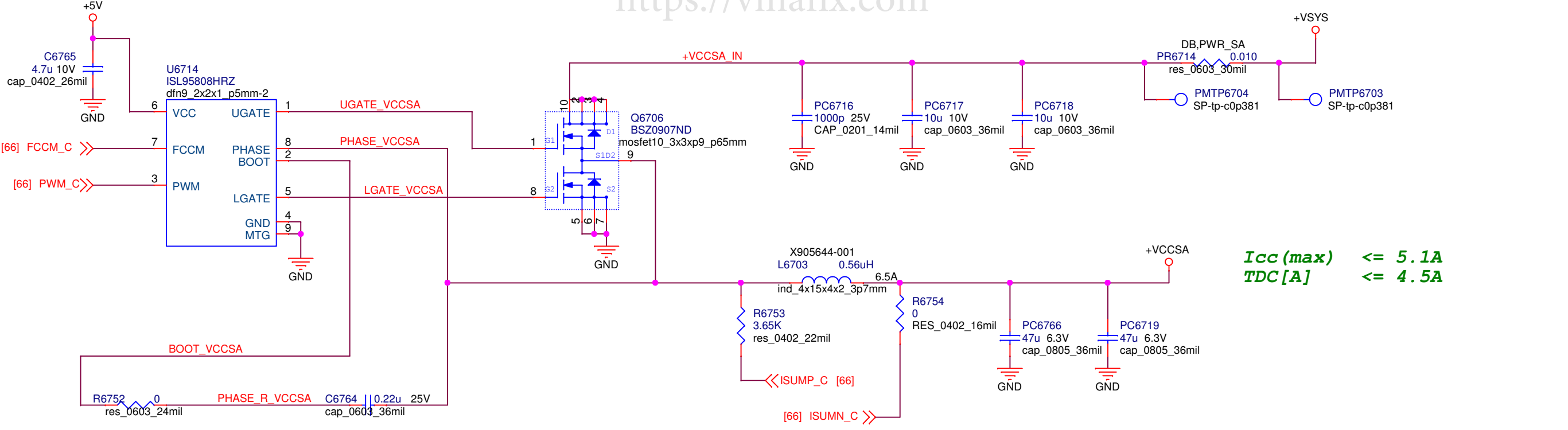
Place RT6606 close to PL6704
Place RT6605 close to Q6708
Place RT6602 close to L6805
Place RT6607 close to L6703
Place RT6904 close to Q6916
Place RT6903 close to PL6905

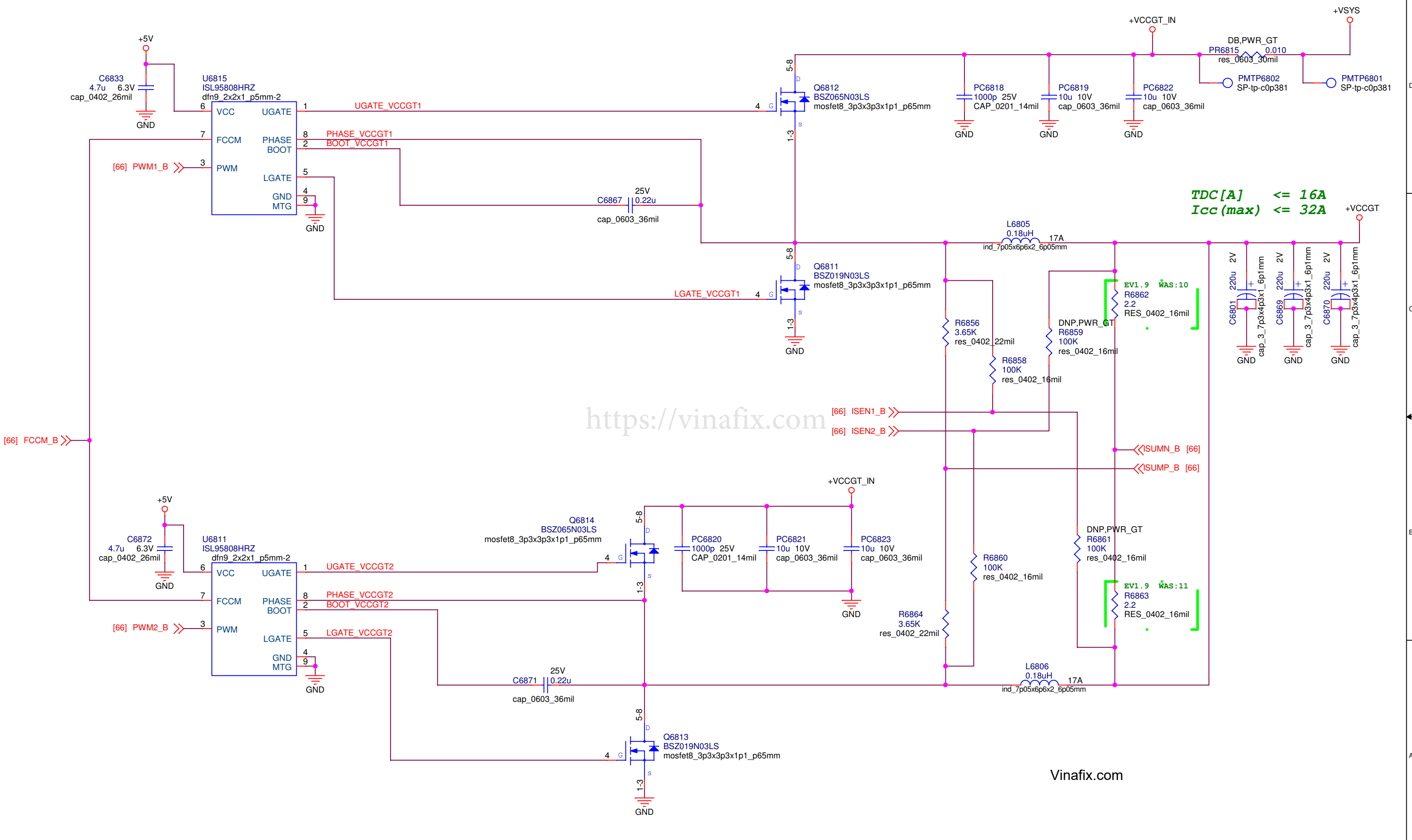
	SKL-U 2+2 (15W)	SKL-U 2+3e (15W)
Intel SPEC		
ICCMAX/TDC of Vcore	28A/21A	29A/21A
ICCMAX/TDC of VCCGT	31A/18A	57A/32A
ICCMAX/TDC of VCCSA	4.5A/3.7A	5.1A/4.5A
ICCMAX/TDC of VCCGTx	N/A	7A/4A
DC_LL of Vcore	2.35 mohm	2.1 mohm
DC_LL of VCCGT	3.1 mohm	2 mohm
DC_LL of VCCSA	10.3 mohm	10.3 mohm
DC_LL of VCCGTx	N/A	6.9 mohm
Change items		
Vcore	No need to changed	No need to changed
VCCGT	R6674 : 150kohm (ICCMAX) R6640 : 1.24kohm (60A OCP) R6644 : 3.09kohm (LL 3.1mohm)	R6674 : 165kohm (ICCMAX) R6640 : 1.69kohm (80A OCP) R6644 : 2.68kohm(LL 2mohm)
VCCSA	No need to changed	No need to changed
VCCGTx	Disable U6916	Enable U6916

	U22	U23E
R6674	150K	165K
R6696	90.9K	88.7K
R6644	3.92K	3.09K
C6624	680pF	390pF
R6640	1.24K	1.69K
R6602	150K	121K
R6618	118K	100K

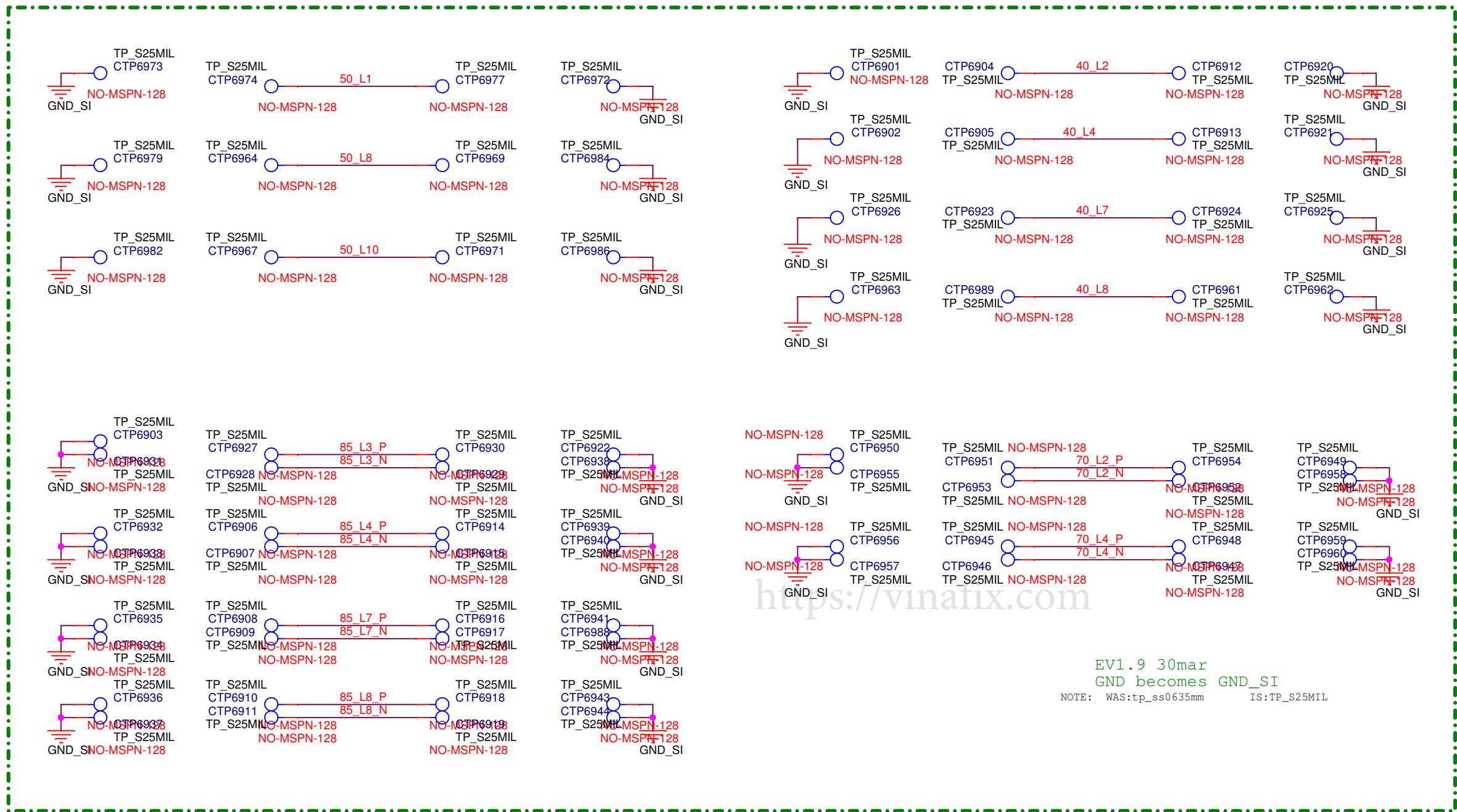


<https://vinafix.com>



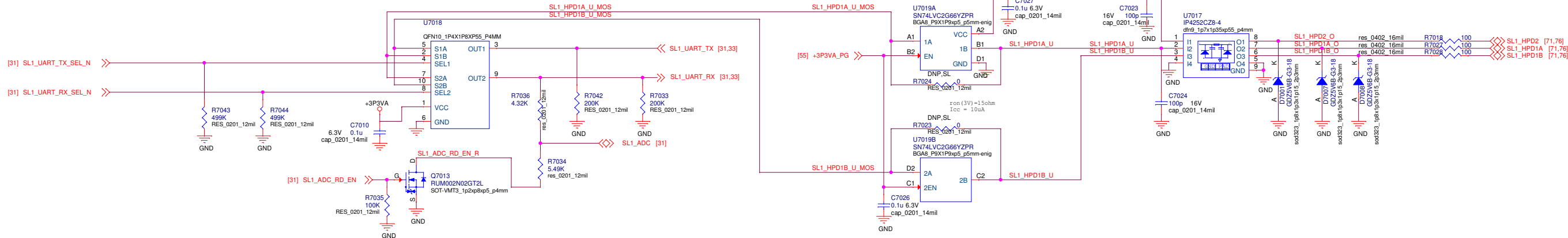


TDC [A] <= 16A
Icc (max) <= 32A

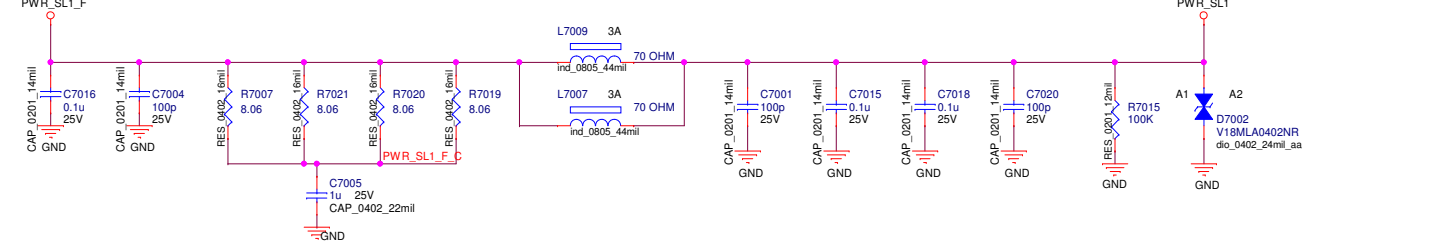
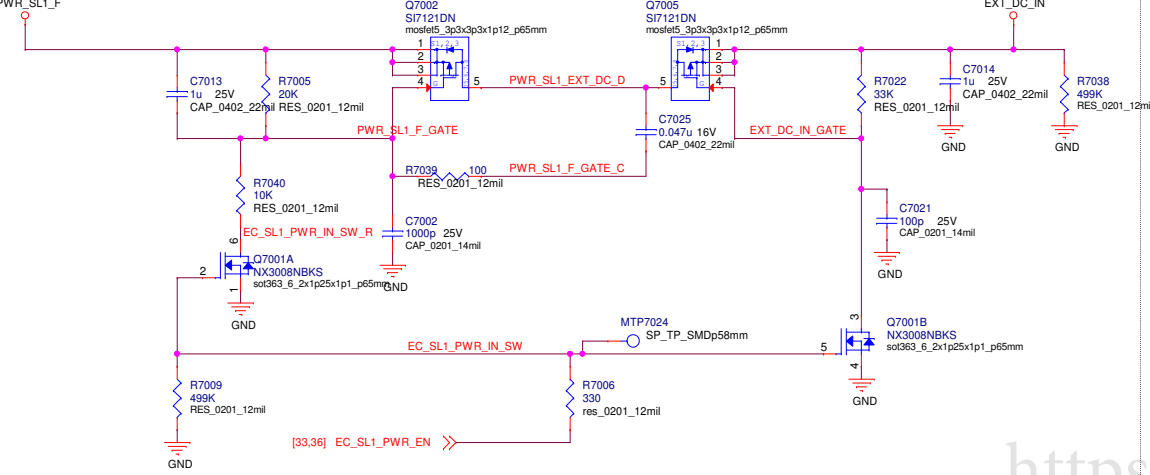


EV1.9 30mar
GND becomes GND_SI
NOTE: WAS:tp_ss0635mm IS:TP_S25MIL

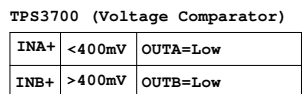
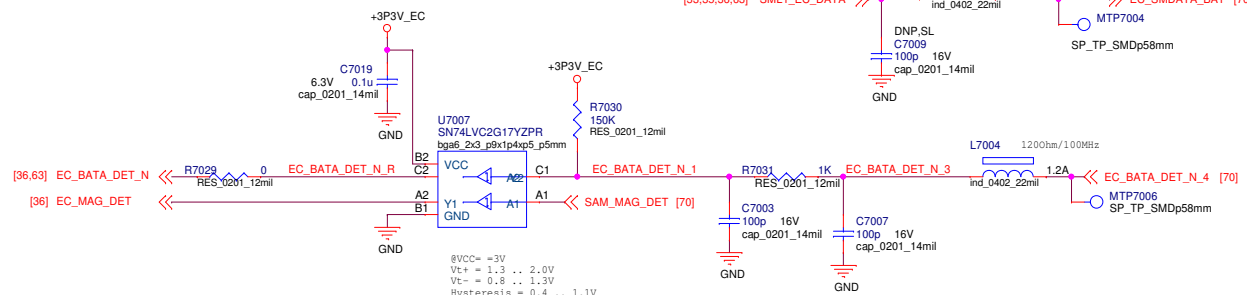
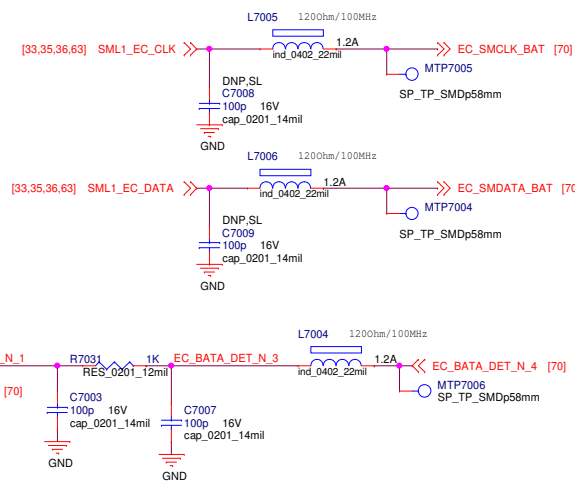
HPD FOR SL1 (ONE/TWO WIRE UART)



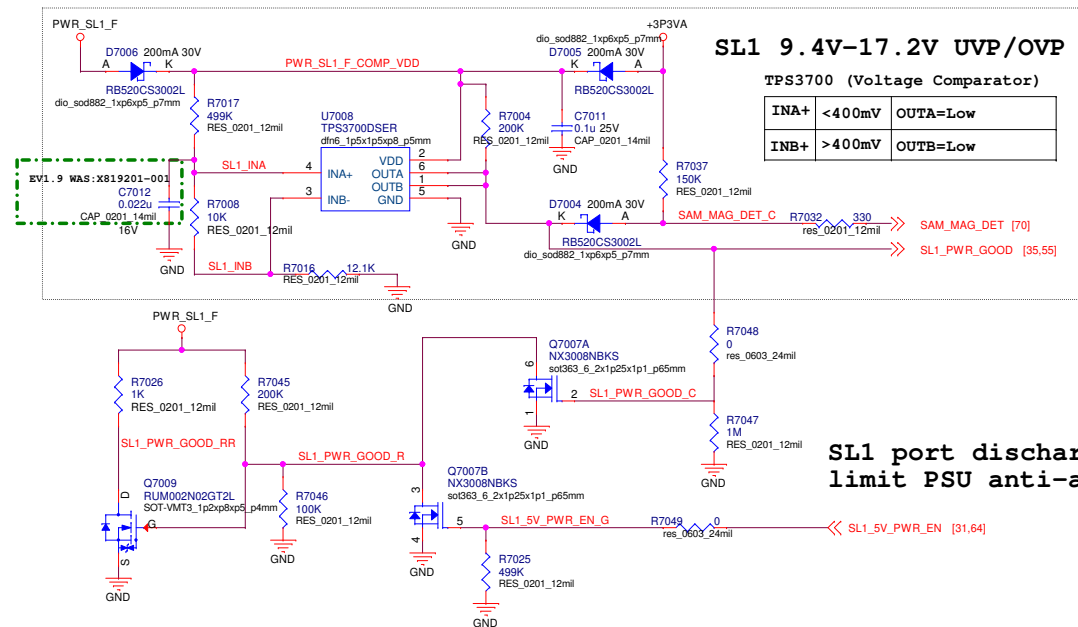
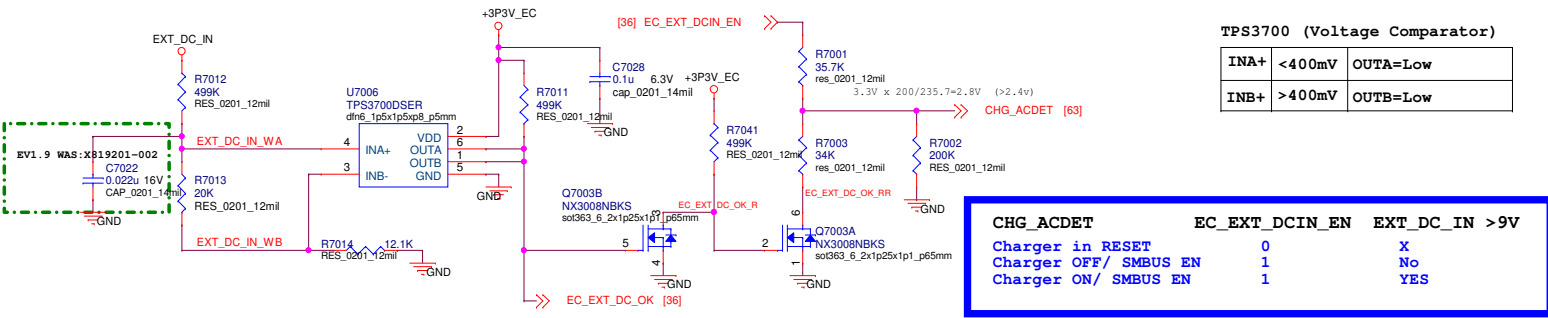
[In] SL1 6-12V PWR to EXT DC IN



Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed



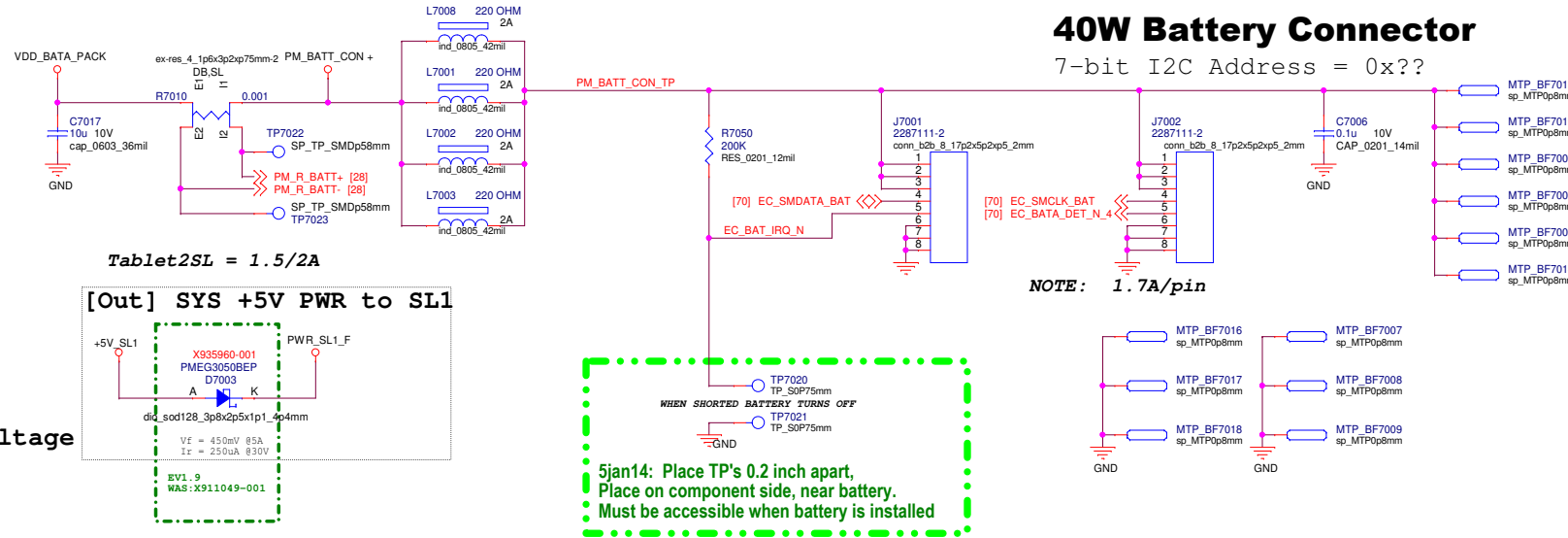
CHG_ACDDET	EC_EXT_DCIN_EN	EXT_DC_IN >9V
Charger in RESET	0	X
Charger OFF/ SMBUS EN	1	No
Charger ON/ SMBUS EN	1	YES



SL1 9.4V-17.2V UVP/OVP

TPS3700 (Voltage Comparator)		
INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

```
SL1 port discharger
limit PSU anti-arc pulse voltage
```

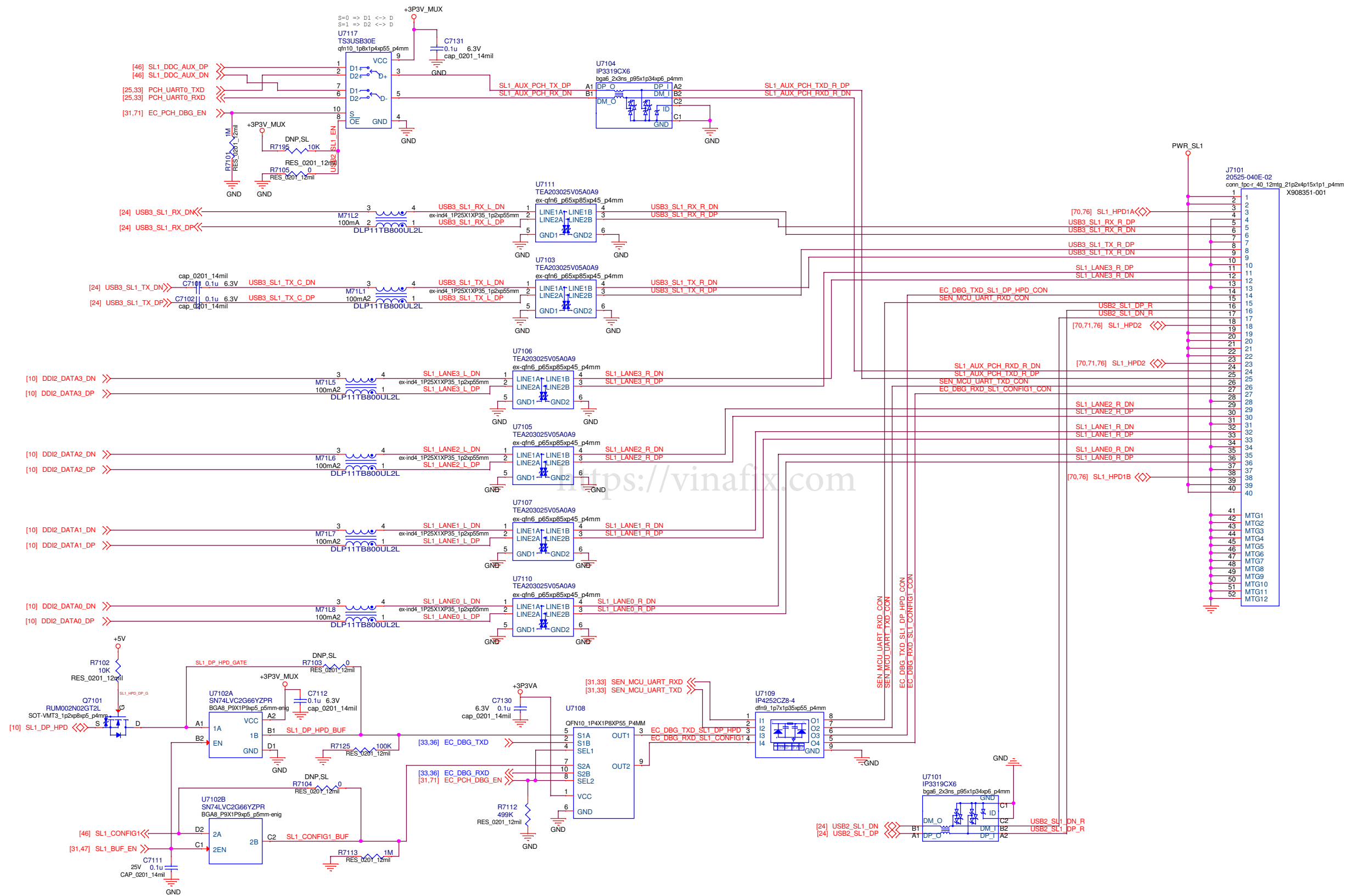


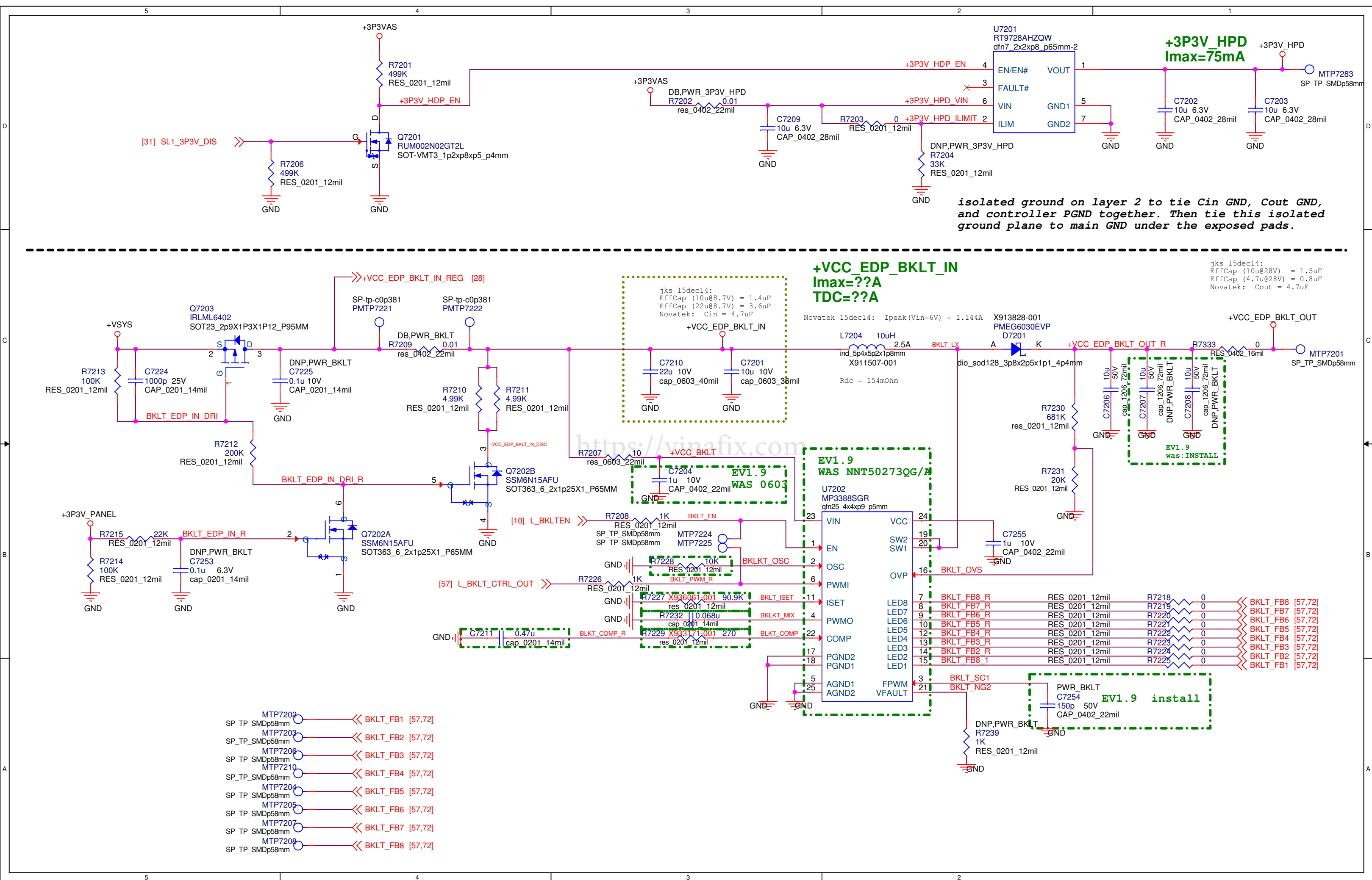
40W Battery Connector

7-bit I2C Address = 0x??

NOTE: 1.7A/pin

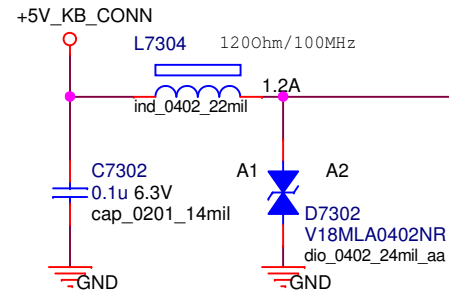
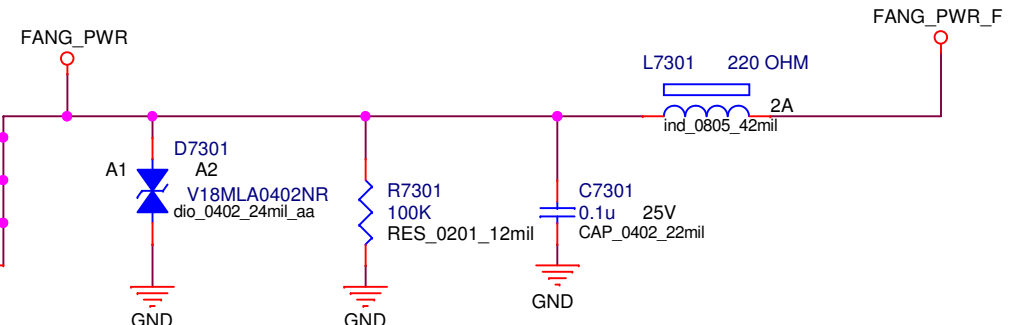
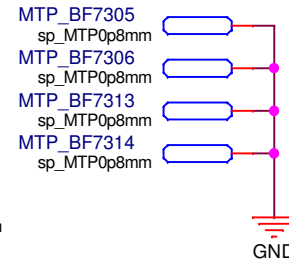
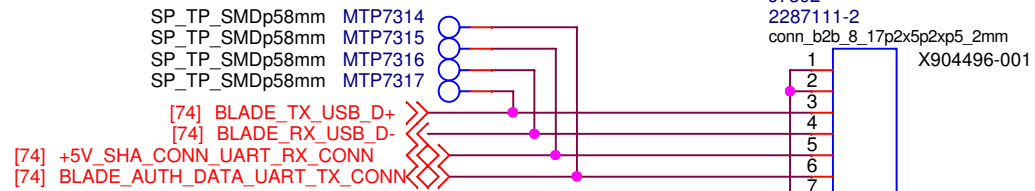
- 5jan14: Place TP's 0.2 inch apart,
Place on component side, near battery.
- Must be accessible when battery is installed



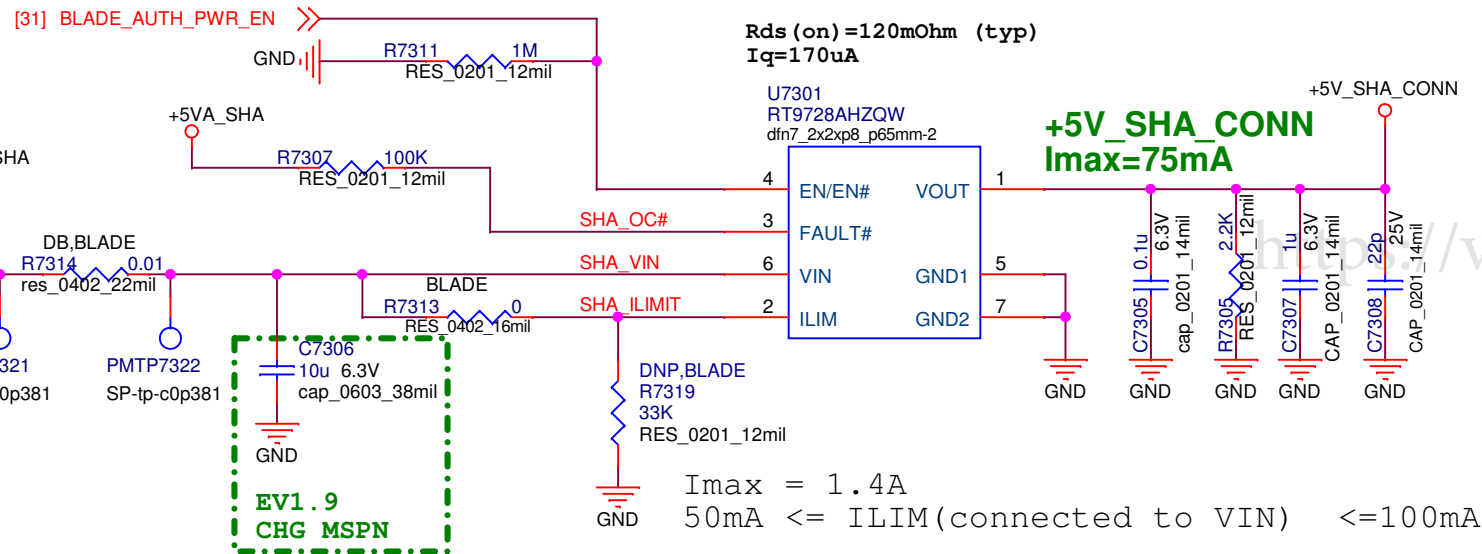


+5V_KB_CONN
Imax = 0.5A

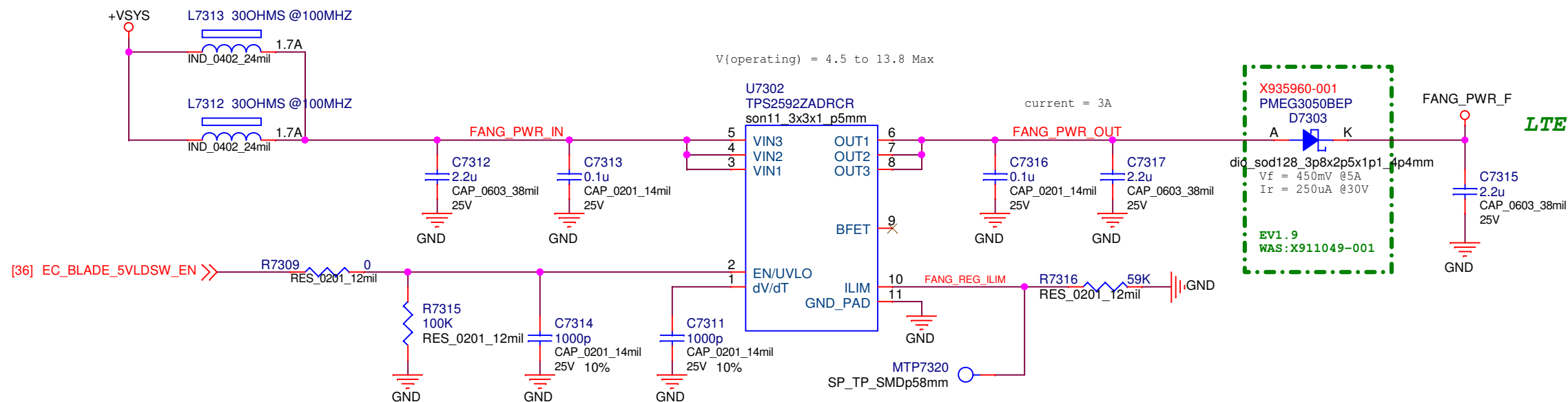
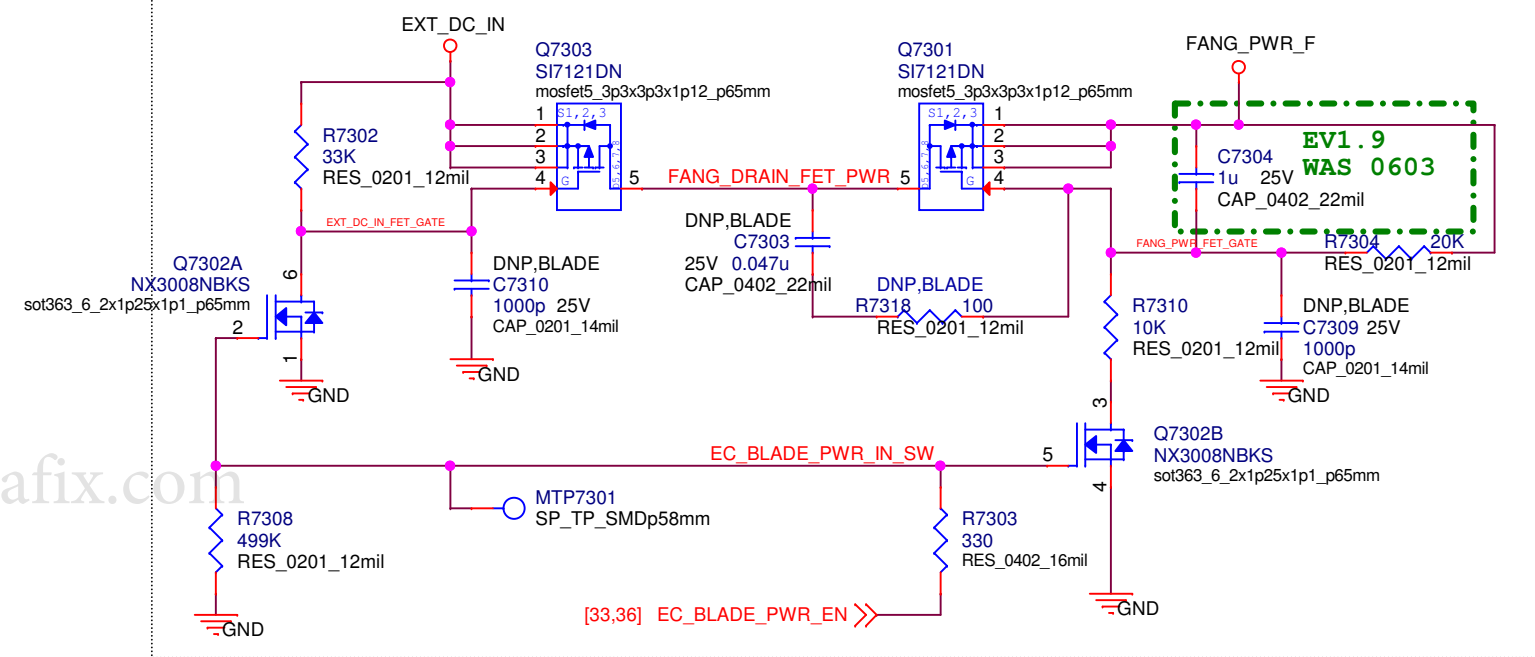
BLADE Connector



eFang power = 3.5A max
using +1 rule



[In] BLADE 6-12V PWR to EXT DC IN Imax=4.5A



LTE eFANG PWR = 2.10A(min)
2.47A(nom)
2.84A(max)

