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CAD Note:
Default component footprint is SMD 0201, X5R, 1% resistors.

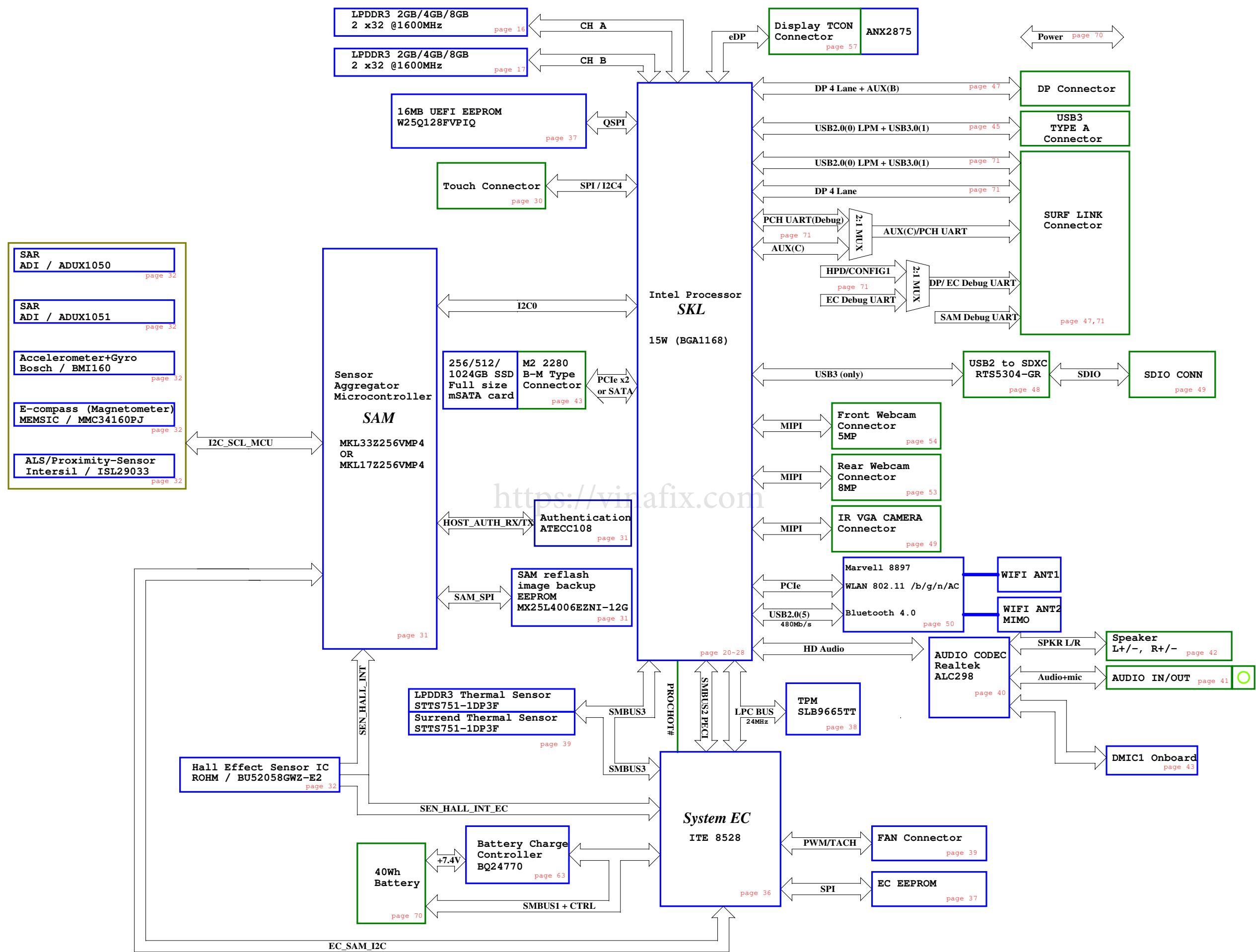
Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

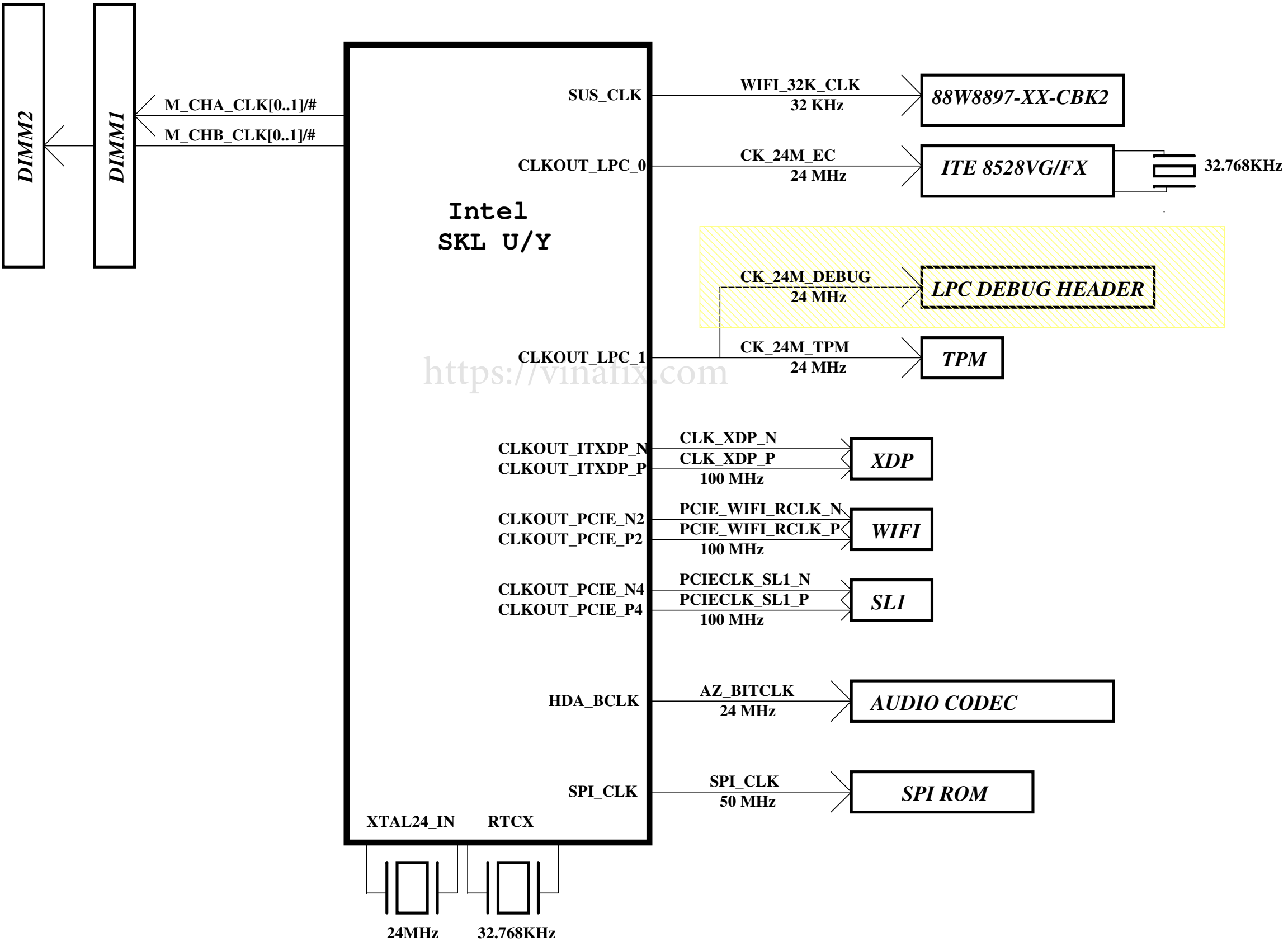
Schematics Change History

Rev.	Date	Comments
Op9	28 Oct 2014	1. Starting with G_EV1_1021-1630.DSN 2. Added SL schematic from page 72 ...\\T\\MB\\DV_RELEASED\\Schematic\\CASTLE2_DV_2014_1021_1100.DSN 3. Added External USB3 schematic from ...\\T\\MB\\DV_RELEASED\\Schematic\\CASTLE2_DV_2014_1021_1100.DSN 4. Added external DP ...\\T\\MB\\DV_RELEASED\\Schematic\\CASTLE2_DV_2014_1021_1100.DSN 5. Added IR_CAMERA from Front Camera...put in page 49 6. Removed page 73 PCIe GPU 7. Added Blade from T 8. Removed P72 T2B Pwr Transistors
Op10	3 Nov 2014	1. Changing to NVDC 2. Replaced GTX with GT, kept bypass caps 3. Replaced Charger with BQ24770
Op11	3 Nov 2014	1. Replace SKL-U with SKL-Y
Op12	11 Nov 2014	1. Model DDR connection from Intel SDS
Op13	18 Nov 2014	1. Added FUB information to all components 2. Changed Decretes.. sizing caps
Op14	20 Nov 2014	1. Added +5VA_SHA 2. Added T Cost Down/XCN's 3. Added SL +5V load Switch & Caps 4. Added Blade +5V load Switch & Caps
Op15	26 Nov 2014	1. Removed Boost 2. Re-adjusted usb ports on CPU 3. Removed Audio DSP
Op16	03 Dec 2014	1. changed +1VSB regulator 2. changed IR Camera/added diode 3. added power numbers from 0.91 PDG, Oct14 4. changed BLADE connector 5. cpu decoupling caps changed 6. changed +5V/+3V inductors (place holder)
Op17	05 Dec 2014	1. swapped M_A_CAA with MA_CAB on U1601/U1602 2. added two SAR chips, P32 3. remove tp's from csi lines on (p23) 4. change from 10 ceramic to 3 tantalum-poly on usb3 typeA (p45) 5. remove the RSENSE from output of +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) 6. change RSENSE input to 0402 from 0603 for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) input regulator 7. change inductor for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58) to HMLE20161B-1R0MDR-01 8. change RSENSE input to 0402 from 0603 for +5V_TS,+5V_SDXC,+5V_AUDIO,+5V, +5V_FAN(p64) 9. change RSENSE input to 0402 from 0603 for +3P3V_PANEL,+3P3V,+3P3V_SENSOR,+1P8V_DMIC (p65) 10. Replacing the SL connector with X908351-001 11. Replace PL5901 and PL5902 with CMLE042T-2R2MS-01 12. Replace 0402 1uF 6.3V with 0201 1uF 6.3V X5R 13. Replace L7201 with TOKO #A919CY-100M 14. Added VSYS -> BLADE FANG supply (p73)
Op18	09 Dec 2014	1. Reduced sizes of parts for Cameras (Resistors/Caps/Regulators)
Op19	12 Dec 2014	1. All 47uF caps become 0805/1mmZ 2. All 10uF caps become 0402...4V/6.3V
Op20	15 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x4 2. Shui Changes 3. more Shui Changes
Op21	16 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x5 2. changes from EV_schematic_issue_check_1216_JDM1.xlsx 3. changed name of +6_12 to +V_ALWAYS_ON 4. Removed 2 Mikes & Front Mike & added FPC conn 5. Added 2nd BLADE connector
Op22	17 Dec 2014	1. Replaced SD connector with AY531465T 2. changes from EV_schematic_issue_check_viola_1217_JDM1.xlsx
Op23 current		1. See apexUfixes_revXpXX.xlsx

CAD Note:
Default component footprint is SMD 0201, X5R, 1% resistors S = Short after design fixed
Property: BUILD-OPT
DNP = Not Installed Part.

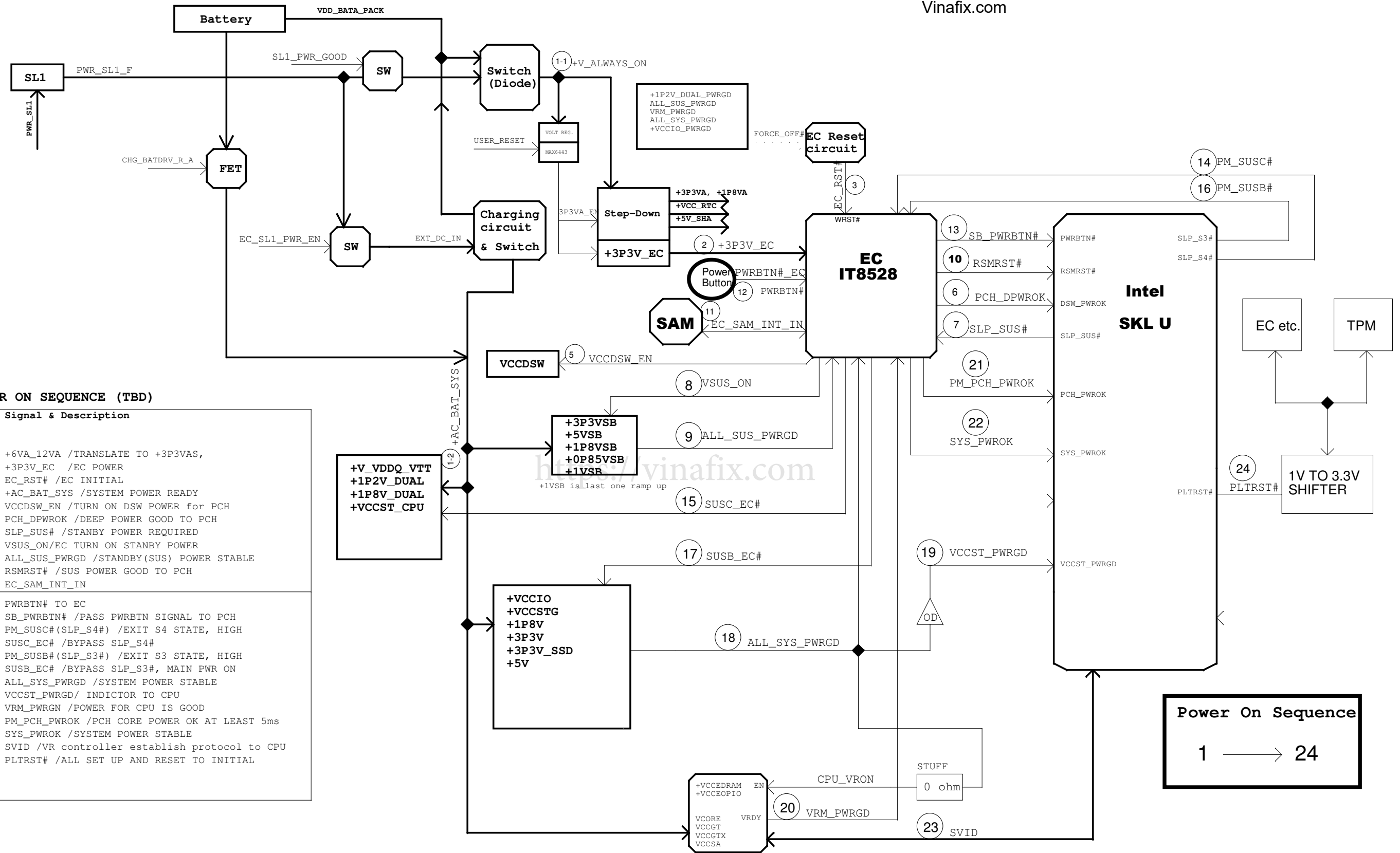


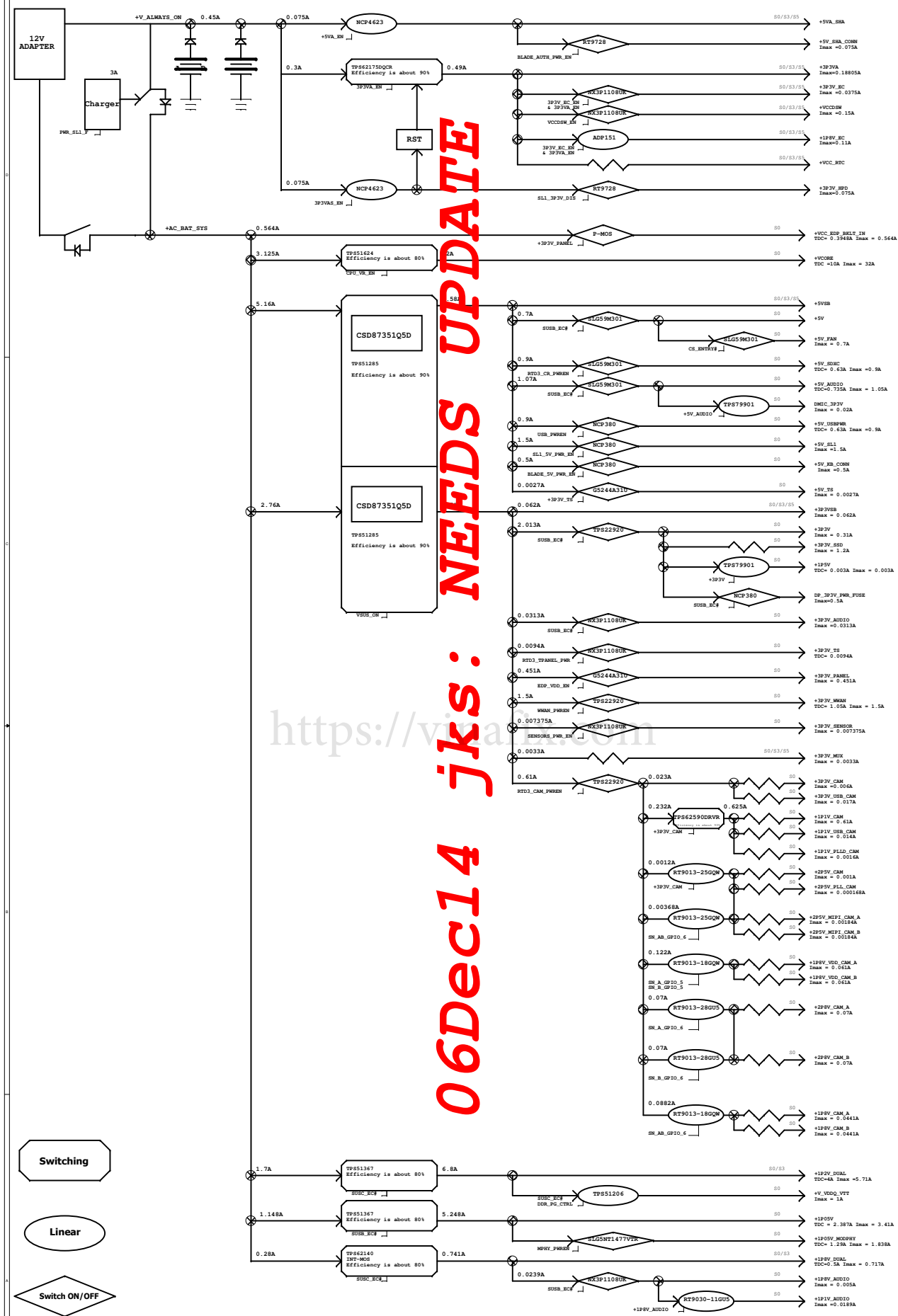
HSW Buffer Through Mode for Pre-Silicon



POWER ON SEQUENCE (TBD)

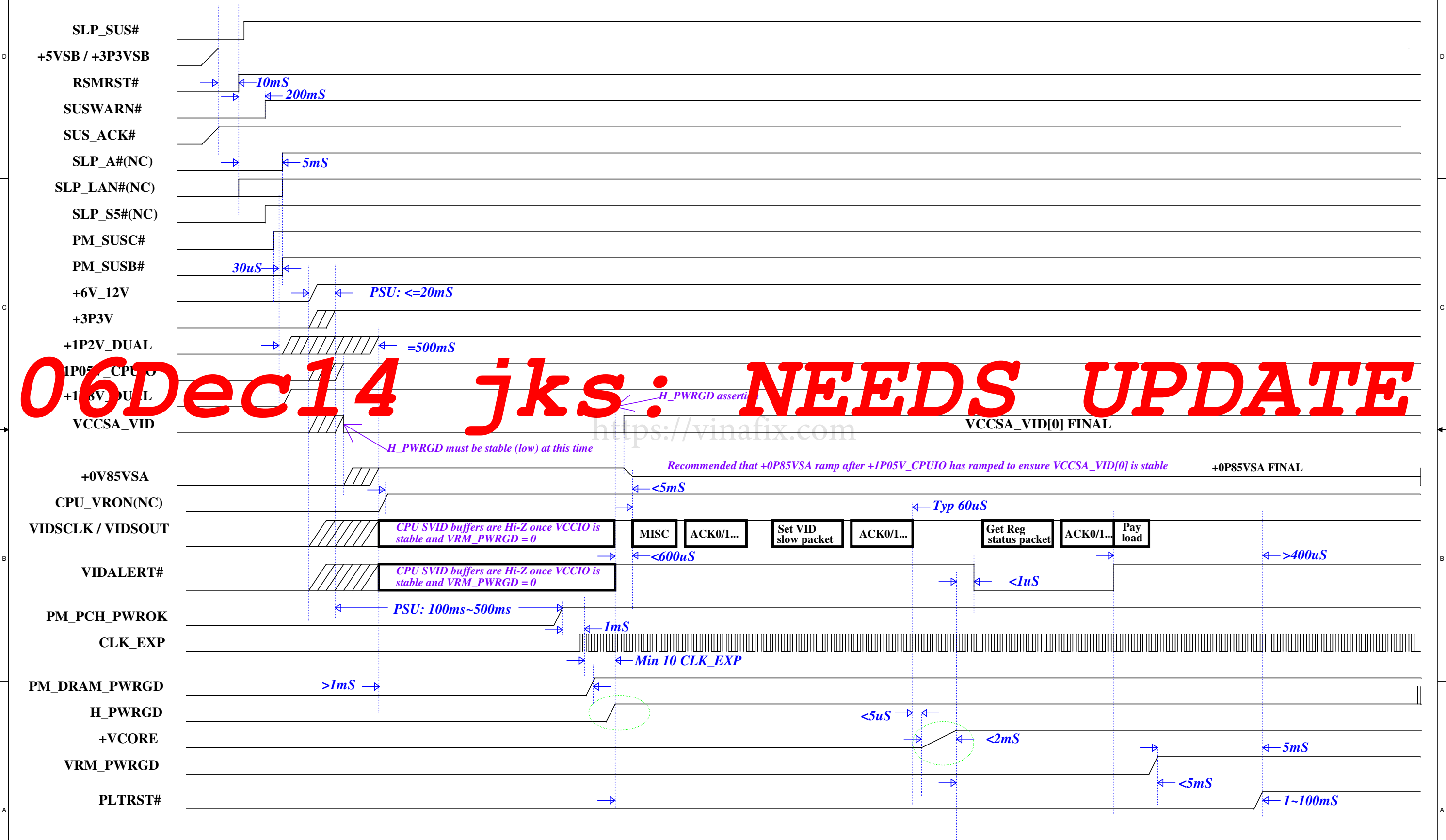
STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4	+AC_BAT_SYS /SYSTEM POWER READY
5	VCCDSW_EN /TURN ON DSW POWER for PCH
6	PCH_DPWROK /DEEP POWER GOOD TO PCH
7	SLP_SUS# /STANBY POWER REQUIRED
8	VSUS_ON/EC TURN ON STANBY POWER
9	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10	RSMRST# /SUS POWER GOOD TO PCH
11	EC_SAM_INT_IN
12	PWRBTN# TO EC
13	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15	SUSC_EC# /BYPASS SLP_S4#
16	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19	VCCST_PWRGD/ INDICATOR TO CPU
20	VRM_PWRGN /POWER FOR CPU IS GOOD
21	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
22	SYS_PWROK /SYSTEM POWER STABLE
23	SVID /VR controller establish protocol to CPU
24	PLTRST# /ALL SET UP AND RESET TO INITIAL





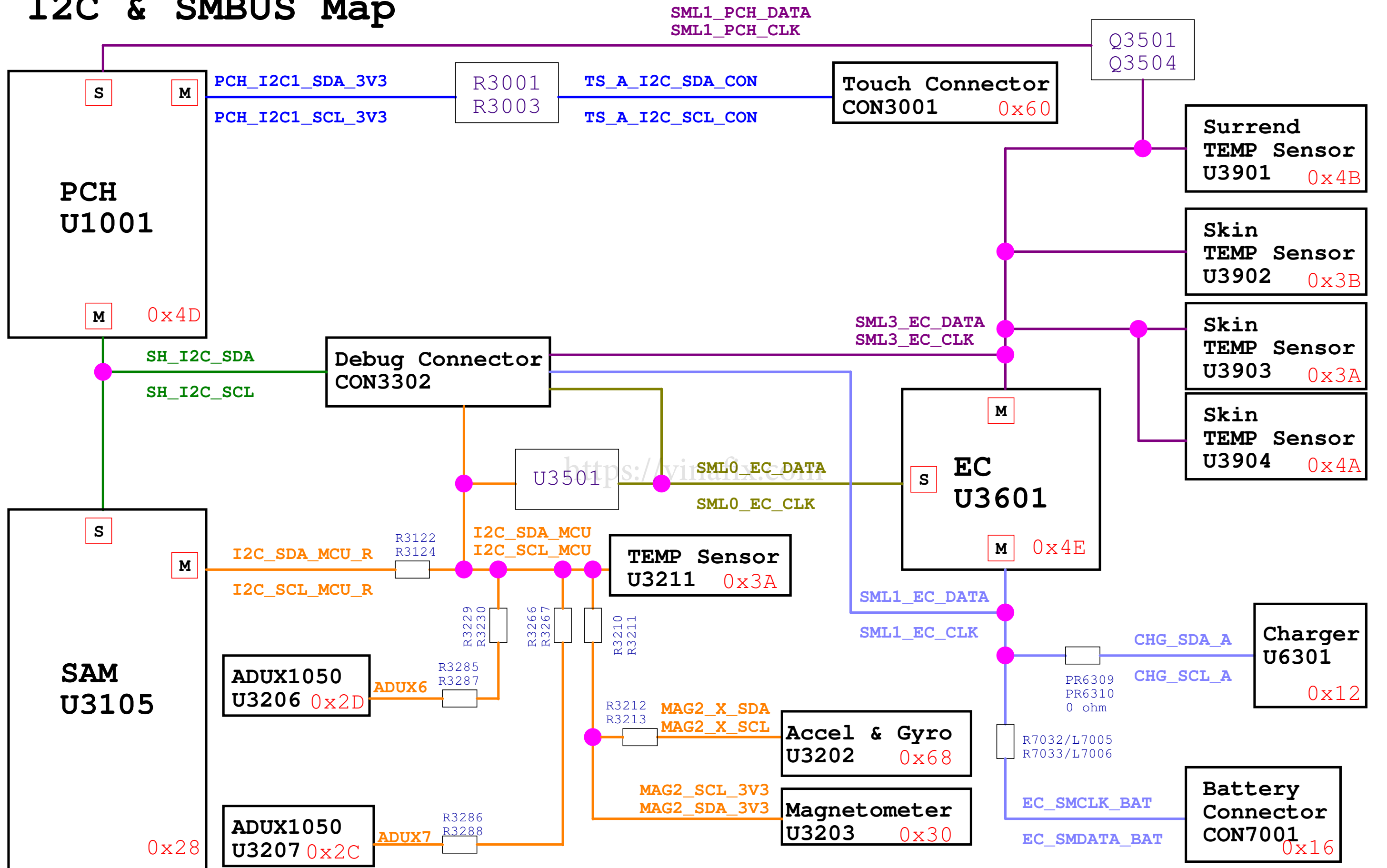
[illegible]

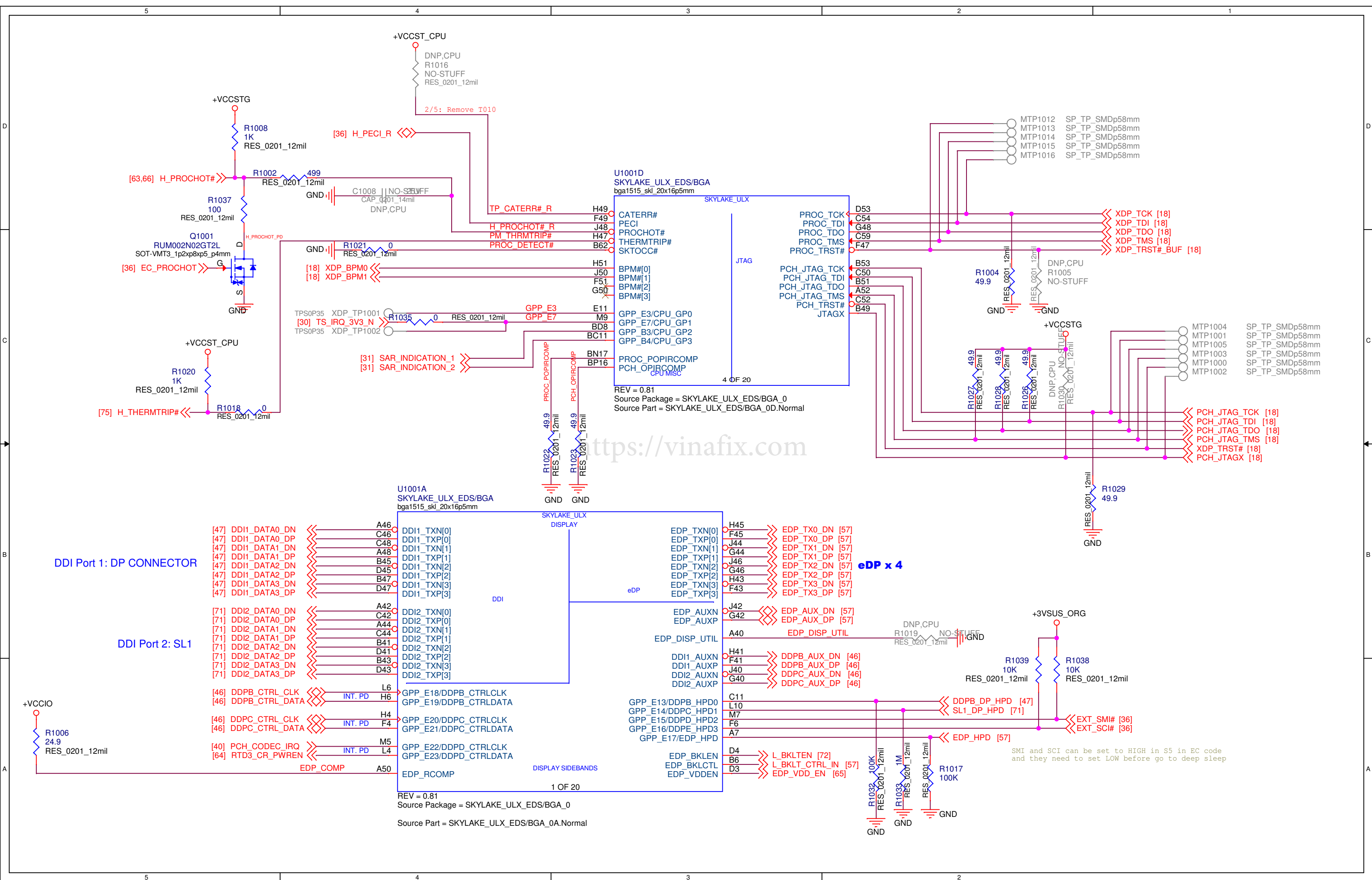
S5 to S0 Power Sequence

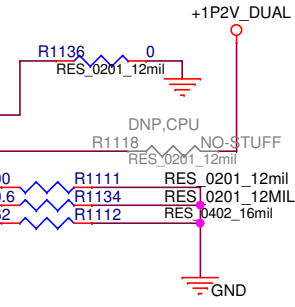
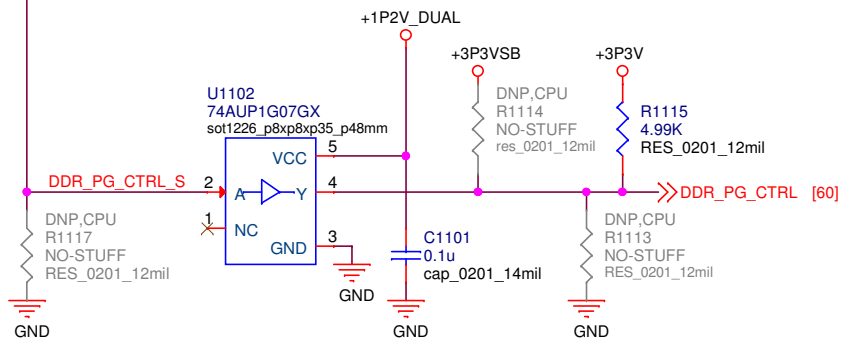
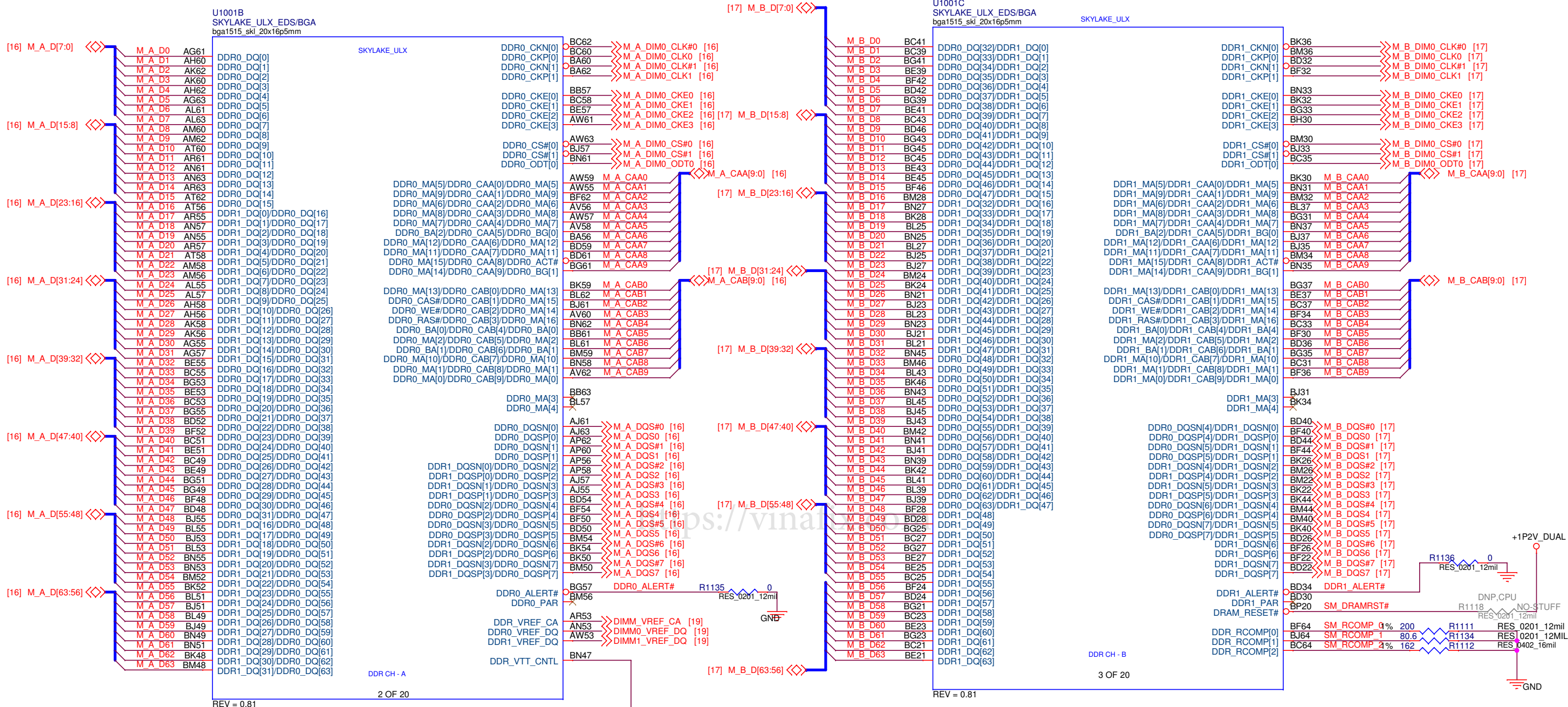


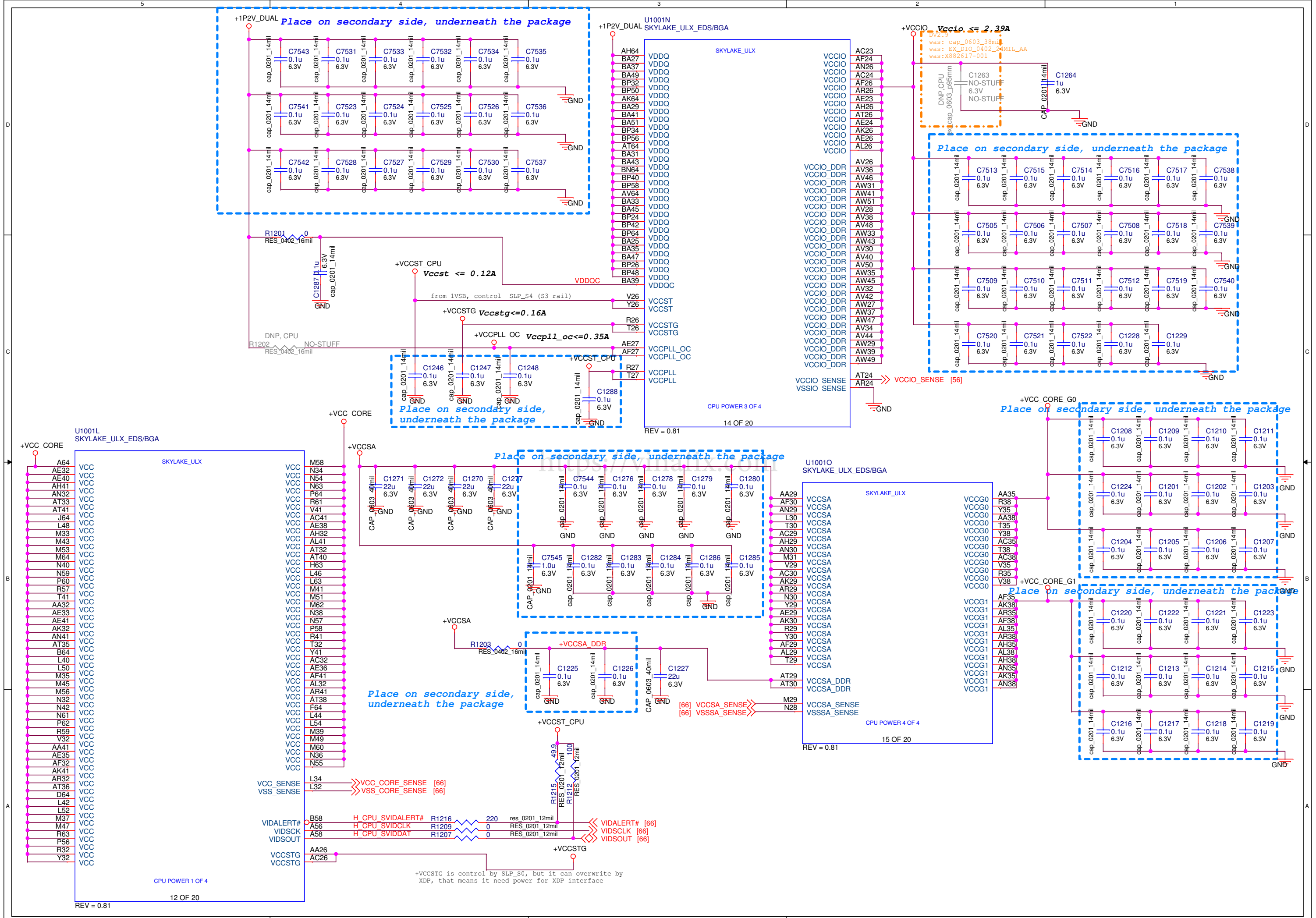
06Dec14 jks: NEEDS UPDATE

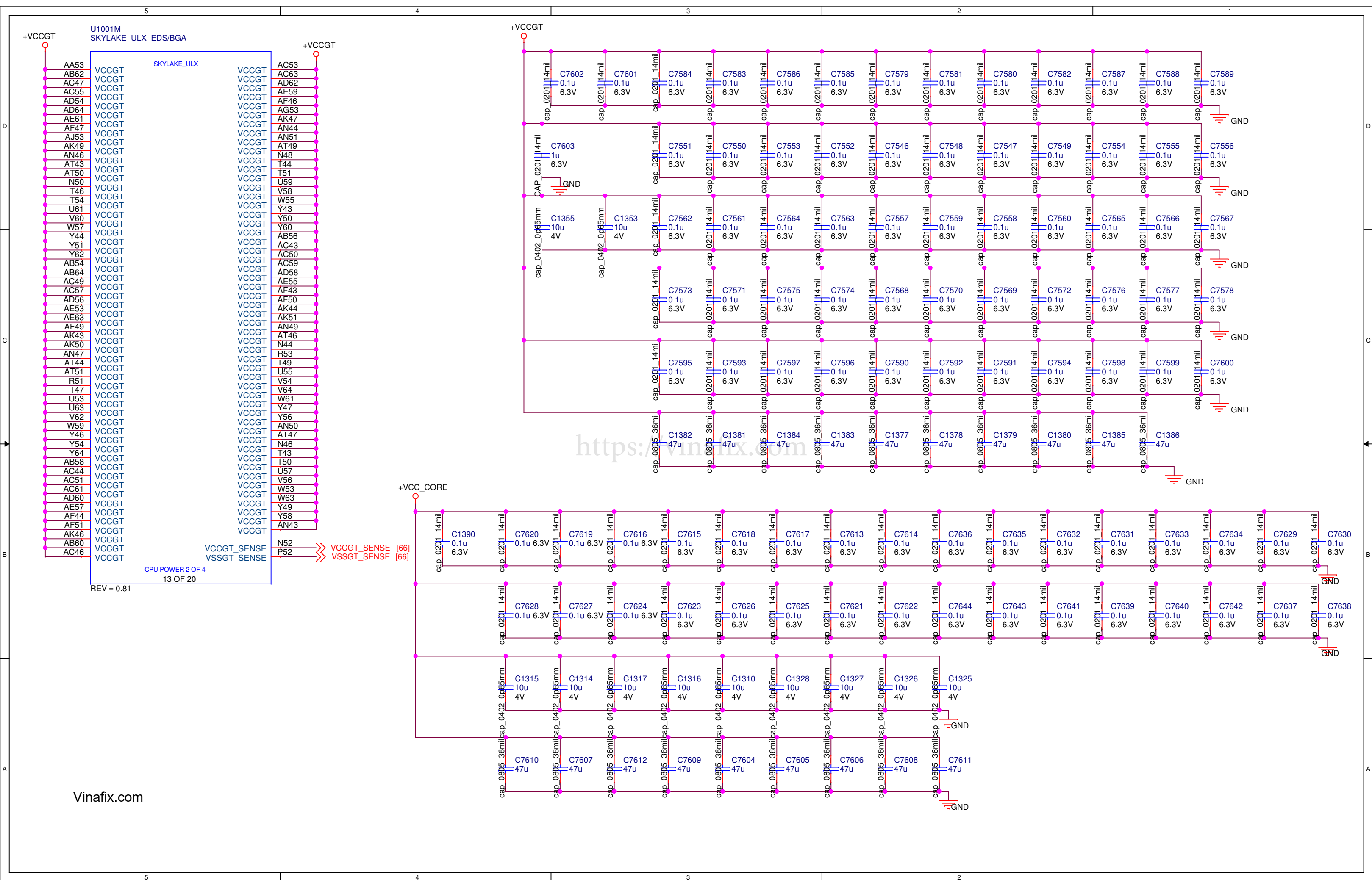
I2C & SMBUS Map

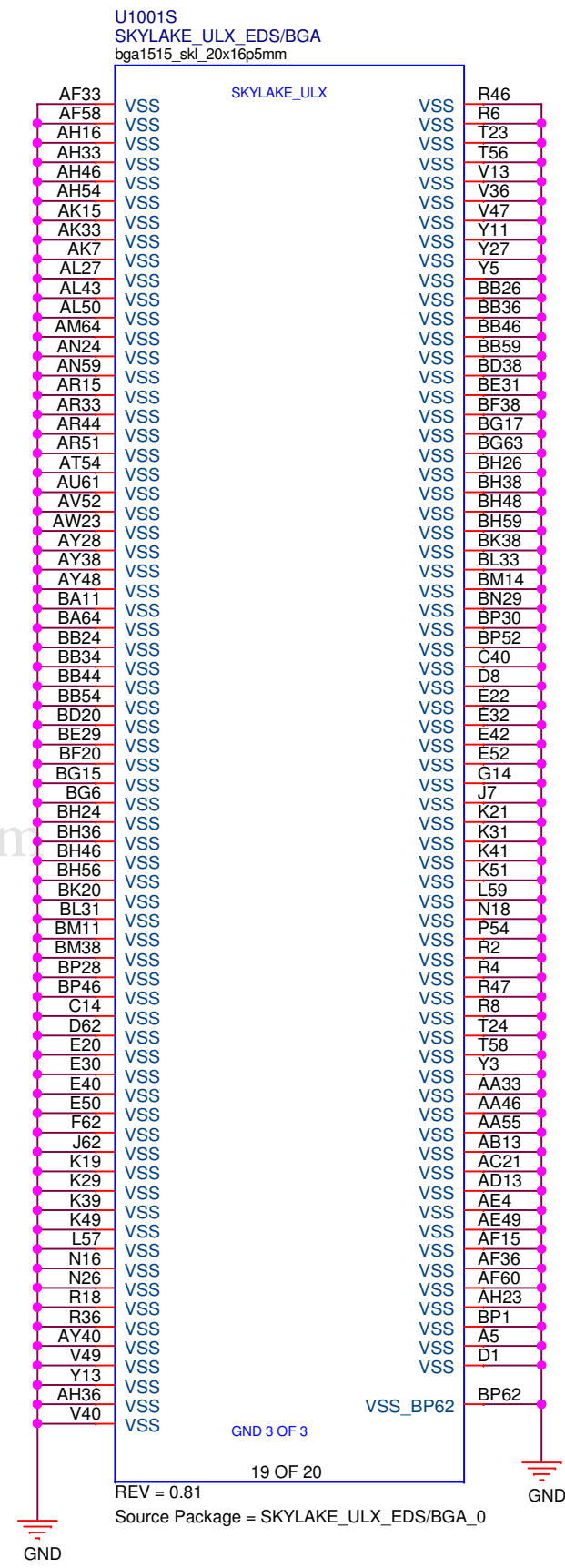
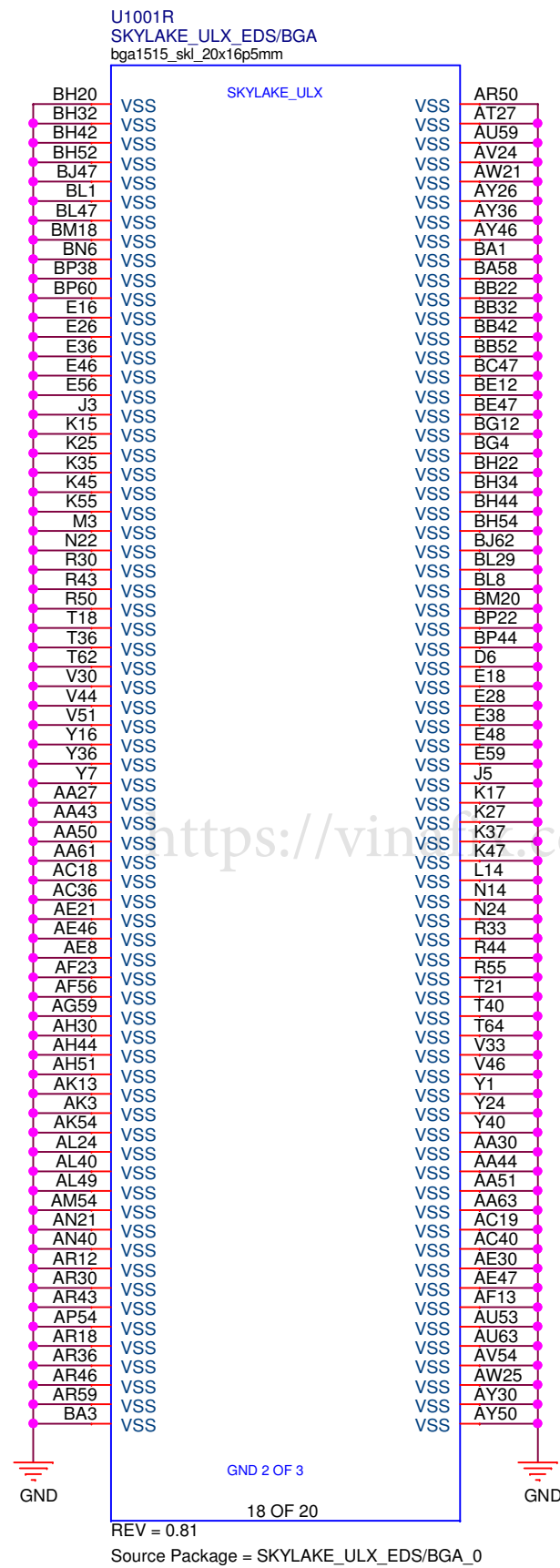
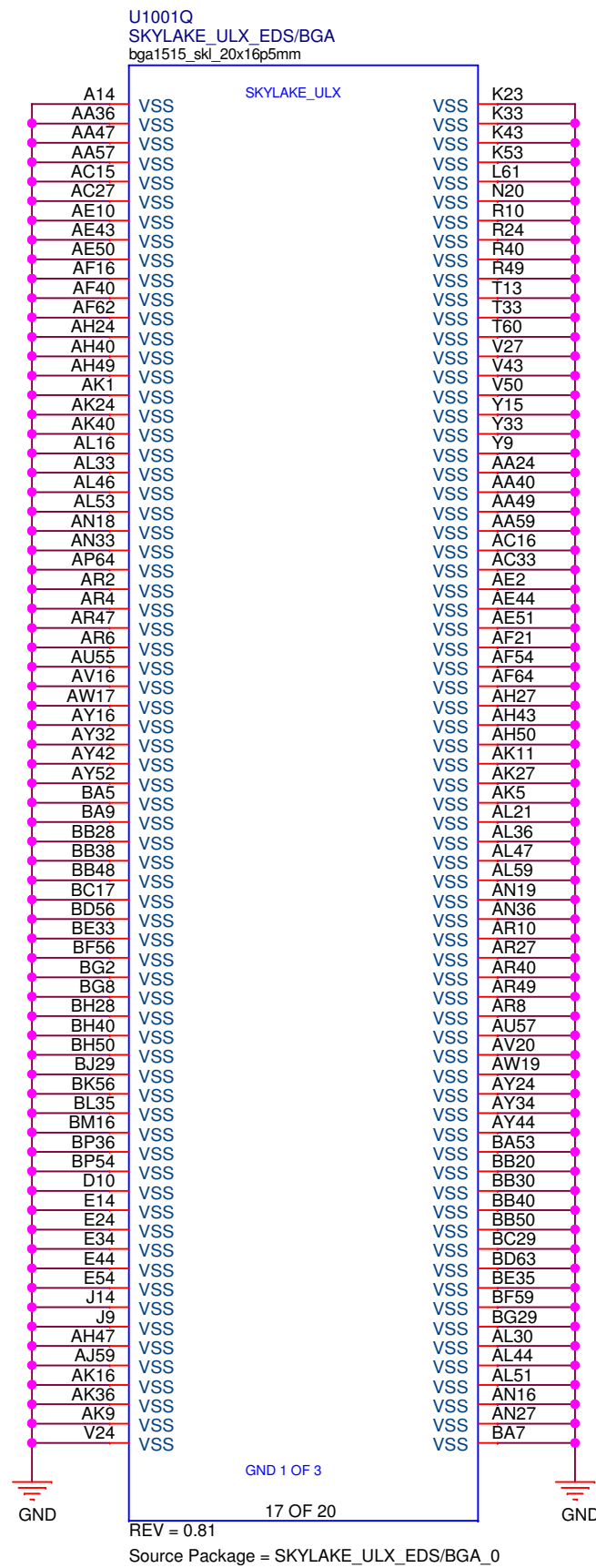


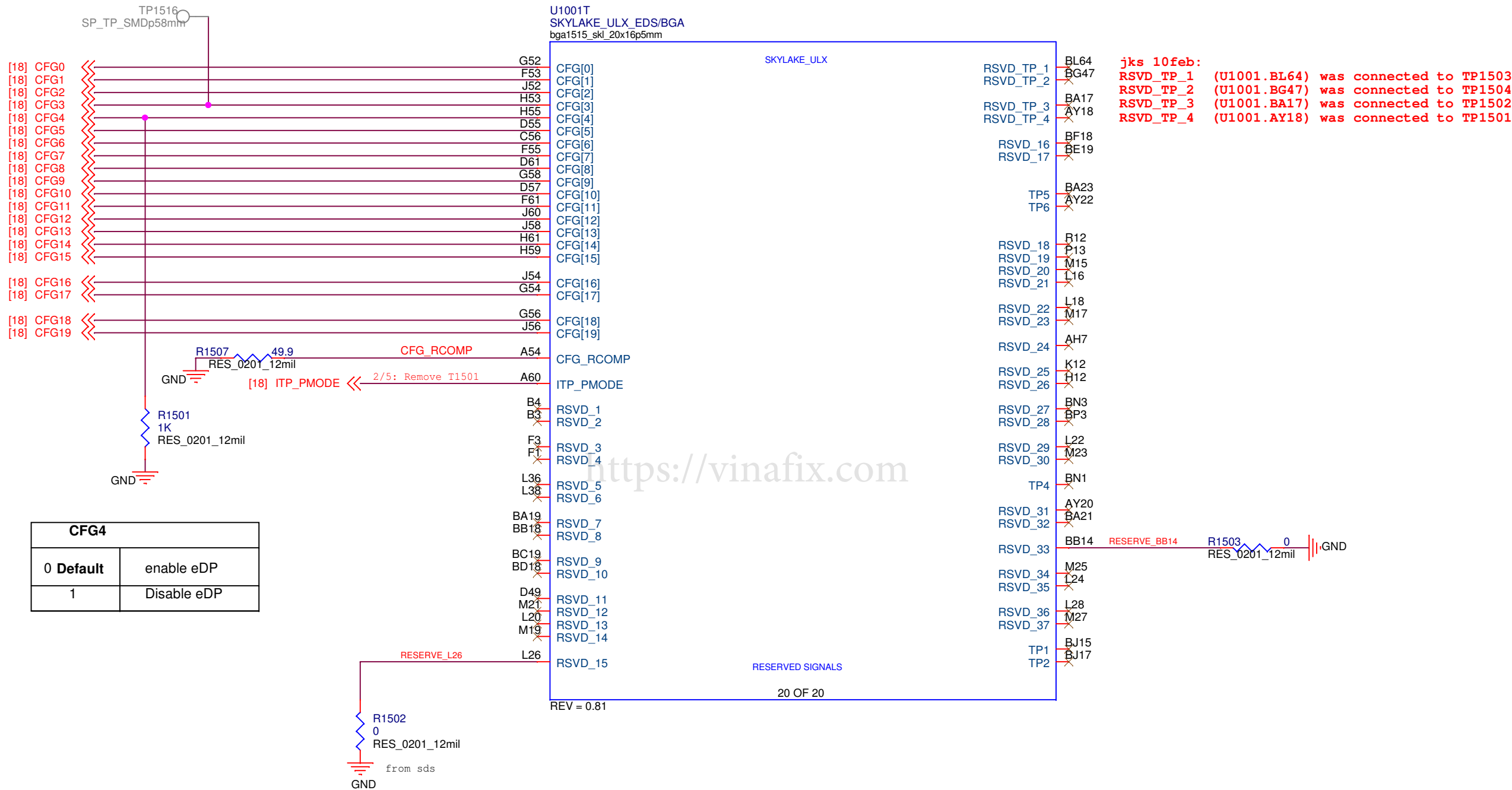


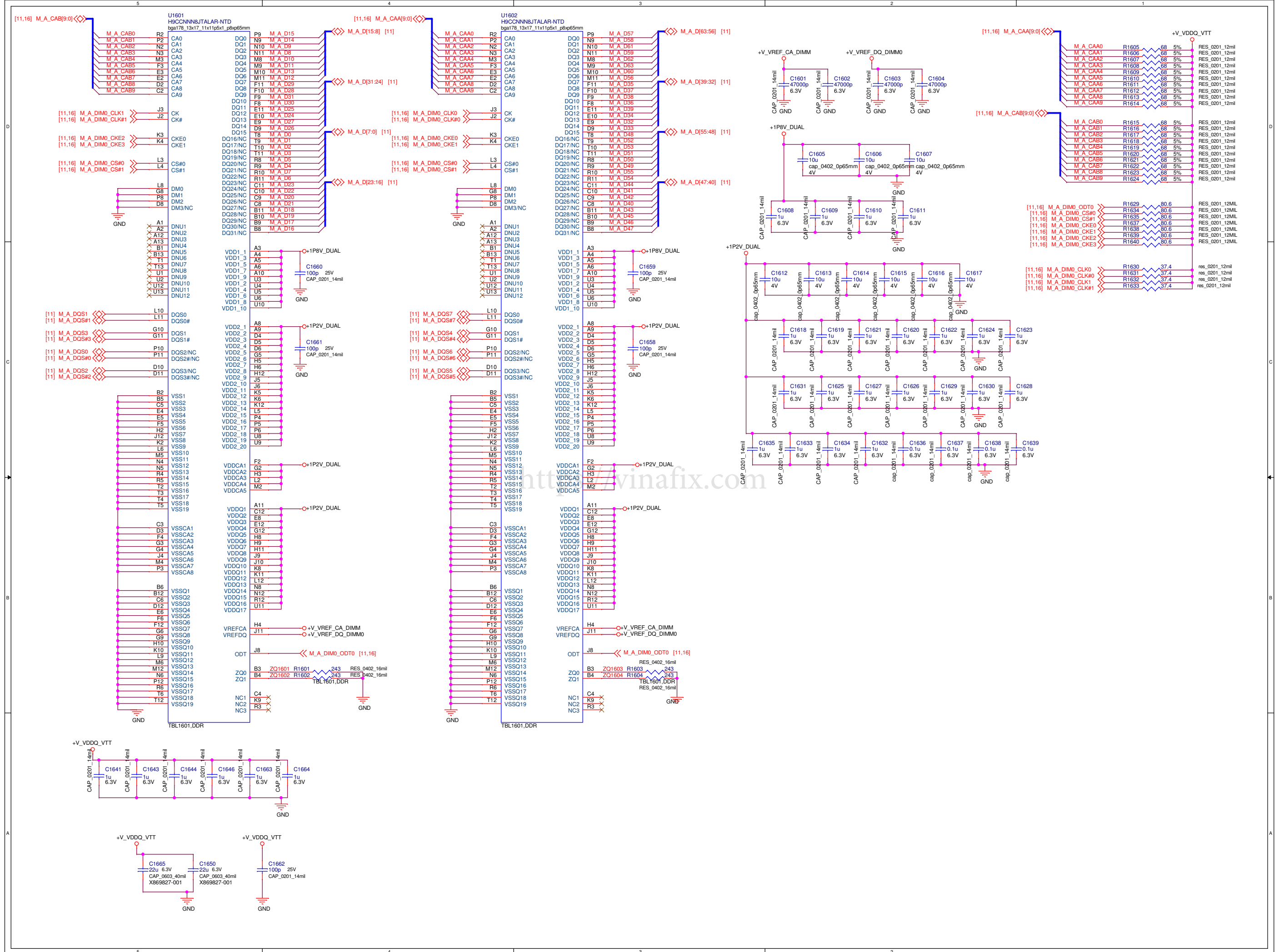






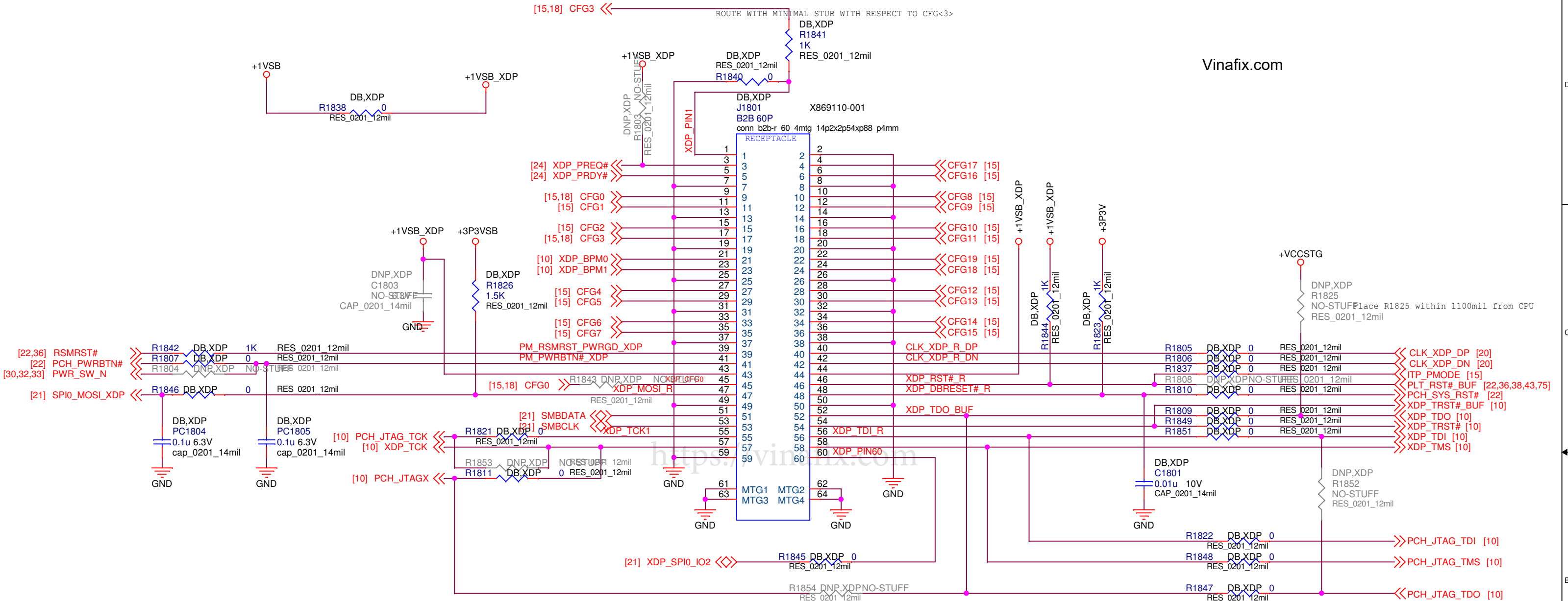






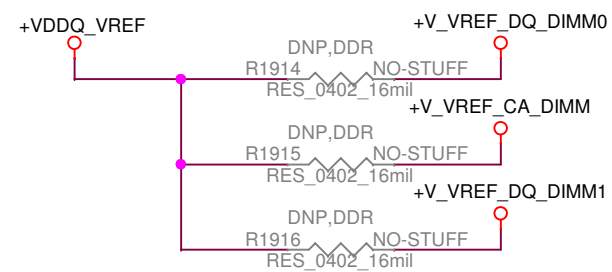
PRIMARY XDP connector

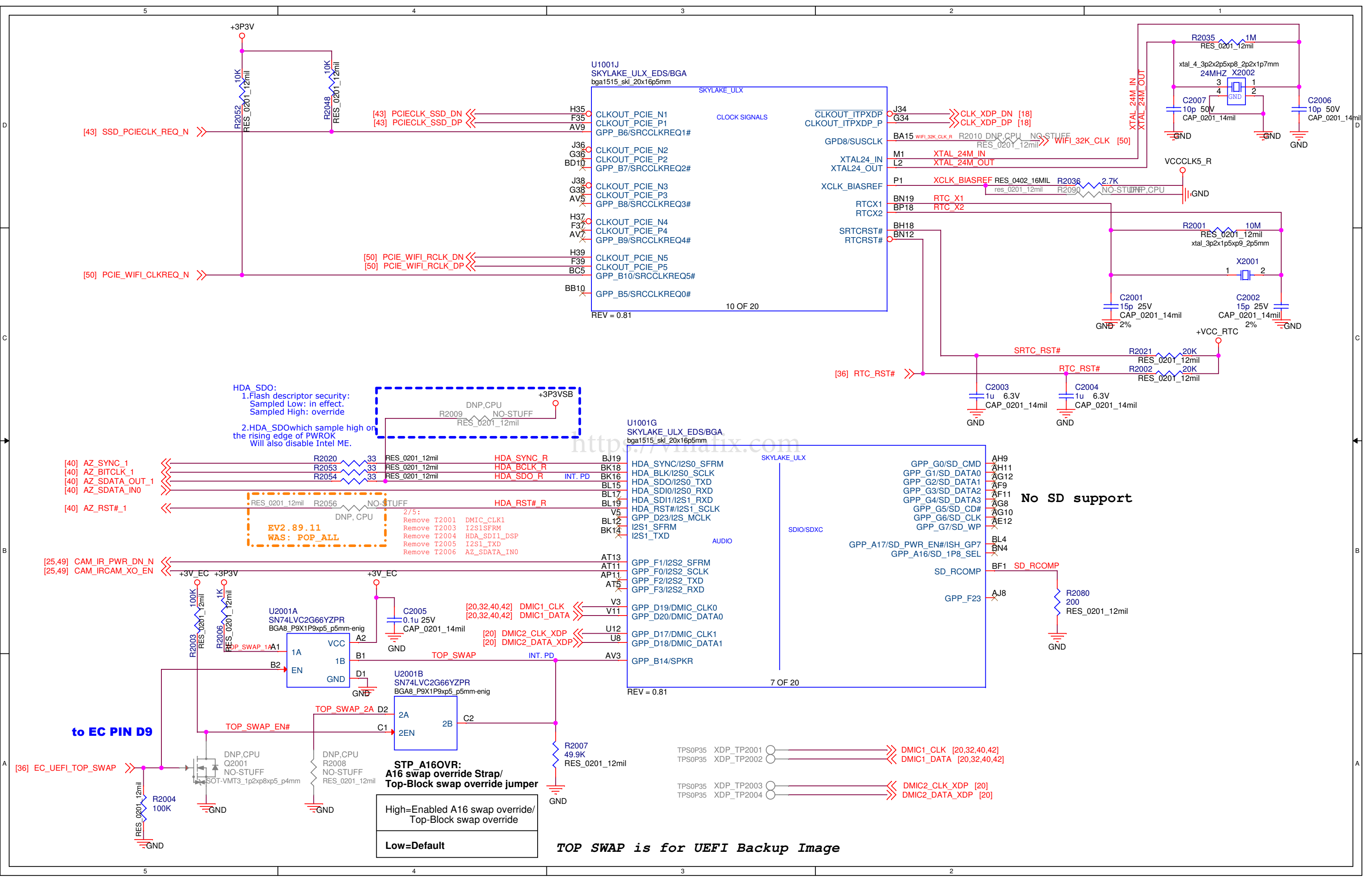
Vinafix.com

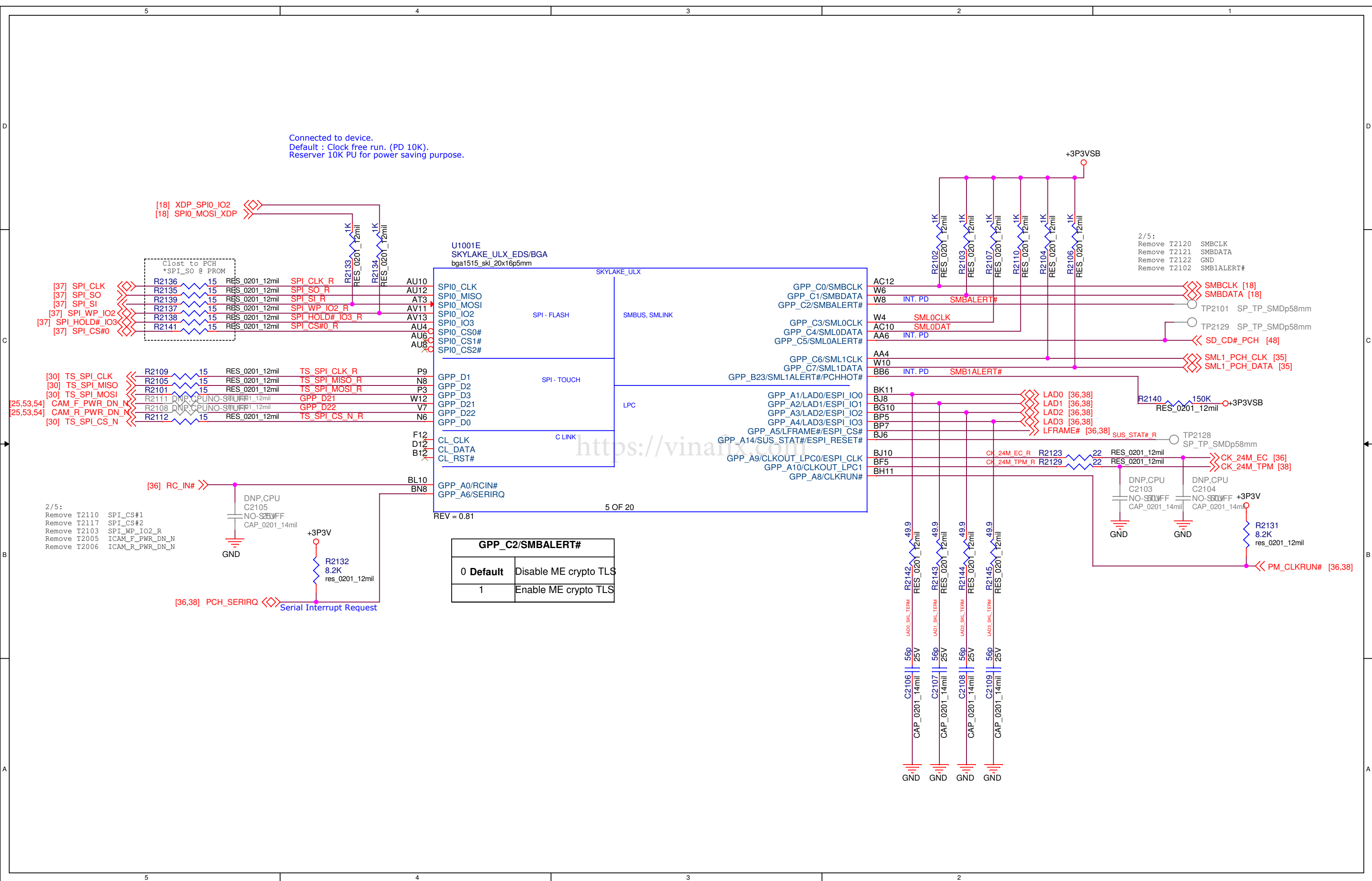


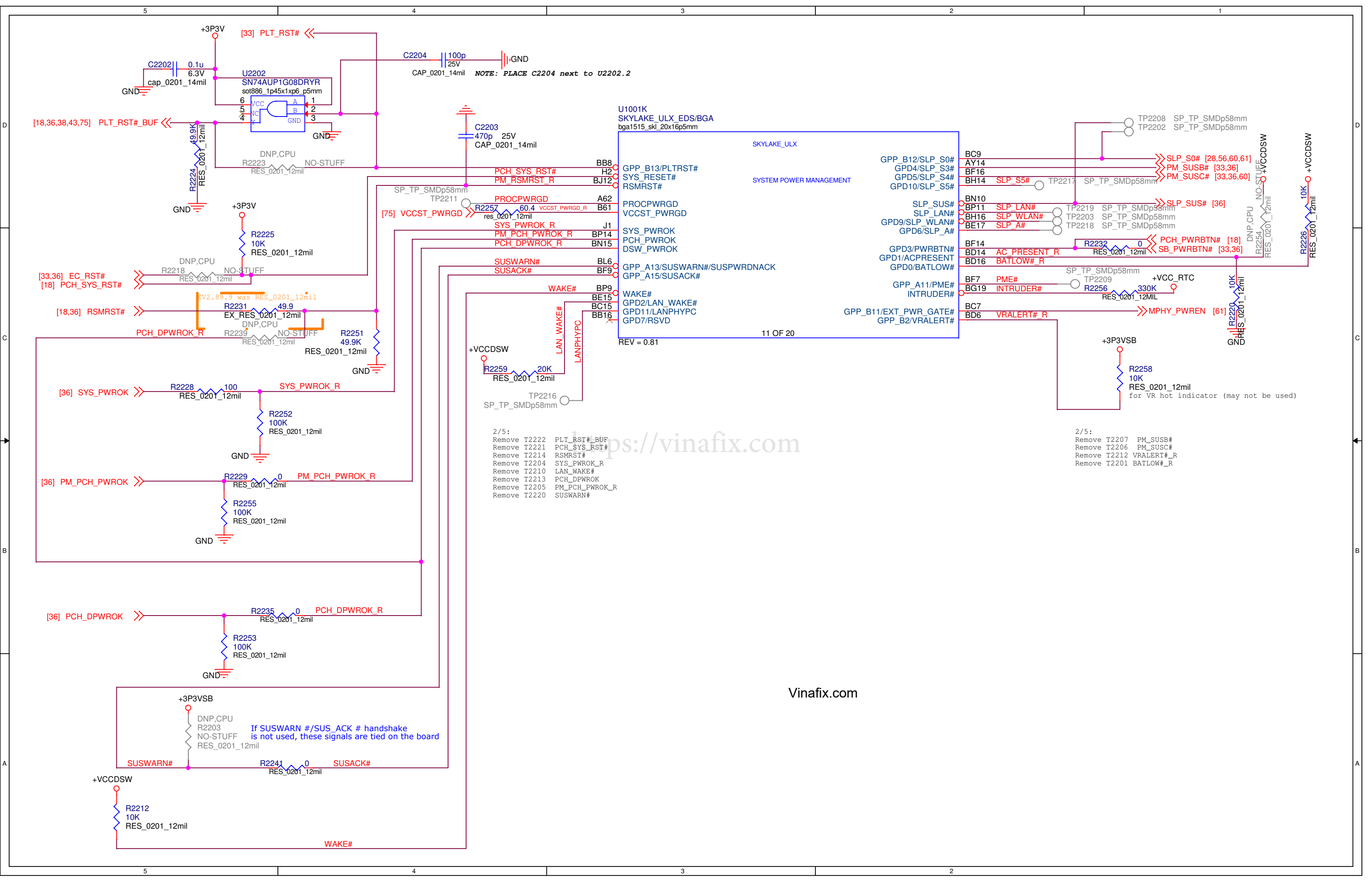
For the signals only go to XDP, the 0R should be close to XDP connector.
For the signals to both XDP and target circuit, the option resistor location should follow the target signal routing.

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



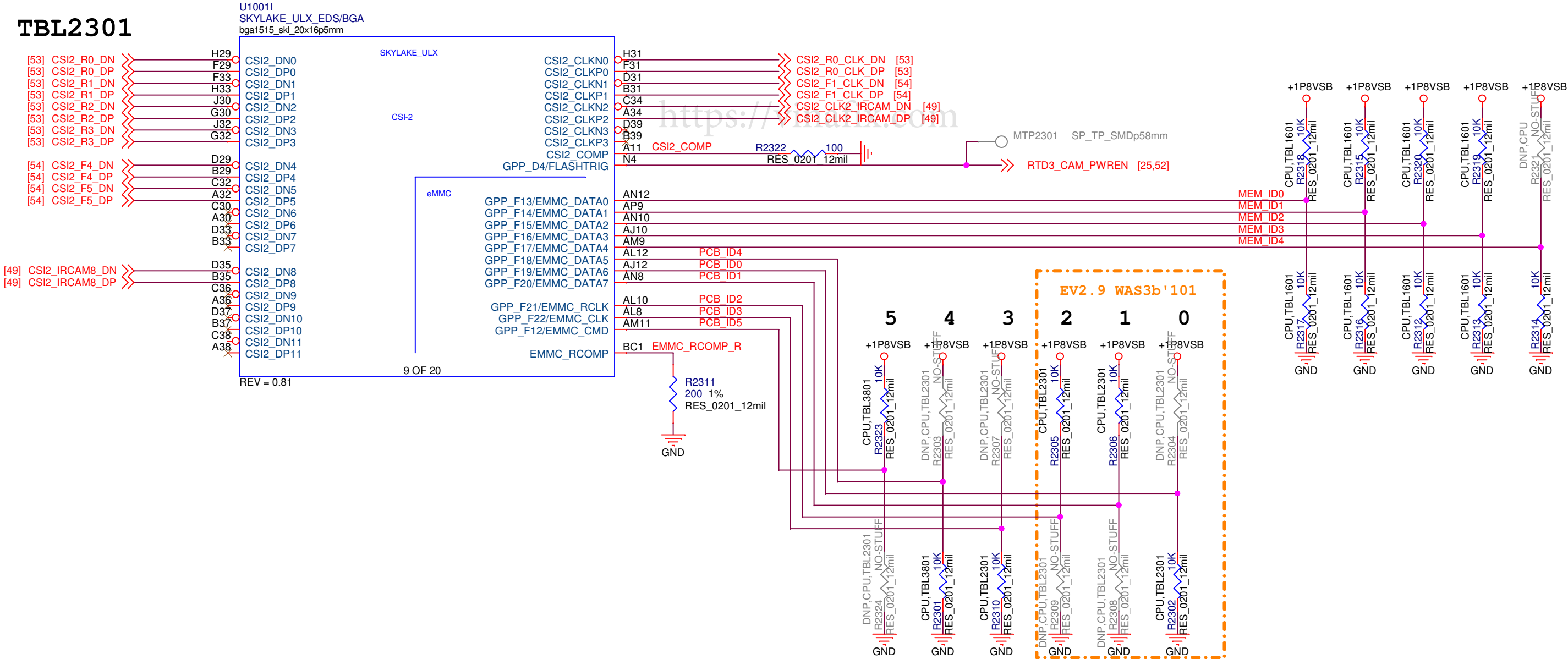






Rev 4	EC Processor ID		PCH Processor ID	TPM			EC Board Rev	PCH Board ID[3:0]				DRAM Manufacturer		RAM Speed	RAM Size & Calibration		
Signal	EC_ID1	ED_ID0	PCB_ID5	PCB_ID4			R3619	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0	MEM_ID1	MEM_ID0	MEM_ID4	MEM_ID3	MEM_ID2	ZQ1
	1 = R3642 0 = R3643	1 = R3640 0 = R3641	1 = R2323 0 = R2324	1 = R2303 0 = R2301	R3813 R3815 R3816	R3814		1 = R2307 0 = R2310	1 = R2305 0 = R2309	1 = R2306 0 = R2308	1 = R2304 0 = R2302	1 = R2315 0 = R2316	1 = R2318 0 = R2317	1 = R2321 0 = R2314	1 = R2319 0 = R2313	1 = R2320 0 = R2312	R1602 R1604 R1702 R1704
	U22 = 0 U23E=1 Y = 0 S = 1	U22 = 0 U23E=0 Y = 1 S = 1	U = 0 Y = 1	Infineon = 0 Nation Z = 1	Infineon = DNP NationZ = POP	Infineon = POP NationZ =DNP						Hynix = 0 Samsung = 0	Hynix = 0 Samsung = 1	1600 LPDDR3 = 0 1866 LPDDR3 = 1	4GB = 0 8GB = 0 16GB = 1	4 GB = 0 8 GB = 1 16 GB = 0	4GB = DNP 8GB = POP 16GB = POP
EV 0.9							80.6 Ω	0	0	0	0						
EV 1.0							169 Ω	0	0	0	1						
EV 1.5							698 Ω	0	0	1	0						
EV 1.9							909 Ω	0	0	1	1						
EV 2.0							1180 Ω	0	1	0	0						
EV 2.1							1500 Ω	0	1	0	1						
EV 2.9							2000 Ω	0	1	1	0						

TBL2301



jks 11nov14: different from G
was on PCI11&12...
PCIE7&8 was used by GPU

PCIE SSD

PCIE WIFI

SP_TP_SMDp58mm TP2417
SP_TP_SMDp58mm TP2418

[18] XDP_PRDY#
[18] XDP_PREQ#

1%
R2401 100
RES_0201_12mil

TP2419
SP_TP_SMDp58mm

PCIE RCOMPN
PCIE RCOMPP

PIRQA#

U1001H
SKYLAKE_ULX_EDS/BGA
bga1515_sk1_20x16p5mm

C20
A20
G20
J20
PCIE1_RXN/USB3_5_RXN
PCIE1_RXP/USB3_5_RXP
PCIE1_TXN/USB3_5_TXN
PCIE1_TXP/USB3_5_TXP

B19
D19
F19
H19
PCIE2_RXN/USB3_6_RXN
PCIE2_RXP/USB3_6_RXP
PCIE2_TXN/USB3_6_TXN
PCIE2_TXP/USB3_6_TXP

C22
A22
G22
J22
PCIE3_RXN
PCIE3_RXP
PCIE3_TXN
PCIE3_TXP

B21
D21
F21
H21
PCIE4_RXN
PCIE4_RXP
PCIE4_TXN
PCIE4_TXP

C24
A24
G24
J24
PCIE5_RXN
PCIE5_RXP
PCIE5_TXN
PCIE5_TXP

B23
D23
F23
H23
PCIE6_RXN
PCIE6_RXP
PCIE6_TXN
PCIE6_TXP

C26
A26
G26
J26
PCIE7_RXN/SATA0_RXN
PCIE7_RXP/SATA0_RXP
PCIE7_TXN/SATA0_TXN
PCIE7_TXP/SATA0_TXP

B25
D25
F25
H25
PCIE8_RXN/SATA1A_RXN
PCIE8_RXP/SATA1A_RXP
PCIE8_TXN/SATA1A_TXN
PCIE8_TXP/SATA1A_TXP

C28
A28
G28
J28
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP

B27
D27
F27
H27
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP

A9
B10
PCIE_RCOMPN
PCIE_RCOMPP

D51
B55
BF3
PROC_PRDY#
PROC_PREQ#
GPP_A7/PIRQA#

REV = 0.81

SKYLAKE_ULX

SSIC / USB3

PCIE/USB3/SATA

USB2

8 OF 20

USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP

USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP

USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP

USB3_4_RXN
USB3_4_RXP
USB3_4_TXN
USB3_4_TXP

USB2N_1
USB2P_1

USB2N_5
USB2P_5

USB2N_7
USB2P_7

USB2N_3
USB2P_3

USB2N_9
USB2P_9

USB2N_2
USB2P_2

USB2_COMP
USB2_ID
USB2_VBUSSENSE

GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2

GPP_E0/SATAXPCEI0/SATAGP0
GPP_E1/SATAXPCEI1/SATAGP1
GPP_E2/SATAXPCEI2/SATAGP2

GPP_E8/SATALED#

C16
A16
G16
J16
USB3_CONN_RX_DN [45]
USB3_CONN_RX_DP [45]
USB3_CONN_TX_DN [45]
USB3_CONN_TX_DP [45]

B15
D15
F15
H15
USB3_SL1_RX_DN [71]
USB3_SL1_RX_DP [71]
USB3_SL1_TX_DN [71]
USB3_SL1_TX_DP [71]

C18
A18
G18
J18
USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP

B17
D17
F17
H17
USB3_SDXC_RX_DN [48]
USB3_SDXC_RX_DP [48]
USB3_SDXC_TX_DN [48]
USB3_SDXC_TX_DP [48]

AJ6
AJ4
USB2_CONN_DN [45]
USB2_CONN_DP [45]

AH5
AH3
USB2_BT_DN [50]
USB2_BT_DP [50]

AF5
AF3
USB2_BLADE_DN [74]
USB2_BLADE_DP [74]

AL6
AL4
AG6
AG4
USB2N_3
USB2P_3

AM3
AM5
USB2_SL1_DN [71]
USB2_SL1_DP [71]

N2
AF7
AE6
USB2_COMP
RES_0402_16mil
GND

N12
M11
F8
B8
GPP_E10
GPP_E11
GPP_E12

F10
H10
L8
GPP_E4
GPP_E5
DEVSLP2

G11
J11
N10
GPP_E0
GPP_E1
GPP_E2

H8
GPP_E8

USB3 TYPE A

USB3 SL1

USB3 SDXC

USB2 TYPE A

BT

USB2 BLADE

USB2 SL1

RES_0201_12mil R2420 10K
RES_0201_12mil R2421 10K
RES_0201_12mil R2422 10K
RES_0201_12mil R2423 10K

USB_CONN_OC# [45]

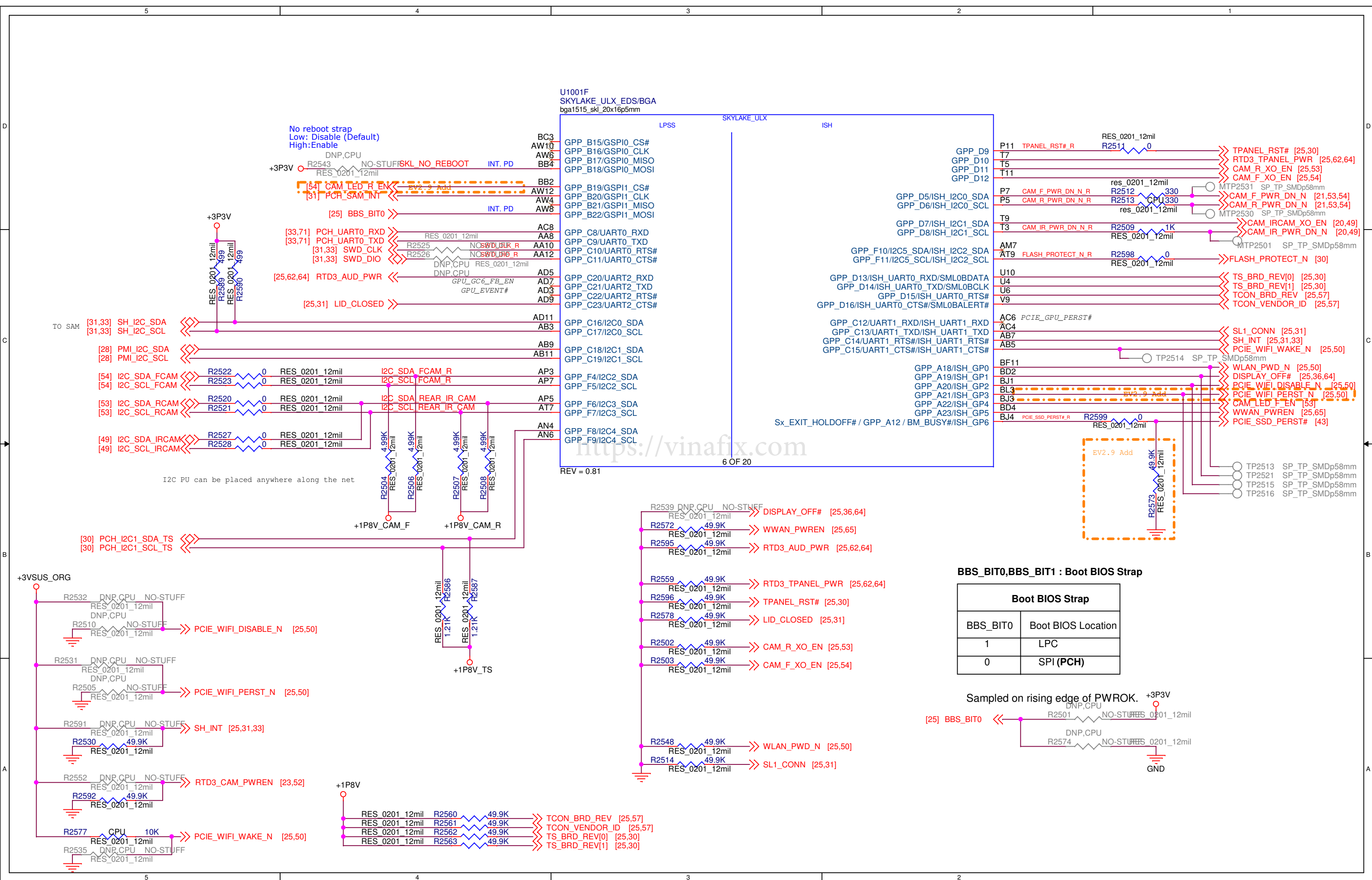
R2406 DNP CPUNO-ST15F B201_12mil XDP_TP2400 TPS0P35
R2405 DNP CPUNO-ST15F B201_12mil XDP_TP2401 TPS0P35
R2407 DNP CPUNO-ST15F B201_12mil XDP_TP2402 TPS0P35
R2408 DNP CPUNO-ST15F B201_12mil XDP_TP2403 TPS0P35

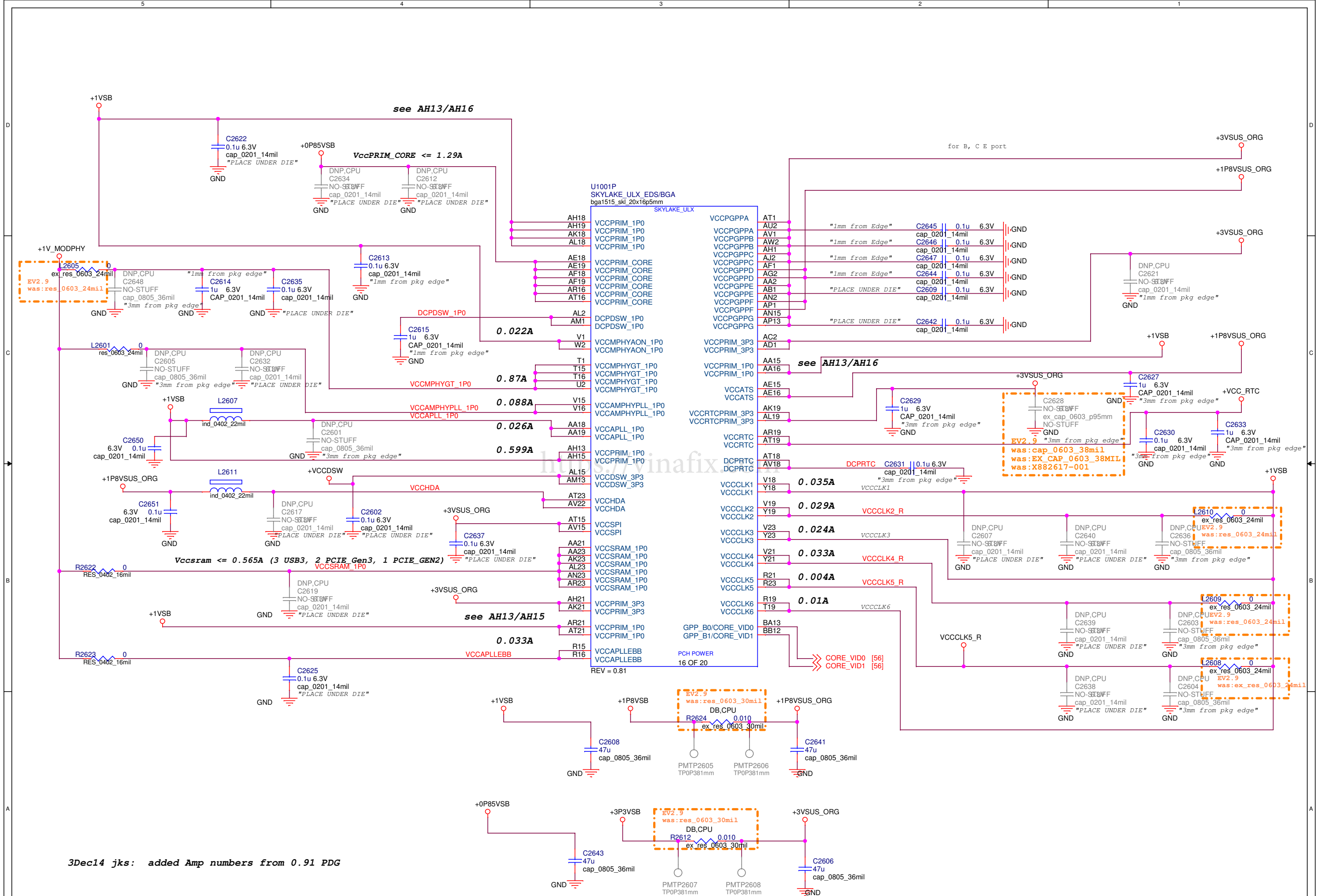
R2415 DNP CPUNO-ST15F B201_12mil XDP_TP2404 TPS0P35
R2414 DNP CPUNO-ST15F B201_12mil XDP_TP2405 TPS0P35
R2416 DNP CPUNO-ST15F B201_12mil XDP_TP2406 TPS0P35

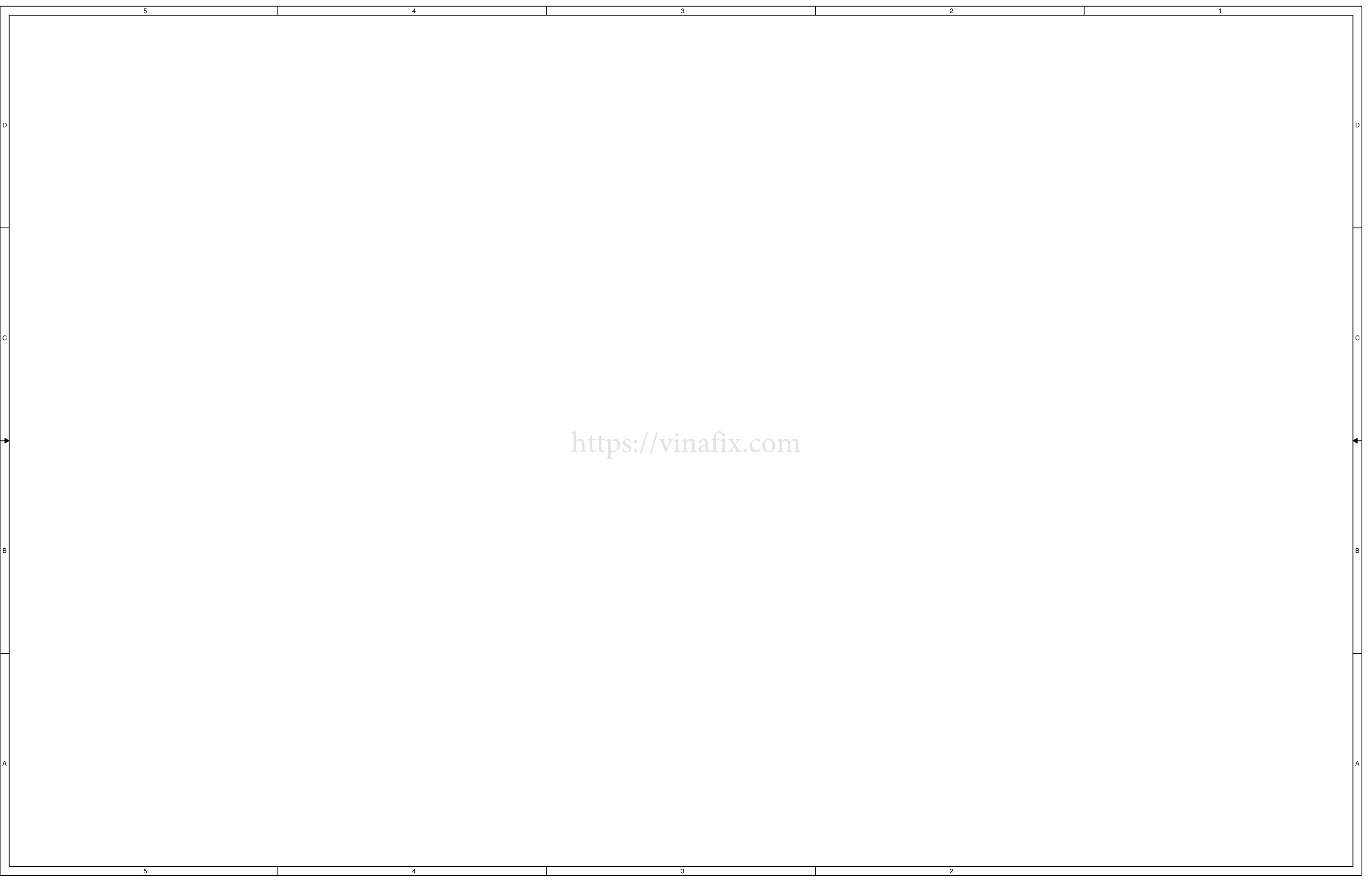
R2410 DNP CPUNO-ST15F B201_12mil XDP_TP2407 TPS0P35
R2411 DNP CPUNO-ST15F B201_12mil XDP_TP2408 TPS0P35
R2412 DNP CPUNO-ST15F B201_12mil XDP_TP2409 TPS0P35

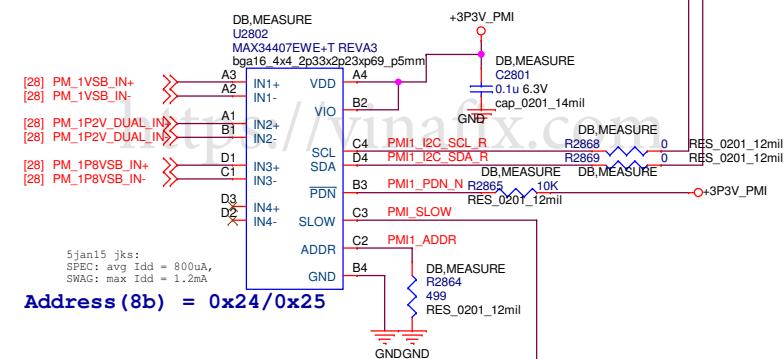
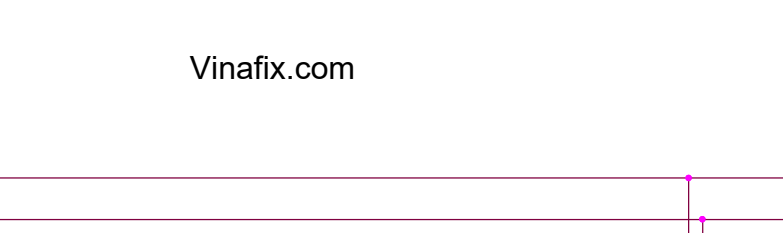
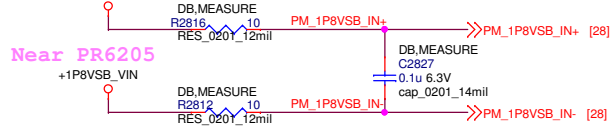
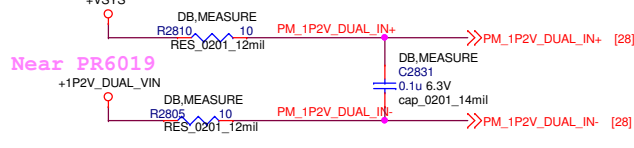
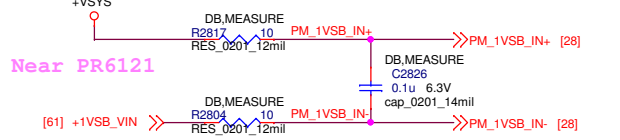
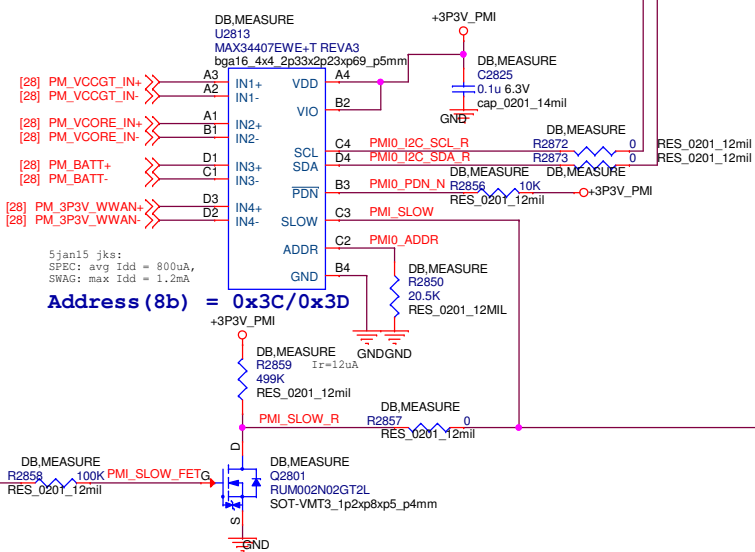
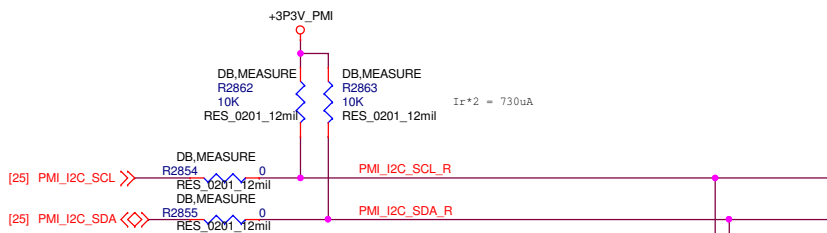
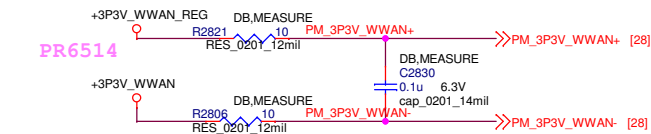
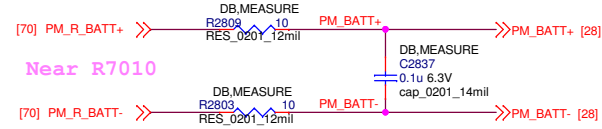
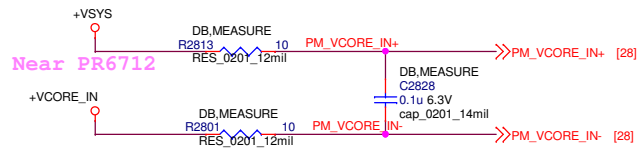
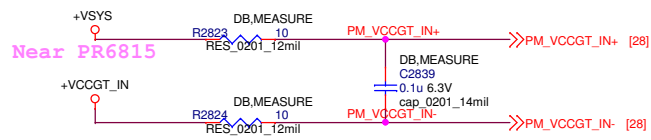
R2413 DNP CPUNO-ST15F B201_12mil XDP_TP2410 TPS0P35

R2403 0 RES_0201_12mil
R2409 0 RES_0201_12mil
DEVSLP_SSD [43]
SSD_SATA_PCIE_DET_N [43]



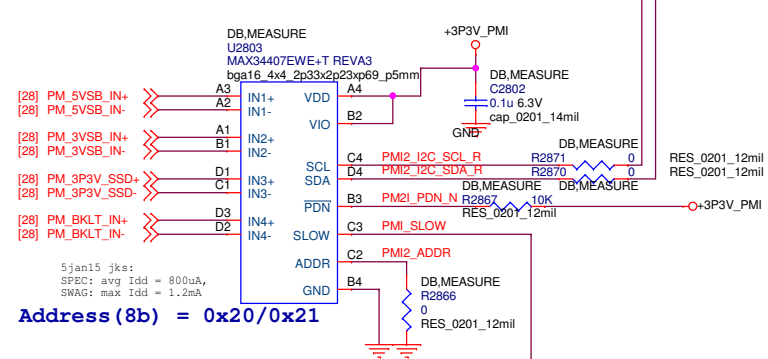
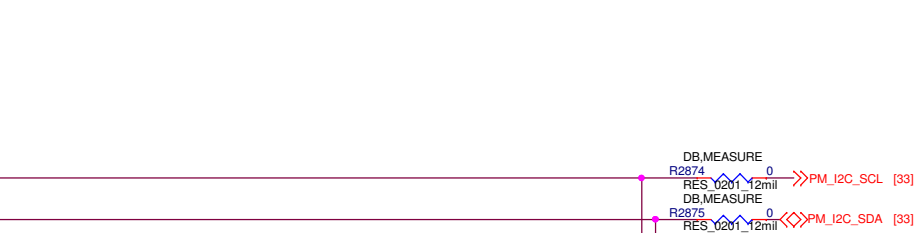
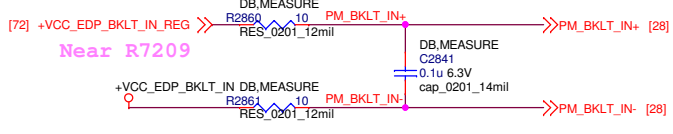
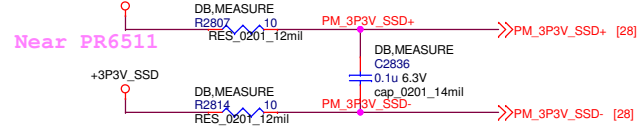
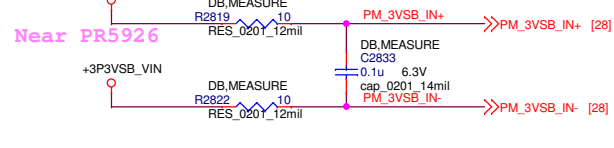
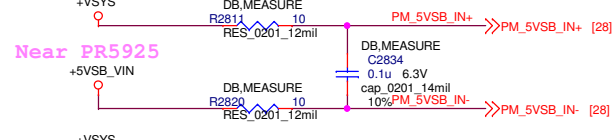






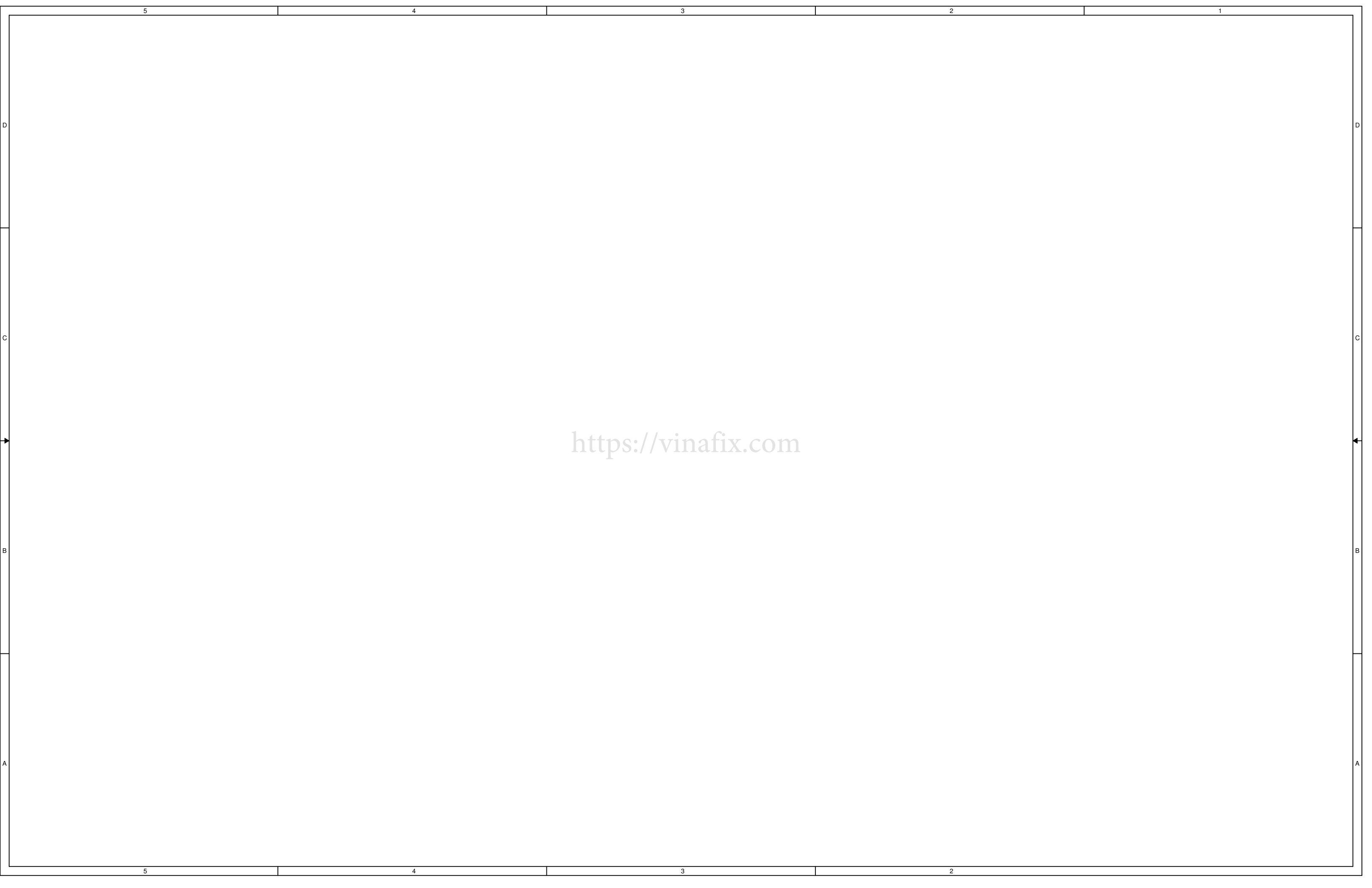
Resistor Address for MAX3440

20.5K	=>	2x3C/2x3D
11.0K	=>	2x38/2x39
5.90K	=>	2x34/2x35
3.16K	=>	2x30/2x31
1.74K	=>	2x2C/2x2D
931K	=>	2x28/2x29
499	=>	2x24/2x25
GND	=>	2x20/2x21



Resistor Address for MAX3440

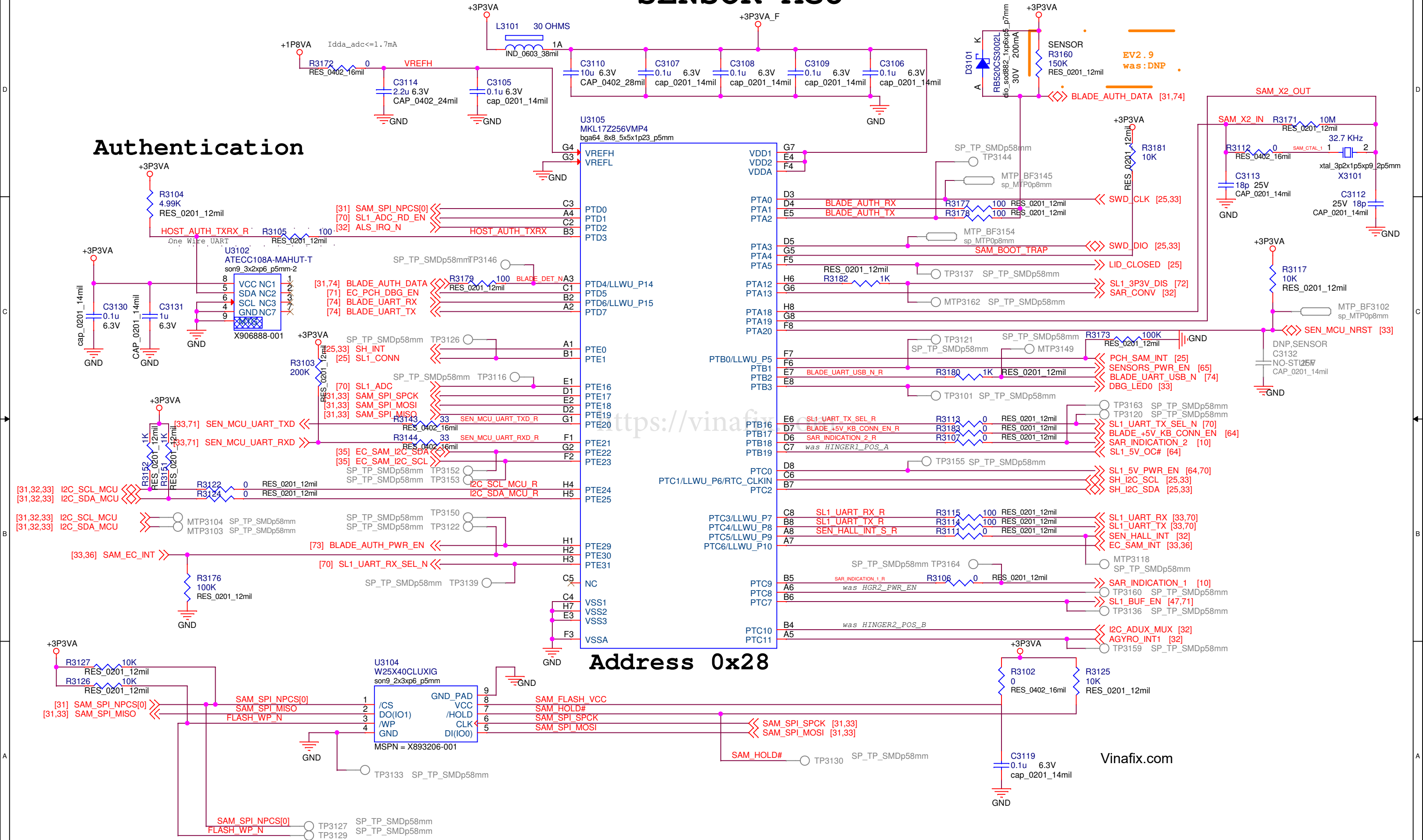
20.5K	=>	2x3C/2x3D
11.0K	=>	2x38/2x39
5.90K	=>	2x34/2x35
3.16K	=>	2x30/2x31
1.74K	=>	2x2C/2x2D
931K	=>	2x28/2x29
499	=>	2x24/2x25
GND	=>	2x20/2x21



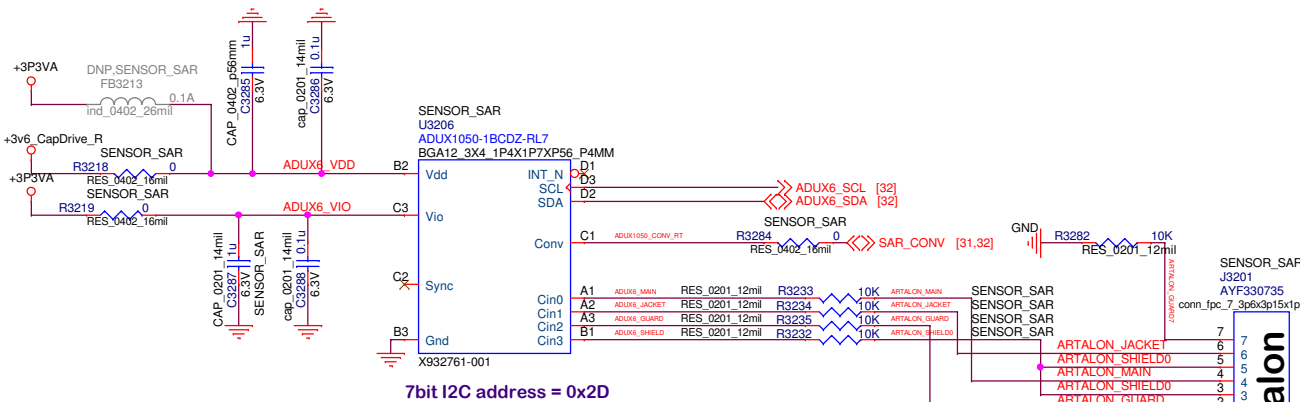
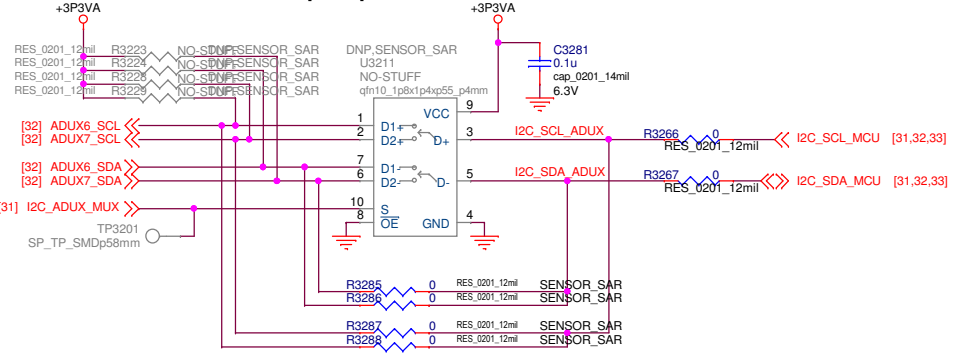
SENSOR MCU

Authentication

Address 0x28

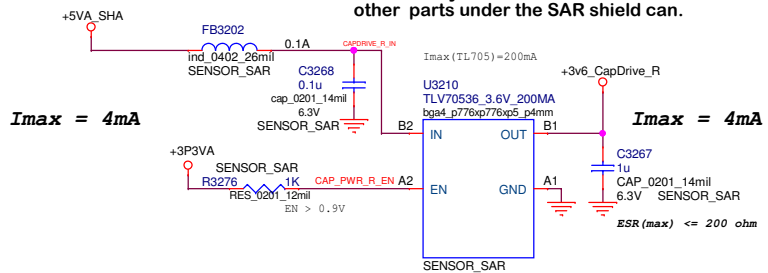


WiFi envelope protection drivers

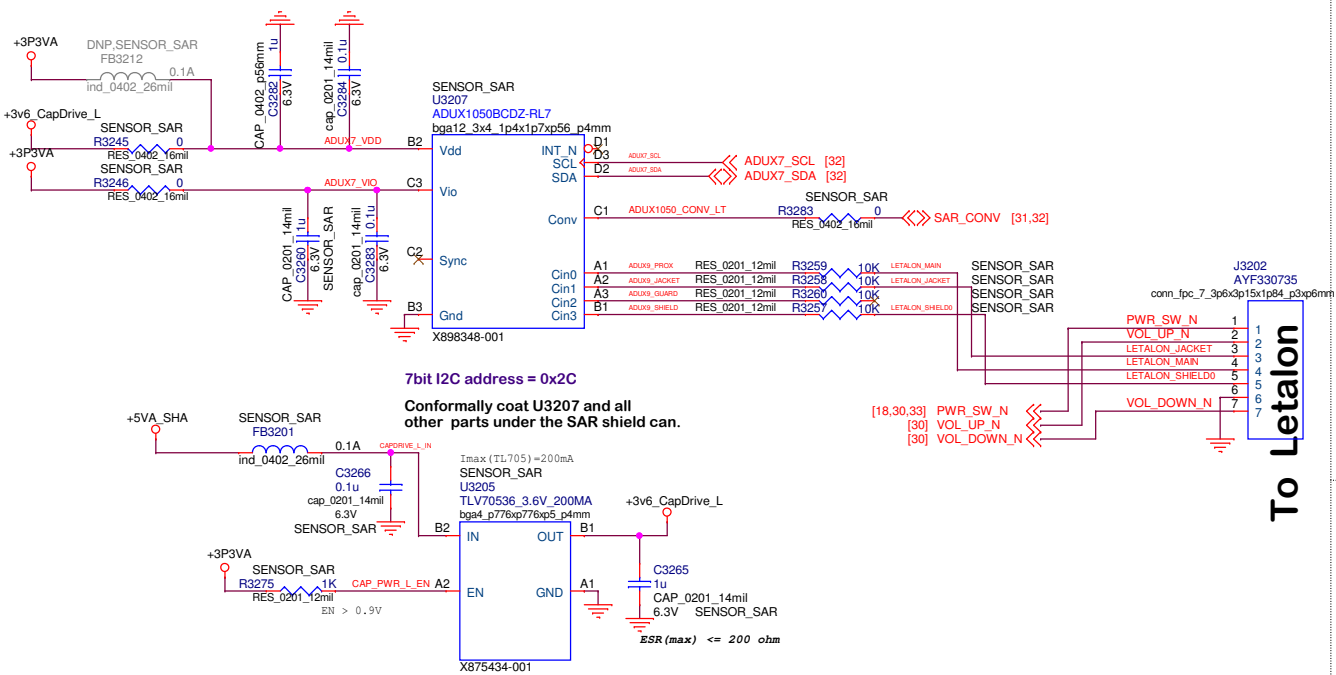


7bit I2C address = 0x2D

Conformally coat U3206 and all other parts under the SAR shield can.


$$I_{max} = 4mA$$
$$I_{max} = 4mA$$

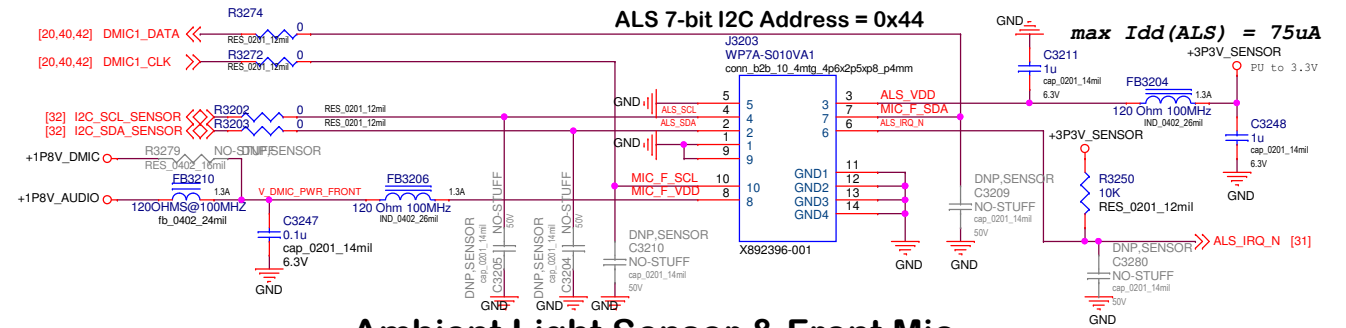
ESR (max) $\leq 200 \text{ ohm}$



7bit I2C address = 0x2C

Conformally coat U3207 and all other parts under the SAR shield can.

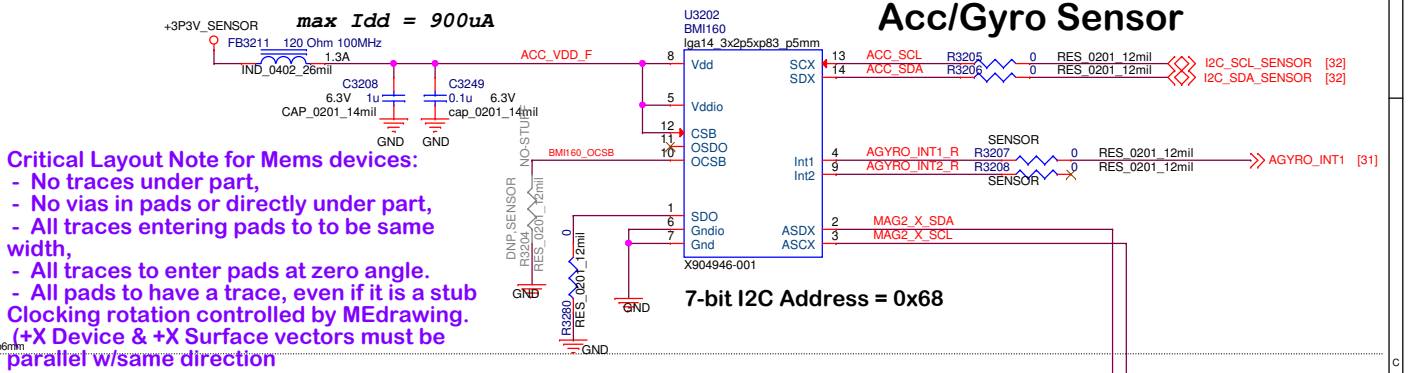
ESR (max) <= 200 ohm



ALS 7-bit I2C Address = 0x44

$\max I_{dd}(ALS) = 75\mu A$

Ambient Light Sensor & Front Mic



Critical Layout Note for Mems devices:

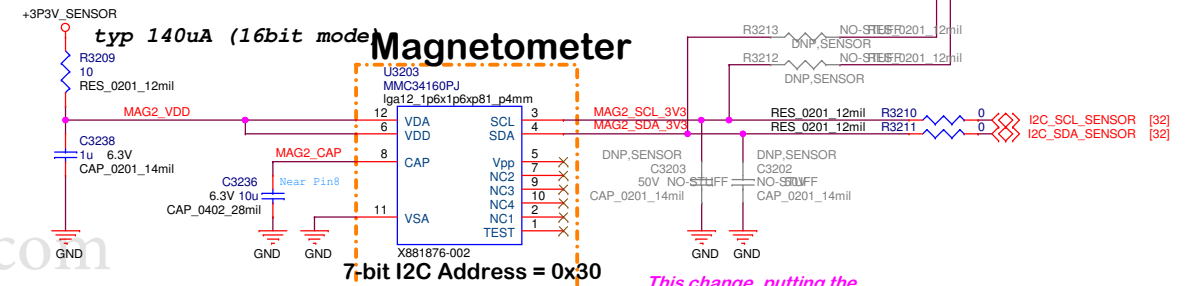
- No traces under part,
 - No vias in pads or directly under part,
 - All traces entering pads to be same width,
 - All traces to enter pads at zero angle.
 - All pads to have a trace, even if it is a stub
- Clockwise rotation controlled by MEDrawing.
- (+X Device & +X Surface vectors must be parallel w/same direction)

$$\max I_{dd} = 900\mu A$$

Acc/Gyro Sensor

7-bit I2C Address = 0x68

le Magnetometer

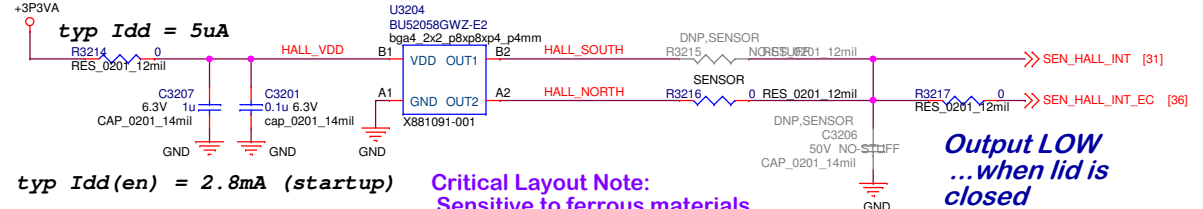


Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be $>8\text{mm}$ remote
No traces carrying $>8\text{mA}$ within 10mm
... on any layer.
Clocking rotation controlled by MEdrawing.

7-bit I2C Address = 0x30

This change, putting the MAG behind the AGyro allows us to take advantage of the time-stamped FIFO in the AGyro to reduce power consumption and address load on the I2C bus -- in addition to improving jitter filtering in post processing. Eventually this will enable IR range camera frame syncing.

Hall Effect Sensor

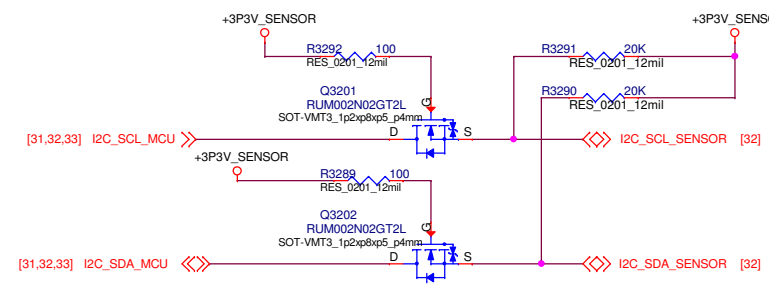


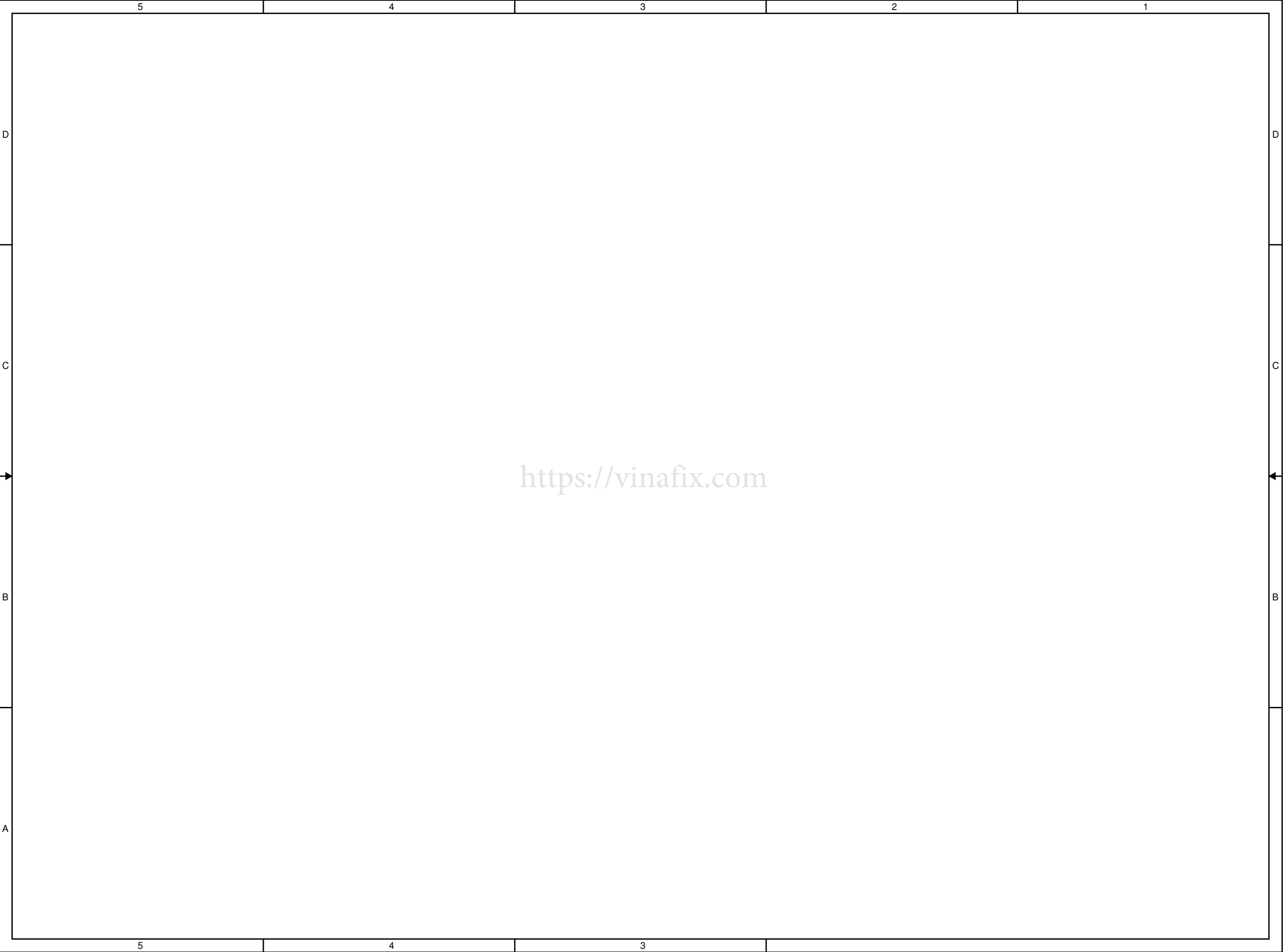
$typ\ I_{dd} = 5\mu A$

$$typ\ I_{dd}(en) = 2.8mA\ (startup)$$

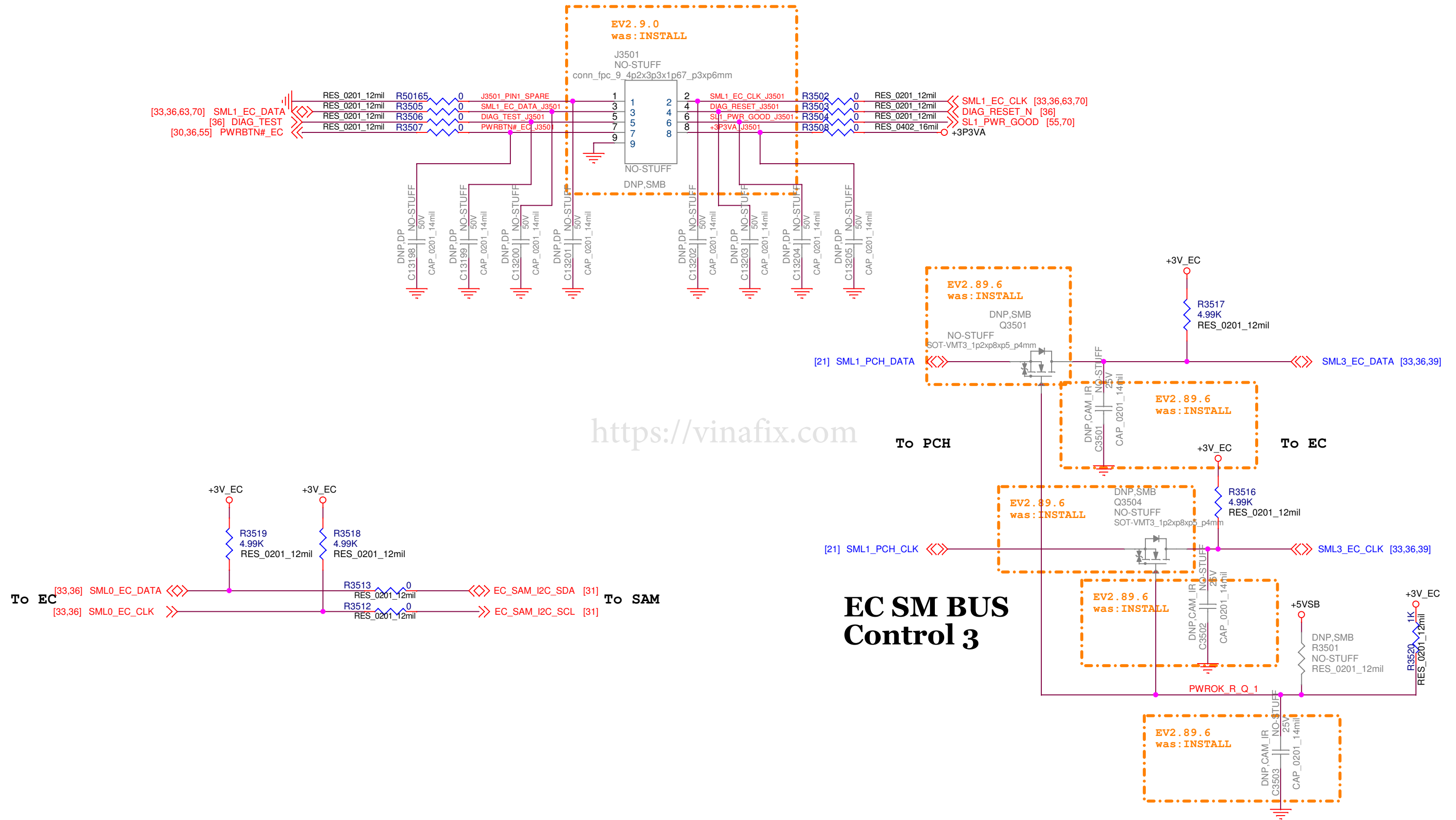
*Output LOW
...when lid is
closed*

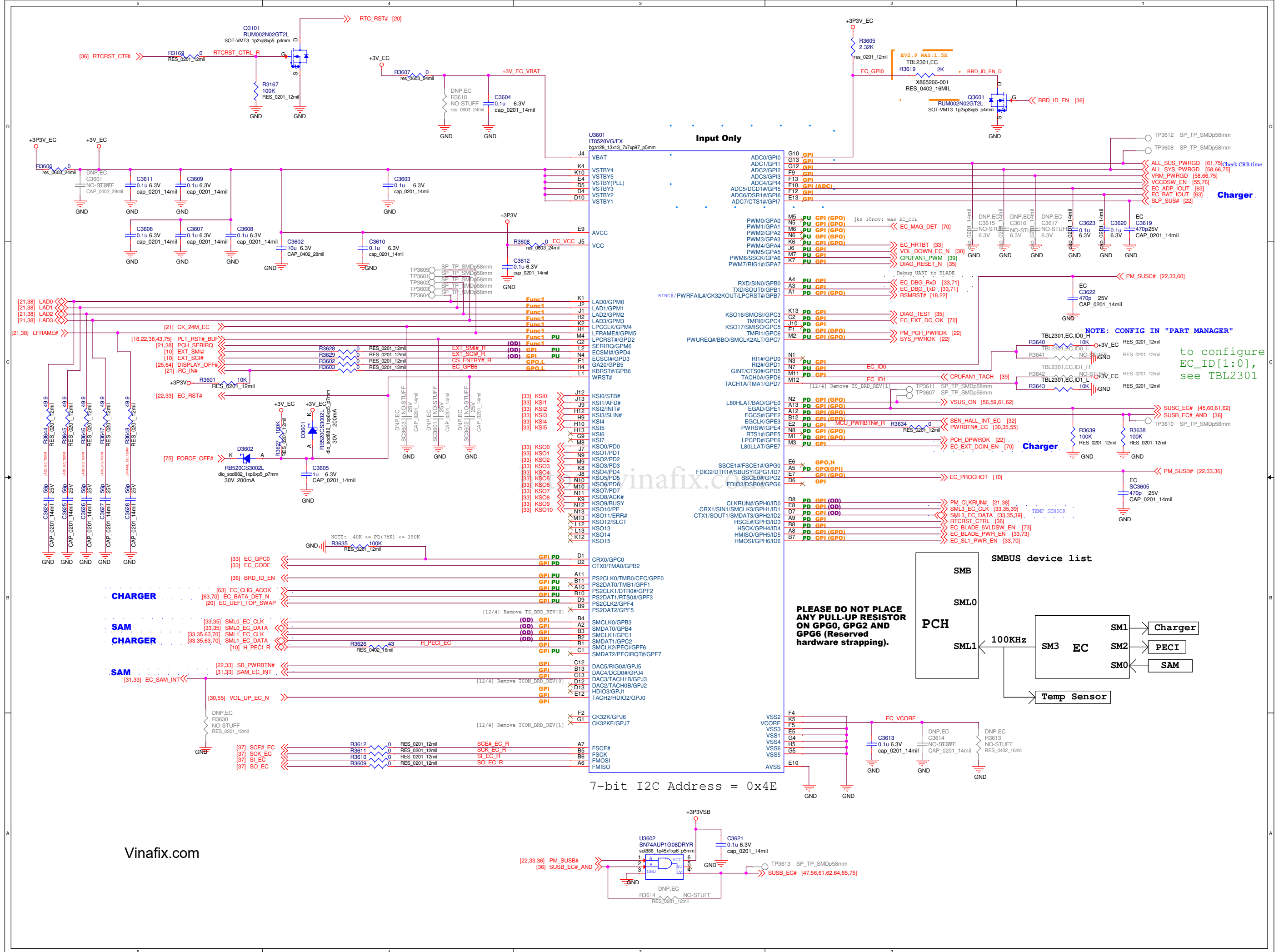
Critical Layout Note:
Sensitive to ferrous materials
Do not mount under a steel shield can
If mounted on Glass side of board,
Trigger may occur
as early as 30Gauss North B-field
or as late as 50Gauss North B-field
Be careful not to mount within 15mm
of speaker autofocus camera or other
magnet.
X-Y location controlled by MEdrawing.





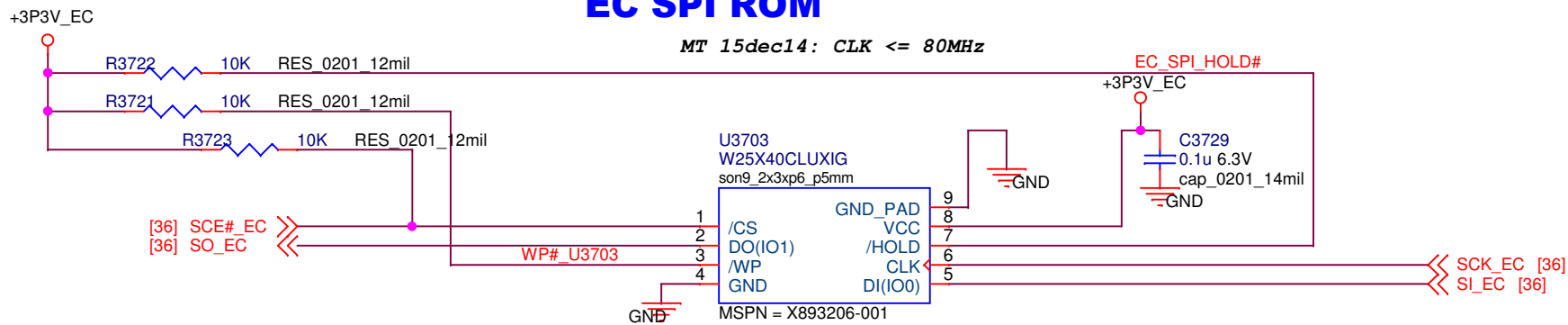
DIAGNOSTIC CONNECTOR





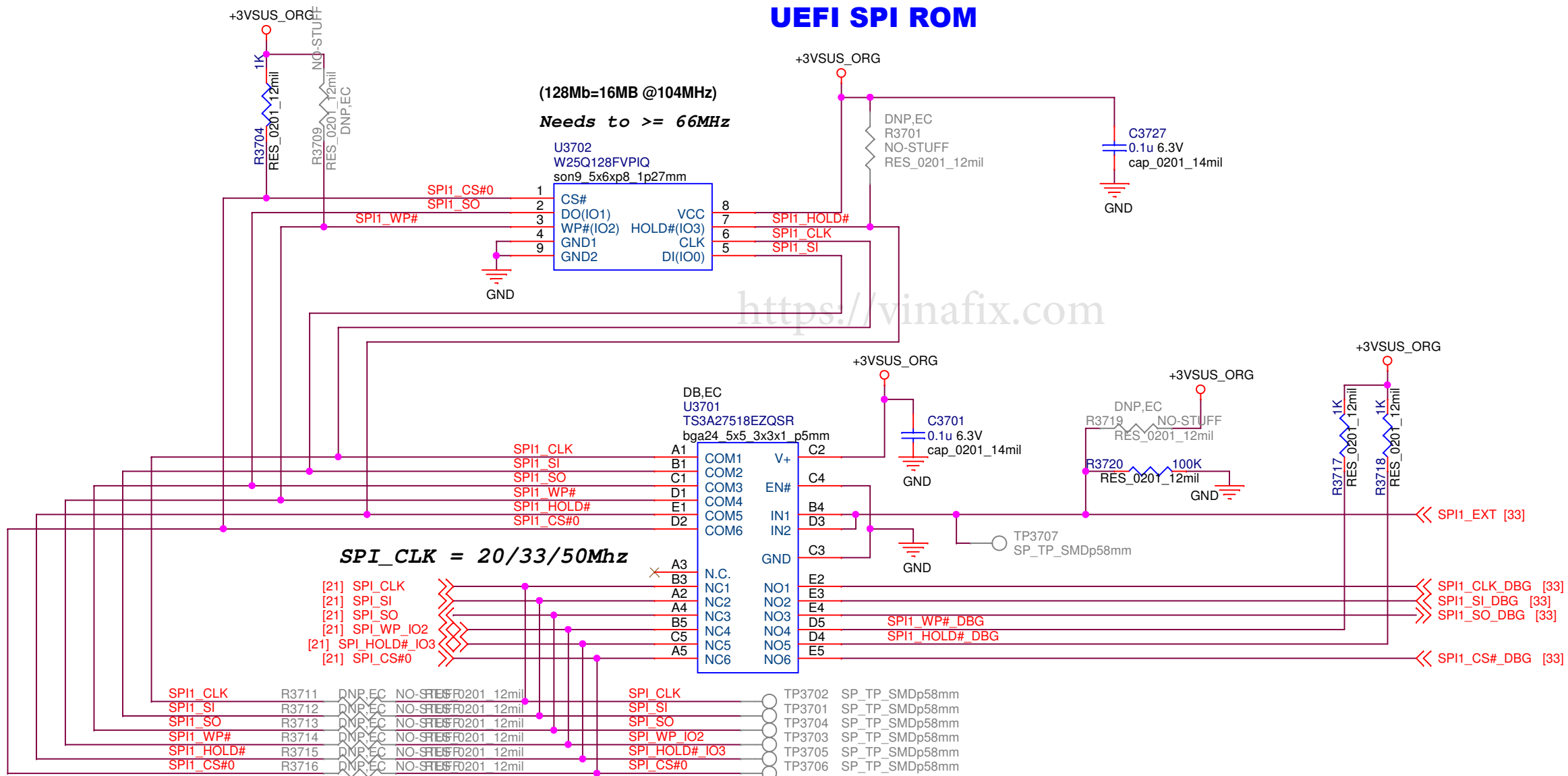
EC SPI ROM

MT 15dec14: CLK <= 80MHz



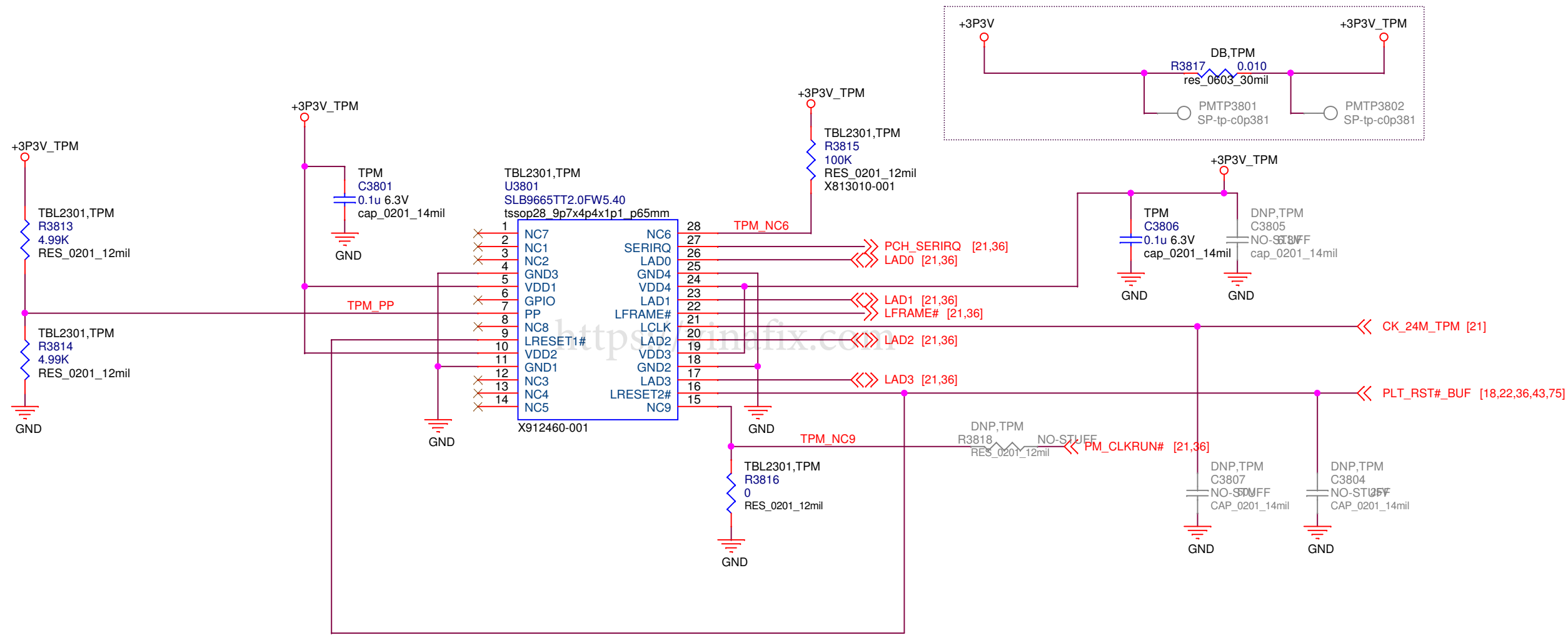
UEFI SPI ROM

(128Mb=16MB @104MHz)
Needs to >= 66MHz



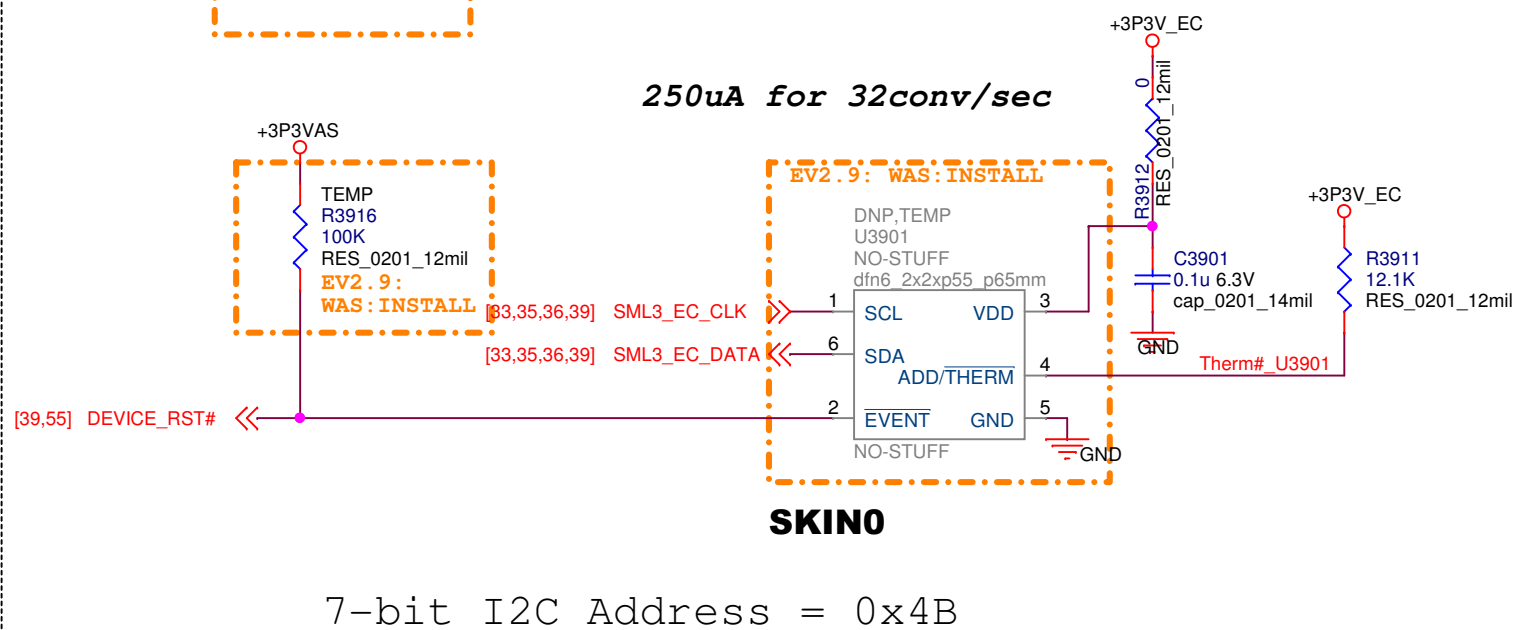
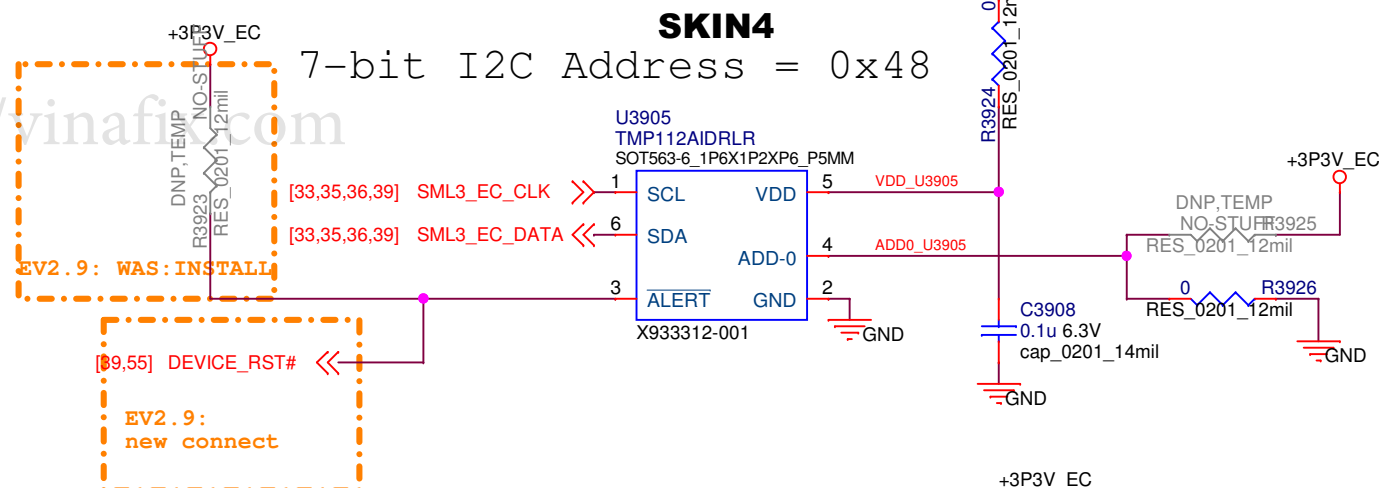
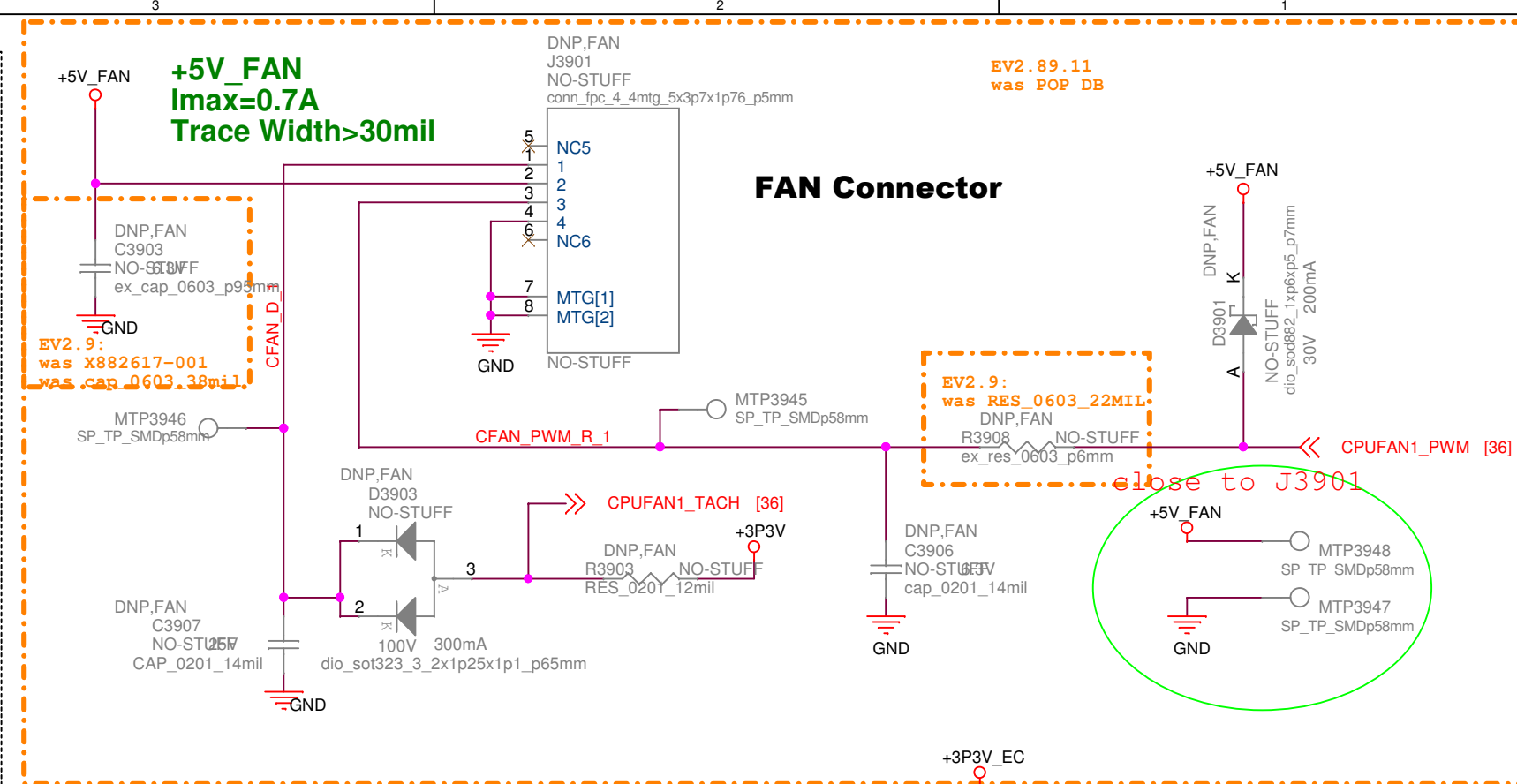
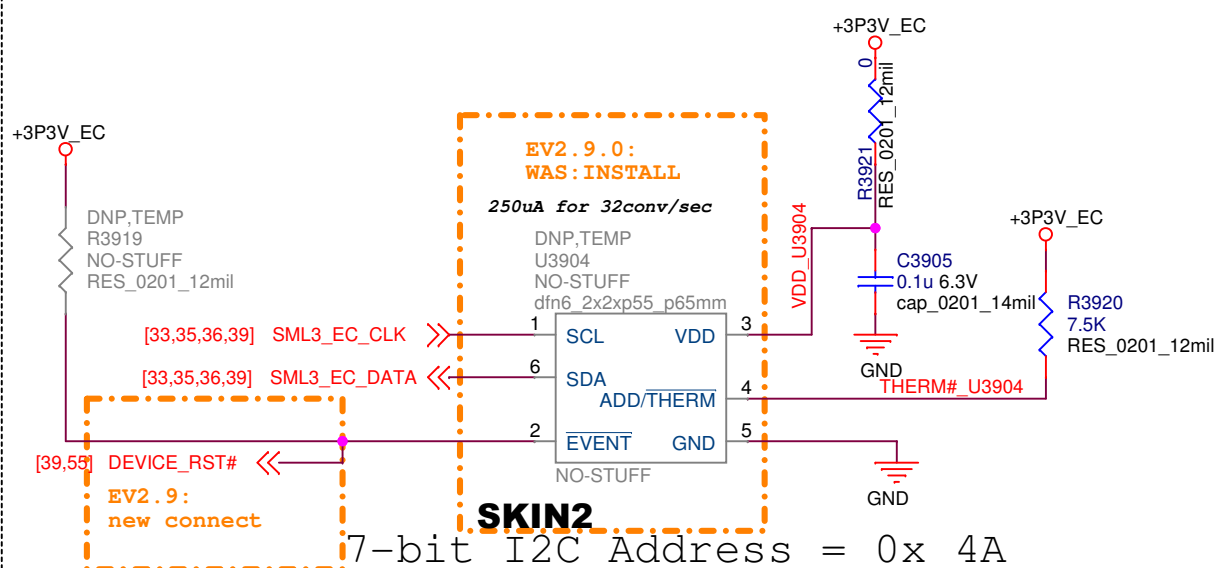
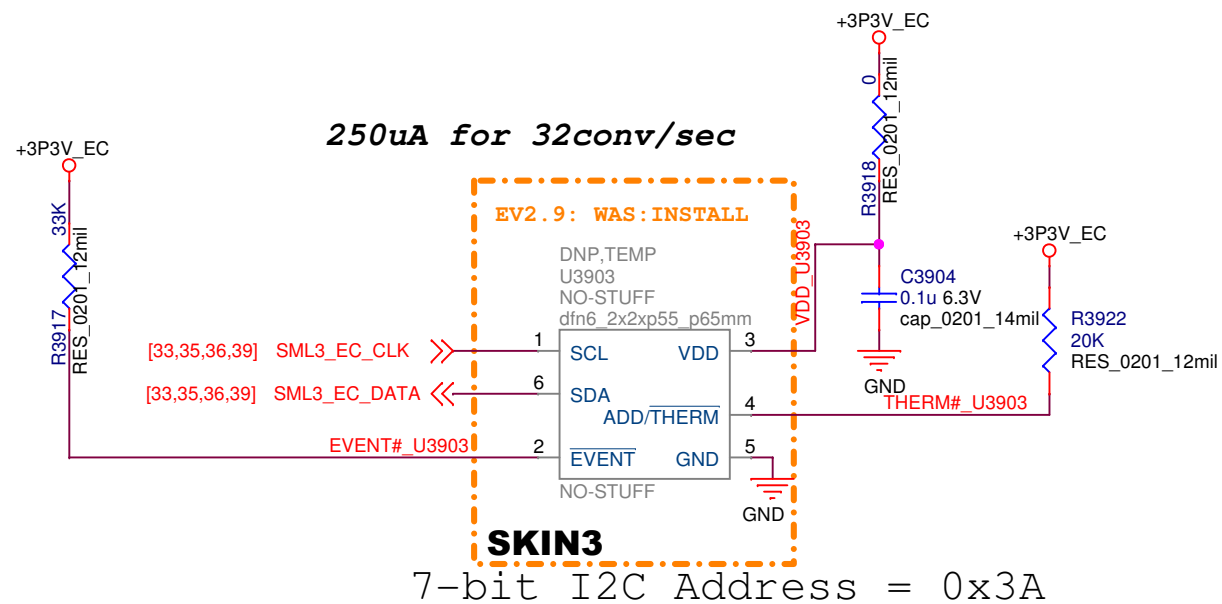
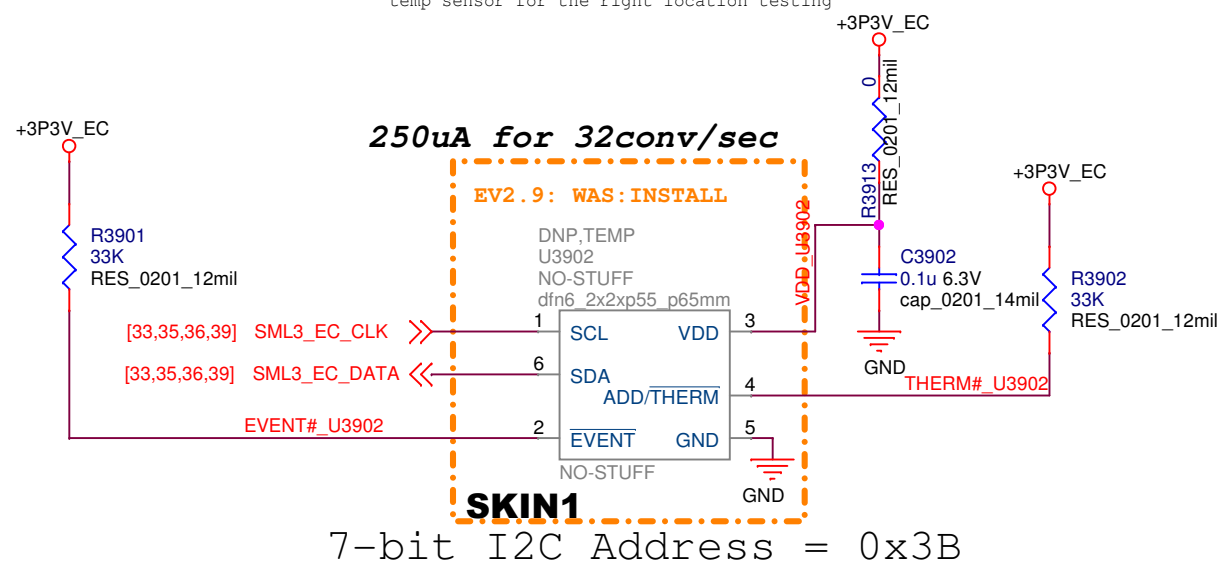
IN1/IN2 = L => COM to NC
IN1/IN2 = H => NC to COM

Trusted Platform Module

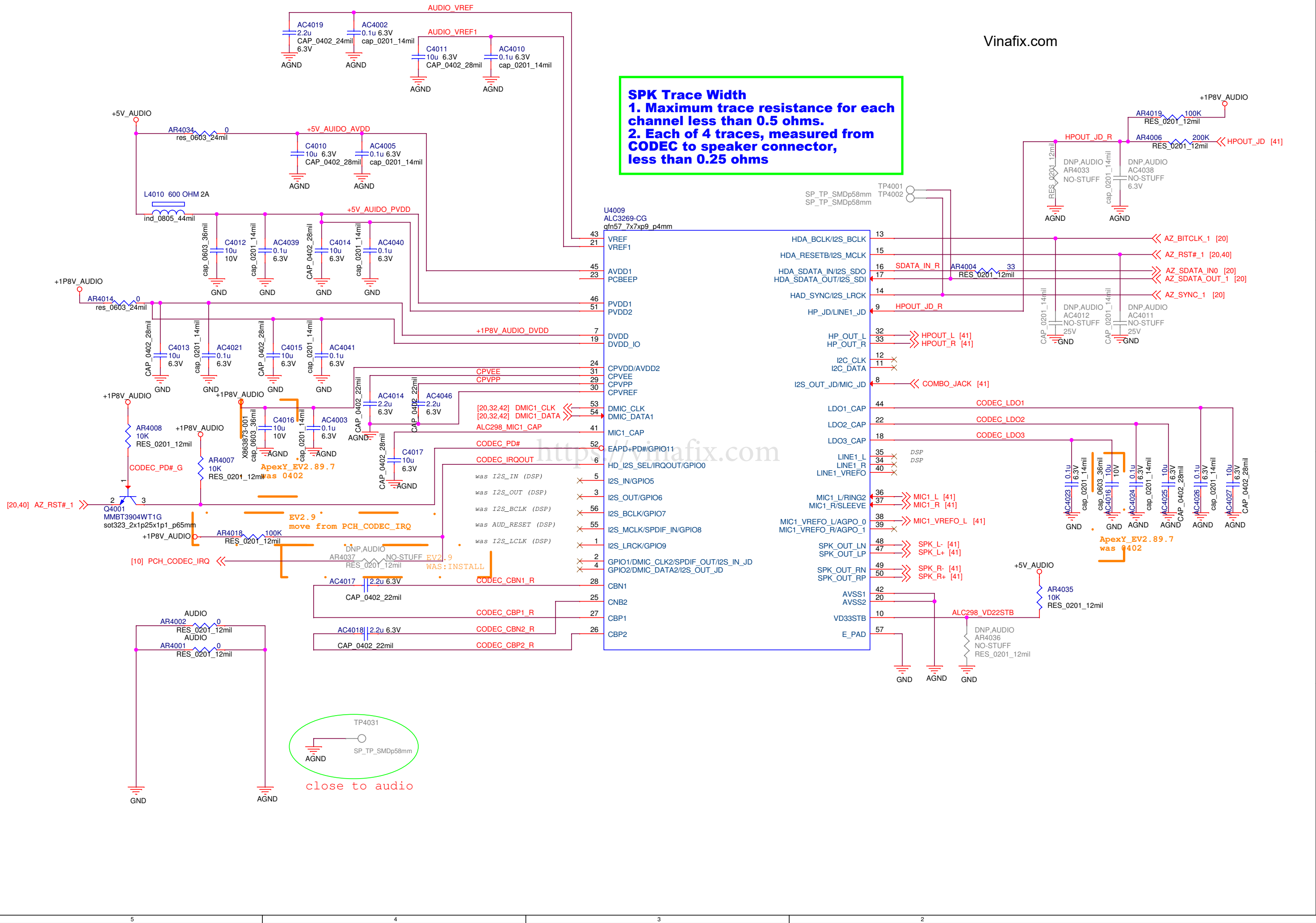


jks 6dec14: Only one sensor will be used for final product

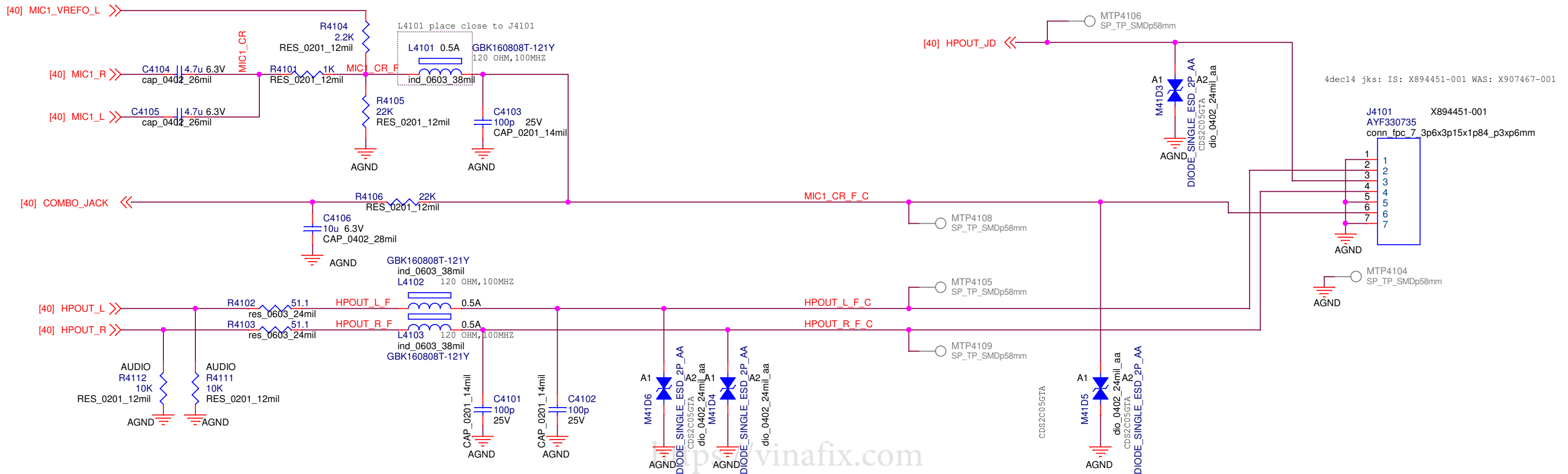
temp sensor for the right location testing



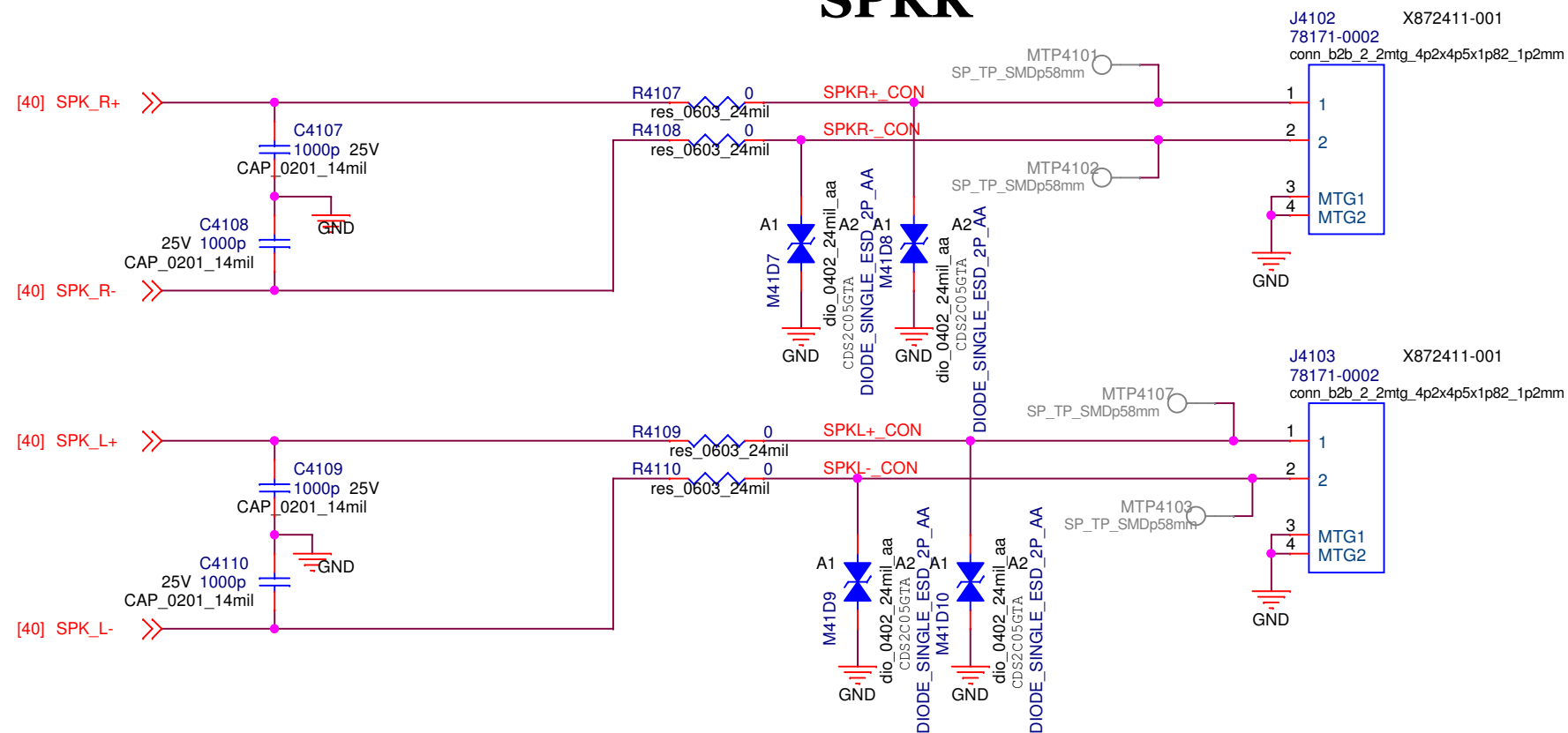
SPK Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

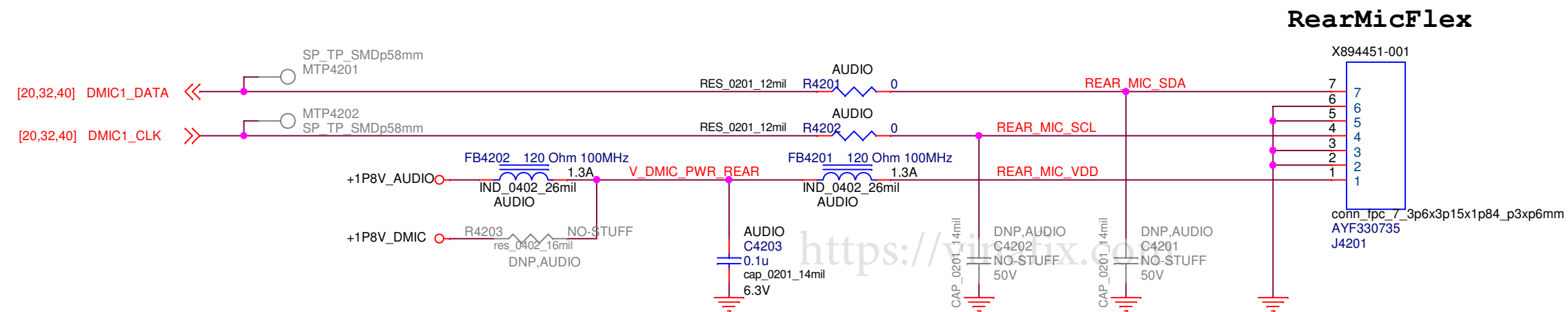


Audio Jack/MIC1 Combo Jack



SPKR







[24] USB3_CONN_RX_DN <<
[24] USB3_CONN_RX_DP <<

[24] USB3_CONN_TX_DN >> C4513 0.1u 6.3V USB3_CONN_TX_C_DN
[24] USB3_CONN_TX_DP >> C4512 0.1u 6.3V USB3_CONN_TX_C_DP

[24] USB2_CONN_DP <<<
[24] USB2_CONN_DN <<<

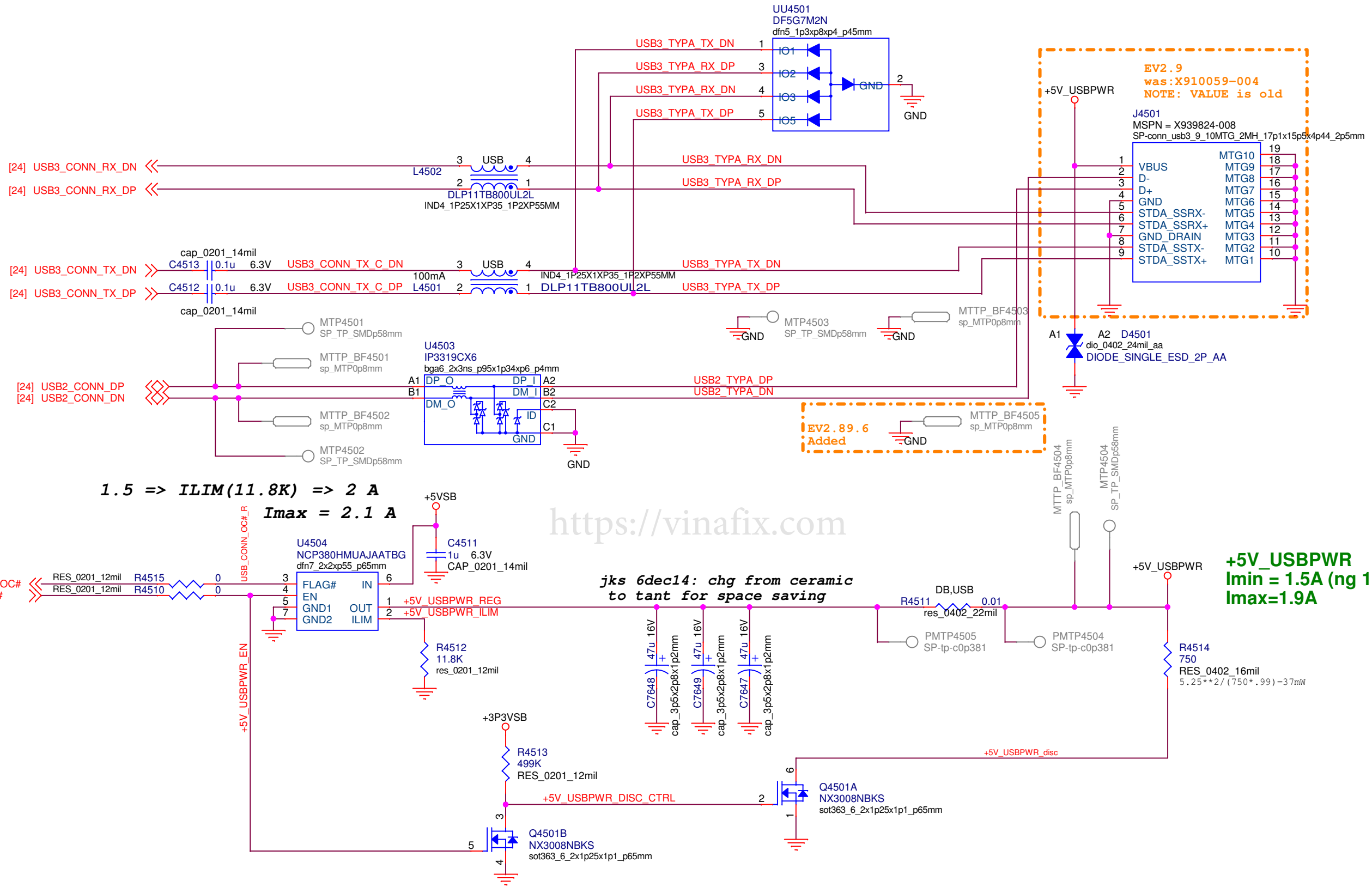
1.5 => ILIM(11.8K) => 2 A
Imax = 2.1 A

[24] USB_CONN_OC# <<<
[36,60,61,62] SUSC_EC# <<<

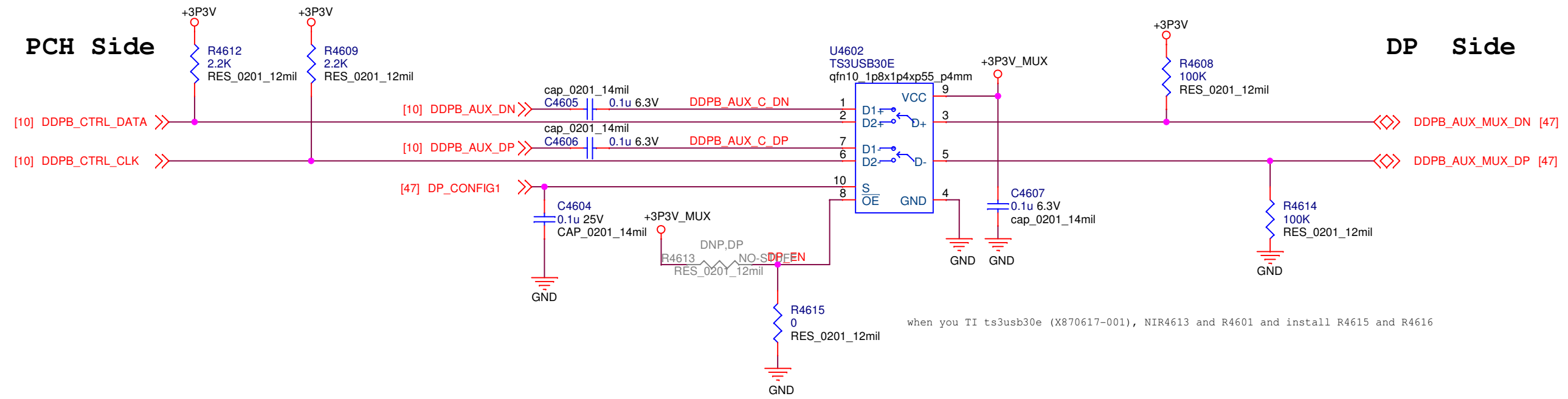
<https://vinafix.com>

jks 6dec14: chg from ceramic
to tant for space saving

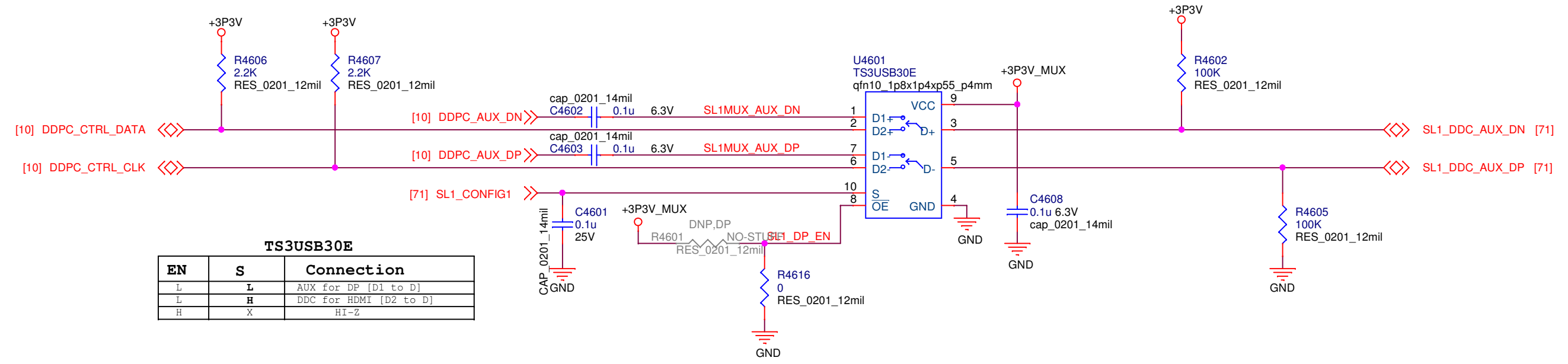
+5V_USB_PWR
Imin = 1.5A (ng 19dec14)
Imax=1.9A

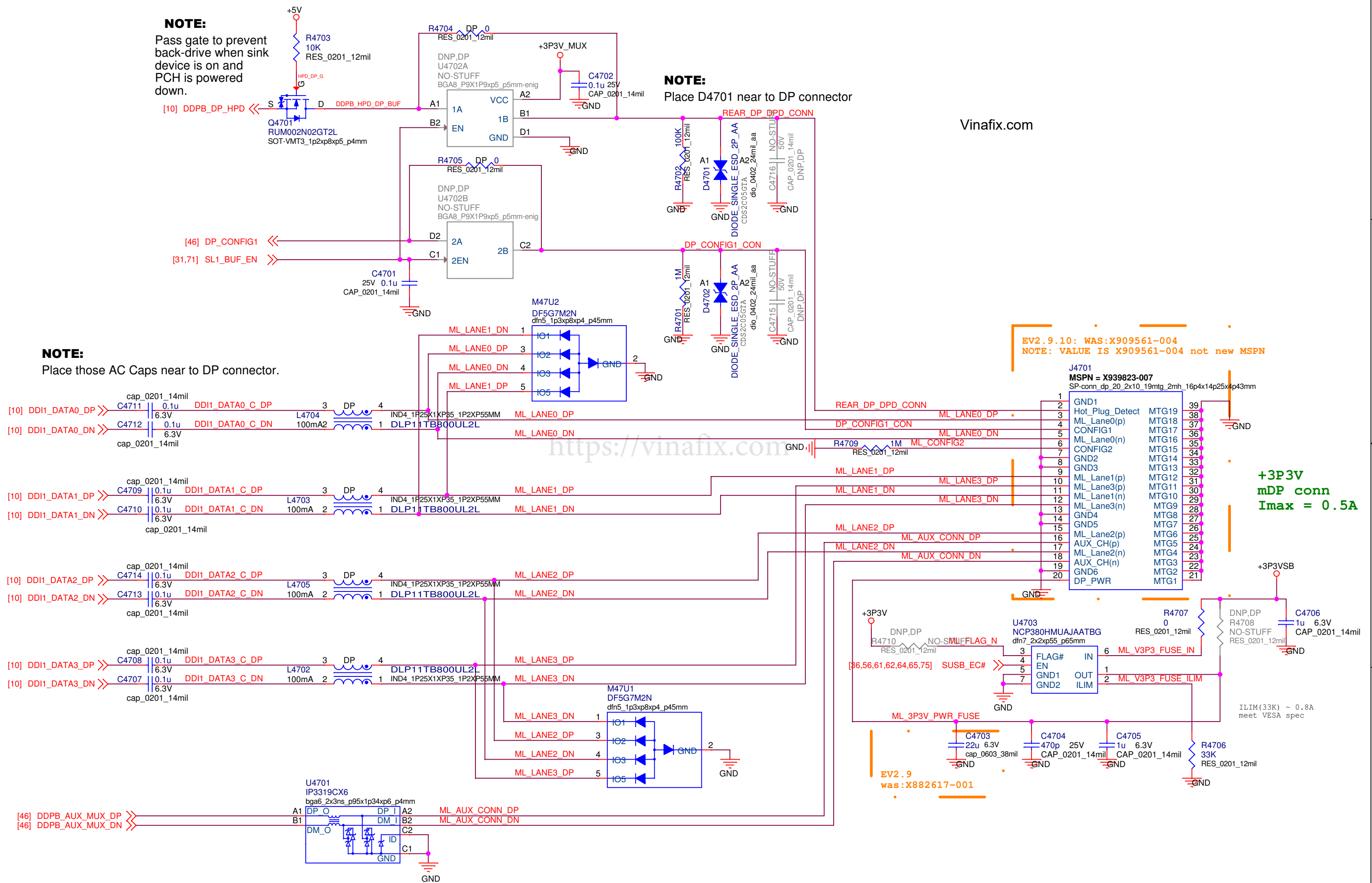


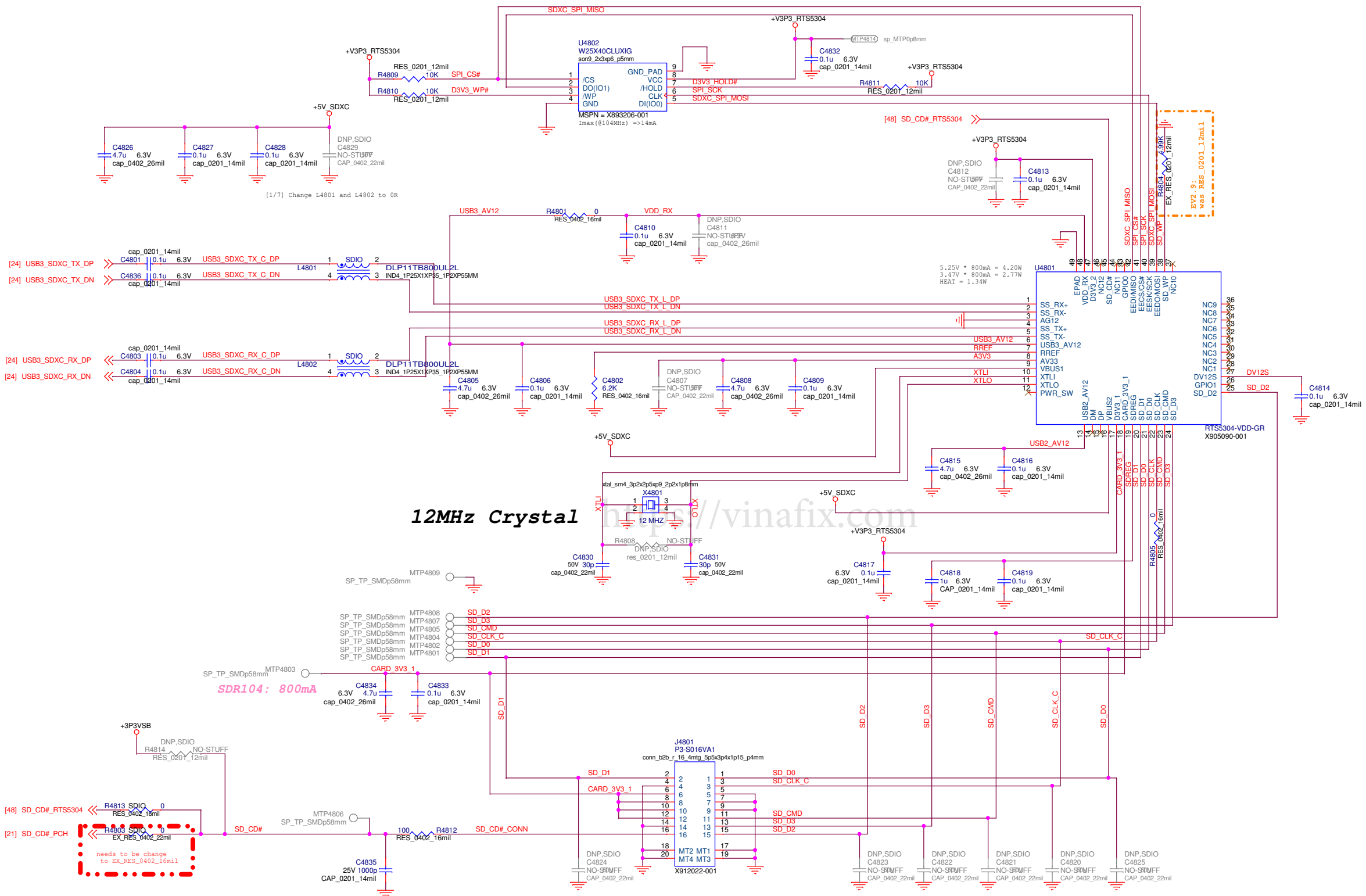
mDP mux to HDMI/DVI Dongle control



SL1 DP mux to HDMI/DVI Dongle control







12MHz Crystal

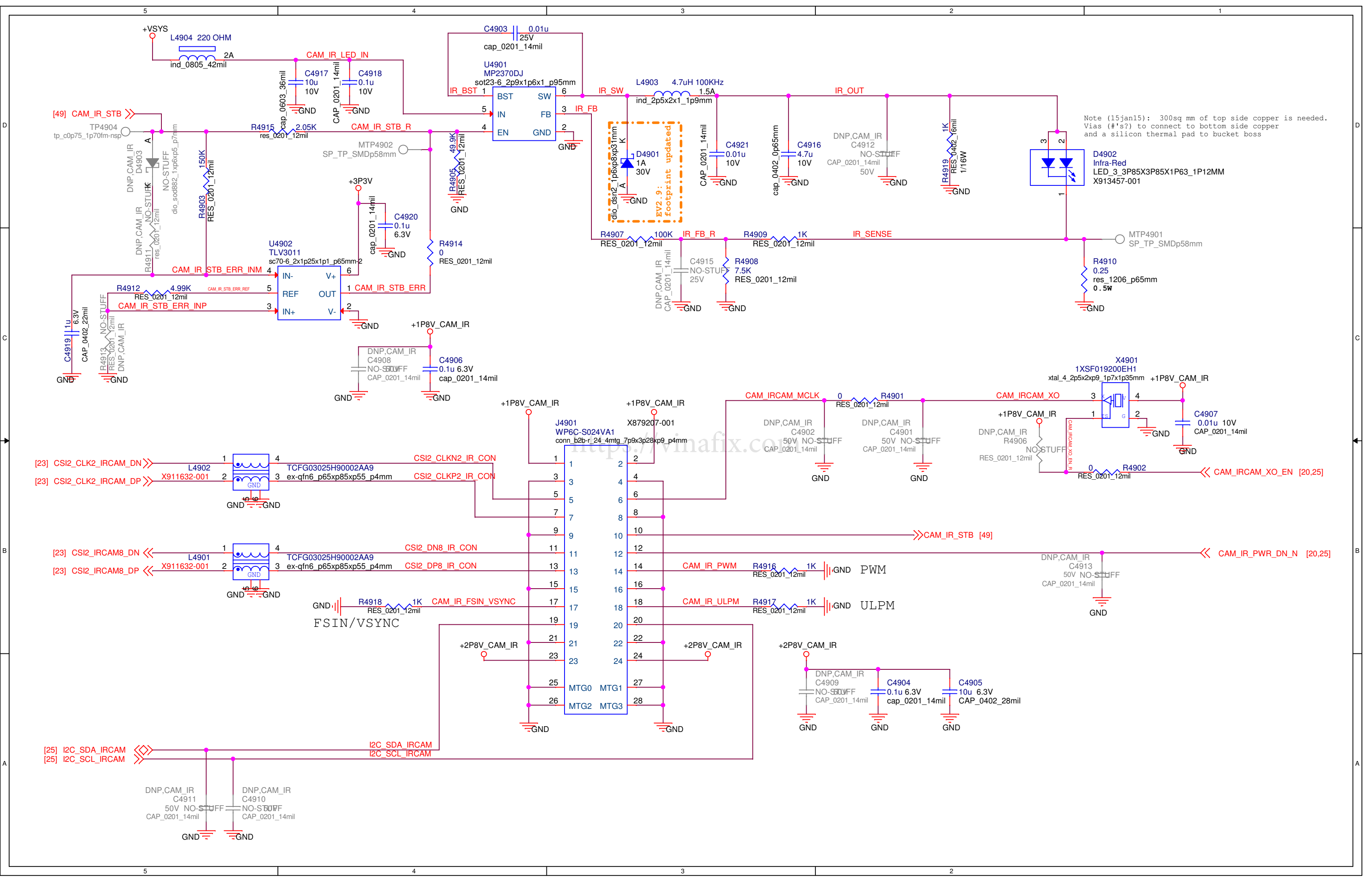
http://vinafix.com

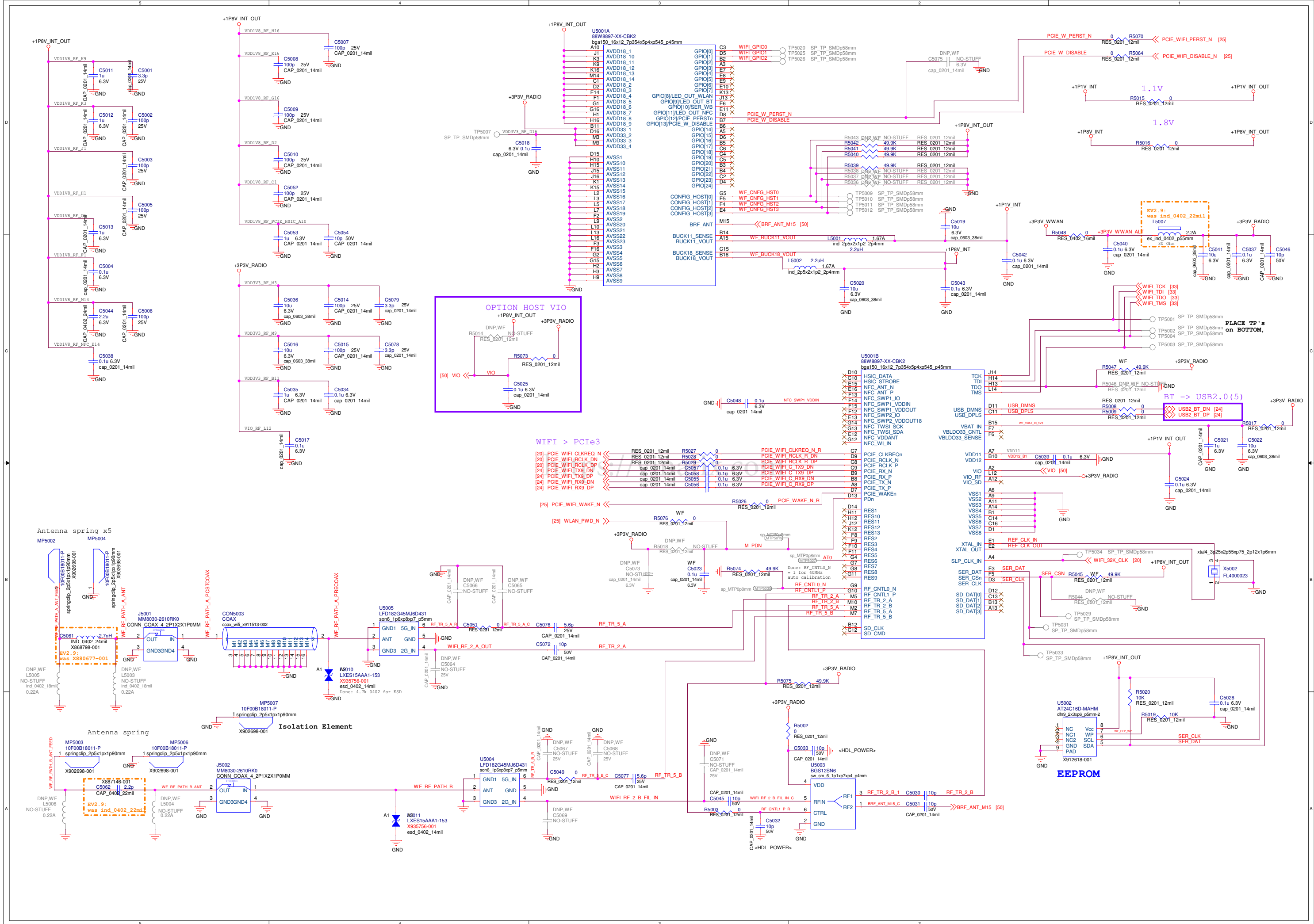
SDR104: 800ma

[48] SD_CD#_RTS5304
[21] SD_CD#_PCH
needs to be change
to EX_RES_0402_16mil

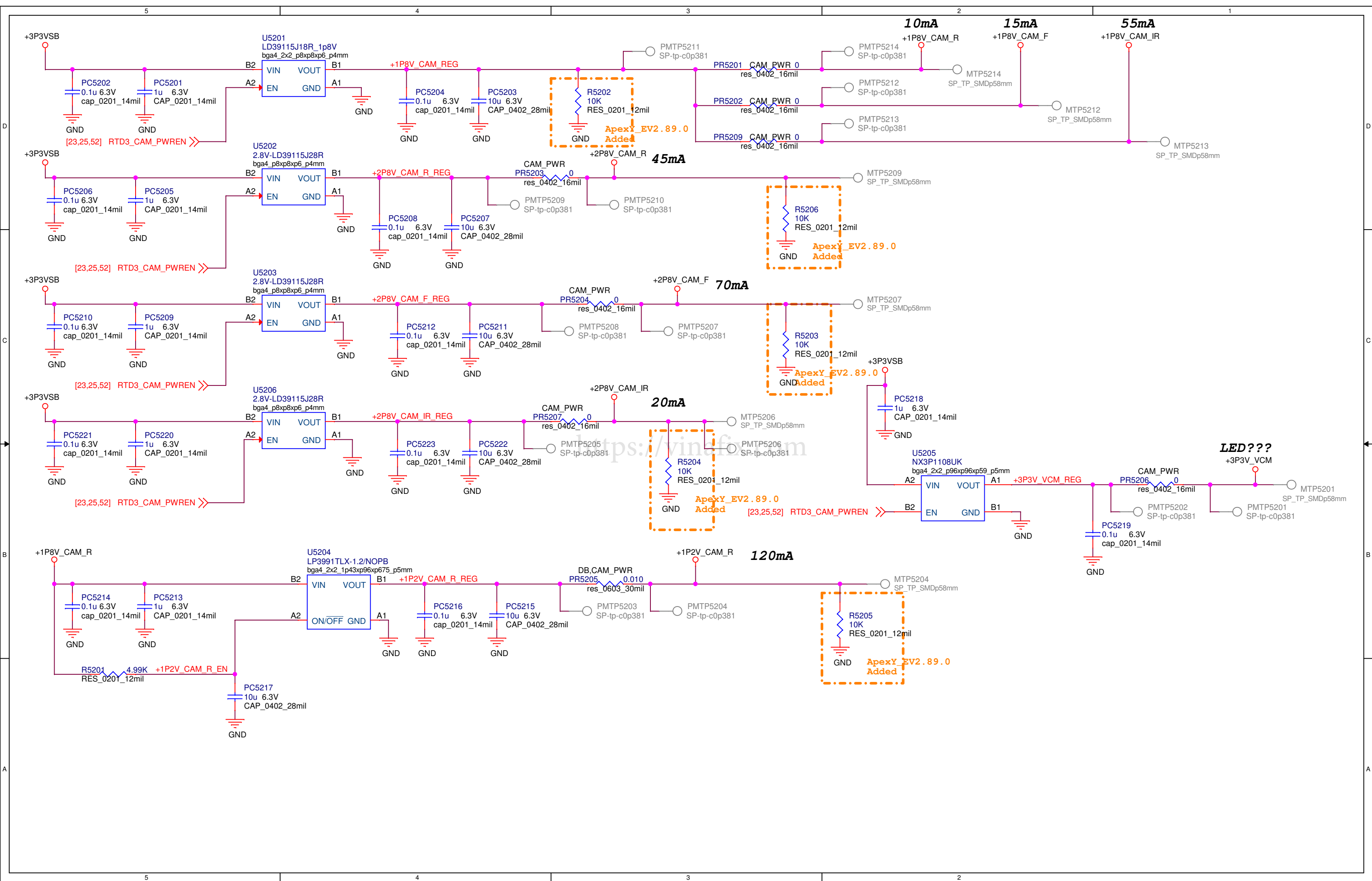
EY2.9:
was RES_0201_12mil1

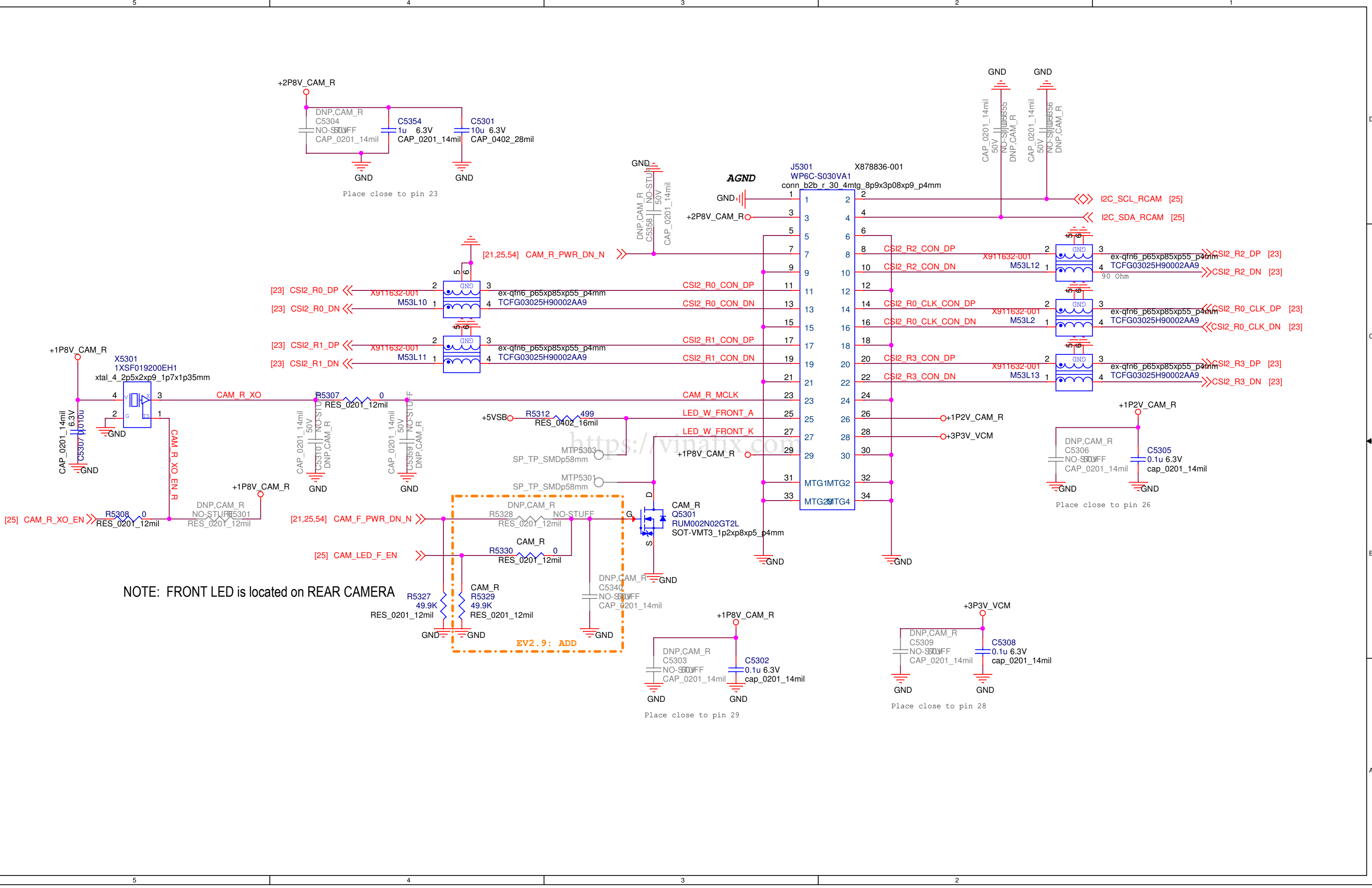
SD_CD#_CONN

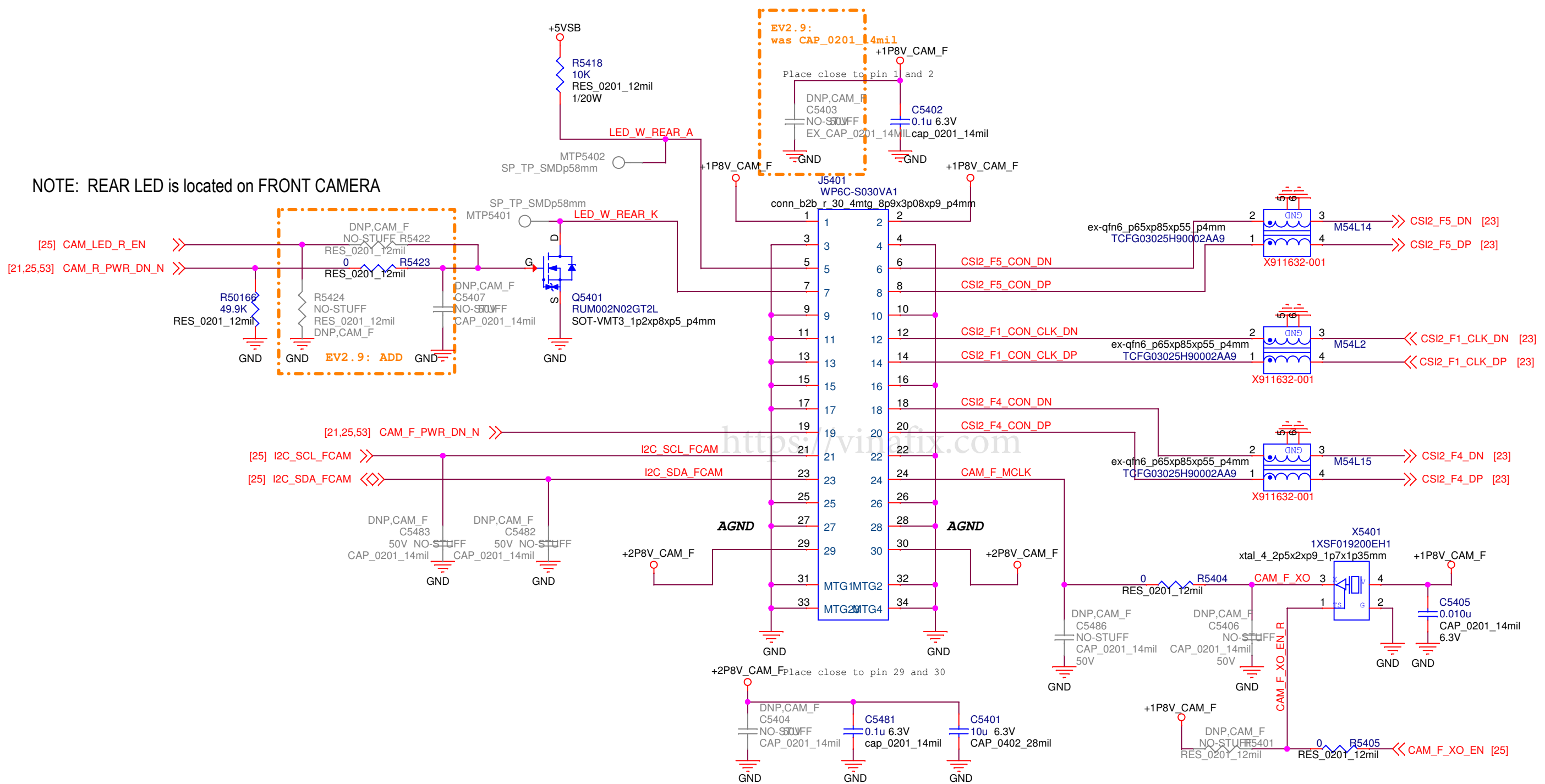


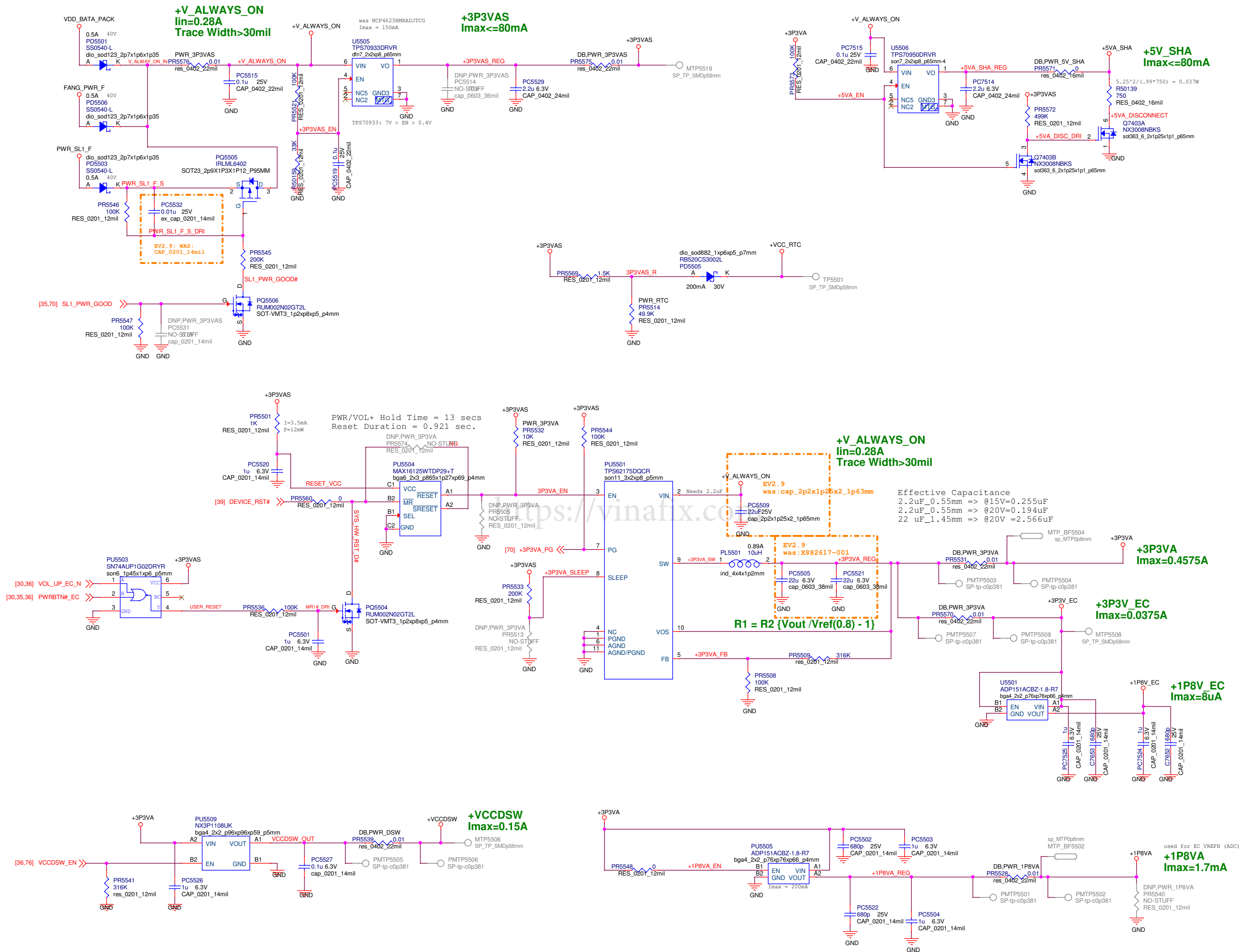


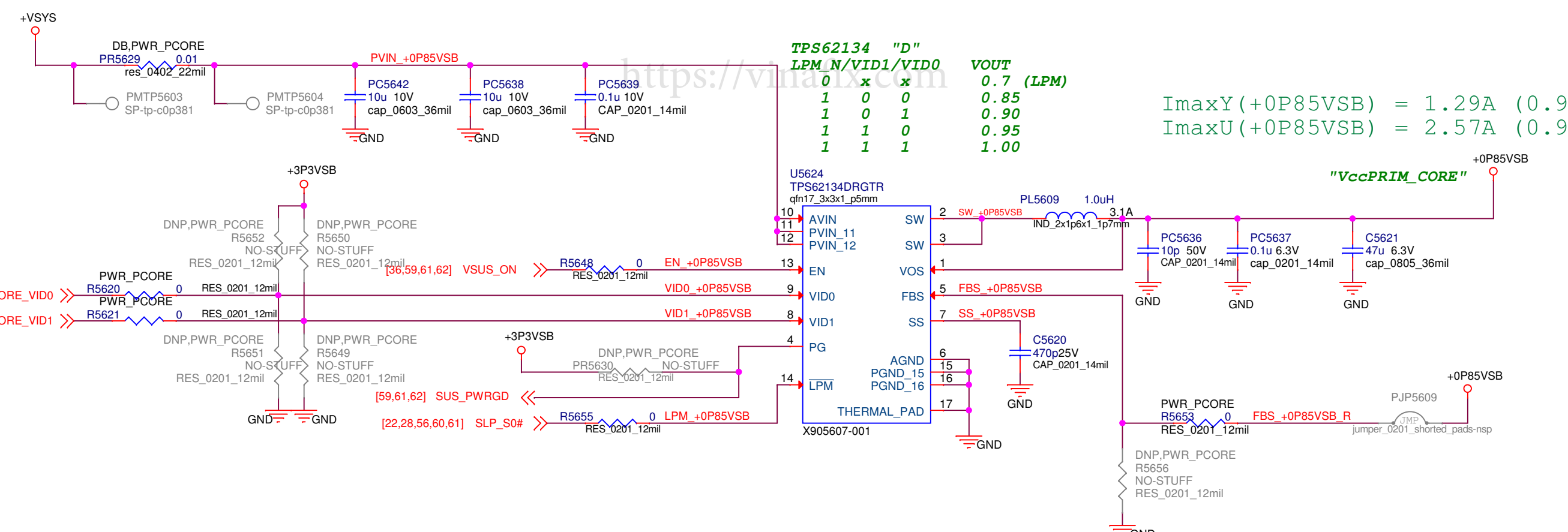
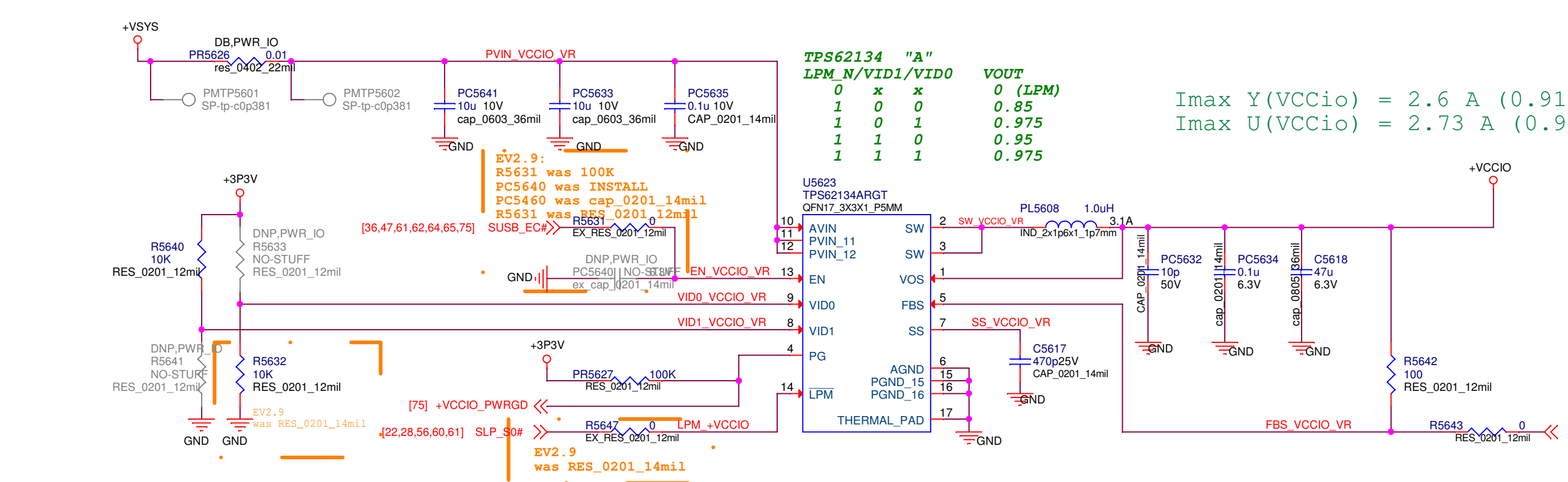
EMPTY
https://vinafix.com

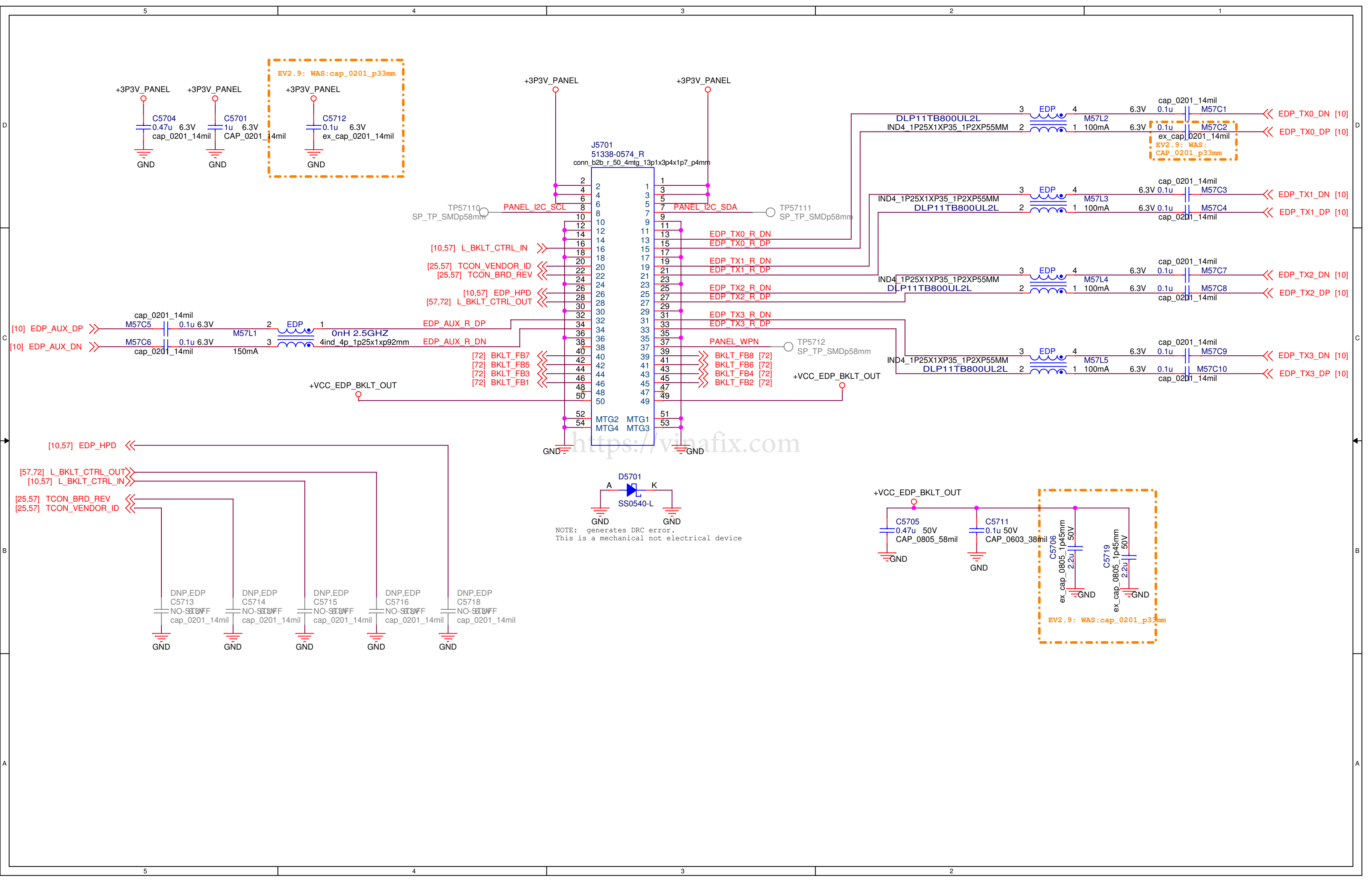




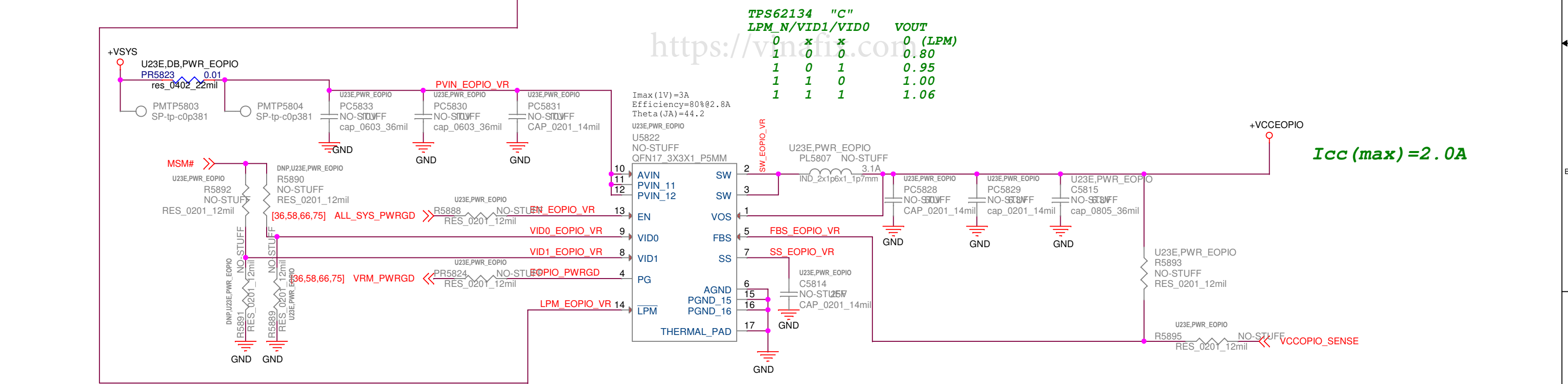
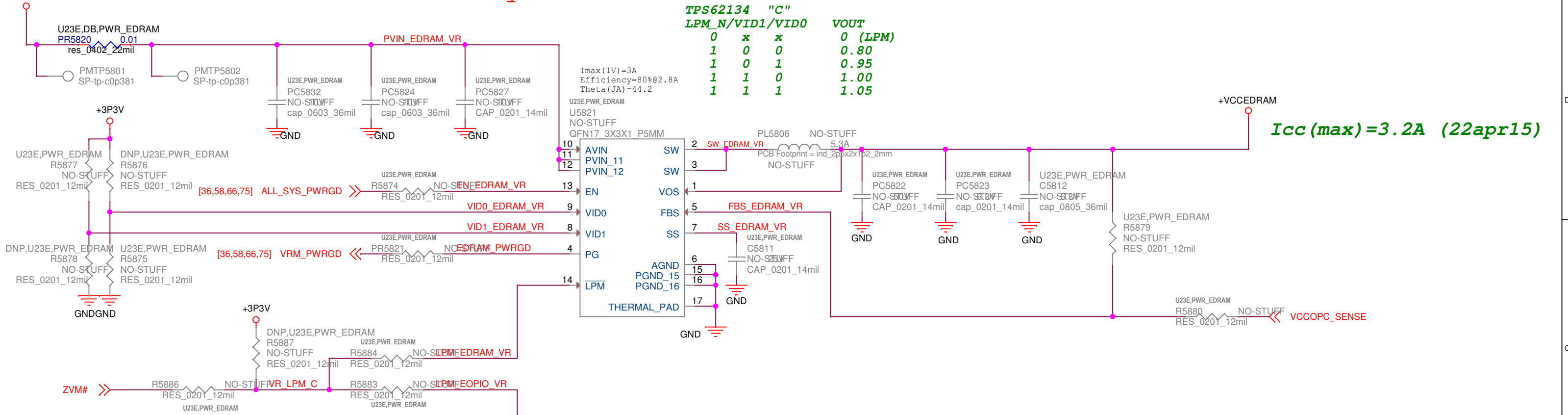








Parts only installed for 23e SKU





EV2.9: Change

Low power mode for Connected Standby

[11,60] DDR_PG_CTRL
[22,28,56,61] SLP_S0#

OCP =12A

Fsw =800kHz

REFIN = FLOAT (1.2V)

Near DDR

[61] S0iX_EN

+VCCPLL_OC
Imax = 0.350A (15Jan15)

Imax Y(+1P2V_DUAL) = 4.5/3.5 A (0.91 PPDG)
Imax U(+1P2V_DUAL) = 4.5/3.5 A (0.91 PPDG)

+1P2V_DUAL
Imax = 7.950A (15Jan15)
TDC = 3.5A

Imax Y(+V_VDDQ_VTT) = 0.6 A (0.91 PPDG)
Imax U(+V_VDDQ_VTT) = 0.6 A (0.91 PPDG)

+V_VDDQ_VTT
Imax=1A
Trace Width>40mil

+V_VDDQ_VTT
Imax = 0.600A (15Jan15)

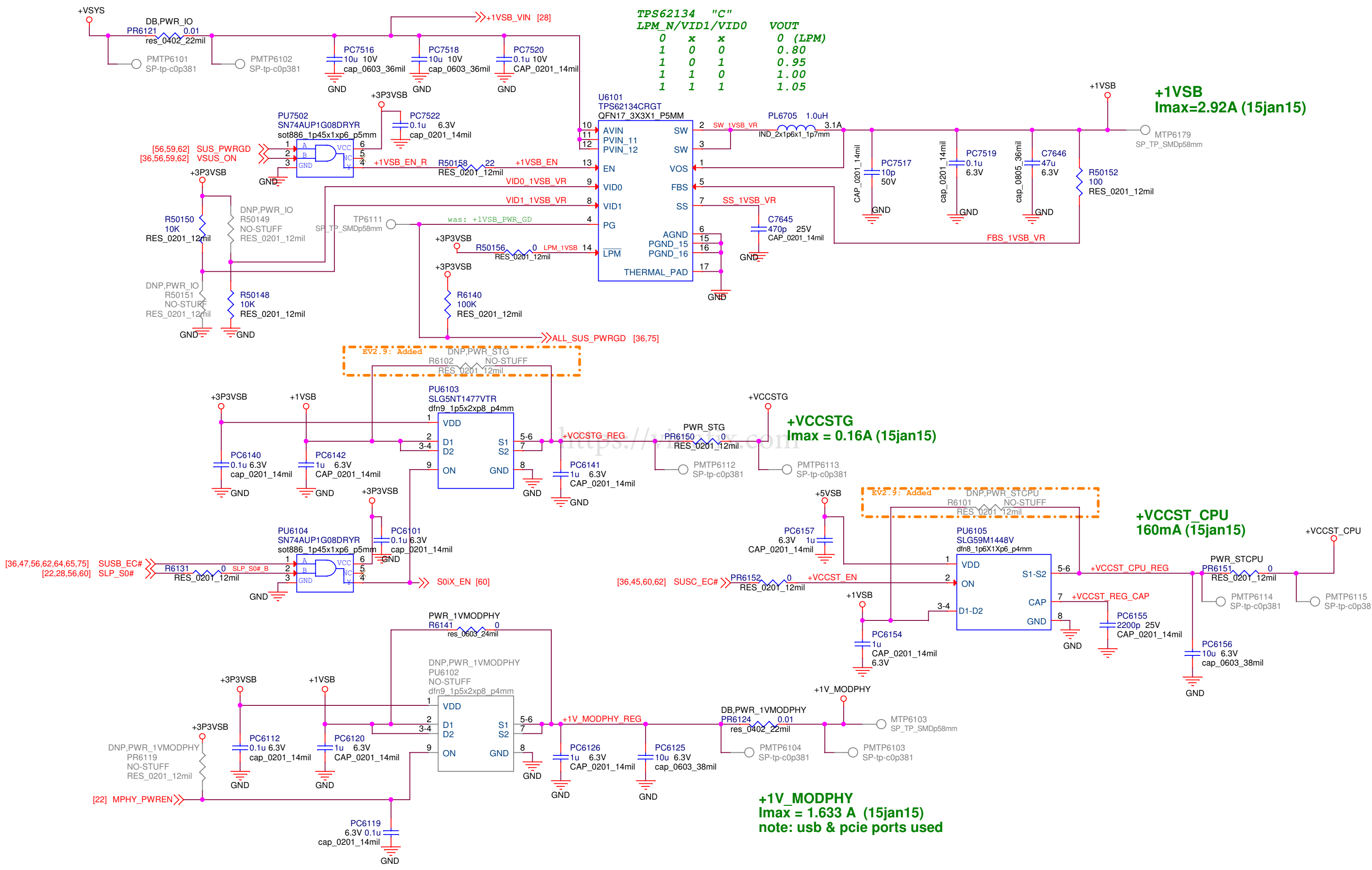
EV2.9: ADD

[22,33,36] PM_SUSC#
[36,45,60,61,62] SUSC_EC#

[36,45,60,61,62] SUSC_EC#

SUSC_EC#_AND [60]

+VSYS
lin=1.7A
Trace Width>80mil



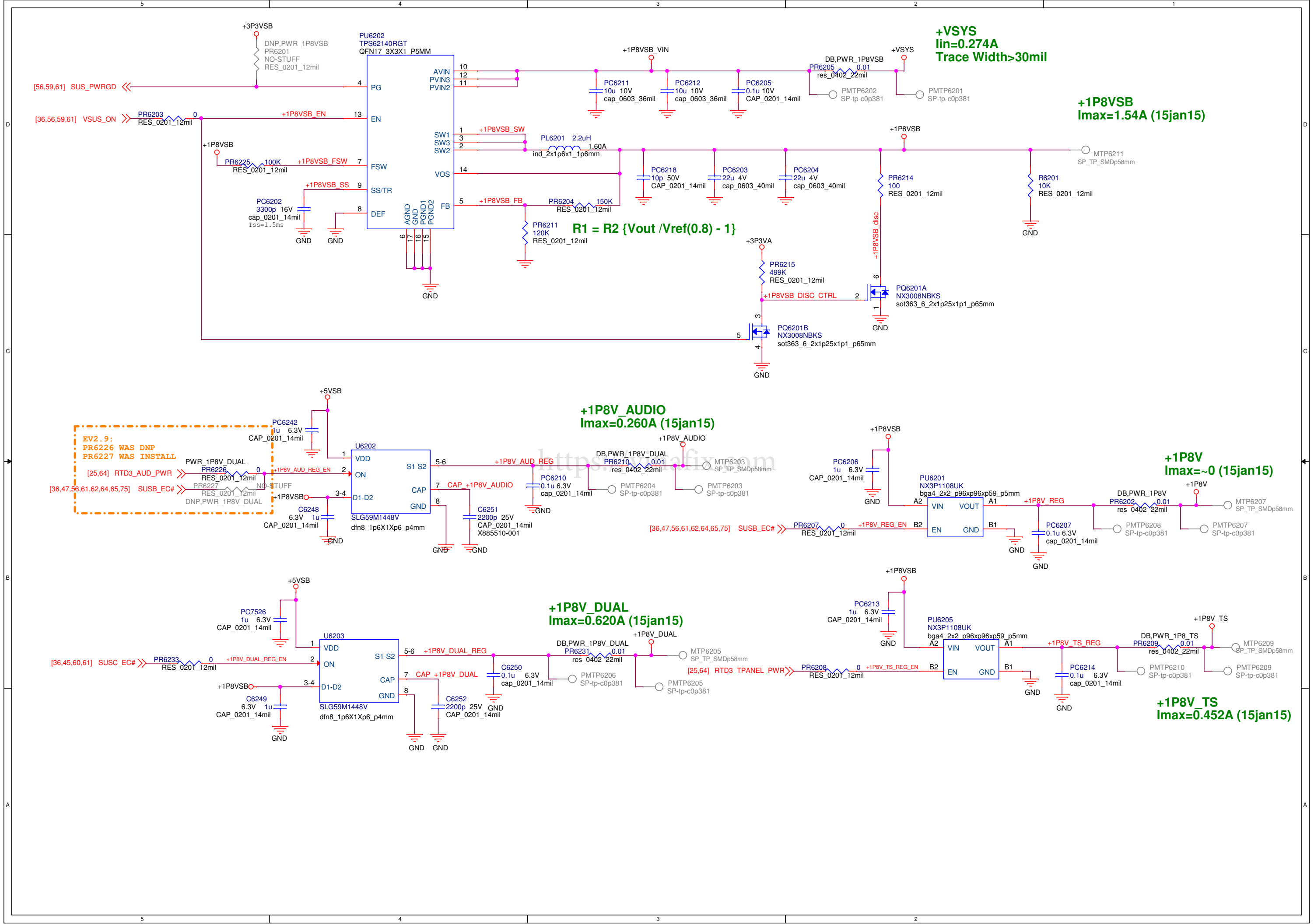
TPS62134 "C"				
LPM_N/VID1/VID0				VOUT
0	x	x		0 (LPM)
1	0	0		0.80
1	0	1		0.95
1	1	0		1.00
1	1	1		1.05

+1VSB
I_{max}=2.92A (15jan15)

+VCCSTG
I_{max} = 0.16A (15jan15)

+VCCSTG_CPU
160mA (15jan15)

+1V_MODPHY
I_{max} = 1.633 A (15jan15)
note: usb & pcie ports used



$C_{gs} \geq 40 \cdot C_{gd}$
 $C_{gs} \cdot 0.9 \geq 40 \cdot C_{gd} \cdot 1.1$
 $C_{gs} \geq (1.1/0.9) \cdot 40 \cdot 1nF$
 $C_{gs} \geq 49nF$

CHGR_VIN
 $I_{in} = 9.731A$
 Trace Width > 389mil

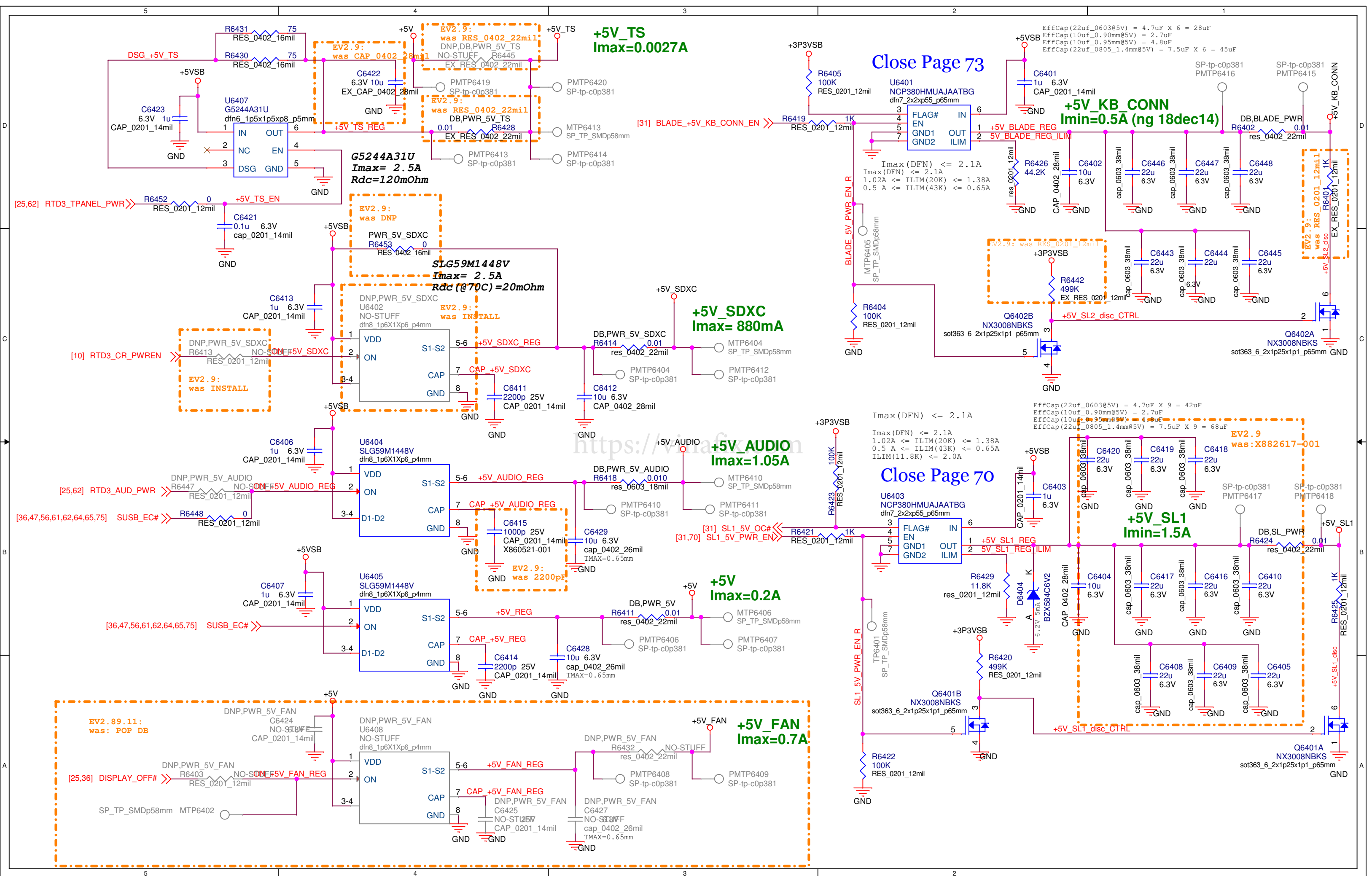
+SYS
 $I_{in} = 8A$
 Trace Width > 320mil

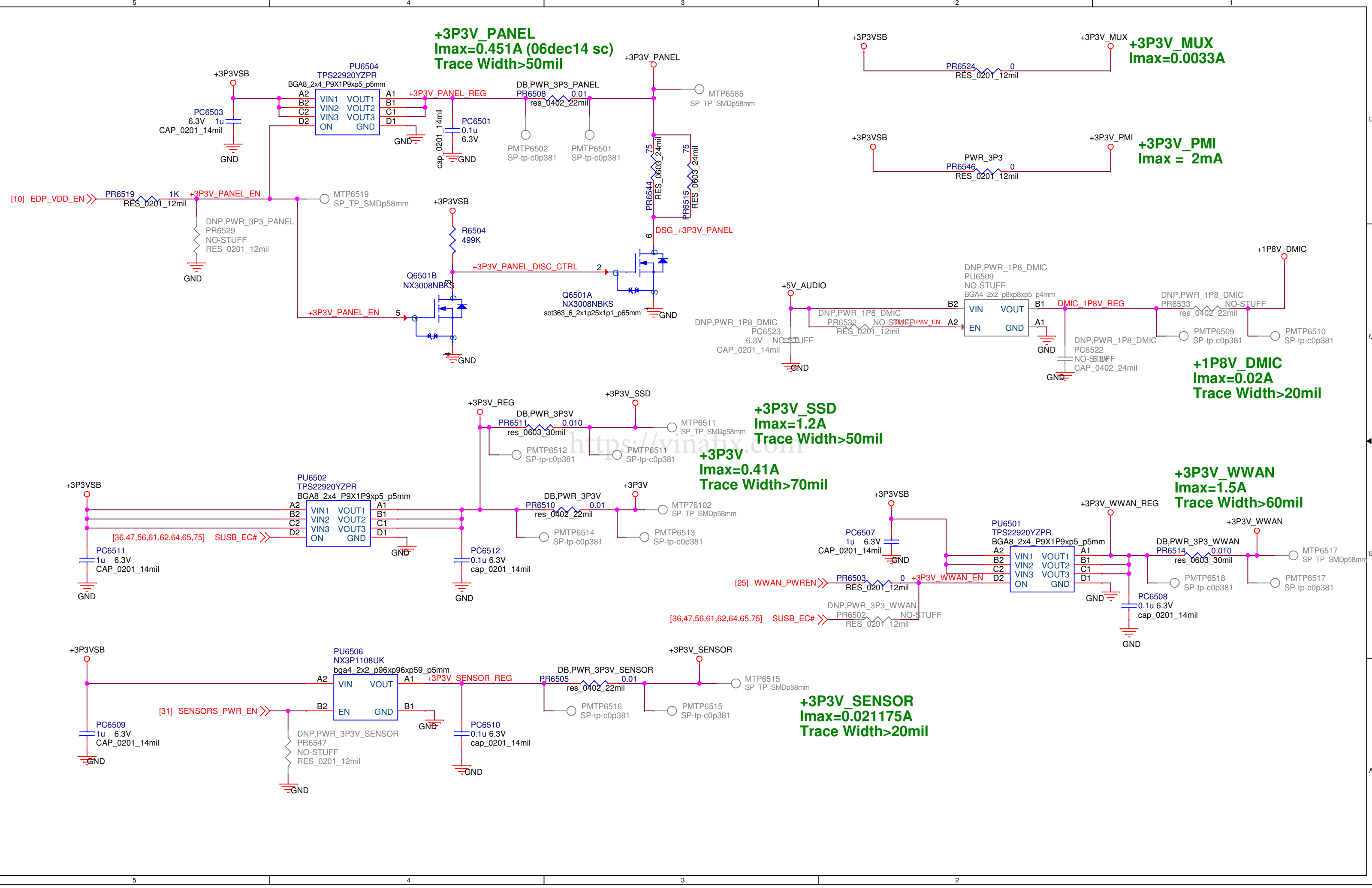
+SYS
 $I_{max} = 12.0A$
 $TDC = 10.0A$

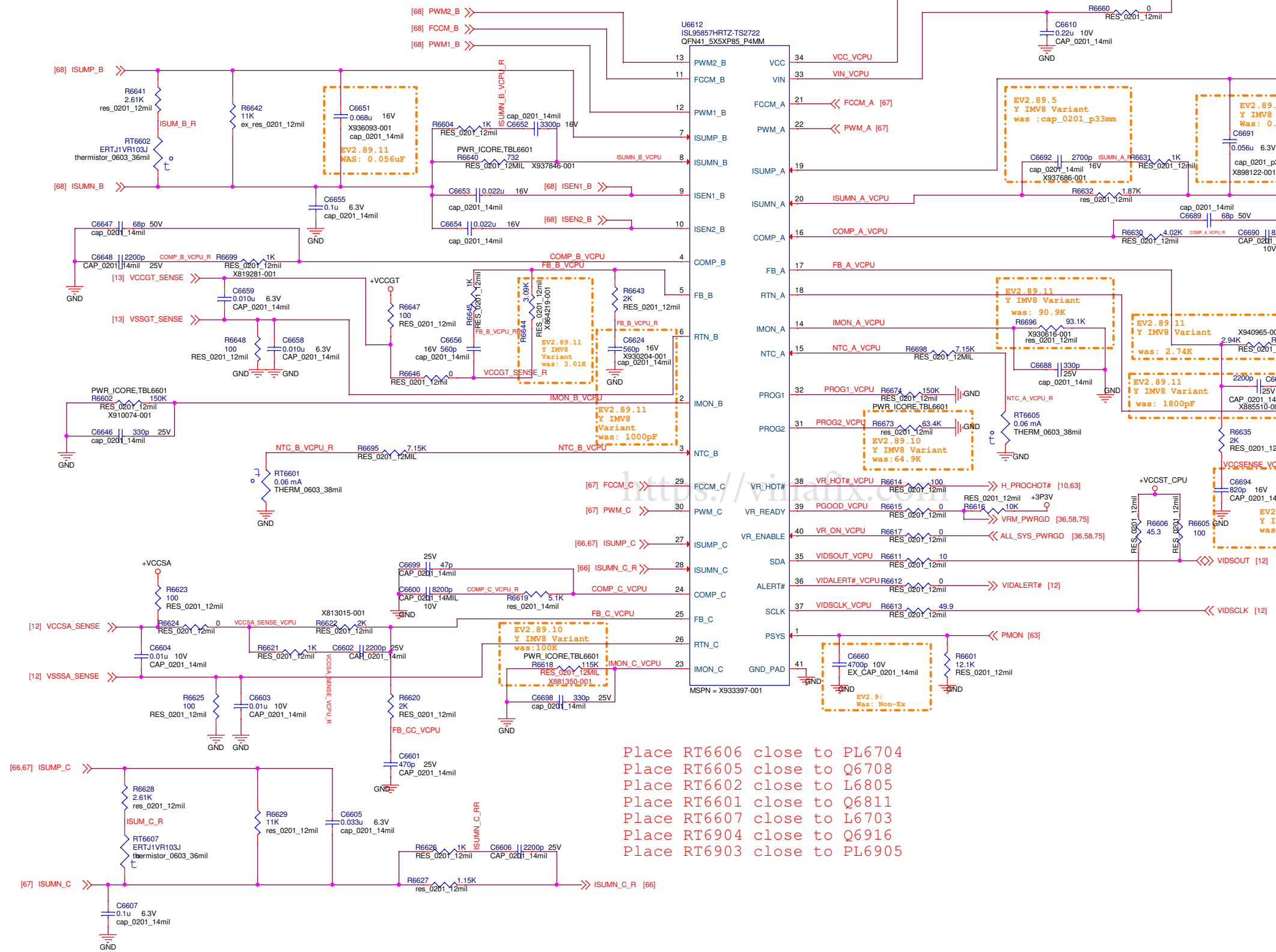
CHGR needs 200uF for loop stability
 $\{2 \cdot f \cdot \pi = 1/\sqrt{L \cdot C}\}$

$EffCap@20V = 3.22uF \cdot 3 = 9.66uF$

$I(ripple) = V_{in} \cdot DutyCycle \cdot (1 - DutyCycle) / (FreqSwitch \cdot L)$
 $I(ripple) = 20\% - 40\% I(charge)$
 $V_{in}(12.6V \pm 10\%) \Rightarrow I(ripple)@2.2uH \Rightarrow 1.93A, 40.5\%$
 $V_{in}(12.6V \pm 10\%) \Rightarrow I(ripple)@3.3uH \Rightarrow 1.29A, 27.0\%$
 assuming 60W, DutyCycle=0.5, Freq=1020KHz

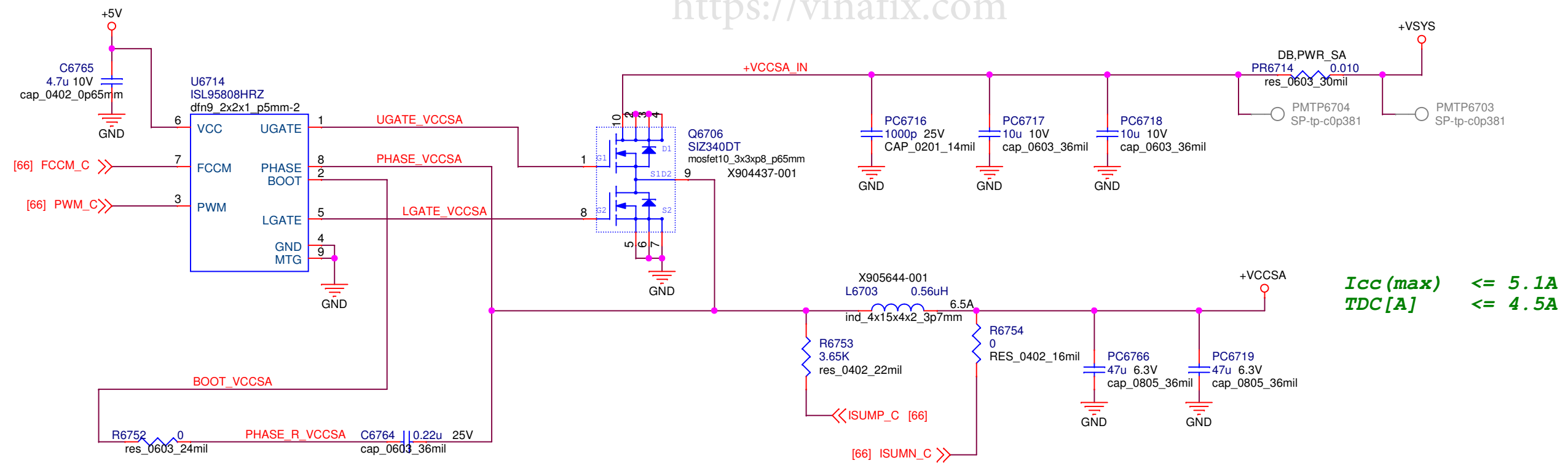
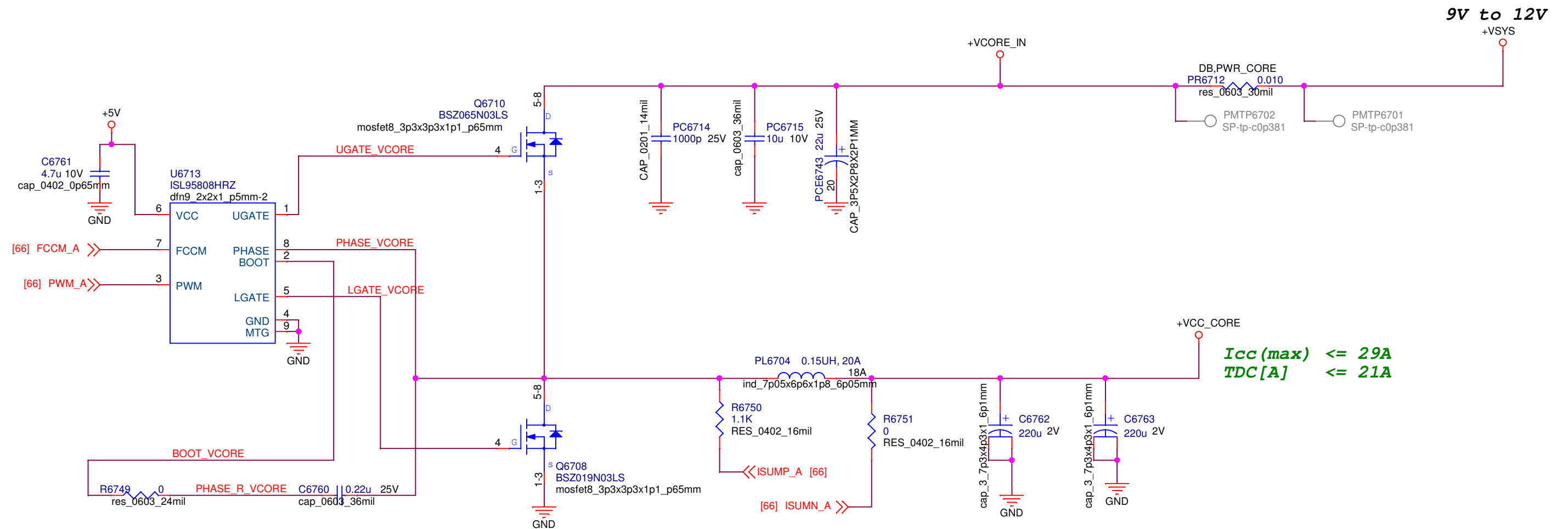


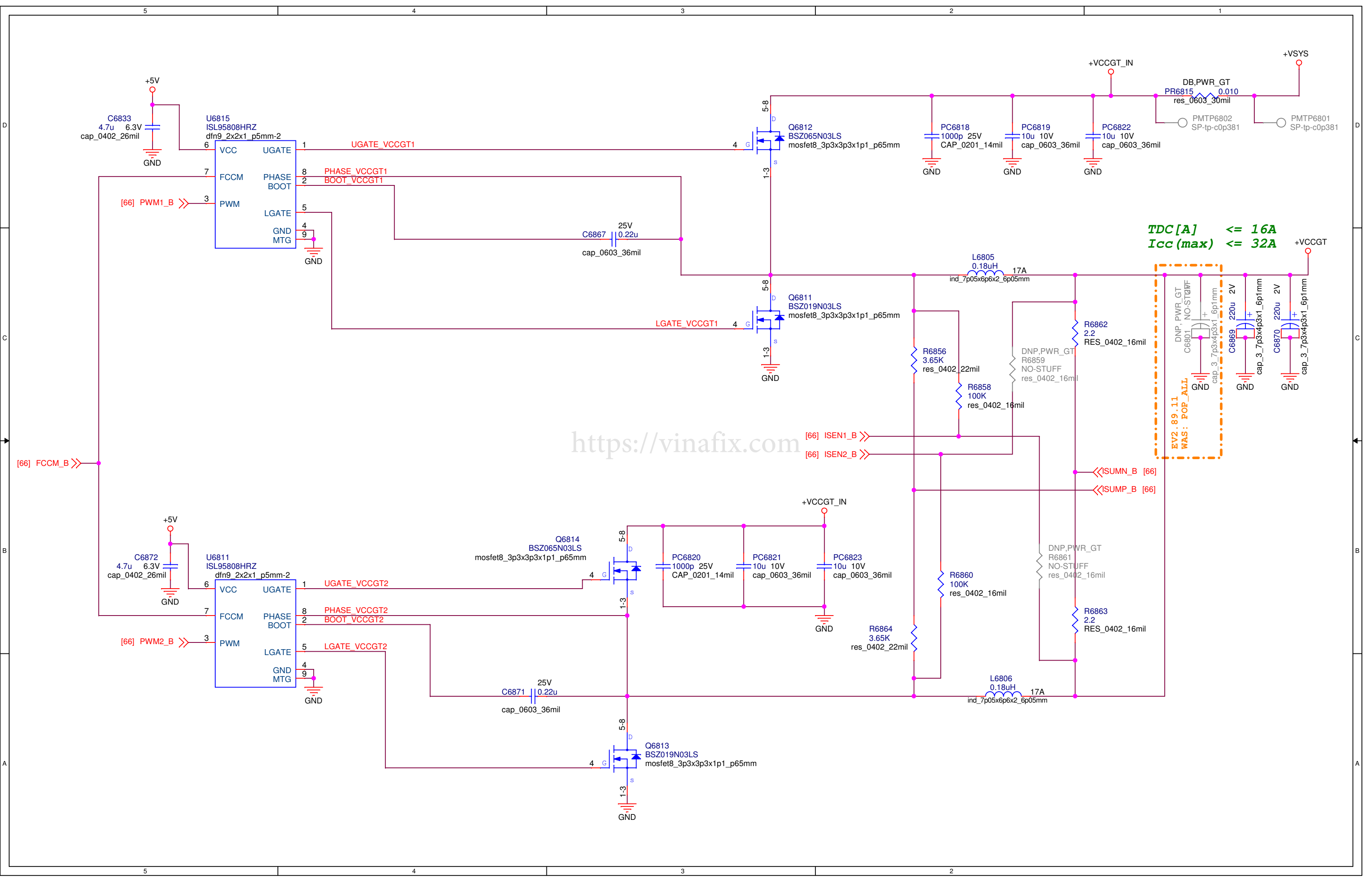


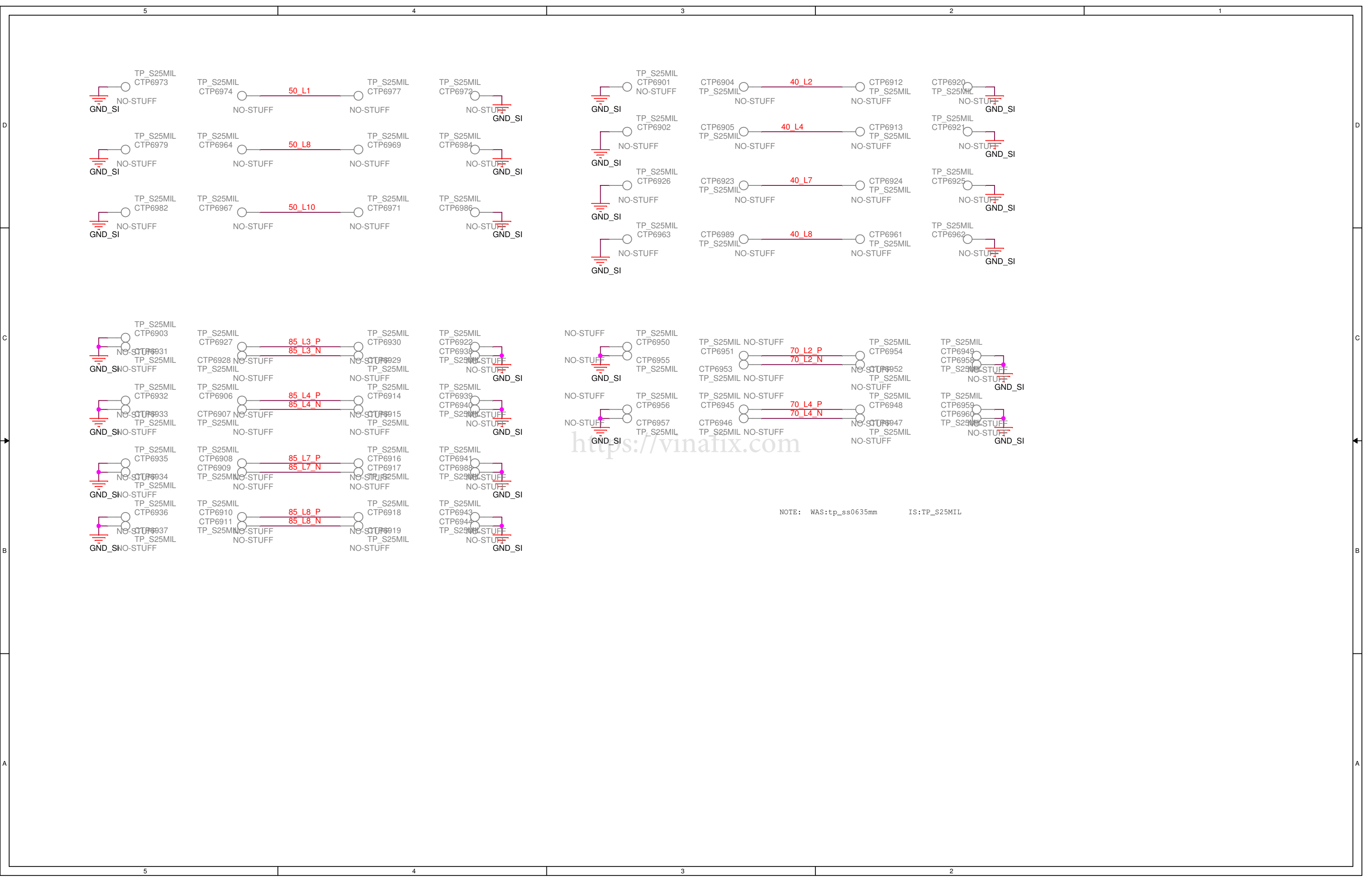


Place RT6606 close to PL6704
Place RT6605 close to Q6708
Place RT6602 close to L6805
Place RT6601 close to Q6811
Place RT6607 close to L6703
Place RT6904 close to Q6916
Place RT6903 close to PL6905

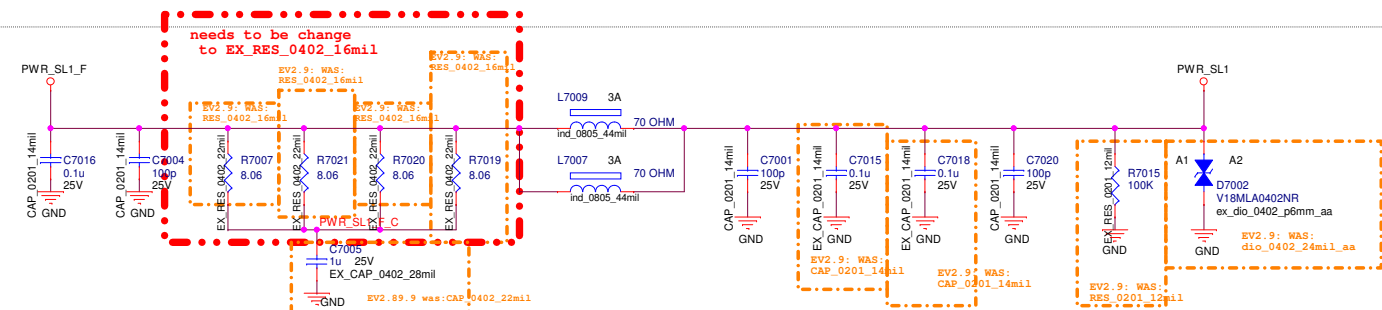
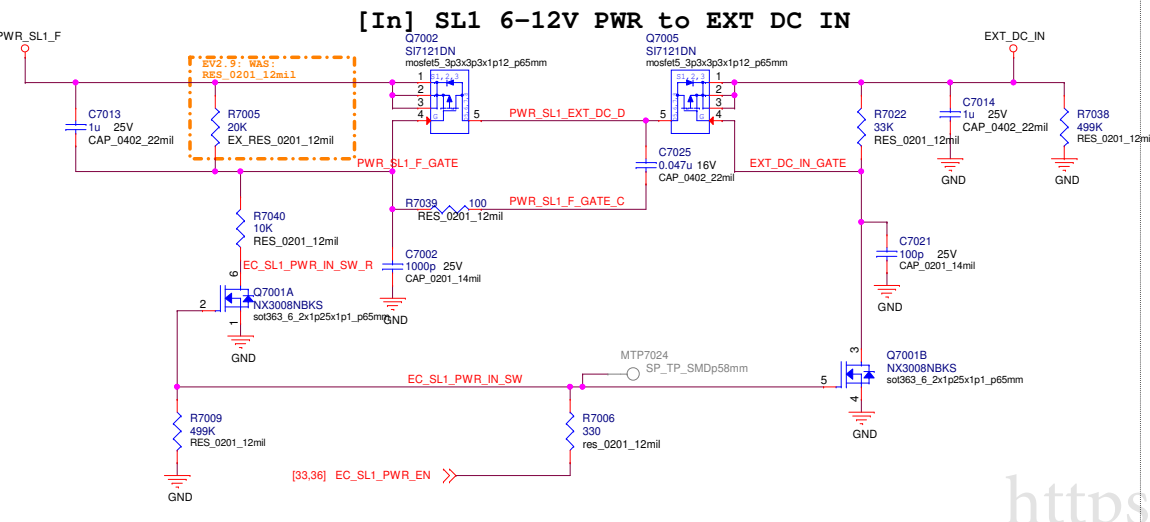
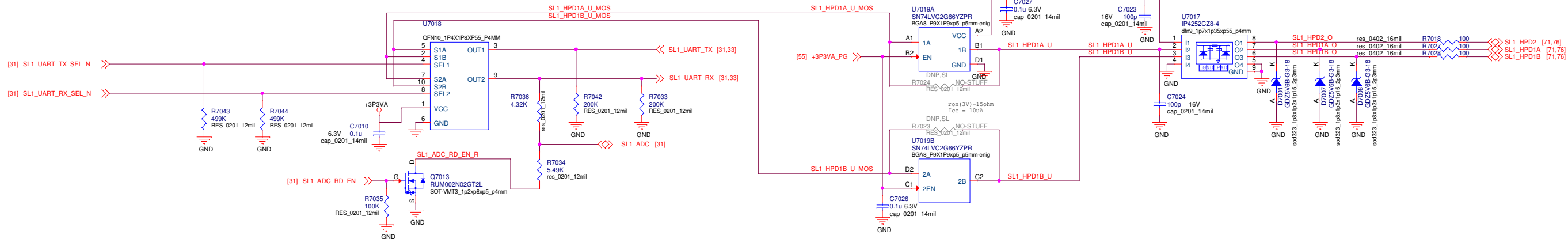
U23e15w to U22 BOM	U23e15w BOM changes	Y22 GT
Prog1	Prog1	Prog1
R6674=150k	R6674=165K	R6674=150k
IA	IA	IA
R6637=1.5k	R6637=1.5k	R6637=2.74k
C6695=2200p	C6695=2200p	C6695=1800p
C6690=8200p	C6690=8200p	C6690=8200p
R6630=4.02k	R6630=4.02k	R6630=4.02k
C6691=0.022u	C6691=0.022u	C6691=0.047uF
C6692=1500p	C6692=1500p	C6692=2700p
R6696=90.9k	R6696=88.7k	R6696=90.9k
C6696=0.010uF	C6696=0.010uF	C6696=820pF
R6632=1.87K	R6632=1.87K	R6632=1.87K
R6750=1.1K	R6750=1.1K	R6750=1.1K
R6633=1.6K	R6633=1.6K	R6633=1.58K
GT	GT+GTx	GT+GTx
R6644=3.92k	R6644=3.09k	R6644=3.09k
C6624=680p	C6624=390p	C6624=1000p
R6640=1.24k	R6640=1.69K	R6640=732
R6602=150k	R6602=121k	R6602=86.6k
C6656=1500p	C6656=1500p	C6656=560p
C6648=2200p	C6648=2200p	C6648=2200p
R6699=3k	R6699=3k	R6699=1K
C6651=0.056u	C6651=0.056u	C6651=0.056u
C6652=3300p	C6652=3300p	C6652=3300p
R6862=2.2	R6862=2.2	R6862=2.2
R6863=2.2	R6863=2.2	R6863=2.2
SA	SA	SA
R6618=118k	R6618=100K	R6618=100K
R6622=1.5k	R6622=1.5k	R6622=2k
C6602=2200p	C6602=2200p	C6602=2200p
C6600=8200p	C6600=8200p	C6600=8200p
R6619=5.1k	R6619=5.1k	R6619=5.1k
C6601=470p	C6601=470p	C6601=470p



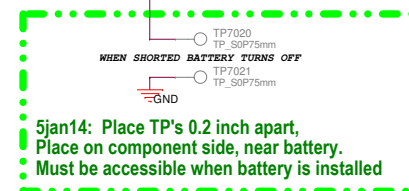
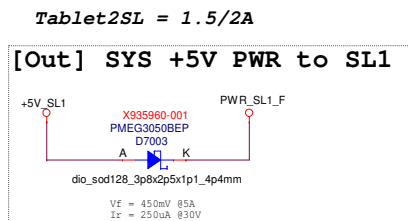
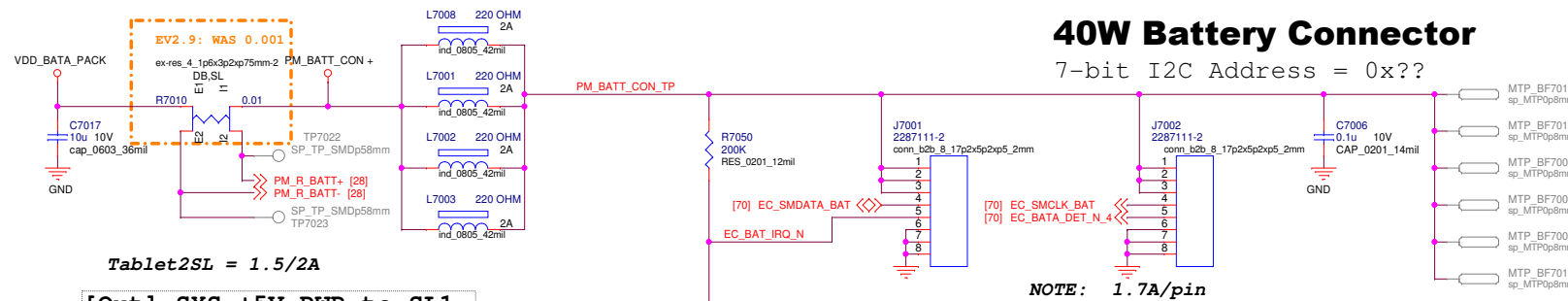
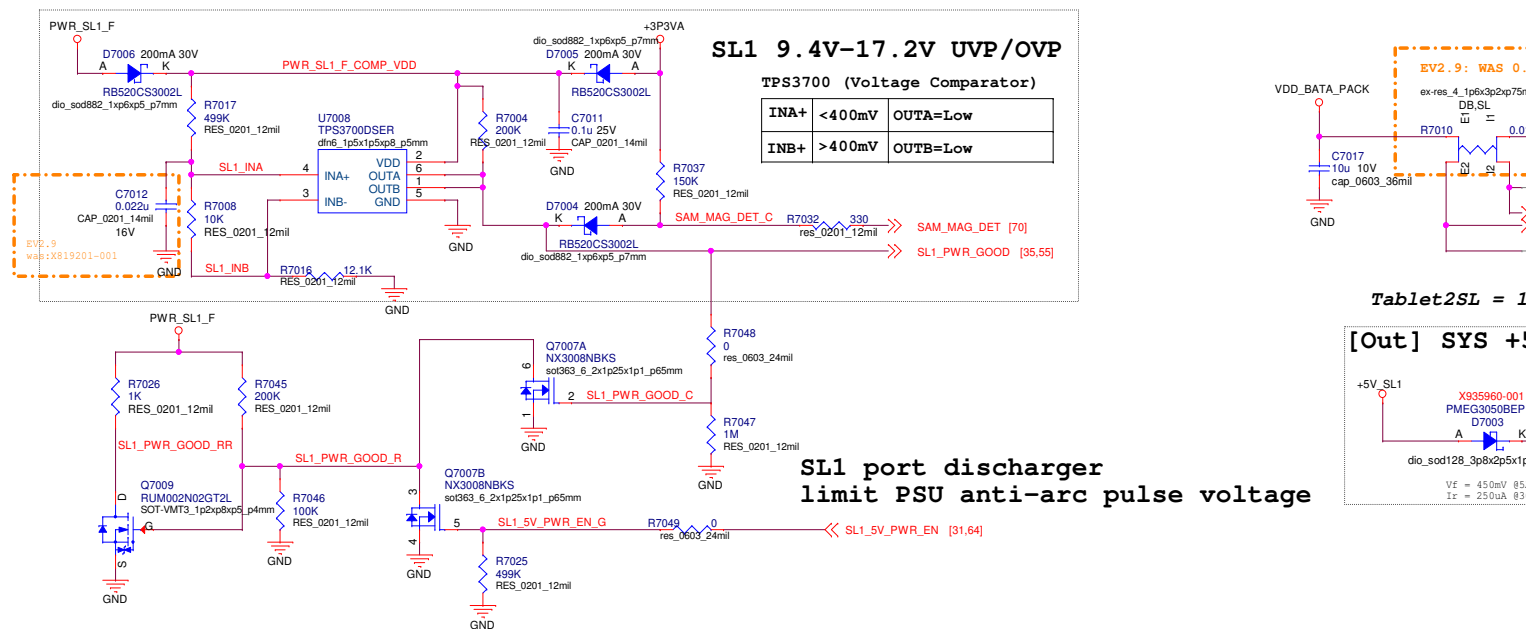
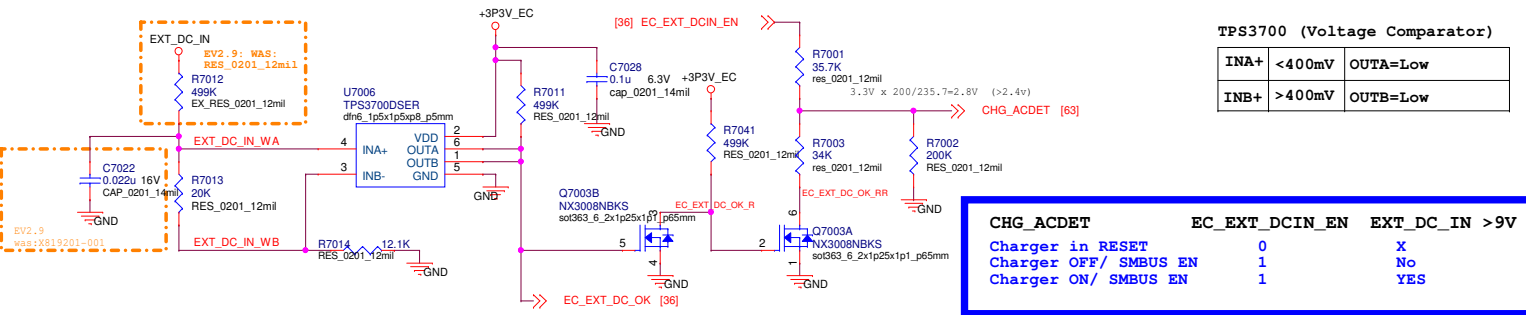
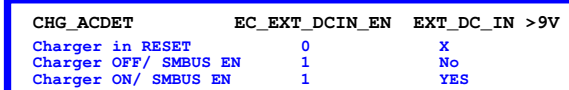
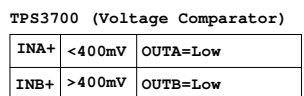
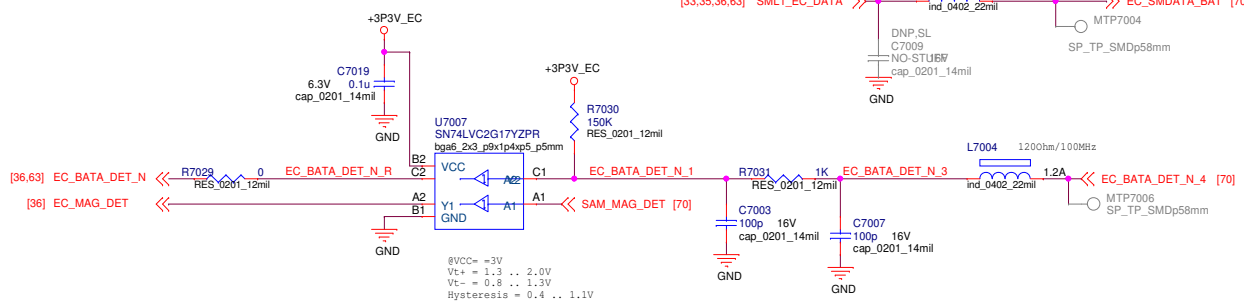
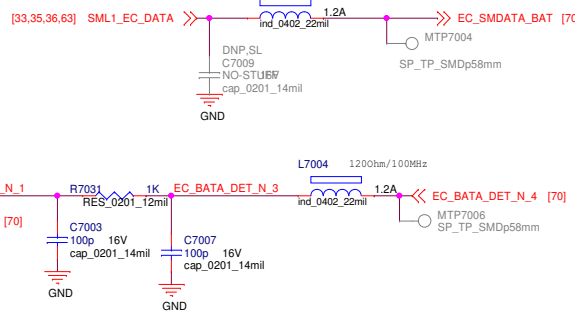
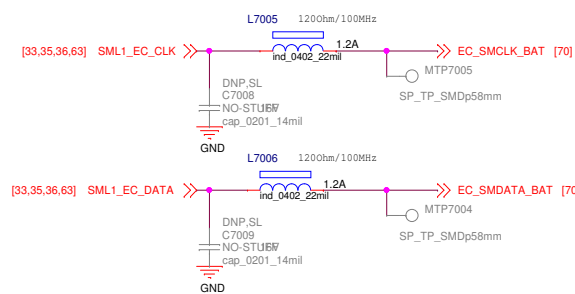




HPD FOR SL1 (ONE/TWO WIRE UART)

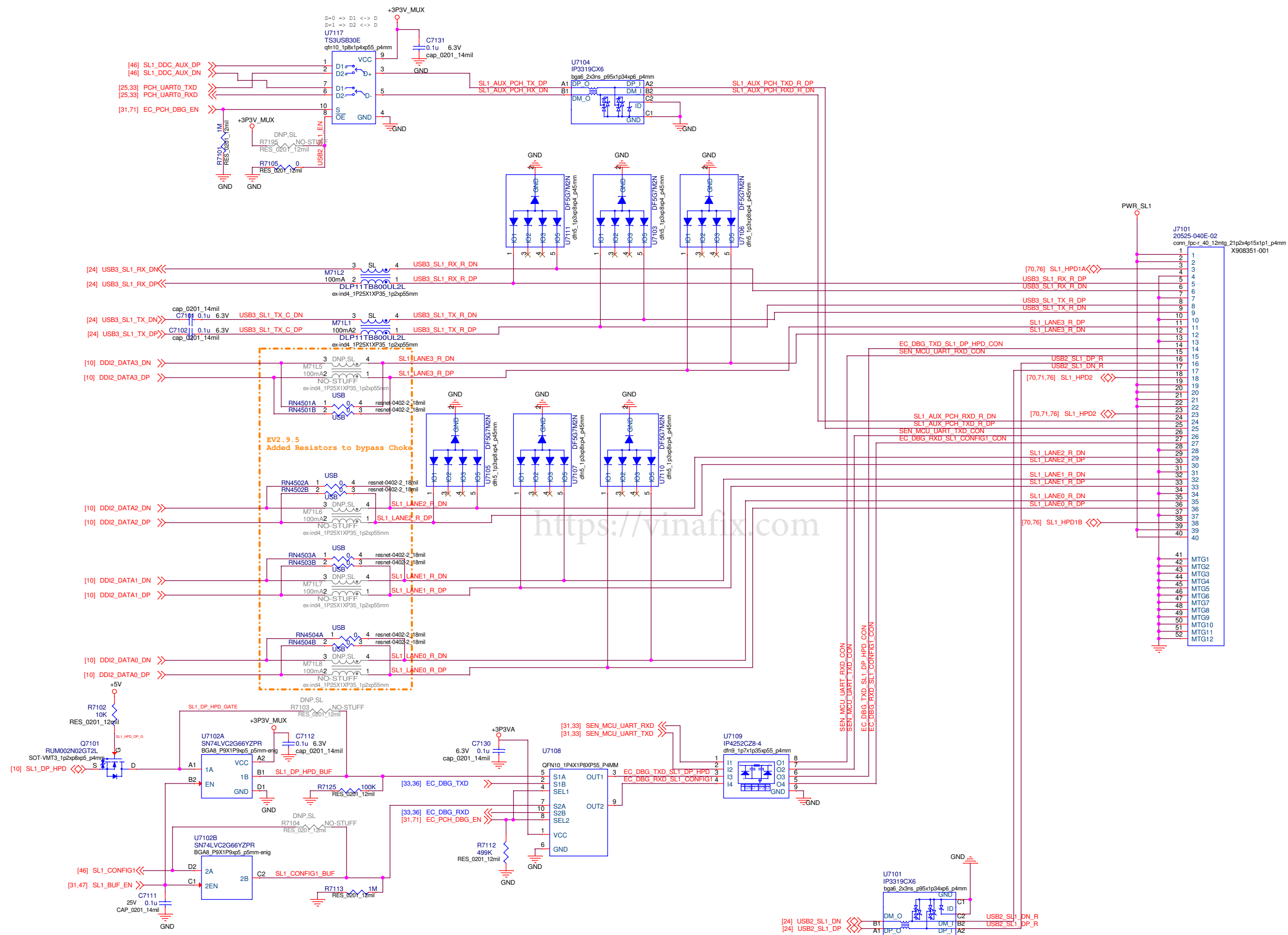


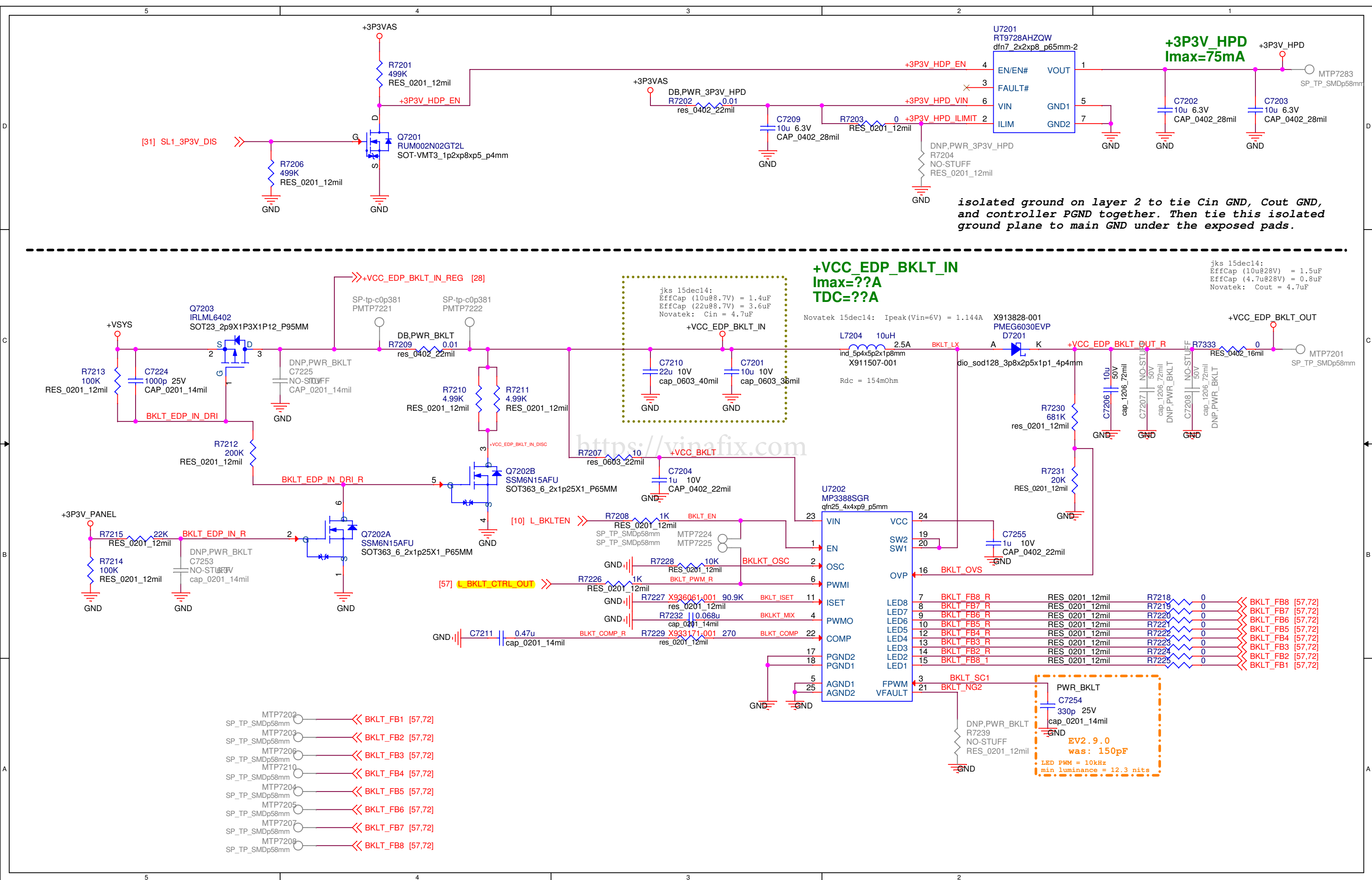
Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed



40W Battery Connector

7-bit I2C Address = 0x??





+5V_KB_CONN
Imax = 0.5A

SP_TP_SMDp58mm MTP7314
SP_TP_SMDp58mm MTP7315
SP_TP_SMDp58mm MTP7316
SP_TP_SMDp58mm MTP7317
[74] BLADE_TX_USB_D+
[74] BLADE_RX_USB_D-
[74] +5V_SHA_CONN_UART_RX_CONN
[74] BLADE_AUTH_DATA_UART_TX_CONN

BLADE Connector

J7302
2287111-2
conn_b2b_8_17p2x5p2xp5_2mm
X904496-001

MTP_BF7305
sp_MTP0p8mm
MTP_BF7306
sp_MTP0p8mm
MTP_BF7313
sp_MTP0p8mm
MTP_BF7314
sp_MTP0p8mm

MTP_BF7309
sp_MTP0p8mm
MTP_BF7310
sp_MTP0p8mm
MTP_BF7311
sp_MTP0p8mm
MTP_BF7312
sp_MTP0p8mm

FANG_PWR

L7301 220 OHM
ind_0805_42mil

FANG_PWR_F

+5V_KB_CONN
L7304 120Ohm/100MHz
ind_0402_22mil
C7302 0.1u 6.3V
cap_0201_14mil
A1
A2
D7302 V18MLA0402NR
dio_0402_24mil_aa

SP_TP_SMDp58mm MTP7319
SP_TP_SMDp58mm MTP7318

J7303
2287111-2
conn_b2b_8_17p2x5p2xp5_2mm
X904496-001

eFang power = 3.5A max
using +1 rule

[31] BLADE_AUTH_PWR_EN

GND
R7311 1M
RES_0201_12mil

Rds(on) = 120mOhm (typ)
Iq = 170uA

U7301
RT9728AHZQW
dfn7_2x2xp8_p65mm-2

+5V_SHA_CONN
Imax=75mA

+5V_SHA_CONN

+5VA_SHA
R7314 0.01
res_0402_22mil
DB, BLADE
PMT7321 SP-tp-c0p381
PMT7322 SP-tp-c0p381

C7306 10u 6.3V
cap_0603_38mil

BLADE
R7313 0
RES_0402_16mil
SHA_ILIMIT
DNP, BLADE
R7319
NO-STUFF
RES_0201_12mil

Imax = 1.4A
50mA <= ILIM (connected to VIN) <= 100mA

+VSYS
L7313 300HMS @100MHZ
IND_0402_24mil
L7312 300HMS @100MHZ
IND_0402_24mil

V(operating) = 4.5 to 13.8 Max

U7302
TPS2592ZADRCR
son11_3x3x1_p5mm

current = 3A

X935960-001
PMEG3050BEP
D7303
dio_sod128_3p8x2p5x1p1_4p4mm
Vf = 450mV @5A
Ir = 250uA @30V

FANG_PWR_F

LTE eFANG PWR = 2.10A(min)
2.47A(nom)
2.84A(max)

[36] EC_BLADE_5VLD SW_EN

R7309 0
RES_0201_12mil

R7315 100K
RES_0201_12mil

C7314 1000p
CAP_0201_14mil
25V 10%

C7311 1000p
CAP_0201_14mil
25V 10%

MTP7320
SP_TP_SMDp58mm

FANG_REG_ILIM
R7316 59K
RES_0201_12mil

C7316 0.1u
CAP_0201_14mil
25V

C7317 2.2u
CAP_0603_38mil
25V

C7315 2.2u
CAP_0603_38mil
25V

