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WV-3 FVT LOGIC SCHEMATICS

WV-3
VER0.1
3/19/2015

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022.DDR4 SO DIMM
023.BLANK
024.BLANK
025.BLANK
026.BLANK
027.BLANK
028.DP SWITCH
029.DP DEMUX
030.BLANK
031.BLANK
032.BLANK
033.BLANK
034.BLANK
035.BLANK
036.BLANK
037.RF COMPONENT
038.LCD/LID/MIC/CAMERA/PWR SW
039.BLANK
040.HDMI CONNECTOR
041.DISPLAY PORT CONNECTOR
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051.MEDIA CARD CONTROLLER
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064.KEYBOARD/TRACK POINT
065.TOUCH PAD/NFC/FPR
066.BLANK
067.FAN CONNECTOR
068.G-SENSOR
069.TPM
070.SMBUS SW/LPC DEBUG PORT
071.THINK ENGINE(1/2)
072.THINK ENGINE(2/2)
073.DC-IN
074.BATTERY INPUT
075.BATTERY CHARGER(BQ24760)
076.BLANK
077.BLANK
078.DC/DC VCC5M/VCC3M(TPS51285B)
079.DC/DC IMVP8(NCP81208)
080.DC/DC CPUCORE(NCP81382)
081.DC/DC VCCGFXCORE_I(NCP81381)
082.DC/DC VCCSA(NCP81380)
083.DC/DC VCC1R0_SUS(TPS51367R)
084.BLANK
085.DC/DC VCC1R2A(TPS51716)
086.DC/DC VCC1R8_SUS(TPS62065)
087.BLANK
088.DC/DC VCC2R5A(TPS62065)
089.BLOCK DIAGRAM
090.BLANK
091.BLANK
092.LOAD SW PCH SUS/TRACK POINT
093.LOAD SW LAN
094.LOAD SW CPU
095.LOAD SW B
096.LOAD SW WWAN & WLAN
097.BLANK
098.PTH FOR SCREW HOLES
099.BLANK
100.NEC LED BOARD

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WOLVERINE3 UMA

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EC Modify History

Date	EC version	File name

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Title: EC HISTORY

Size	Document Number	Rev
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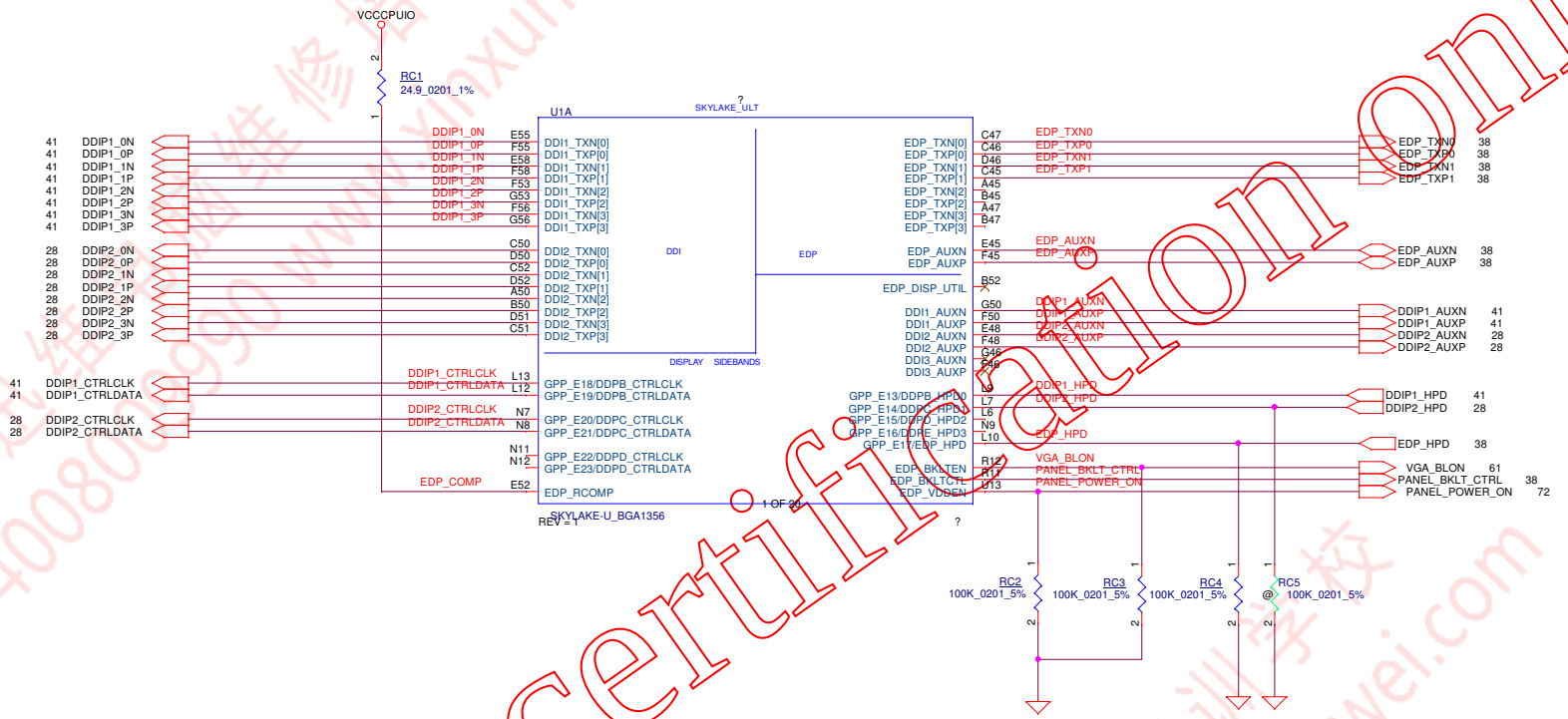
Mini DP



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Title: CPU(1/16) : DDI/EDP

Size	Document Number	Rev
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	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB85	DDR0_DQ[16]	DDR0_DQ[32]
	AW86	DDR0_DQ[17]	DDR0_DQ[33]
	AW83	DDR0_DQ[18]	DDR0_DQ[34]
	AY83	DDR0_DQ[19]	DDR0_DQ[35]
	BA86	DDR0_DQ[20]	DDR0_DQ[36]
	AY86	DDR0_DQ[21]	DDR0_DQ[37]
	BA83	DDR0_DQ[22]	DDR0_DQ[38]
	BB83	DDR0_DQ[23]	DDR0_DQ[39]
	BA81	DDR0_DQ[24]	DDR0_DQ[40]
	AW81	DDR0_DQ[25]	DDR0_DQ[41]
	BB58	DDR0_DQ[26]	DDR0_DQ[42]
	AW69	DDR0_DQ[27]	DDR0_DQ[43]
	BB81	DDR0_DQ[28]	DDR0_DQ[44]
	AY81	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY58	DDR0_DQ[31]	DDR0_DQ[47]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]

22 M_A_DQ[63:0]

SKYLAKE_ULT

U1B

M_A_DQ0 AL71 DDR0_DQ[0]
M_A_DQ1 AL68 DDR0_DQ[1]
M_A_DQ2 AN68 DDR0_DQ[2]
M_A_DQ3 AN69 DDR0_DQ[3]
M_A_DQ4 AL70 DDR0_DQ[4]
M_A_DQ5 AL69 DDR0_DQ[5]
M_A_DQ6 AN70 DDR0_DQ[6]
M_A_DQ7 AN71 DDR0_DQ[7]
M_A_DQ8 AR70 DDR0_DQ[8]
M_A_DQ9 AR68 DDR0_DQ[9]
M_A_DQ10 AU71 DDR0_DQ[10]
M_A_DQ11 AU68 DDR0_DQ[11]
M_A_DQ12 AR71 DDR0_DQ[12]
M_A_DQ13 AR69 DDR0_DQ[13]
M_A_DQ14 AU70 DDR0_DQ[14]
M_A_DQ15 AU69 DDR0_DQ[15]
M_A_DQ16 AF65 DDR1_DQ[0]/DDR0_DQ[16]
M_A_DQ17 AF64 DDR1_DQ[1]/DDR0_DQ[17]
M_A_DQ18 AK65 DDR1_DQ[2]/DDR0_DQ[18]
M_A_DQ19 AK64 DDR1_DQ[3]/DDR0_DQ[19]
M_A_DQ20 AF66 DDR1_DQ[4]/DDR0_DQ[20]
M_A_DQ21 AF67 DDR1_DQ[5]/DDR0_DQ[21]
M_A_DQ22 AK67 DDR1_DQ[6]/DDR0_DQ[22]
M_A_DQ23 AK66 DDR1_DQ[7]/DDR0_DQ[23]
M_A_DQ24 AF70 DDR1_DQ[8]/DDR0_DQ[24]
M_A_DQ25 AF68 DDR1_DQ[9]/DDR0_DQ[25]
M_A_DQ26 AH71 DDR1_DQ[10]/DDR0_DQ[26]
M_A_DQ27 AH68 DDR1_DQ[11]/DDR0_DQ[27]
M_A_DQ28 AF71 DDR1_DQ[12]/DDR0_DQ[28]
M_A_DQ29 AF69 DDR1_DQ[13]/DDR0_DQ[29]
M_A_DQ30 AH70 DDR1_DQ[14]/DDR0_DQ[30]
M_A_DQ31 AH69 DDR1_DQ[15]/DDR0_DQ[31]
M_A_DQ32 BB65 DDR0_DQ[16]/DDR0_DQ[32]
M_A_DQ33 AW65 DDR0_DQ[17]/DDR0_DQ[33]
M_A_DQ34 AW63 DDR0_DQ[18]/DDR0_DQ[34]
M_A_DQ35 AY63 DDR0_DQ[19]/DDR0_DQ[35]
M_A_DQ36 BA65 DDR0_DQ[20]/DDR0_DQ[36]
M_A_DQ37 AY65 DDR0_DQ[21]/DDR0_DQ[37]
M_A_DQ38 BA63 DDR0_DQ[22]/DDR0_DQ[38]
M_A_DQ39 BB63 DDR0_DQ[23]/DDR0_DQ[39]
M_A_DQ40 BA61 DDR0_DQ[24]/DDR0_DQ[40]
M_A_DQ41 AW61 DDR0_DQ[25]/DDR0_DQ[41]
M_A_DQ42 BB59 DDR0_DQ[26]/DDR0_DQ[42]
M_A_DQ43 AW59 DDR0_DQ[27]/DDR0_DQ[43]
M_A_DQ44 BB61 DDR0_DQ[28]/DDR0_DQ[44]
M_A_DQ45 AY61 DDR0_DQ[29]/DDR0_DQ[45]
M_A_DQ46 BA59 DDR0_DQ[30]/DDR0_DQ[46]
M_A_DQ47 AY59 DDR0_DQ[31]/DDR0_DQ[47]
M_A_DQ48 AT66 DDR1_DQ[16]/DDR0_DQ[48]
M_A_DQ49 AU66 DDR1_DQ[17]/DDR0_DQ[49]
M_A_DQ50 AP65 DDR1_DQ[18]/DDR0_DQ[50]
M_A_DQ51 AN65 DDR1_DQ[19]/DDR0_DQ[51]
M_A_DQ52 AN66 DDR1_DQ[20]/DDR0_DQ[52]
M_A_DQ53 AP66 DDR1_DQ[21]/DDR0_DQ[53]
M_A_DQ54 AT65 DDR1_DQ[22]/DDR0_DQ[54]
M_A_DQ55 AU65 DDR1_DQ[23]/DDR0_DQ[55]
M_A_DQ56 AT61 DDR1_DQ[24]/DDR0_DQ[56]
M_A_DQ57 AU61 DDR1_DQ[25]/DDR0_DQ[57]
M_A_DQ58 AP60 DDR1_DQ[26]/DDR0_DQ[58]
M_A_DQ59 AN60 DDR1_DQ[27]/DDR0_DQ[59]
M_A_DQ60 AN61 DDR1_DQ[28]/DDR0_DQ[60]
M_A_DQ61 AP61 DDR1_DQ[29]/DDR0_DQ[61]
M_A_DQ62 AT60 DDR1_DQ[30]/DDR0_DQ[62]
M_A_DQ63 AU60 DDR1_DQ[31]/DDR0_DQ[63]

DDR CH A

SKYLAKE-U_BGA1356
REV = 1
2 OF 20

DDR0_CKN[0] AU53 -M_A_DDRCLK0_1866M
DDR0_CKP[0] AT53 M_A_DDRCLK0_1866M
DDR0_CKN[1] AU55 -M_A_DDRCLK1_1866M
DDR0_CKP[1] AT55 M_A_DDRCLK1_1866M

DDR0_CKE[0] BA56 M_A_CKE0
DDR0_CKE[1] BB56 M_A_CKE1
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56

DDR0_CS#[0] AU45 -M_A_CS0
DDR0_CS#[1] AU43 -M_A_CS1
DDR0_ODT[0] AT45 -M_A_ODT0
DDR0_ODT[1] AT43 -M_A_ODT1

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 M_A_A5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 M_A_A9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 M_A_A6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 M_A_A8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AW52 M_A_A7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AY55 M_A_BG0 → M_A_BG0 22
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] AW54 M_A_A12 → M_A_A12 22
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA54 M_A_A11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55 M_A_ACT_N → M_A_ACT_N 22
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54 M_A_BG1 → M_A_BG1 22

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 M_A_A13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48 -M_A_CAS → -M_A_CAS 22
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46 -M_A_WE → -M_A_WE 22
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50 -M_A_RAS → -M_A_RAS 22
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AU52 M_A_BS0 → M_A_BS0 22
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 M_A_BS1
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48 M_A_A10 → M_A_BS1 22
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 M_A_A1
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 M_A_A0
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 M_A_A3
DDR0_MA[3] BA50 M_A_A4
DDR0_MA[4] BB52

DDR0_DQSN[0] AM70 -M_A_DQS0
DDR0_DQSP[0] AM69 M_A_DQS0
DDR0_DQSN[1] AT69 -M_A_DQS1
DDR0_DQSP[1] AT70 M_A_DQS1
DDR0_DQSN[2] AH66 -M_A_DQS2
DDR0_DQSP[2] AH65 M_A_DQS2
DDR0_DQSN[3] AG69 -M_A_DQS3
DDR0_DQSP[3] AG70 M_A_DQS3
DDR0_DQSN[4] BA64 -M_A_DQS4
DDR0_DQSP[4] AY64 M_A_DQS4
DDR0_DQSN[5] AY60 -M_A_DQS5
DDR0_DQSP[5] BA60 M_A_DQS5
DDR0_DQSN[6] AR66 -M_A_DQS6
DDR0_DQSP[6] AR65 M_A_DQS6
DDR0_DQSN[7] AR61 -M_A_DQS7
DDR0_DQSP[7] AR60 M_A_DQS7

DDR0_ALERT# AW50 M_A_ALERT_N → M_A_ALERT_N 22
DDR0_PAR AT52 M_A_PARITY → M_A_PARITY 22

DDR_VREF_CA AY67
DDR0_VREF_DQ AY68 1 → DDR4_VREF_CA_M3 22
DDR1_VREF_DQ BA67 @TP17 Test_Point_40MIL

DDR_VTT_CNTL AW67 DDR_PG_CTRL

M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 → M_A_A[0..13] 22

M_A_DQS0 -M_A_DQS1 -M_A_DQS2 -M_A_DQS3 -M_A_DQS4 -M_A_DQS5 -M_A_DQS6 -M_A_DQS7 → -M_A_DQS[0..7] 22

M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7 → M_A_DQS[0..7] 22

VCC3M
RC8 100K_0201_5%
VCC1R2A
85 DDR_VTT_PG_CTRL
DDR_VTT_PG_CTRL
QC1 DTC015TMT2L_VMT3
RC9 10K_0201_5%

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

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Title: CPU(2/16) : DDR4

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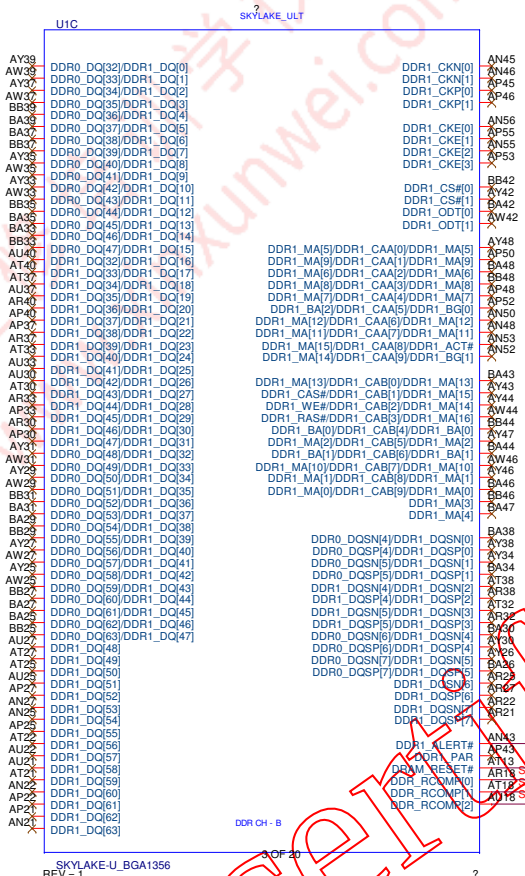
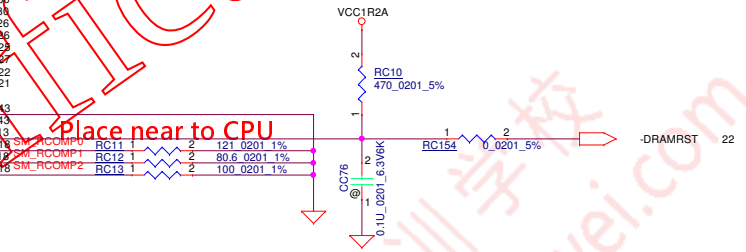
TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF68	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[6]	DDR0_DQ[21]
	AK67	DDR1_DQ[8]	DDR0_DQ[22]
	AK68	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN68	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]



TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]



TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

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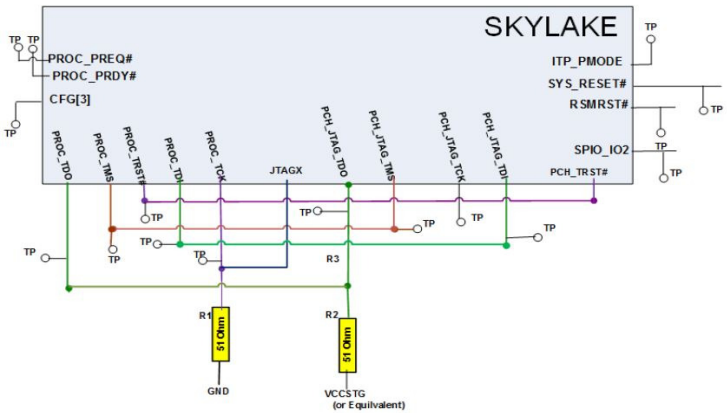
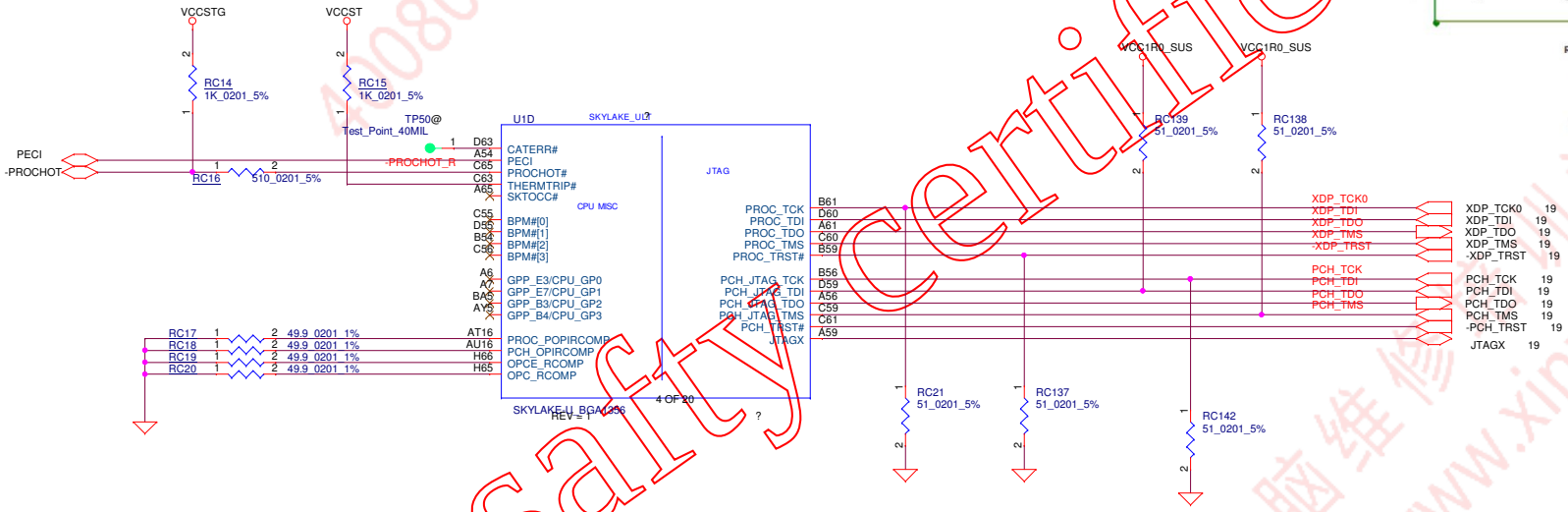
Update description

For DCI debug
RC113 OP, RC148 short(XDP_TDO→ PCH_TDO)
RC138 OP, RC145 short(XDP_TMS→ PCH_TMS)
RC137 OP, RC147 short(XDP_TRST→ PCH_TRST)
RC142 OP, RC143 short(XDP_TCK0→ JTAGX)
RC139 OP, RC146 short(XDP_TDI→ PCH_TDI)





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Title: CPU(4/16) : MISC/JTAG

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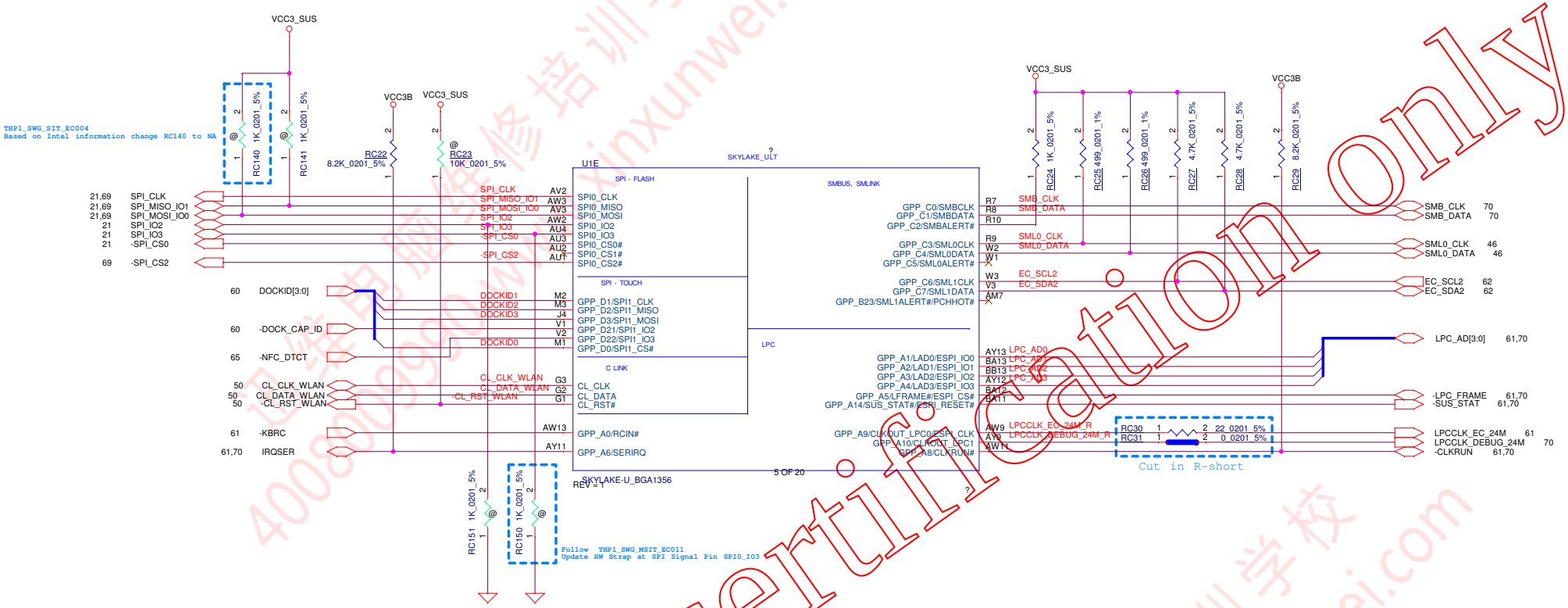

TABLE : Functional Strap

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

<- LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

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Title: CPU(5/16) : LPC/SPI/SMBUS/C-LINK

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TABLE : Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

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Title: CPU(6/16) : LPSS/ISH

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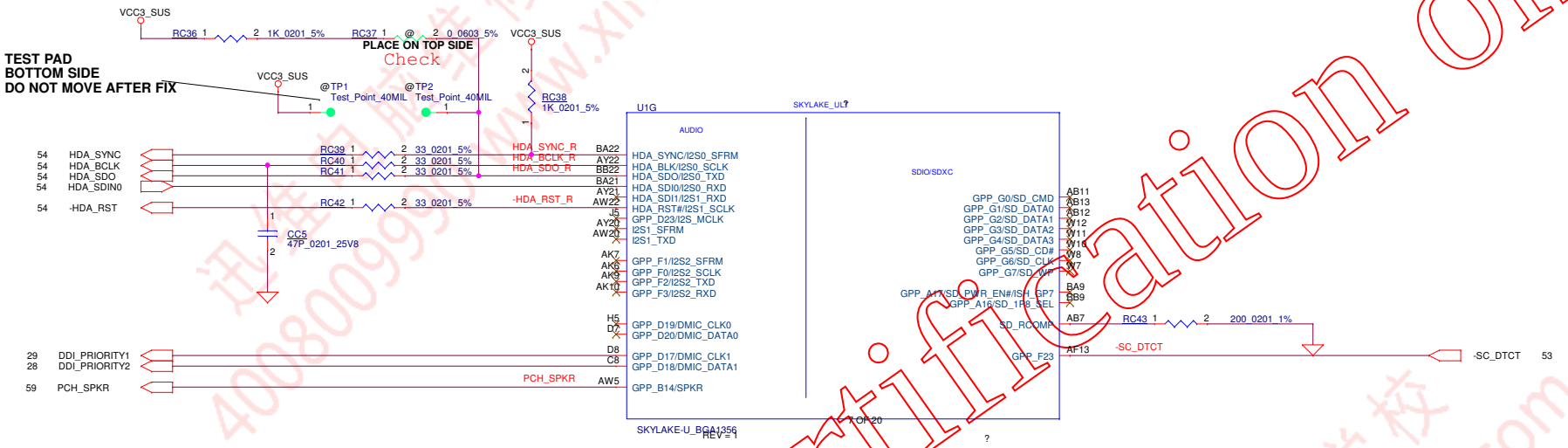
TABLE : Functional Strap

HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



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Title: CPU(7/16) : AUDIO/SDXC

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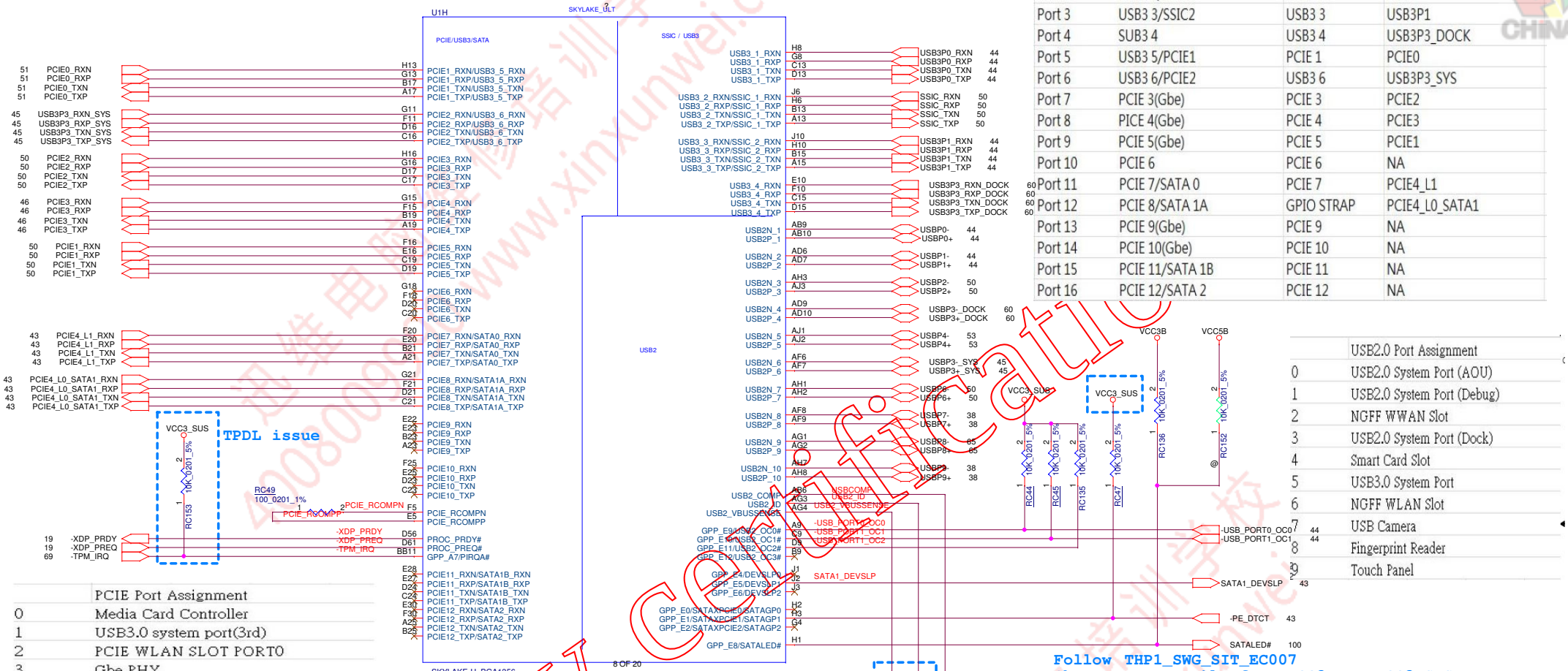
	FLEXIBLE I/O Port Configuration	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC1	USB3 2	SSIC
Port 3	USB3 3/SSIC2	USB3 3	USB3P1
Port 4	SUB3 4	USB3 4	USB3P3_DOCK
Port 5	USB3 5/PCIE1	PCIE 1	PCIE0
Port 6	USB3 6/PCIE2	USB3 6	USB3P3_SYS
Port 7	PCIE 3(Gbe)	PCIE 3	PCIE2
Port 8	PICE 4(Gbe)	PCIE 4	PCIE3
Port 9	PCIE 5(Gbe)	PCIE 5	PCIE1
Port 10	PCIE 6	PCIE 6	NA
Port 11	PCIE 7/SATA 0	PCIE 7	PCIE4_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE4_L0_SATA1
Port 13	PCIE 9(Gbe)	PCIE 9	NA
Port 14	PCIE 10(Gbe)	PCIE 10	NA
Port 15	PCIE 11/SATA 1B	PCIE 11	NA
Port 16	PCIE 12/SATA 2	PCIE 12	NA



	USB2.0 Port Assignment
0	USB2.0 System Port (AOU)
1	USB2.0 System Port (Debug)
2	NGFF WWAN Slot
3	USB2.0 System Port (Dock)
4	Smart Card Slot
5	USB3.0 System Port
6	NGFF WLAN Slot
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

	PCIE Port Assignment
0	Media Card Controller
1	USB3.0 system port(3rd)
2	PCIE WLAN SLOT PORT0
3	Gbe PHY
4	PCIE WLAN SLOT PORT1
5	Reserved
6	PCIE
7	SATA/PCIE
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved

	USB3.0 Port Assignment
0	USB3.0 System Port (AOU)
1	M2.WWAN Slot (SSIC)
2	USB3.0 System Port (Debug)
3	USB3.0 System Port (Docking)
4	(PCIE1)
5	USB3.0 System Port

	SATA Port Assignment
0	PCIE 7
1A	SATA/PCIE HDD
1B	NA
2	NA

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Title: 010_CPU(8/16) : PCIE/USB/SATA

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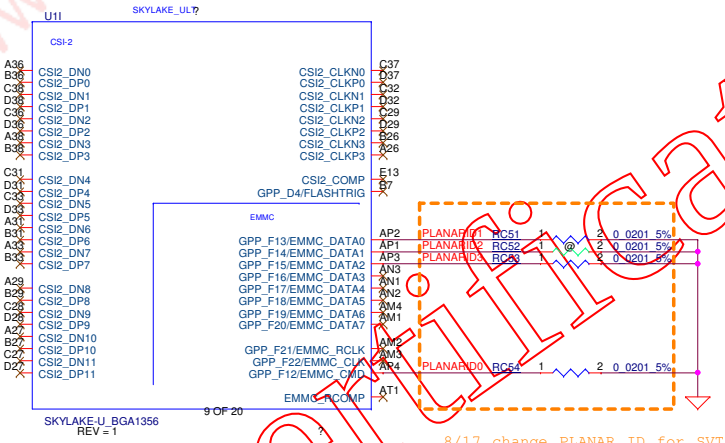

8/17 change PLANAR ID for SVT

LEVEL	PLANAR ID			
	3	2	1	0
	RC53	RC52	RC51	RC54
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE	PLANAR ID [3..0]
SDV	0000
FVT	0001
SIT	0010
SIT-R	0011
SVT	**0100**

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Title: *CPU(9/16) : CSI-2/EMMC*

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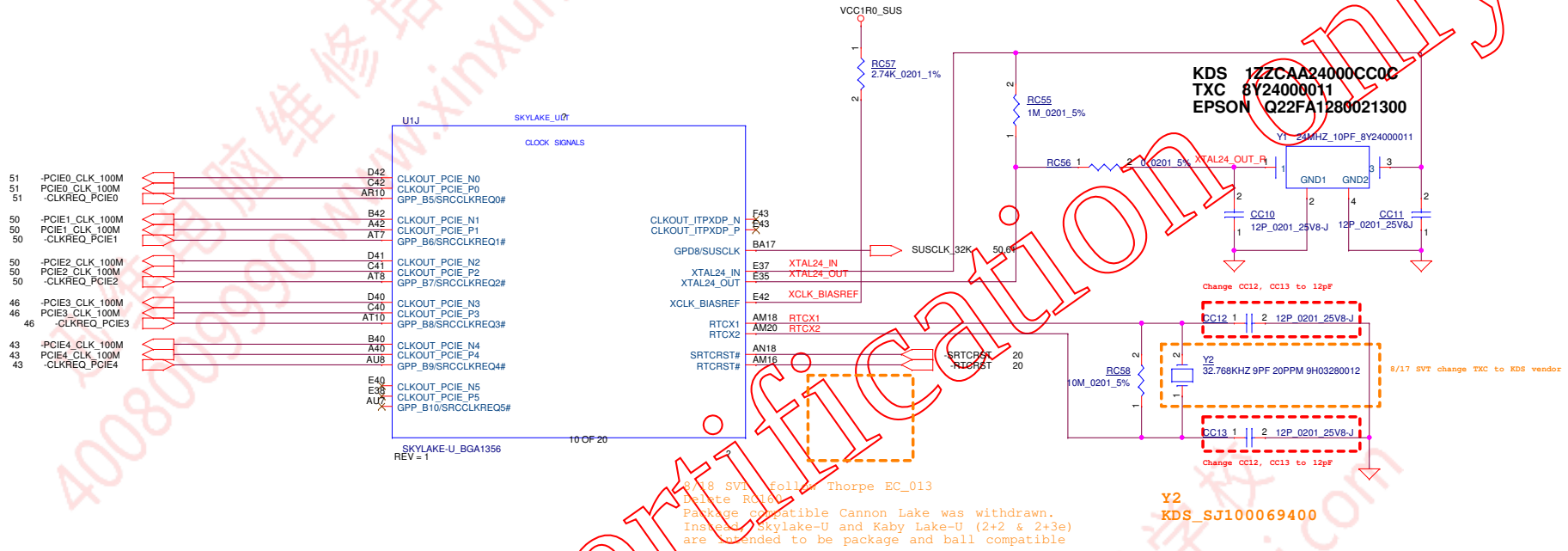

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Title: CPU(10/16) : CLOCK SIGNALS

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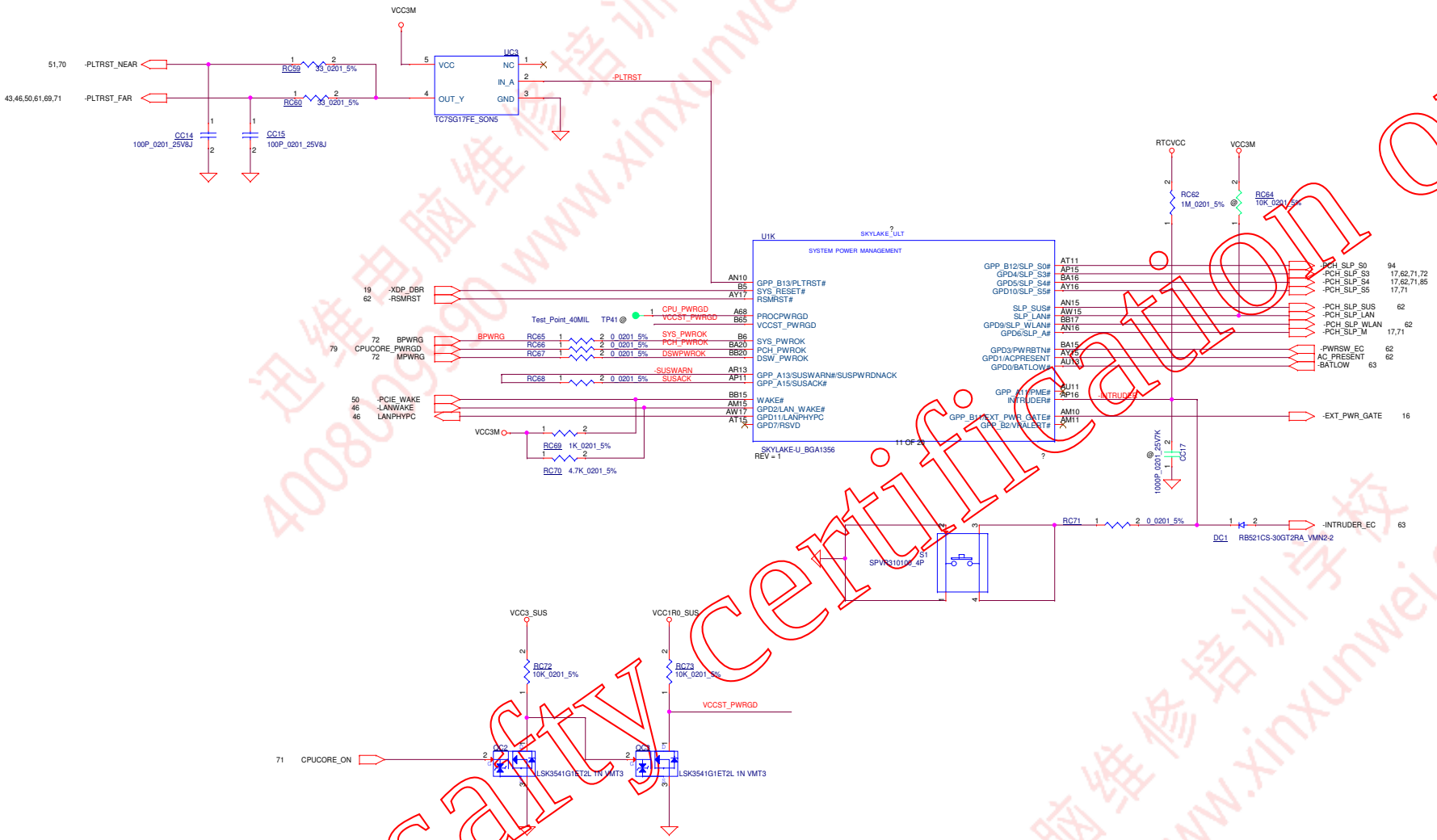

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Title: CPU(11/16) : SYSTEM PM

Size	Document Number	Rev
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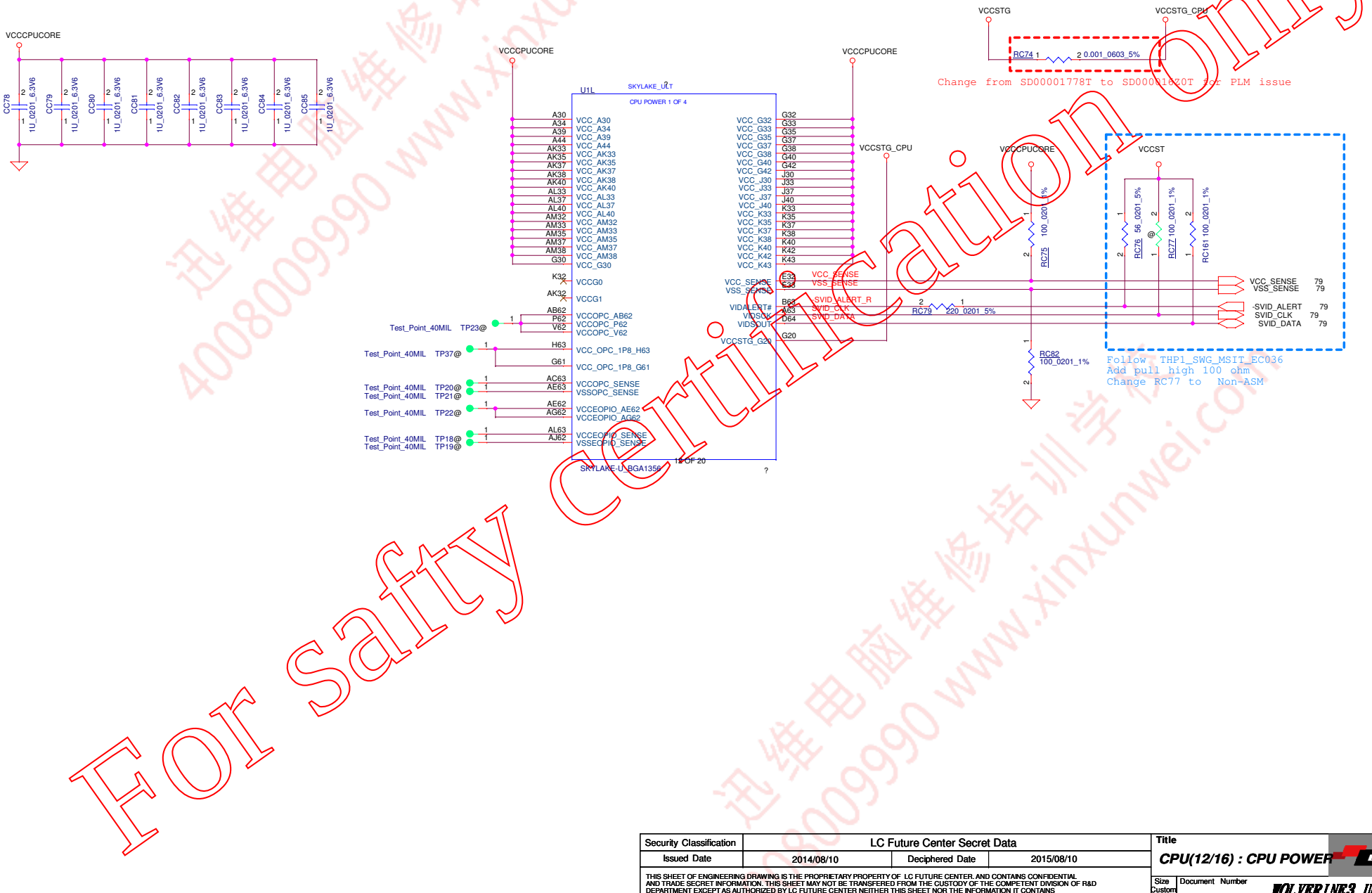

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Title: CPU(12/16) : CPU POWER

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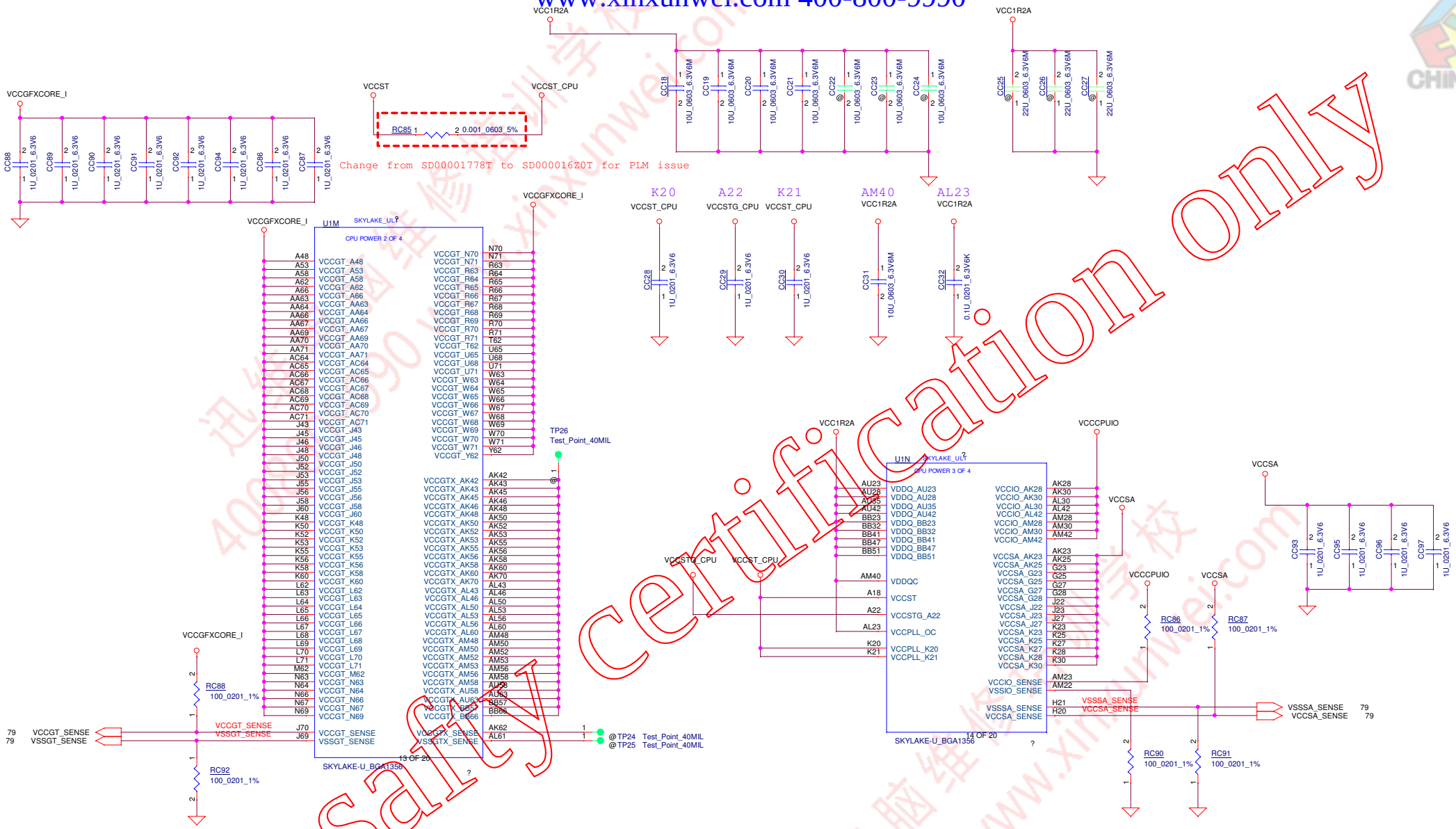

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Title: CPU(13/16) : CPU POWER

Size: Custom	Document Number: WOLVERINE3 UMA	Rev: 0.1
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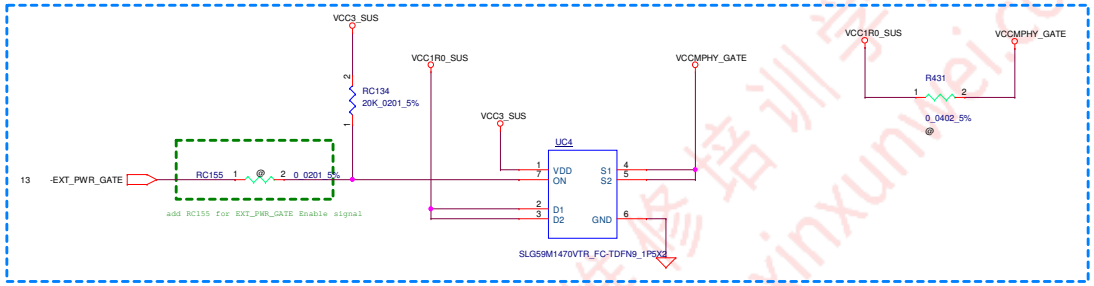
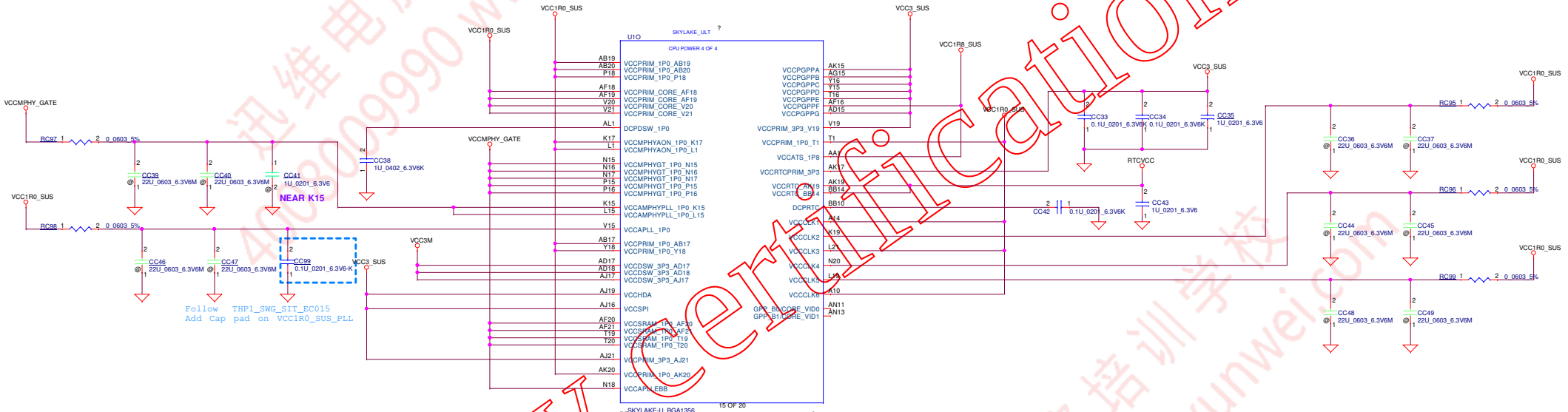
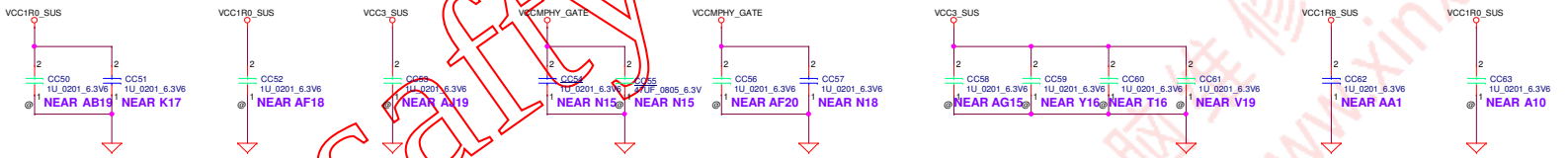
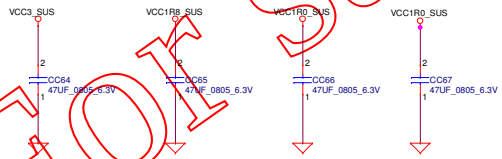


Follow THP1_SWG_SIT_EC021



Follow THP1_SWG_SIT_EC015
Add Cap pad on VCC1R0_SUS_PLL





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Title: CPU(6/16) : PCH POWER

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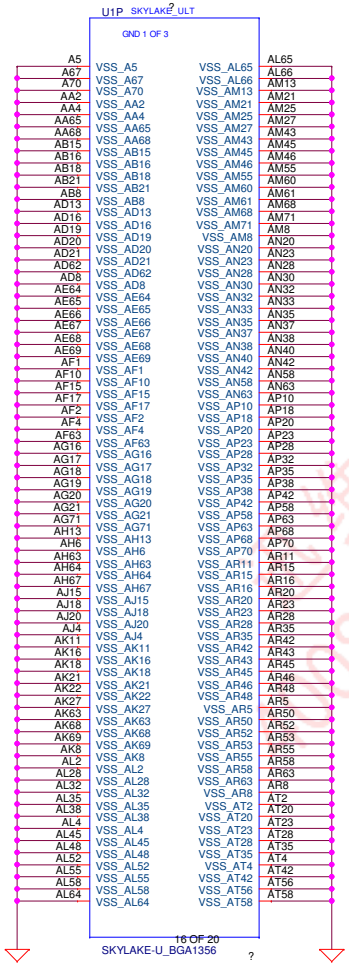
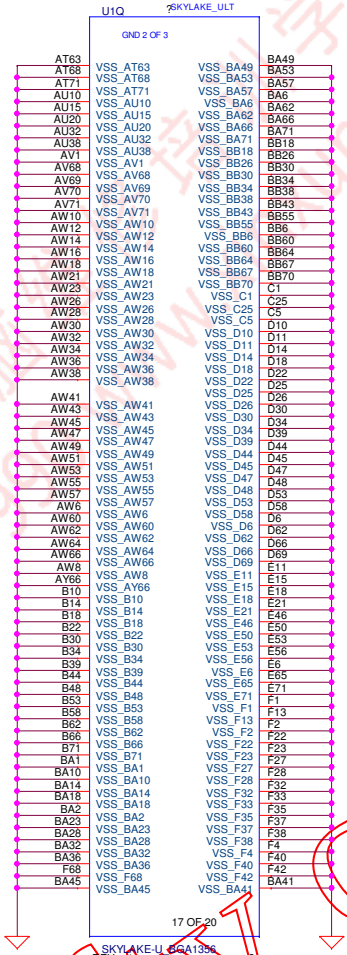
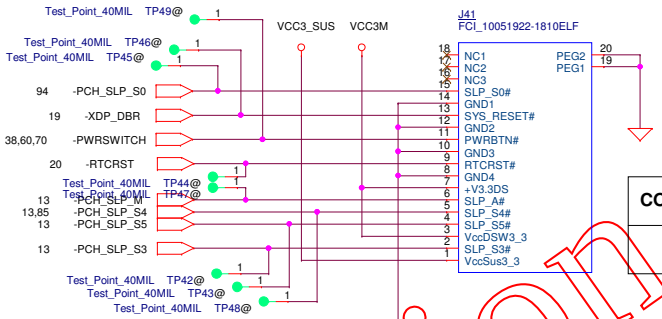
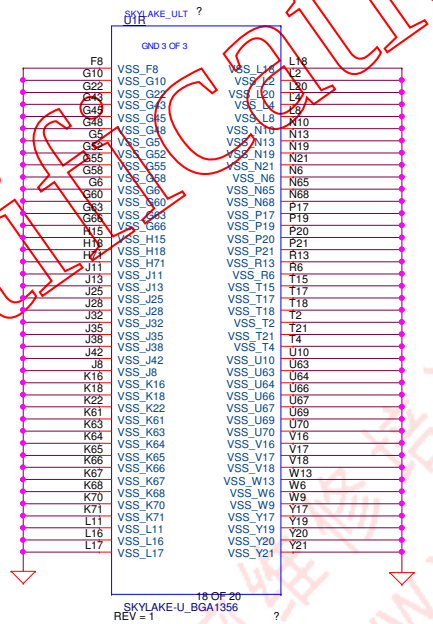




APS/PETS interface



CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM



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Title: CPU(15/16) : GND

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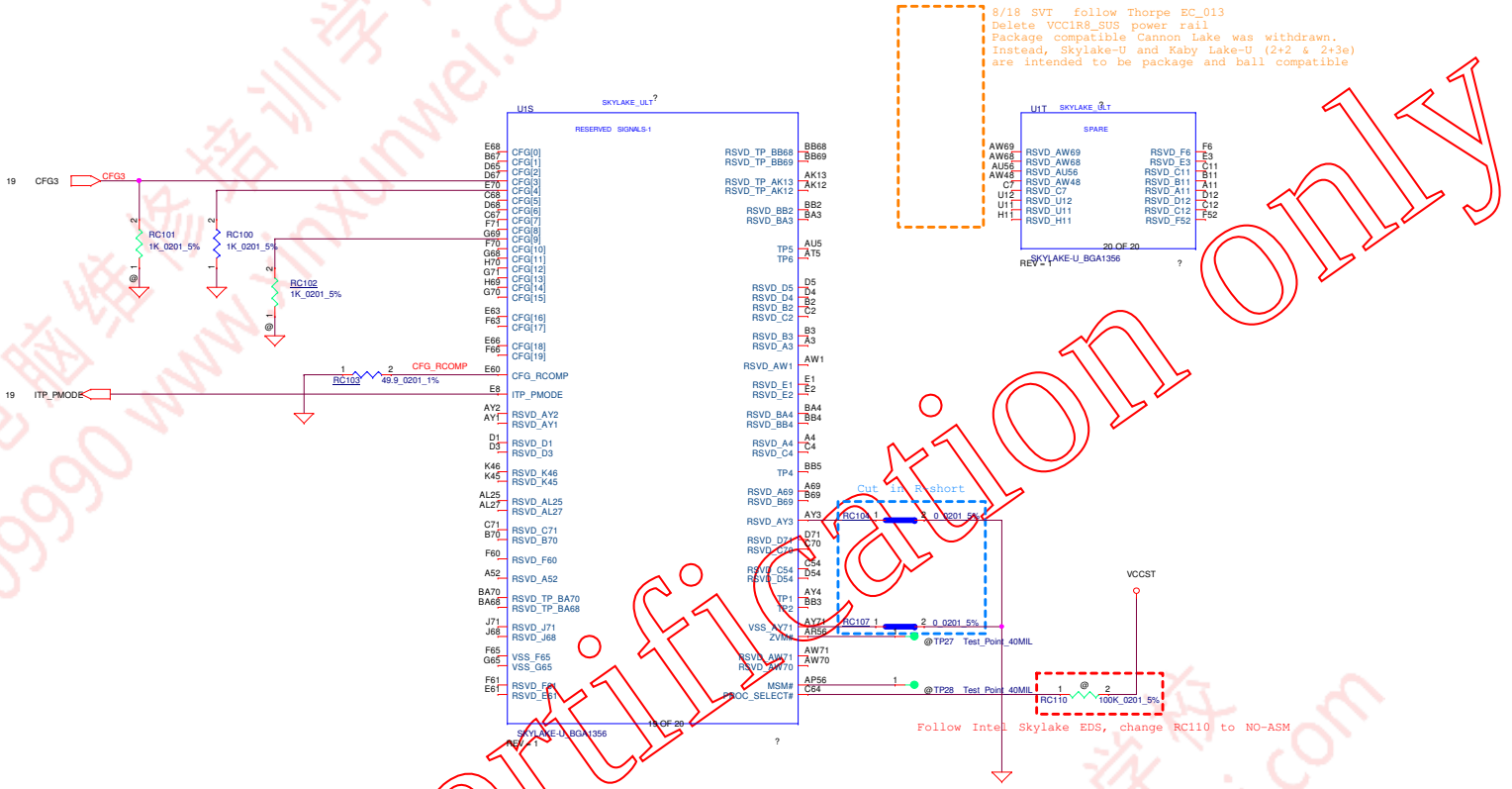
TABLE

CFG0 : Stall Reset Sequence **after PCU PLL Lock until de-asserted** **1 : No Stall** **0 : Stall**
CFG4 : eDP Enable **1 : Disabled** **0 : Enabled**
CFG9 : SVID Bus Communication **1 : Enabled** **0 : Disabled**



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Title	CPU(16/16) : CFG/RESERVED	
Size: Custom	Document Number: WOLV RIN 3 UMA	Rev: 0.1
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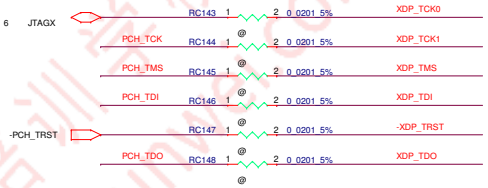

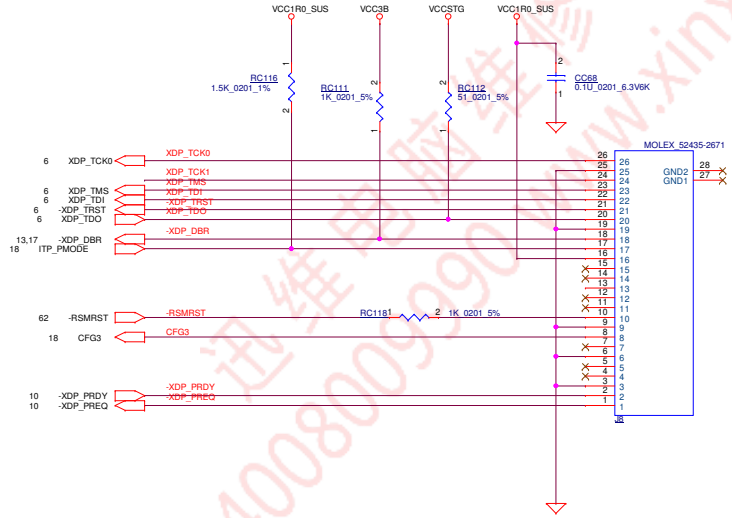

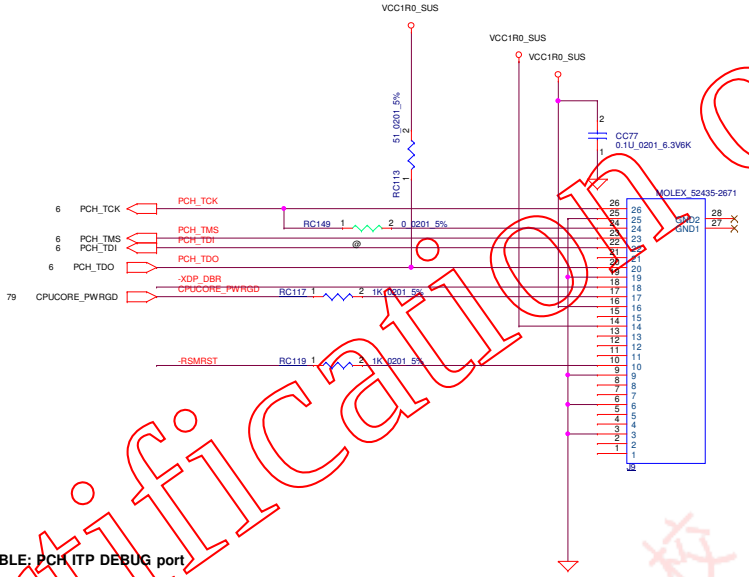

TABLE: CPU ITP DEBUG PORT

SIGNAL	REF DES	Planar only	BOX
TDO	RC109	ASM	ASM
TRST#	RC113	ASM	ASM
DBRST#	RC110	ASM	ASM
RESET#	RC111	ASM	ASM
PWRGD	RC112	ASM	ASM
CONNECTOR	J8	ASM	NO ASM

NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

TABLE: PCH ITP DEBUG port

SIGNAL	REF DES	Planar only	BOX
TDO	RC114	ASM	ASM
TMS	RC116	ASM	ASM
TDI	RC115	ASM	ASM
TCK	RC117	ASM	ASM
CPUCORE_PWRGD	RC118	ASM	ASM
-RSMRST	RC119	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

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Title: XDP CONNECTOR

Size	Document Number	Rev
Custom	WOLV RIN 3 UMA	0.1

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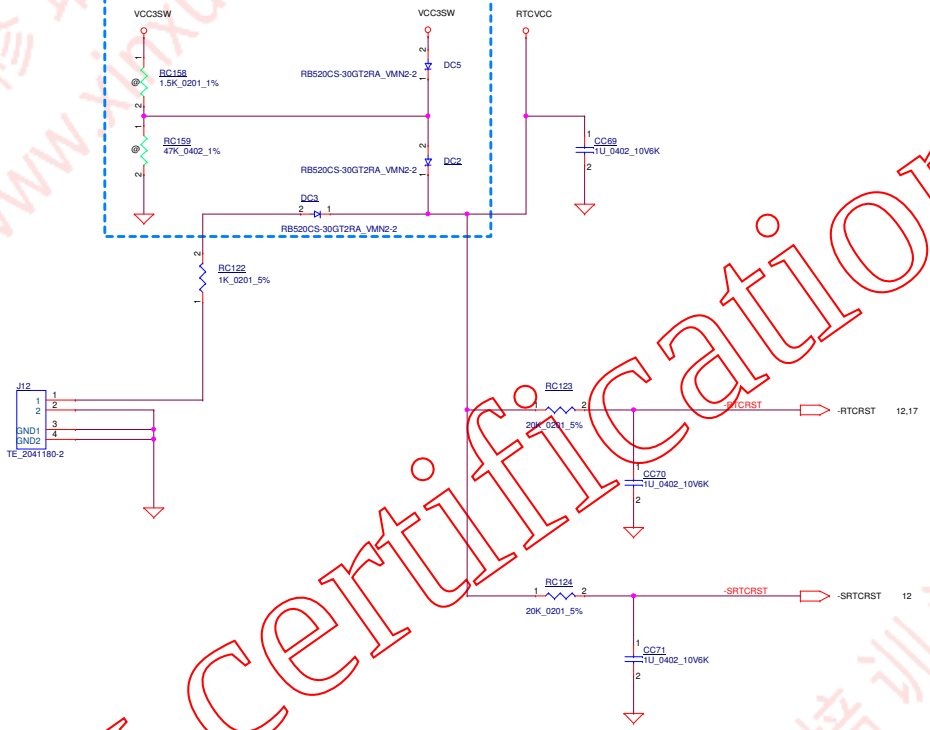
Follow THP1_SWG_SIT_EC022
Update Assembly Option of RTCVCC External Circuit



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Title: RTC BATTERY

Size	Document Number	Rev
Custom	WOLV RIN 3 UMA	0.1

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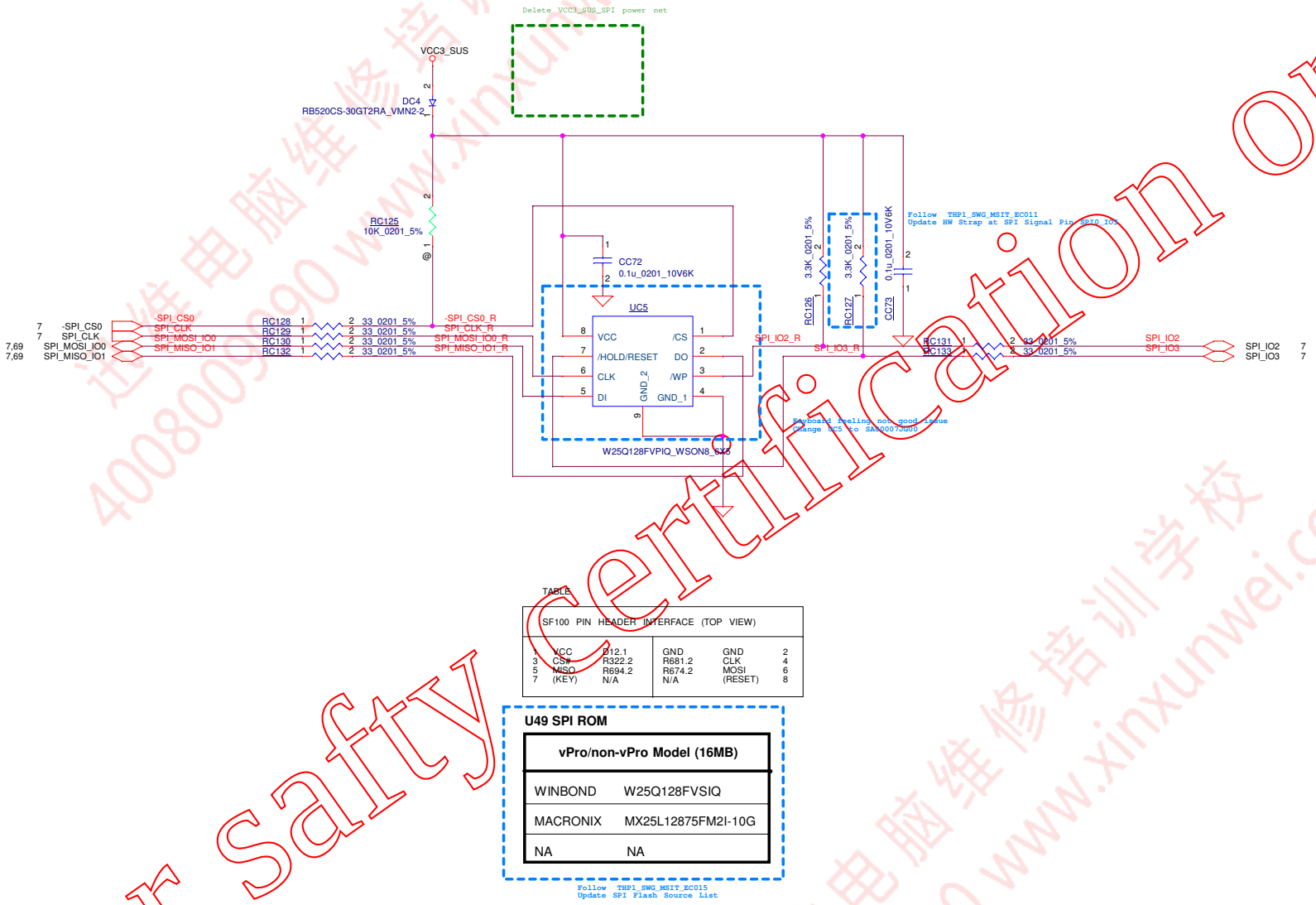

TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)				
1	VCC	D12.1	GND	2
3	CS#	R322.2	GND	4
5	MISO	R694.2	CLK	6
7	(KEY)	N/A	MOSI (RESET)	8
			N/A	

U49 SPI ROM

vPro/non-vPro Model (16MB)	
WINBOND	W25Q128FVSIQ
MACRONIX	MX25L12875FM2I-10G
NA	NA

Follow THP1_SWG_MSIT_EC015
Update SPI Flash Source List

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Title	SPI FLASH		
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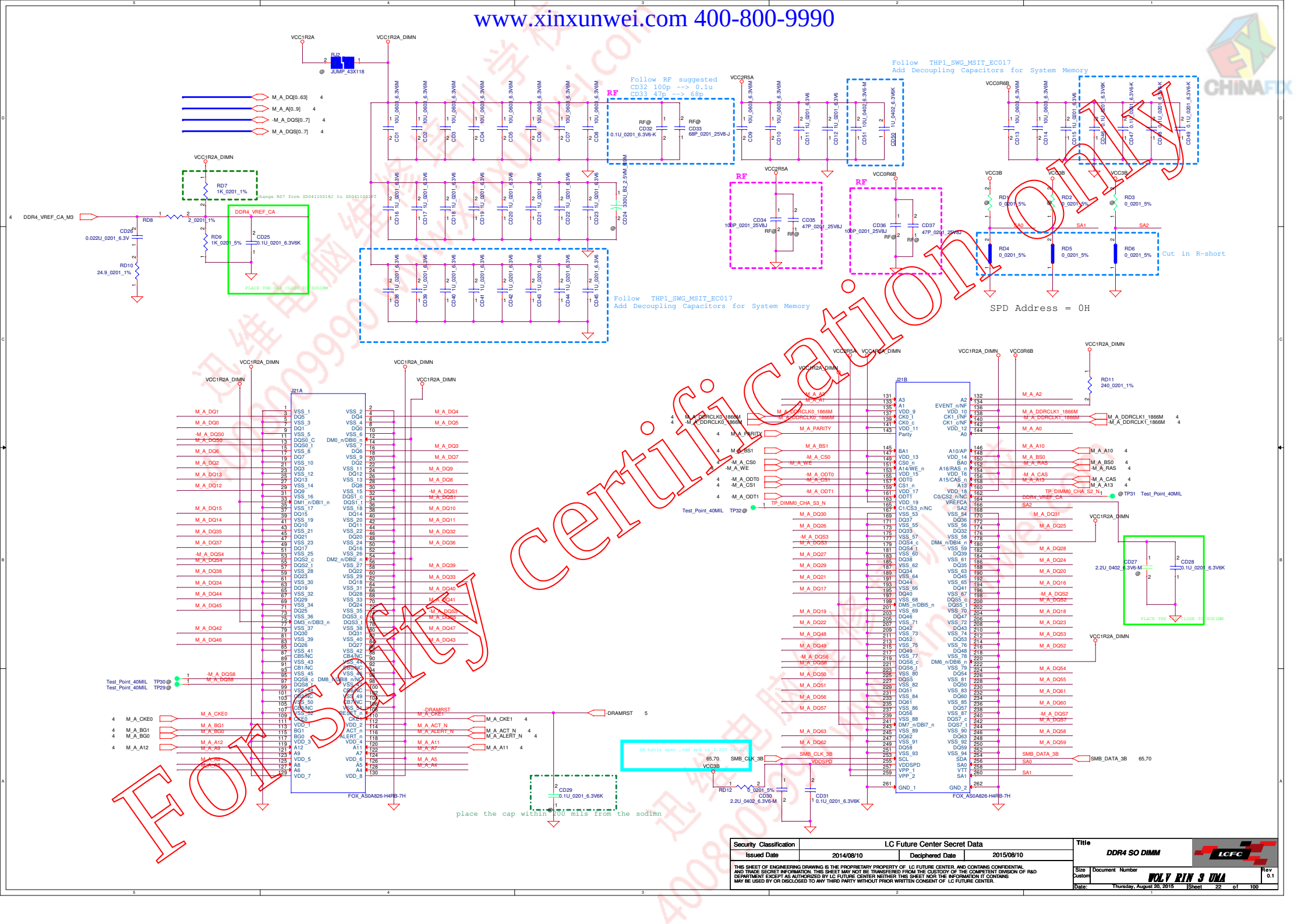

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Title	DDR4 SO DIMM		
Size	Document Number		Rev
Custom	WOLV RIN 3 UMA		0.1
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VCC3B — RX55 1 — 2 0 0603 5% — VCC3B_PS8338B

Reserved 0 ohm for power consumption test

VCC3B_PS8338B

Change power rail name for VCC3B_PS8338B

0.01U_0201_10V7K CX18 · 0.1U_0201_6.3V6K C16 · 0.1U_0201_6.3V6K CX2 · 0.1U_0201_6.3V6K CX4 · 0.01U_0201_10V7K CX17

UX1

VDD33_1 VDD33_2 VDD33_3 VDD33_4 VDD33_5

3 DDIP2_HPD — IN_HPD — IN_CA_DET

VCC3B — RX30 4.7K_0402_5% — RX31 4.7K_0402_5%

3 DDIP2_0P — CX5 0.1U_0201_6.3V6K — DDIP2_0P_C — IN_D0p
3 DDIP2_0N — CX6 0.1U_0201_6.3V6K — DDIP2_0N_C — IN_D0n
3 DDIP2_1P — CX7 0.1U_0201_6.3V6K — DDIP2_1P_C — IN_D1p
3 DDIP2_1N — CX8 0.1U_0201_6.3V6K — DDIP2_1N_C — IN_D1n
3 DDIP2_2P — CX9 0.1U_0201_6.3V6K — DDIP2_2P_C — IN_D2P
3 DDIP2_2N — CX10 0.1U_0201_6.3V6K — DDIP2_2N_C — IN_D2n
3 DDIP2_3P — CX11 0.1U_0201_6.3V6K — DDIP2_3P_C — IN_D3p
3 DDIP2_3N — CX12 0.1U_0201_6.3V6K — DDIP2_3N_C — IN_D3n

3 DDIP2_AUXP — DDIP2_AUXP — CX14 0.1U_0201_6.3V6K — DDIP2_AUXP_C — IN_AUXp
3 DDIP2_AUXN — DDIP2_AUXN — CX13 0.1U_0201_6.3V6K — DDIP2_AUXN_C — IN_AUXn

3 DDIP2_CTRLCLK — IN_DDC_SCL
3 DDIP2_CTRLDATA — IN_DDC_SDA

I2C_CTL_EN

Test_Point_40MIL TP34@ — PS8338_PI1 — PI1/SCL_CTL
Test_Point_40MIL TP35@ — PS8338_PI0 — PI0/SDA_CTL

CEXT REXT

CX15 2.2U_0402_6.3V6-M — RX2 4.99K_0201_1% — VCC3B — RX32 4.7K_0402_5% — CFG0 CFG1

VCC3B — RX26 4.7K_0402_5% — PD SW

OUT1_D0p OUT1_D0n OUT1_D1p OUT1_D1n OUT1_D2p OUT1_D2n OUT1_D3p OUT1_D3n → DOCK_DDIP2_0P DOCK_DDIP2_0N DOCK_DDIP2_1P DOCK_DDIP2_1N DOCK_DDIP2_2P DOCK_DDIP2_2N DOCK_DDIP2_3P DOCK_DDIP2_3N

OUT2_D0p OUT2_D0n OUT2_D1p OUT2_D1n OUT2_D2p OUT2_D2n OUT2_D3p OUT2_D3n → DMUX_DDIP2_0P DMUX_DDIP2_0N DMUX_DDIP2_1P DMUX_DDIP2_1N DMUX_DDIP2_2P DMUX_DDIP2_2N DMUX_DDIP2_3P DMUX_DDIP2_3N

OUT1_AUXn_SDA OUT1_AUXp_SCL OUT2_AUXn_SDA OUT2_AUXp_SCL → DOCK_DDIP2_AUXN DOCK_DDIP2_AUXP DMUX_DDIP2_AUXN DMUX_DDIP2_AUXP

OUT1_HPD OUT2_HPD → DOCK_DDIP2_HPD DMUX_DDIP2_HPD

OUT1_CA_DET OUT2_CA_DET → DMUX_DDIP2_CADET

PC10 PC11 PC20 PC21 PEQ → PS8338_PC10 PS8338_PC11 PS8338_PC20 PS8338_PC21 PS8338_PEQ

GND1 GND2 GND3 GPAD

PS8338BQFN60ETR-A1_QFN60_5X9

1M_0402_5% RX21 · 1M_0402_5% RX54

Follow thorpe priority setting

PRIORITY : DOCKING>HDMI>WIGIG

TABLE : Automatic Switching Mode (CFG0 = H) 9 DDI_PRIORITY2

SW (DDI_PRIORITY2)
Port 1 has higher priority when both ports are plugged
Port 2 has higher priority when both ports are plugged

VCC3B

RX9 @ 4.7K_0402_5% — PS8338_PEQ — RX10 @ 4.7K_0402_5%
RX11 @ 4.7K_0402_5% — PS8338_PC10 — RX12 @ 4.7K_0402_5%
RX13 @ 4.7K_0402_5% — PS8338_PC11 — RX14 @ 4.7K_0402_5%
RX15 @ 4.7K_0402_5% — PS8338_PC20 — RX16 @ 4.7K_0402_5%
RX17 @ 4.7K_0402_5% — PS8338_PC21 — RX18 @ 4.7K_0402_5%
RX37 @ 4.7K_0402_5% — PS8338_PI0

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Title: DP SWITCH

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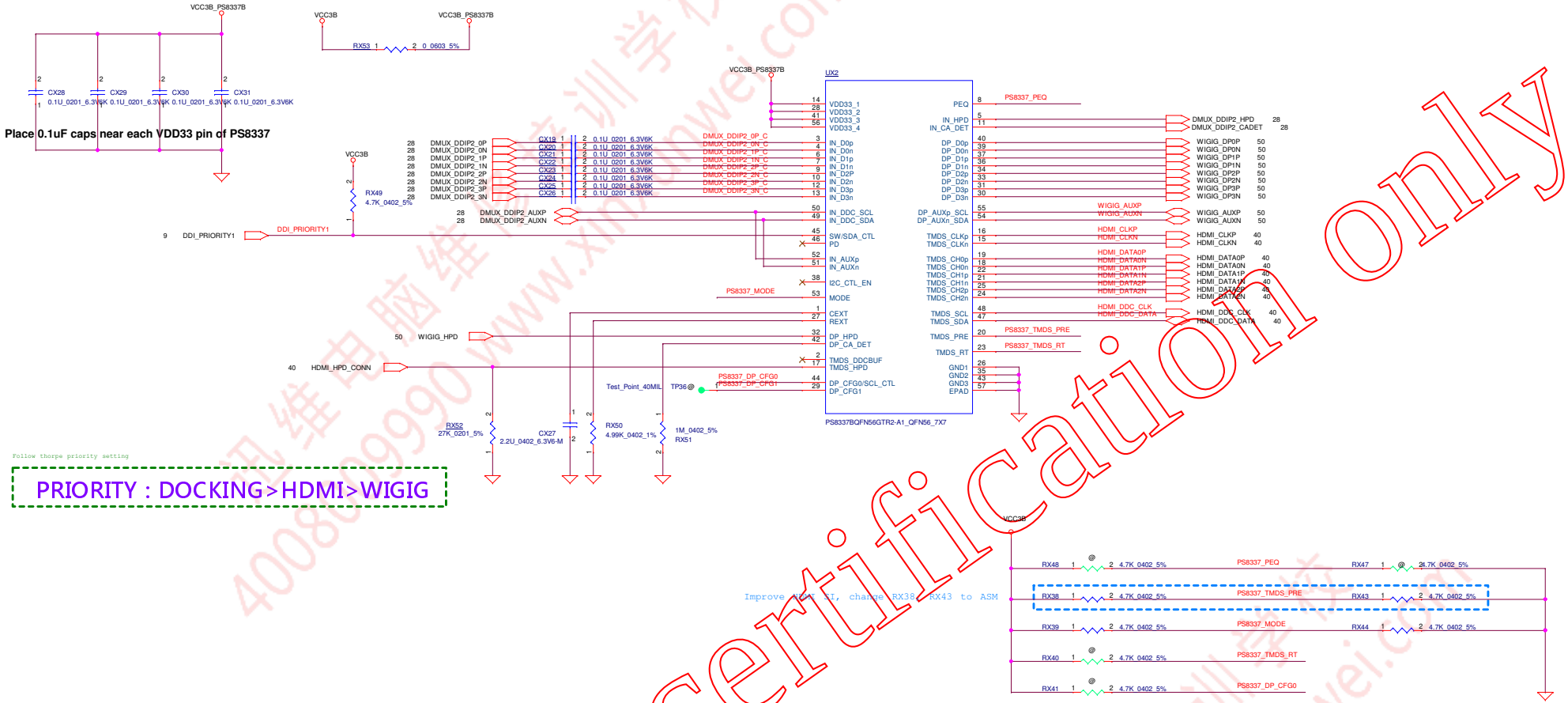

Follow thorpe priority setting

PRIORITY : DOCKING>HDMI>WIGIG

Improve ACAT SI, change RX38~RX43 to ASM

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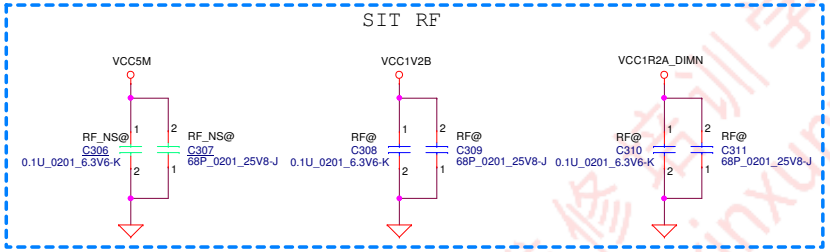
SIT RF



Follow RF suggested, add by pass capacitance to GND

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Title: RF Component

Size	Document Number	Rev
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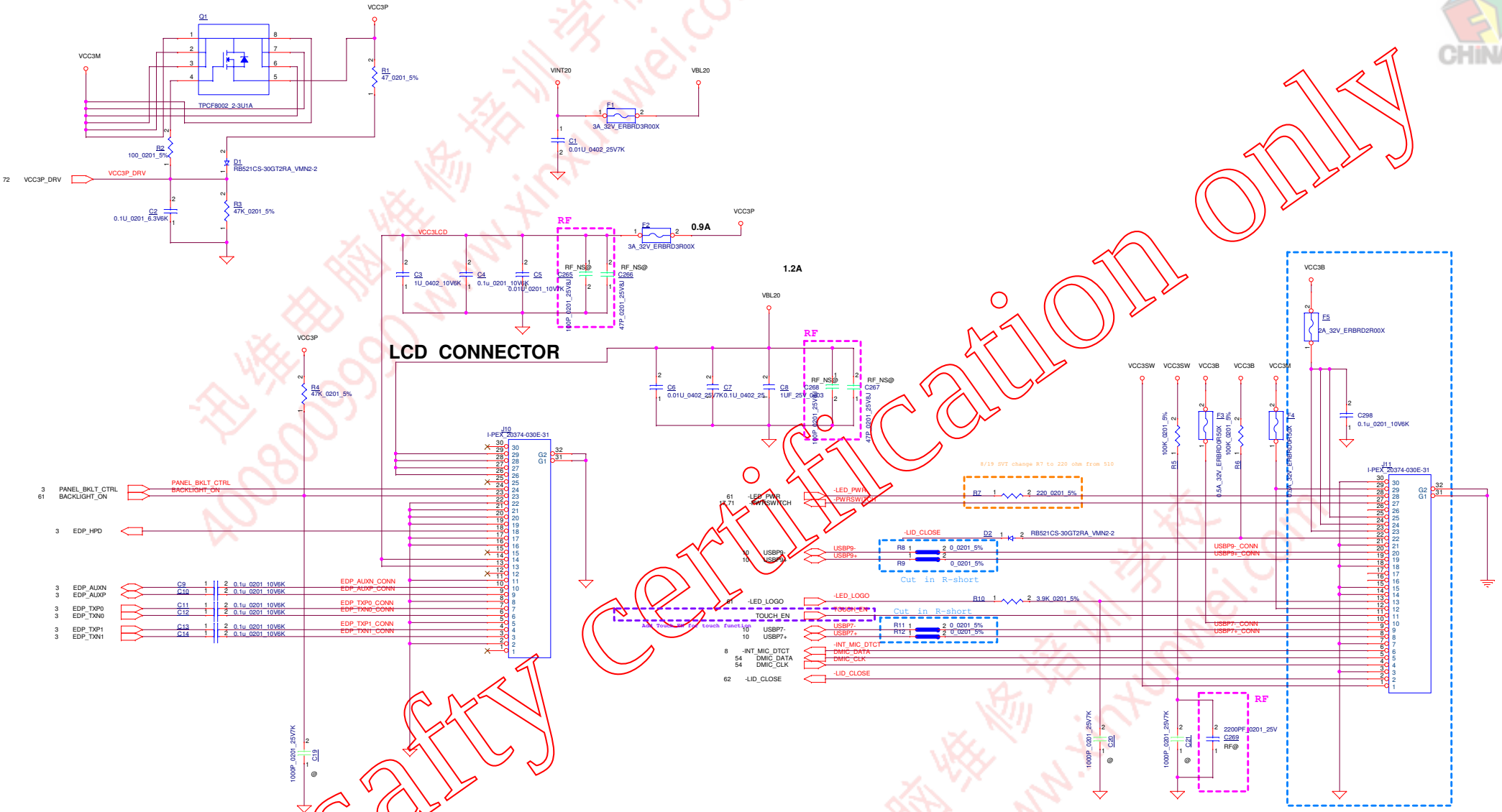

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Title: LCD/LID/MIC/CAMERA/PWR SW

Size	Document Number	Rev
Custom	WOLV RIN 3 UMA	0.1

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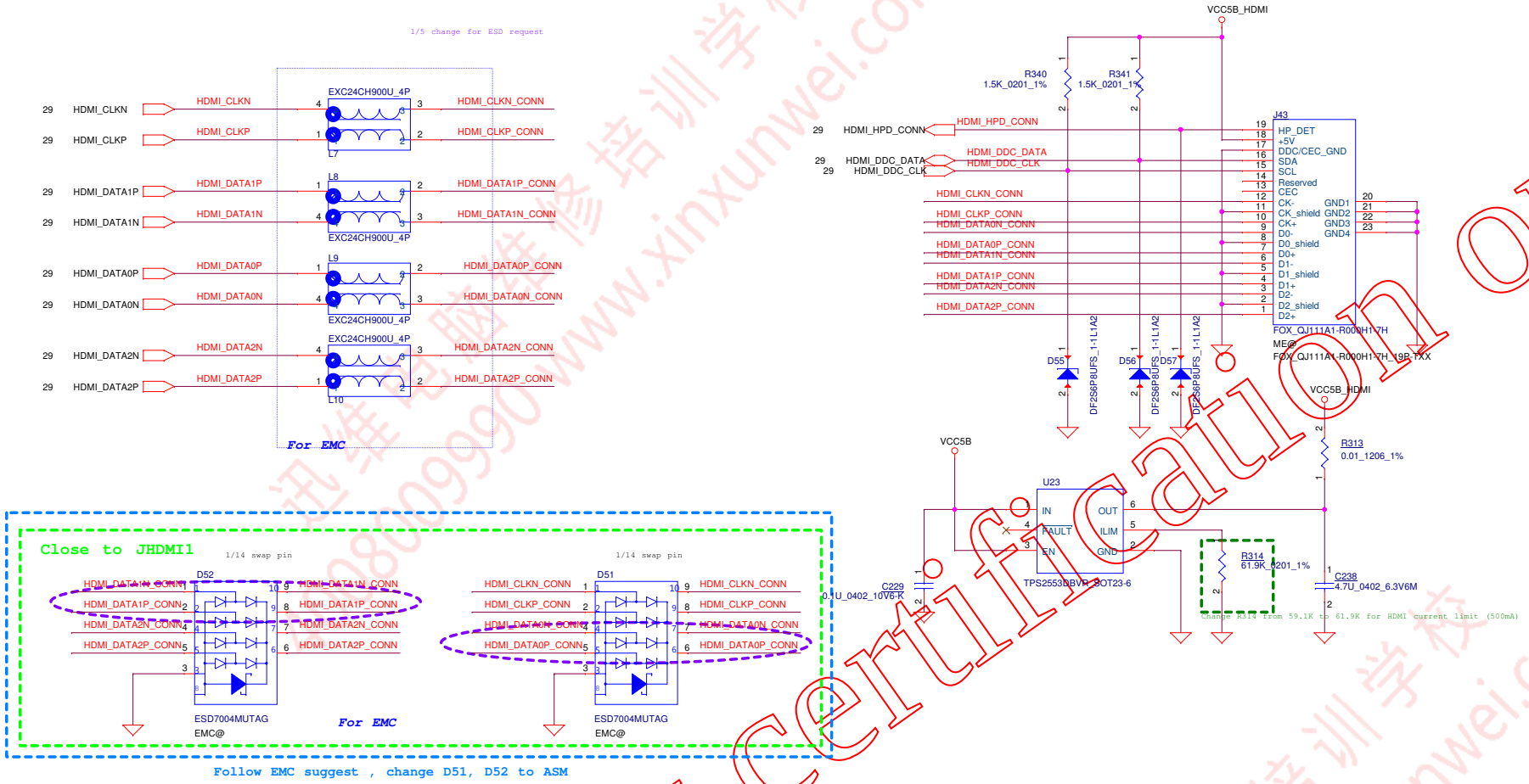

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Title: HDMI CONNECTOR

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Custom	WOLVERINE3 UMA	0.1

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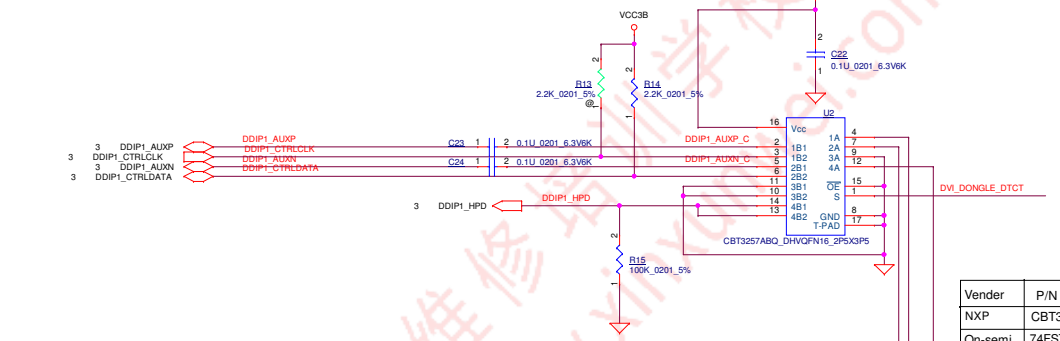
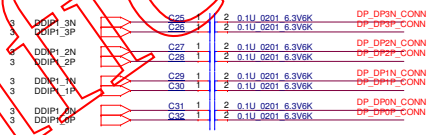
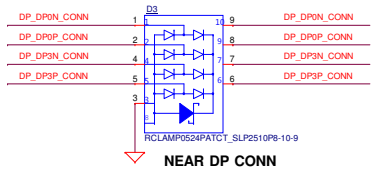
FOR SYSTEM DP NEAR DP CONN

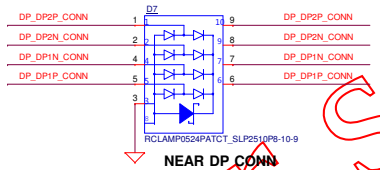


Vender	P/N
NXP	CBT3257ABQ
On-semi	74FST3257MNTWG





NEAR DP CONN



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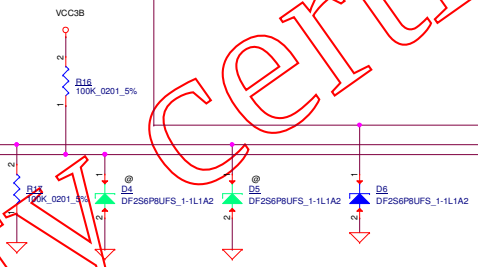
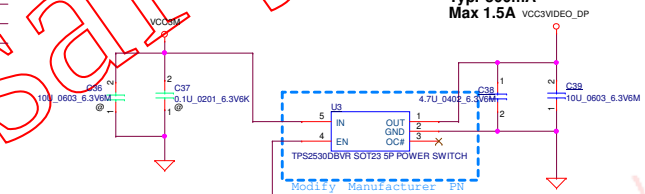
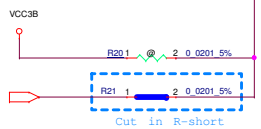


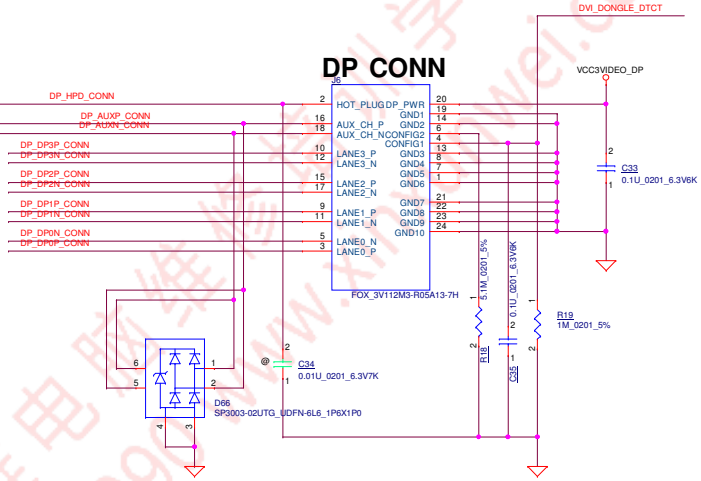
NEAR DP CONN

Typ. 500mA
Max 1.5A





Vender	P/N
TI	TPS2530
On-semi	NCP380HSN05AAT1G



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Title: DISPLAY PORT CONNECTOR

Size	Document Number	Rev
Custom	WOLY_P1N_3_UMA	0.1

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Size: Custom	Document Number: WOLVERINE3 UMA	Rev: 0.1
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OE=L , DISCONNECT
OE=H, A PORT = B PORT

7/10 Add for WD HDD can't power on when peak cable plug into SATA HDD

IFDET
SATA Device GND
PCIe Device 5K PU to Vsource

30	E9	CLKDET
29	E8	REFCLKN
28	E7	REFCLKP
27	S1	GND
26	S2	PETP0/A+
25	S3	PETN0/A-
24	S4	GND
23	S5	PERN0/B-
22	S6	PERP0/B+
21	S7	GND
20	S8	GND
19	S9	PETP1
18	S10	PETN1
17	S11	GND
16	S12	PERN1
15	S13	PERP1
14	S14	GND
13	P2	PERST#
12	P3	CLKREQ#/DEVSLP
11	P4	IFDET
10	P5	GND
9	P6	GND

Add 1K ohm to avoid HDD issue

Follow EMC suggestion, add 0.1uf on -HDD_DTCT

Follow EMC suggestion
Change C75 to 0.1uf

Follow RF suggestion
C271 100p --> 68p
C301 68p --> 0.1u

J1 PINS/9 change to NC for assembly issue

7/10 delete J1pin2 for follow SATA/ SATA EXPRESS spec

CLKDET (DEVICE)
Requires the common RefClk -->GND
Supports SRIS --> not GND

OE=L , DISCONNECT
OE=H, A PORT = B PORT

Mode Configuration Table

EN#	MODE	MODE
0	0	SATA Application
0	1	PCIe Application
1	X	Disable

Equalization Setting:

EQ_A/B are the selection pins for the equalization selection for each direction.

Equalizer setting		
EQ_A/B	@3GHz	@4GHz
0	7dB	8dB
open	4dB (default)	5dB (default)
1	10dB	11dB

De-Emphasis Setting (for PCIe only):

Output DE-Emphasis Setting	
DE	DE-Emphasis
0	-2.5 dB
open	0dB (Default)
1	-4dB

Improve SATA eye diagram, change R348, R349 to ASM

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Title: SATA HDD CONNNECTOR

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Custom	WOLV RIN 3 UMA	0.1

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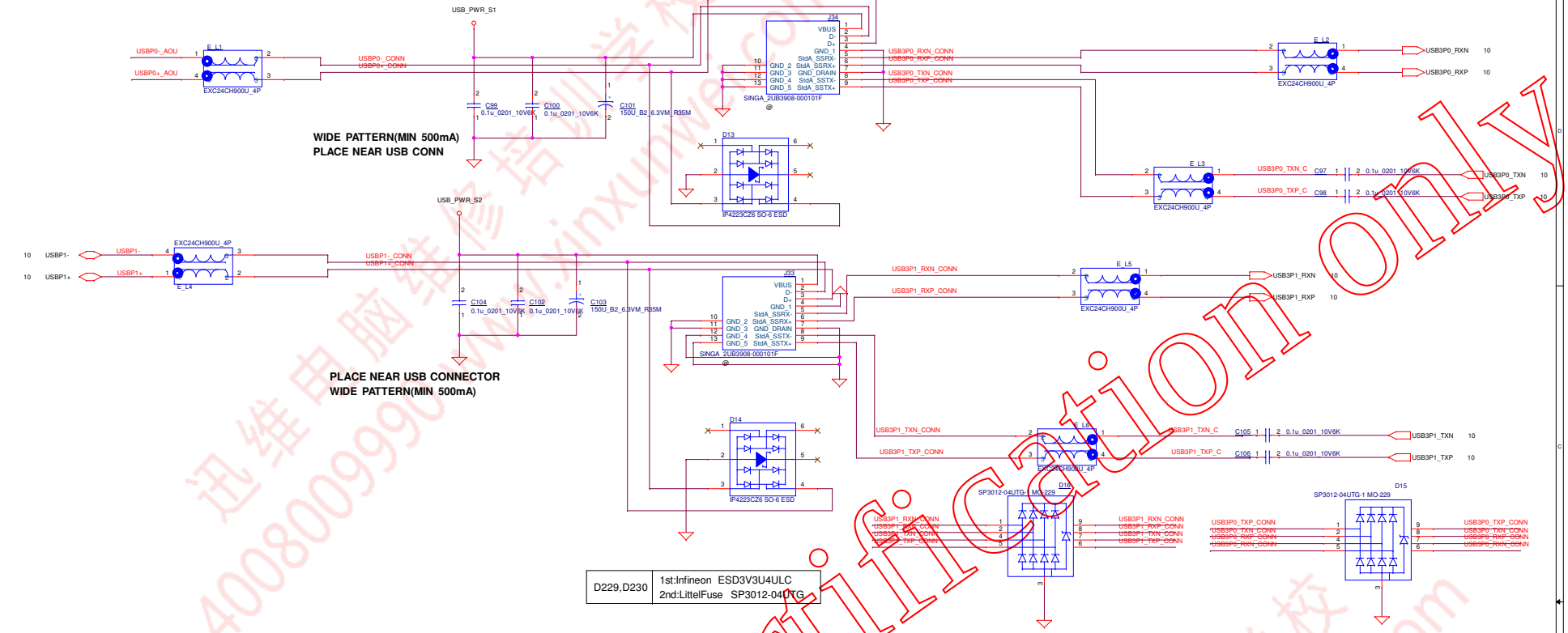
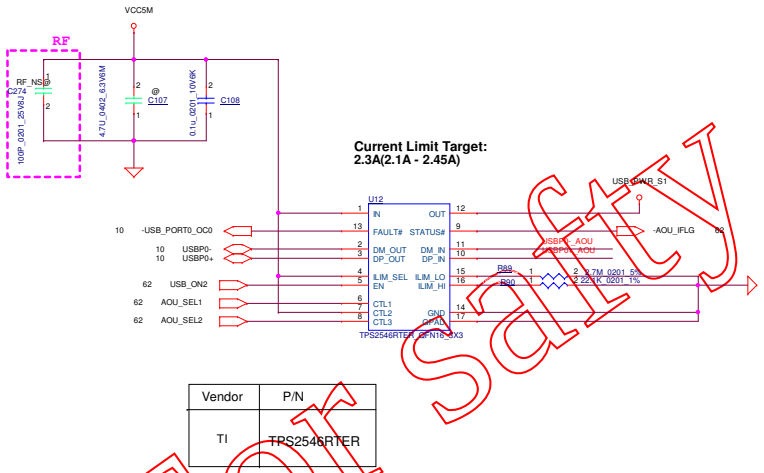


D229,D230	1st:Infineon ESD3V3U4ULC 2nd:LittelFuse SP3012-04UTG



Vendor	P/N
TI	TPS2546RTER

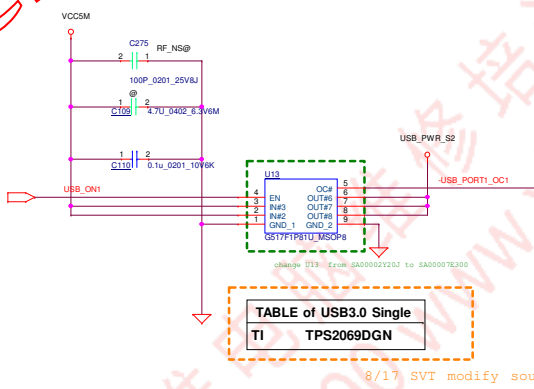


TABLE of USB3.0 Single	
TI	TPS2069DGN

8/17 SVT modify source table

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Title: USB POWER/CONNECTOR

Size	Document Number	Rev
Custom	VOLVERINES DMA	0.1

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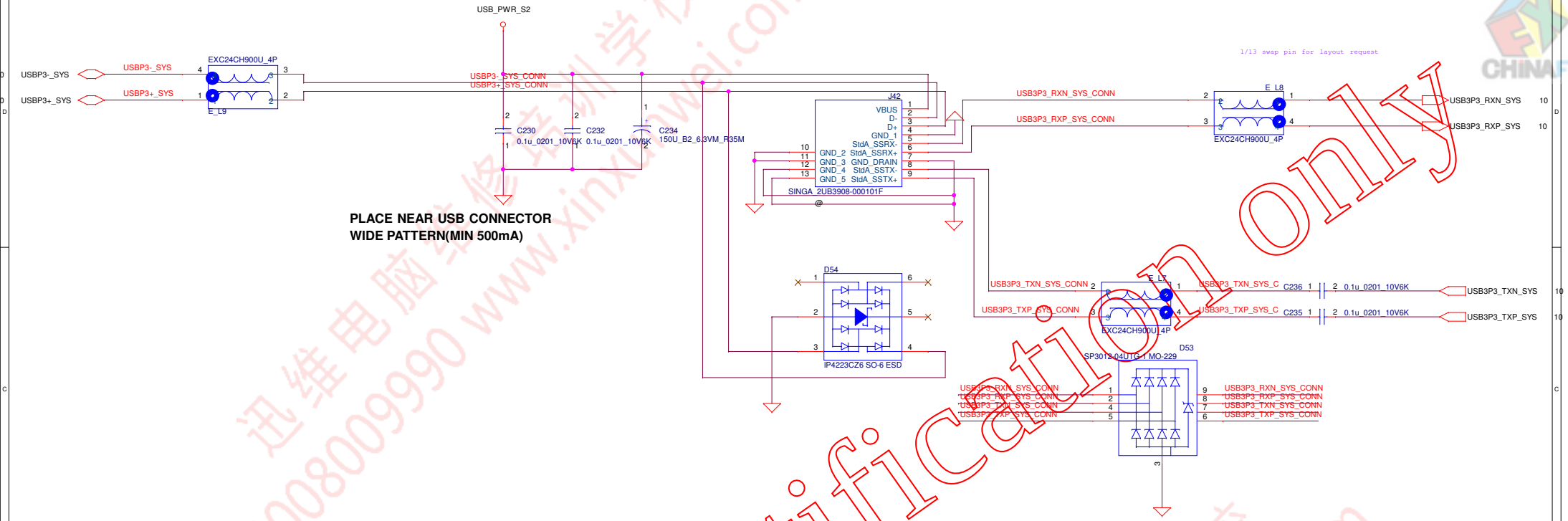

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Title: USB POWER/CONNECTOR

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.24

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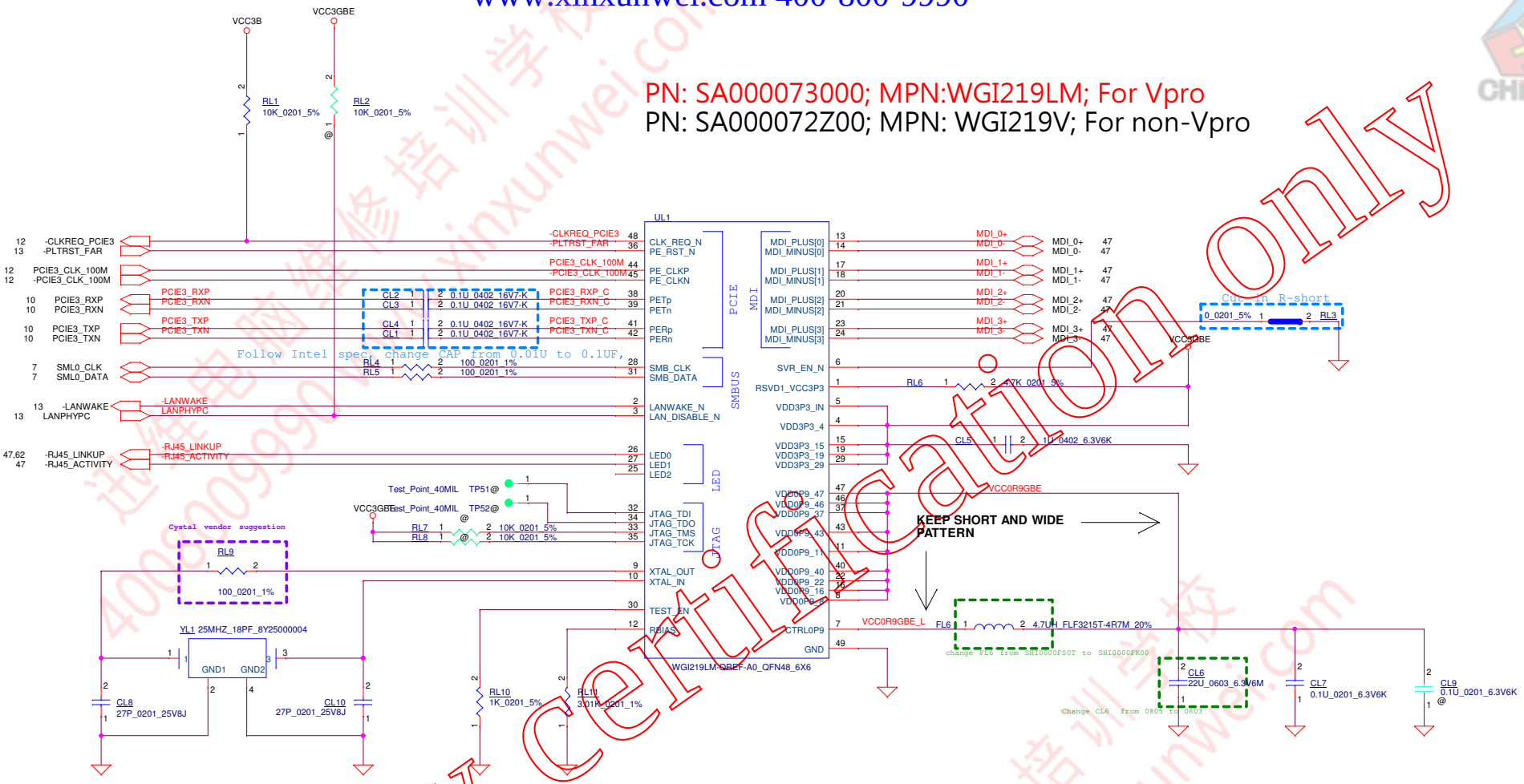
PN: SA000073000; MPN:WGI219LM; For Vpro
PN: SA000072Z00; MPN: WGI219V; For non-Vpro



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Title: GBE CLARKVILLE

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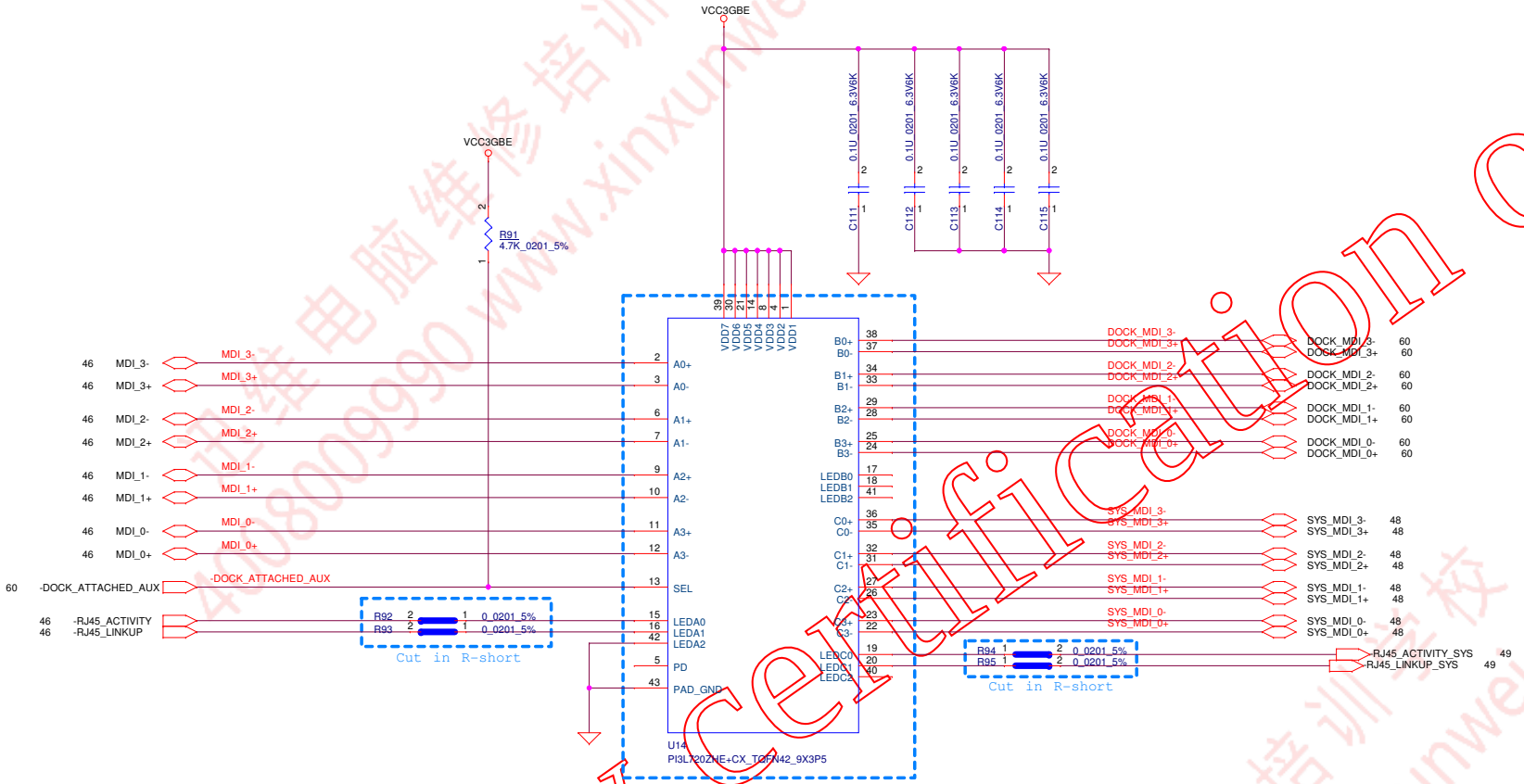

Change LAN switch to SA00007E900

U87

Vendor	P/N
Pericom ST micro Onsemi	PI3L720ZHE STMUX1800E NCN7201

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Title: GBE LAN SWITCH

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 47 of 100

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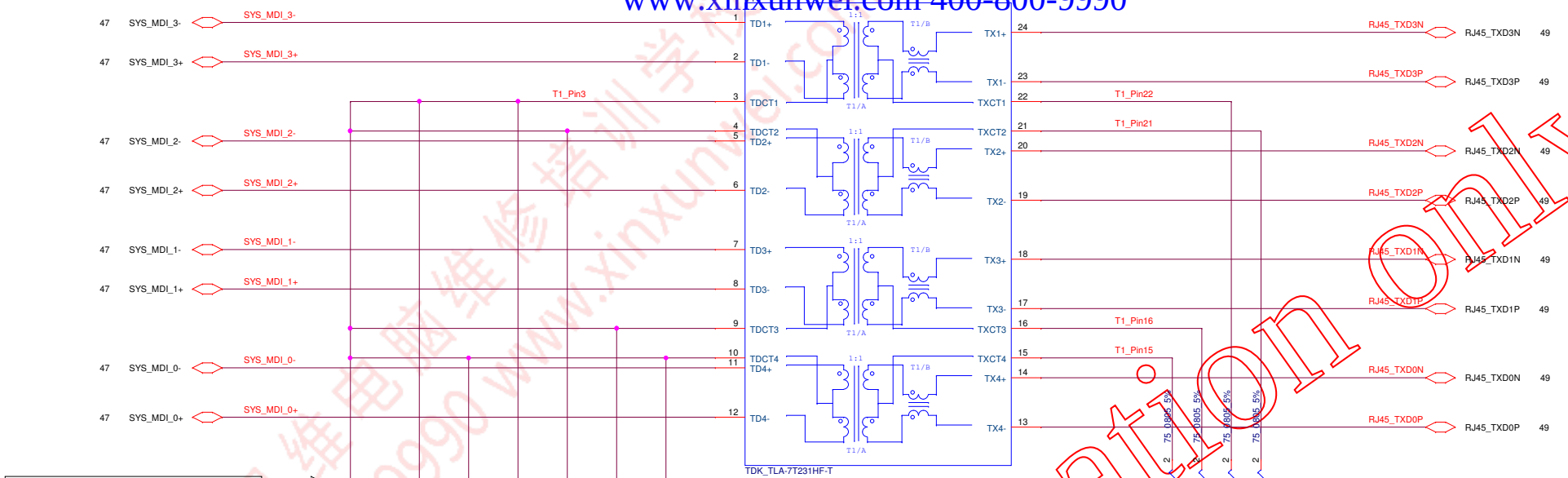


THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

C303
SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

1U 0402 6.3V6K
0.1U 0201 6.3V6K
C116 C117 C118 C119 C120 C121 C123

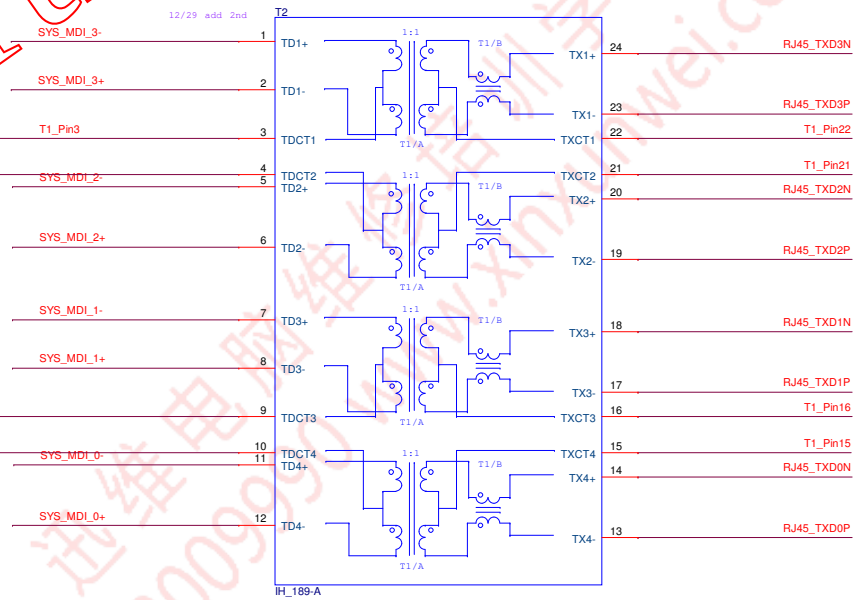
ESD REASON

PATTERN MUST BE SHORT AND WIDE.

R100 1M_0805_5%

C122 100P_1808_2KV

HIGH VOLTAGE 1500PF CAP IS OPTIONAL



Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF

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Title: GBE MAGNETICS

Size: Custom | Document Number: VOLVERINE3 UMA | Rev: 0.1

Date: Thursday, August 20, 2015 | Sheet 48 of 100

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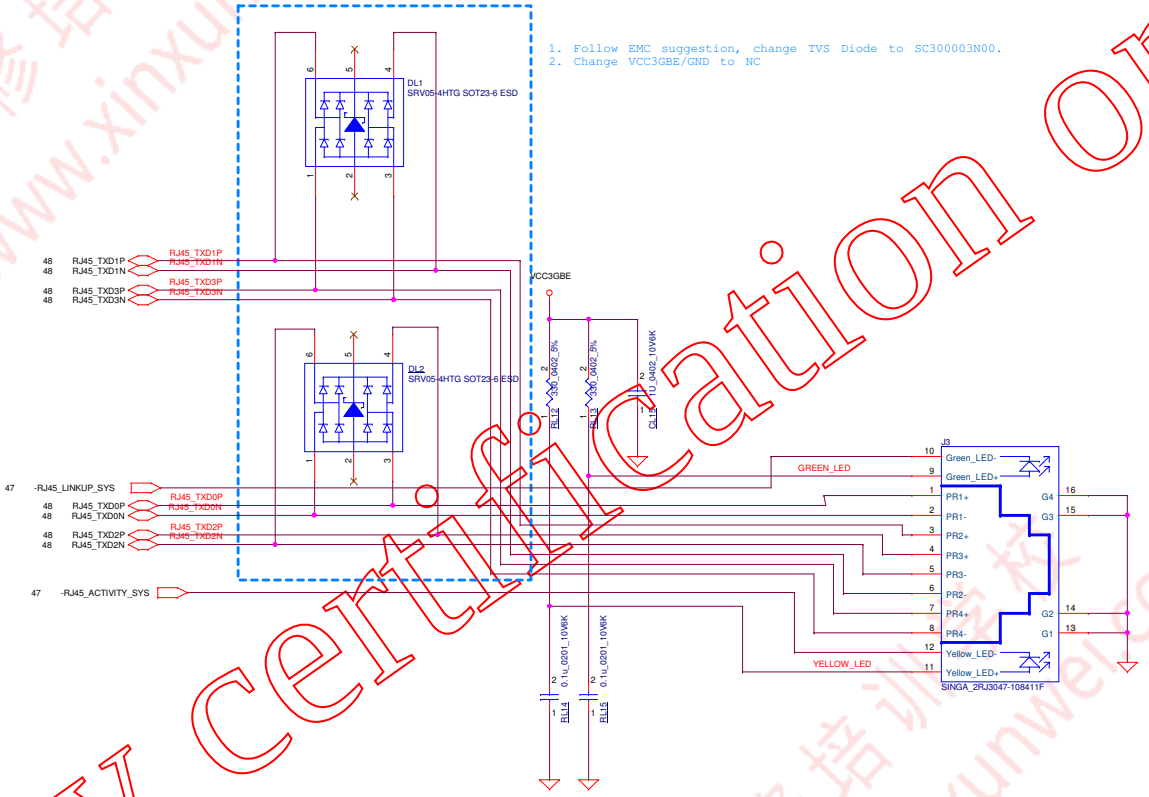

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Title: RJ45 CONNECTOR

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1
Date: Thursday, August 20, 2015	Sheet 49 of 100	

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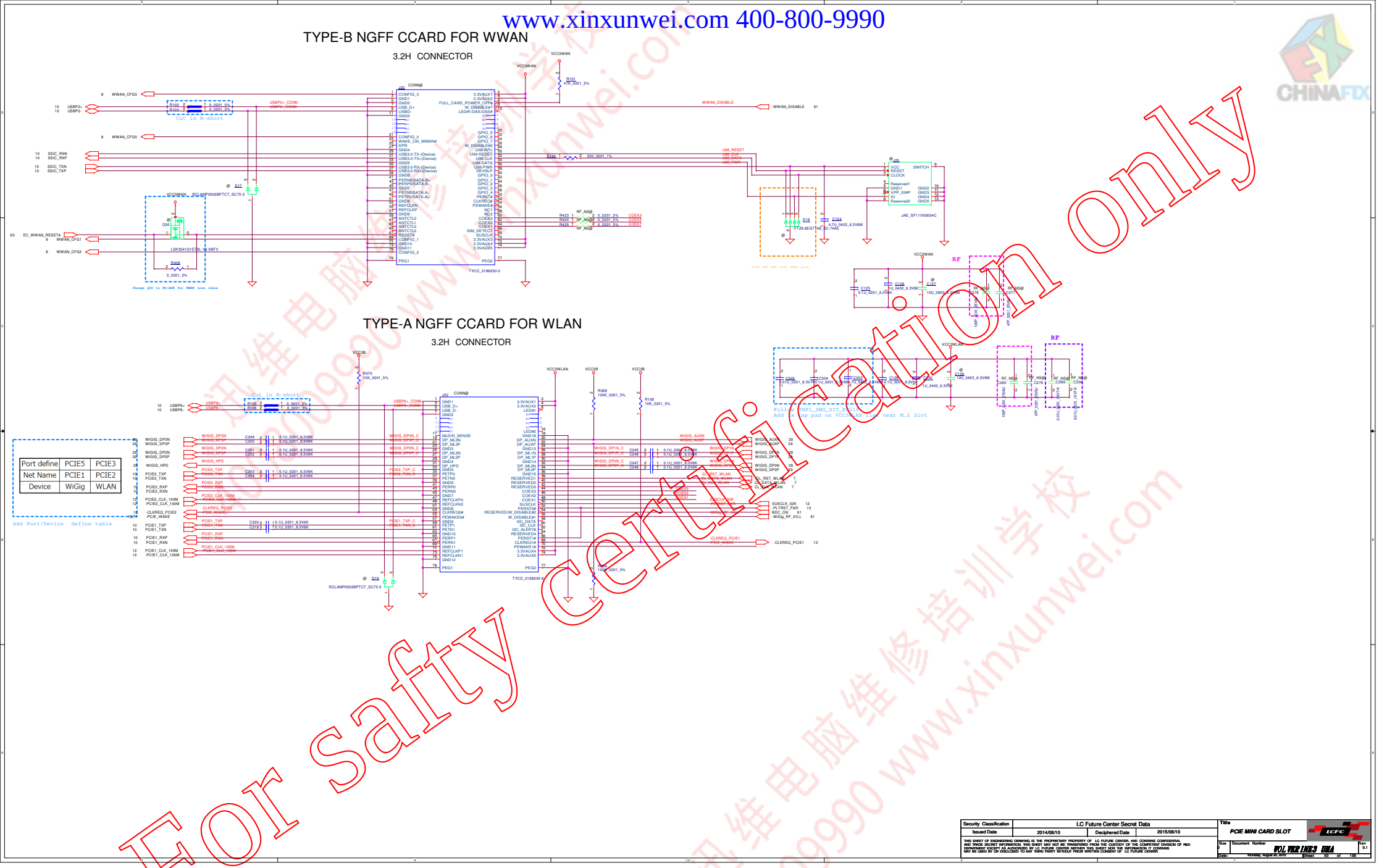

Port define	PCIE5	PCIE3
Net Name	PCIE1	PCIE2
Device	WiGig	WLAN

Security Classification	LC Future Center Secret Data		
Issued Date	2014/08/10	Deciphered Date	2015/08/10

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Title: PCIE MINI CARD SLOT

Size: D | Document Number: WOL VER INES UMA | Rev: 0.1

Date: Thursday, August 21, 2015 | Sheet 50 of 100

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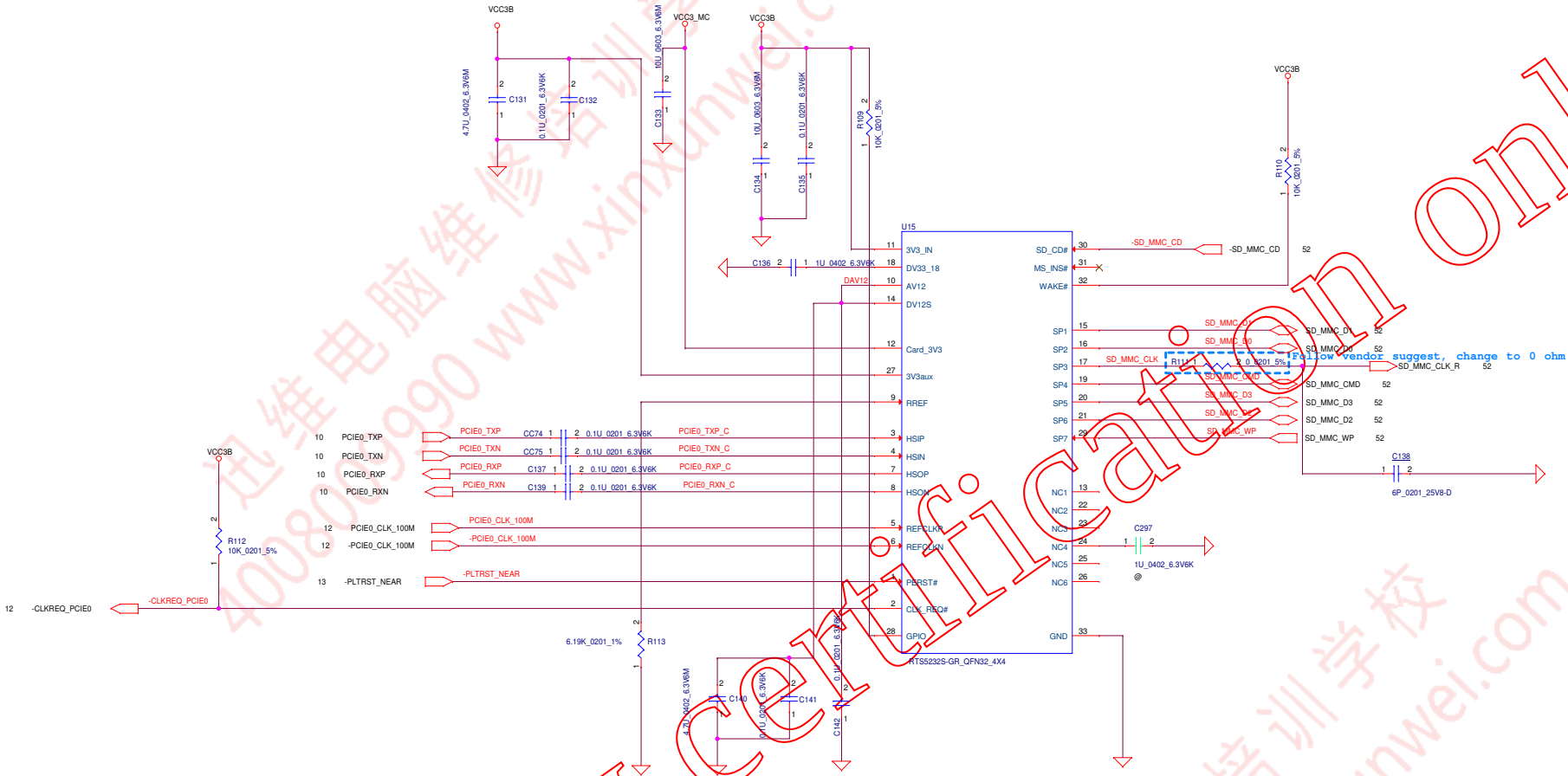

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Title: MEDIA CARD CONTROLLER

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 51 of 100

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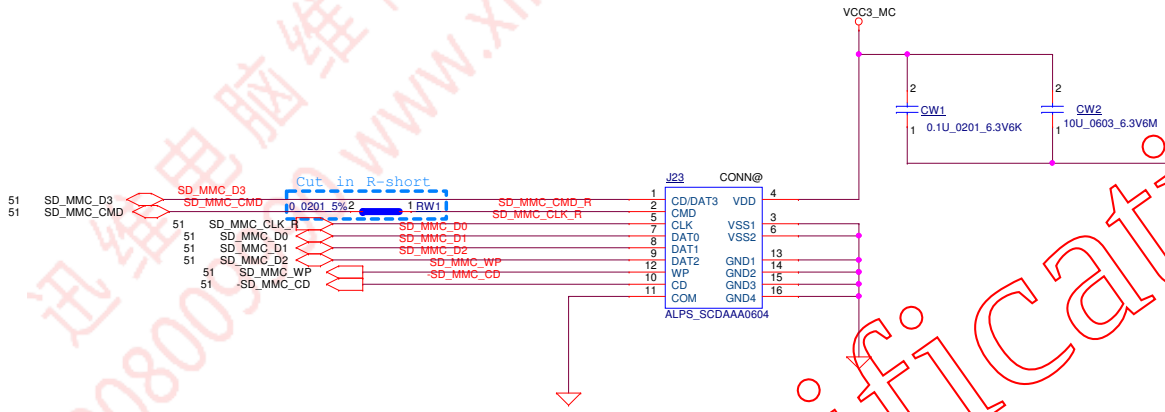

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Title: MEDIA CARD INTERFACE

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

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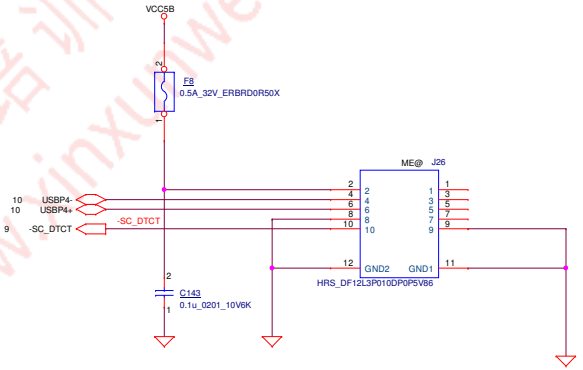

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Title: SMART CARD I/F

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 53 of 100

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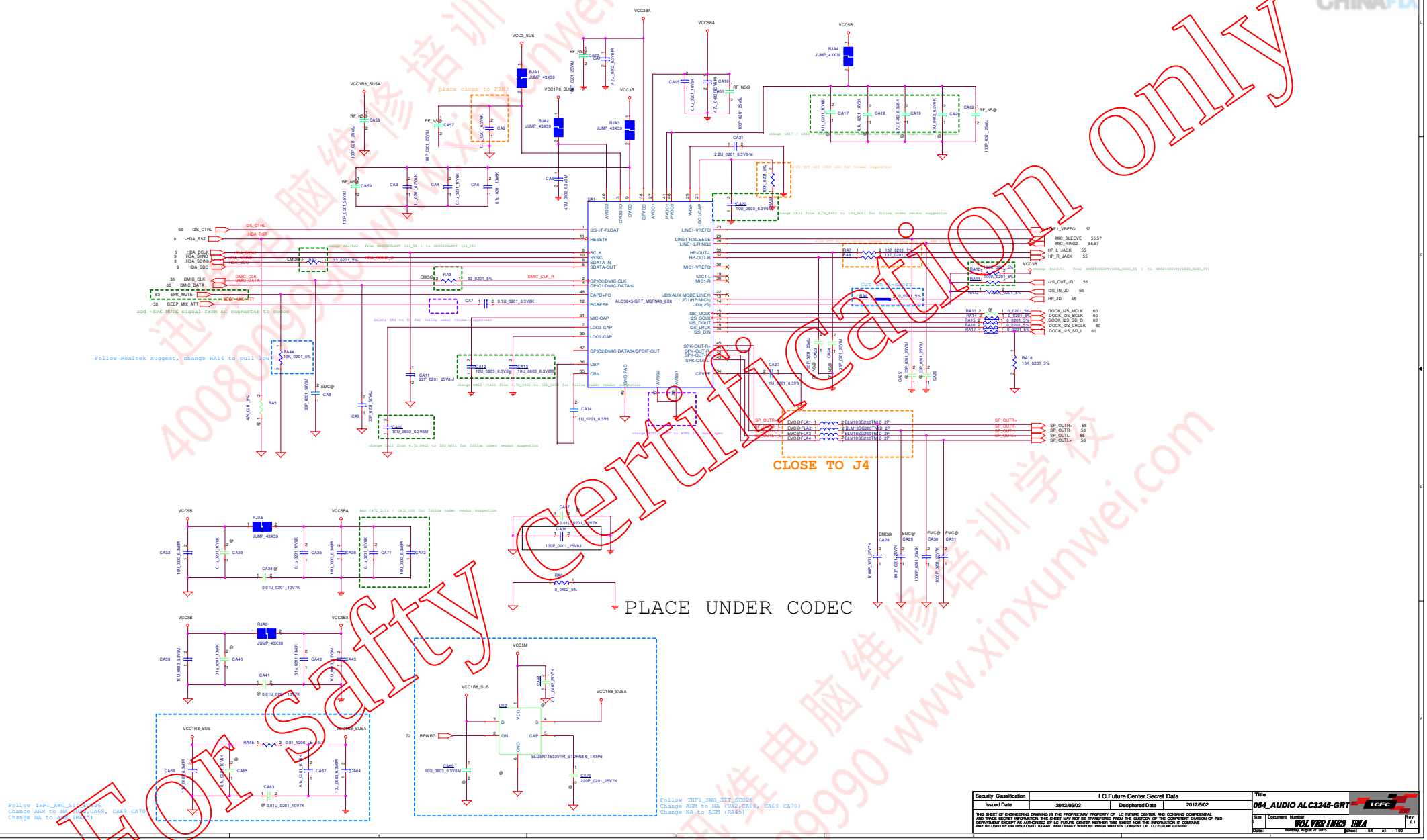

Security Classification	LC Future Center Secret Data			Title
Issued Date	2012/05/02	Deciphered Date	2012/5/02	054_AUDIO ALC3245-GRT

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Size: D | Document Number: WOLVERINES UMA | Rev: 0.1

Date: Thursday, August 27, 2015 | Sheet 54 of 100

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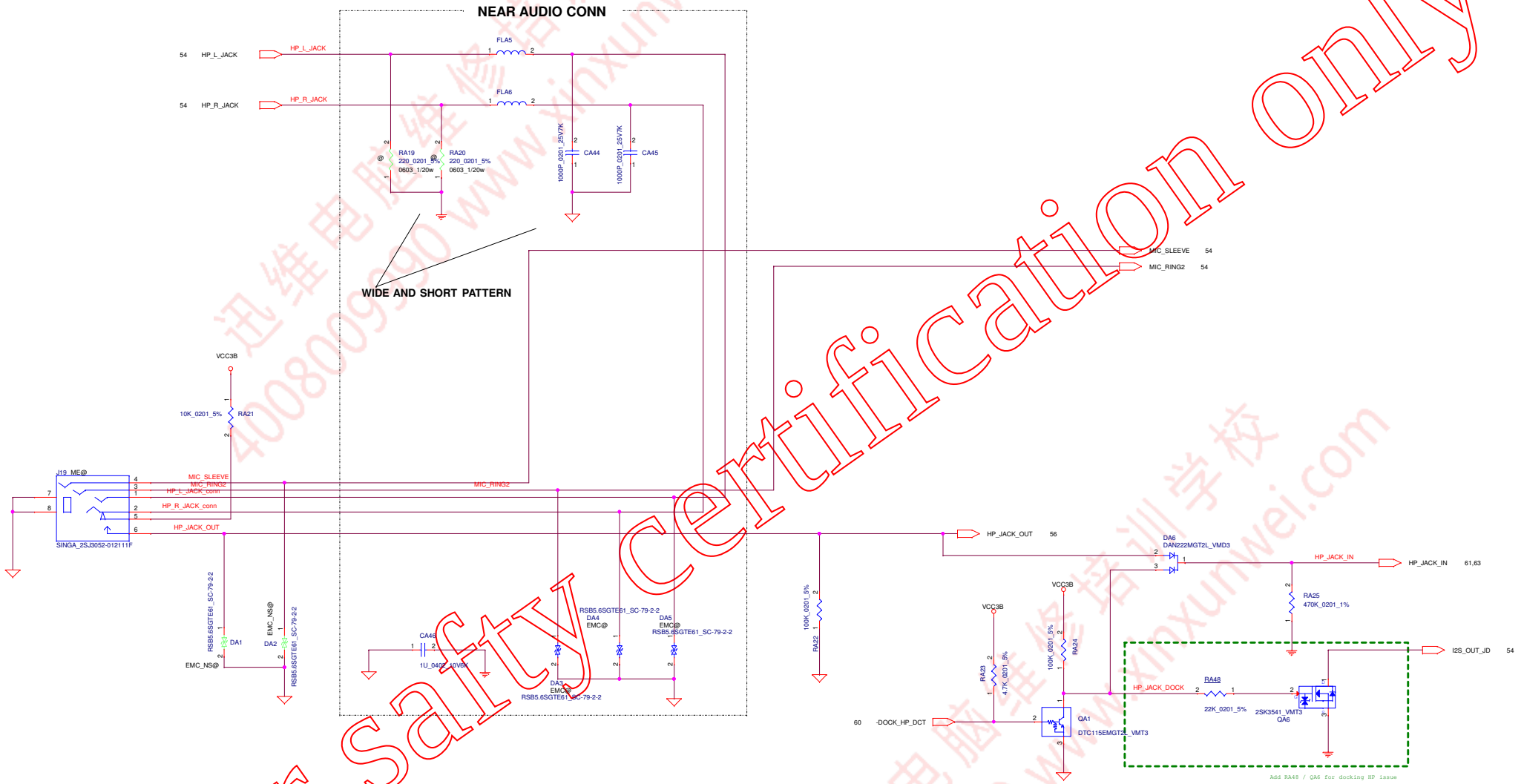

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Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: AUDIO CONNECTOR

Size	Document Number	Rev
Custom	C	0.1

WOLVERINE3 UMA

Date: Thursday, August 20, 2015 Sheet 55 of 100

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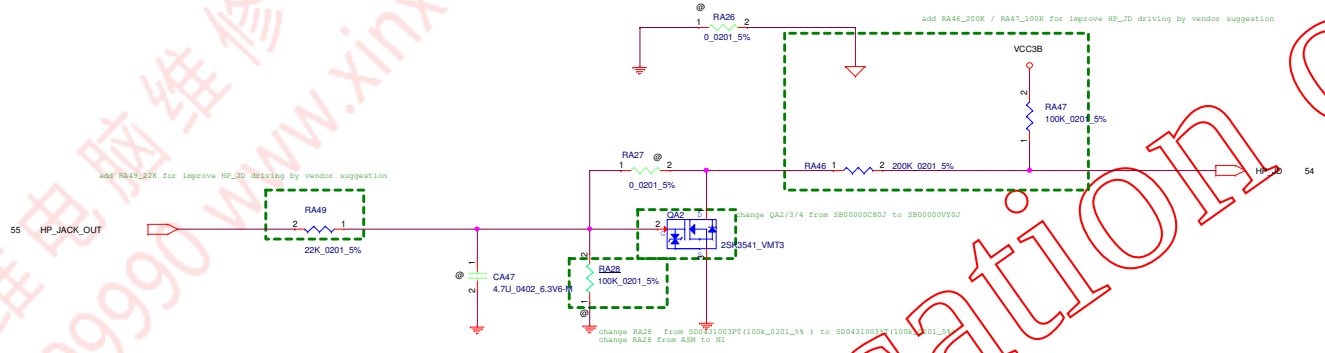
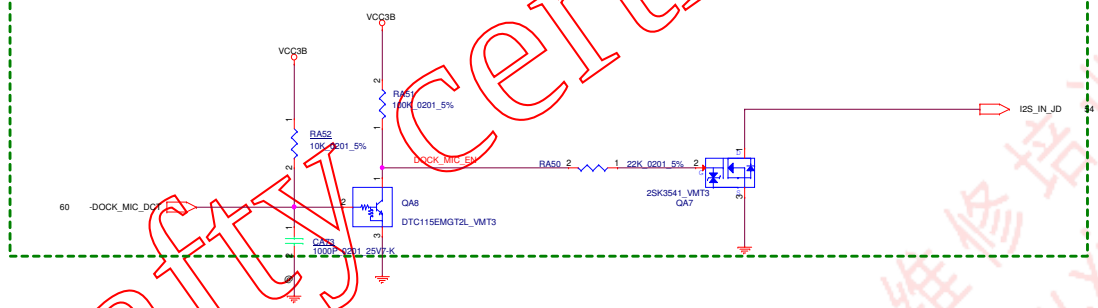


Delete RA29 /RA30 / QA3 for Docking Mic detect issue
Add RA51 / RA52 / QA8 / RA50 / QA7 /CA73 for Docking MIC detect issue



Delete RA31 / RA32 / QA4 for Docking HP detect issue

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Issued Date	2012/05/02	Deciphered Date	2012/5/02

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Title: AUDIO JACK SENSE

Size: Custom	Document Number: C	Rev: 0.1
Date: Thursday, August 20, 2015	Sheet 56 of 100	WOLVERINE3 UMA

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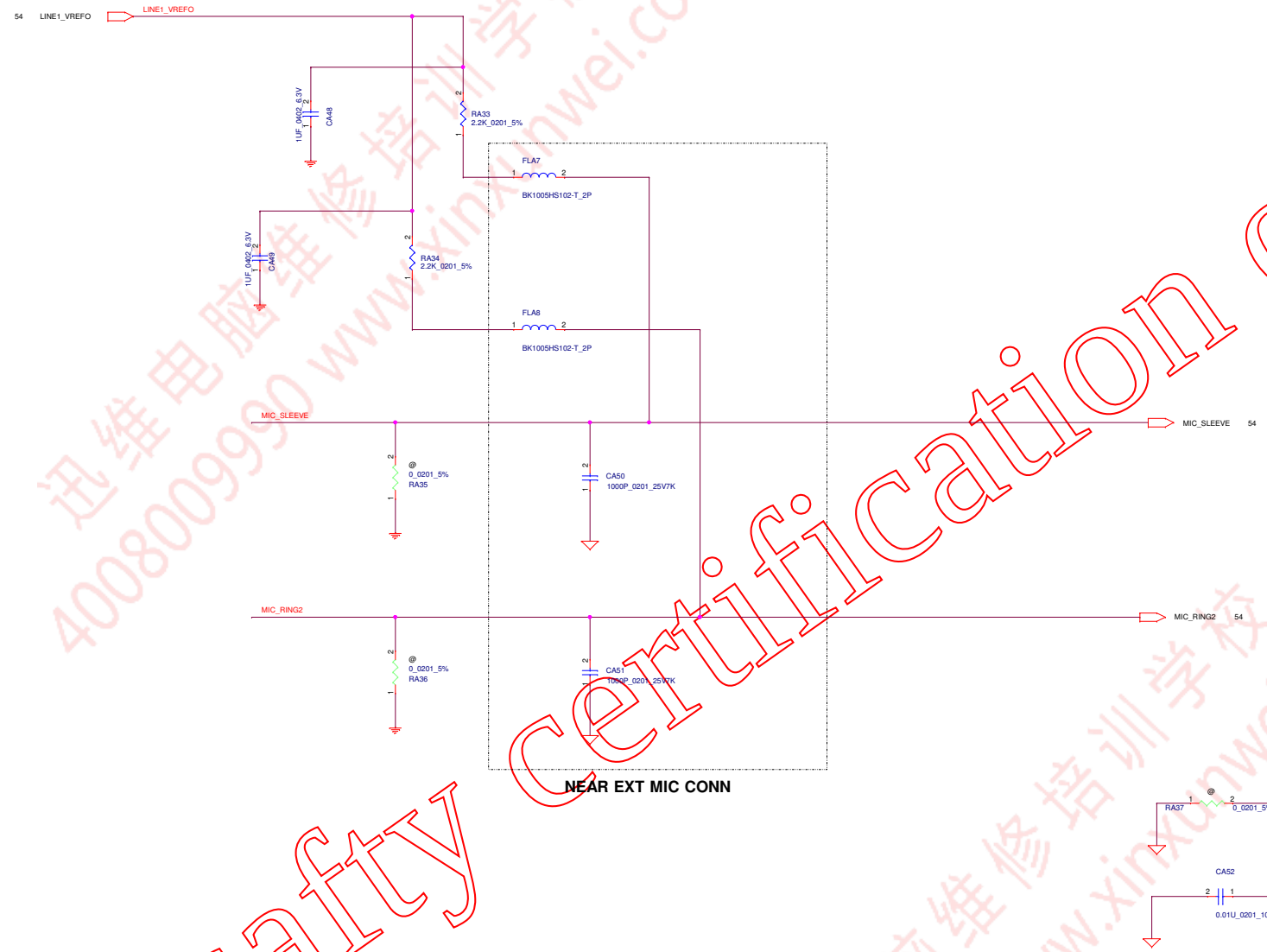

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Title: AUDIO EXT MIC I/F
STING UMA

Size	Document Number	Rev
Custom		0.1

Date: Thursday, August 20, 2015 Sheet 57 of 100

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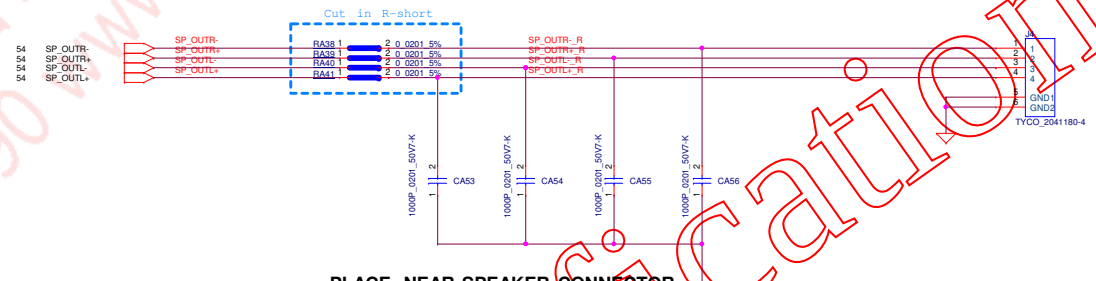

PLACE, NEAR SPEAKER CONNECTOR

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Title: **AUDIO SPEAKER**

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

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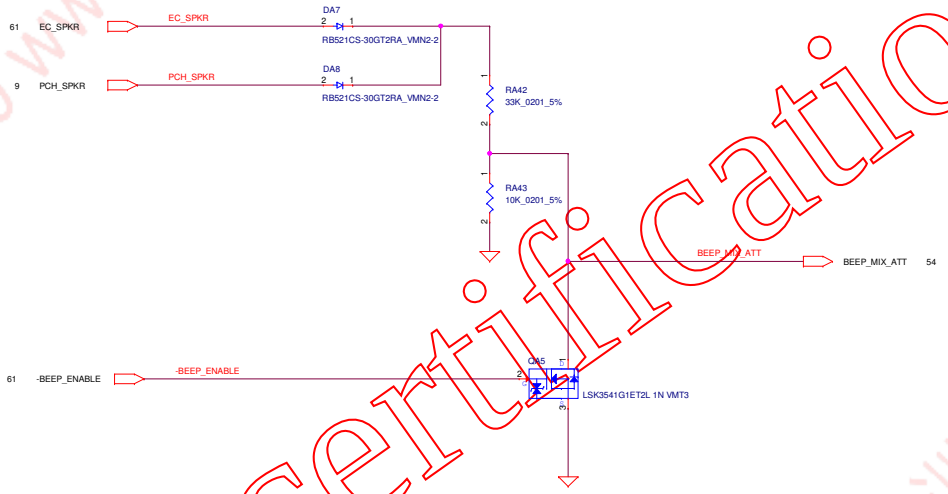

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Title: AUDIO BEEP

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1
Date: Thursday, August 20, 2015	Sheet 59 of 100	

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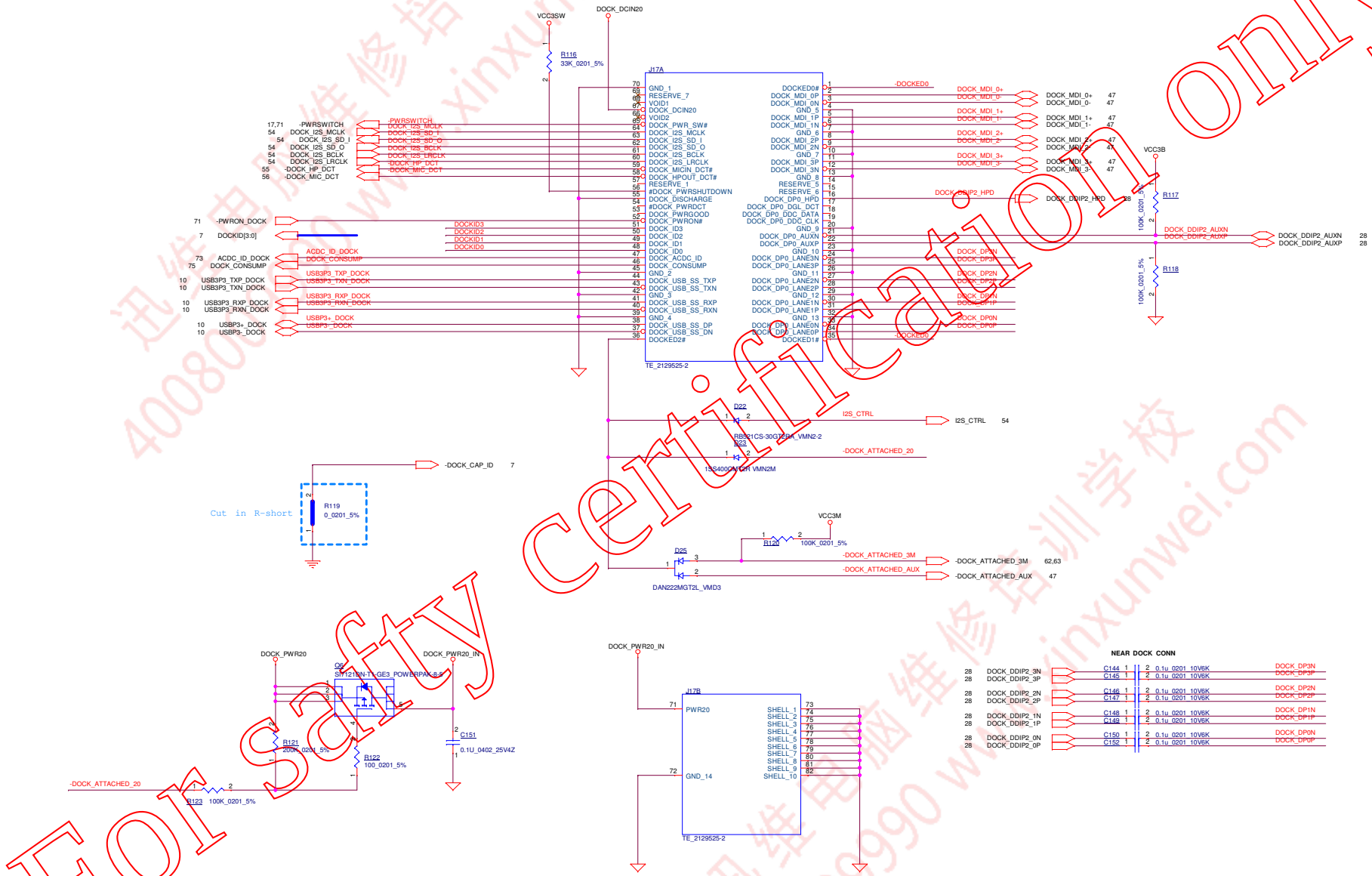
12/9 Delete DDIP2 pull high resistor



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Title: DOCKING CONNECTOR

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 60 of 100

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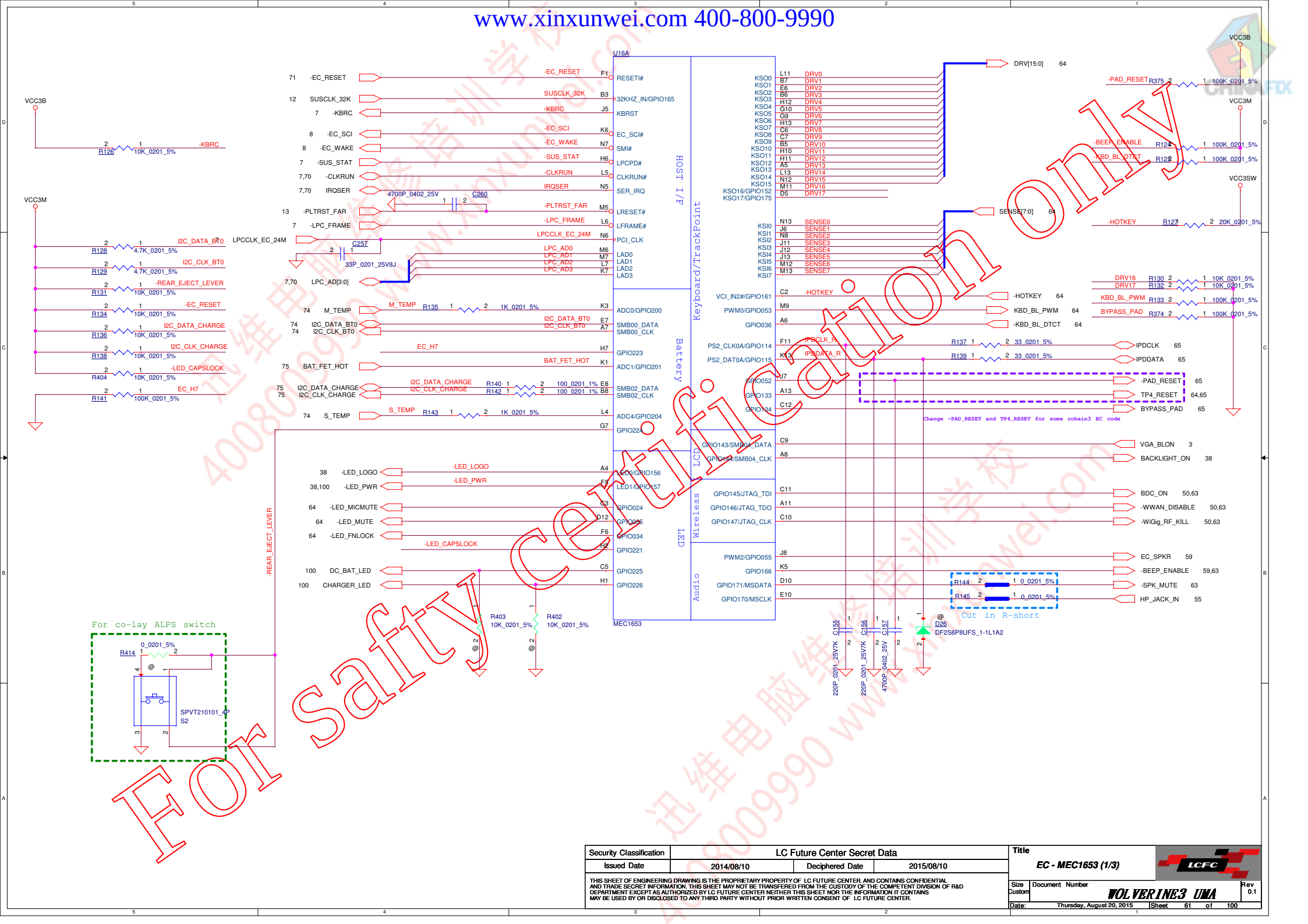

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Title: EC - MEC1653 (1/3)

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 61 of 100

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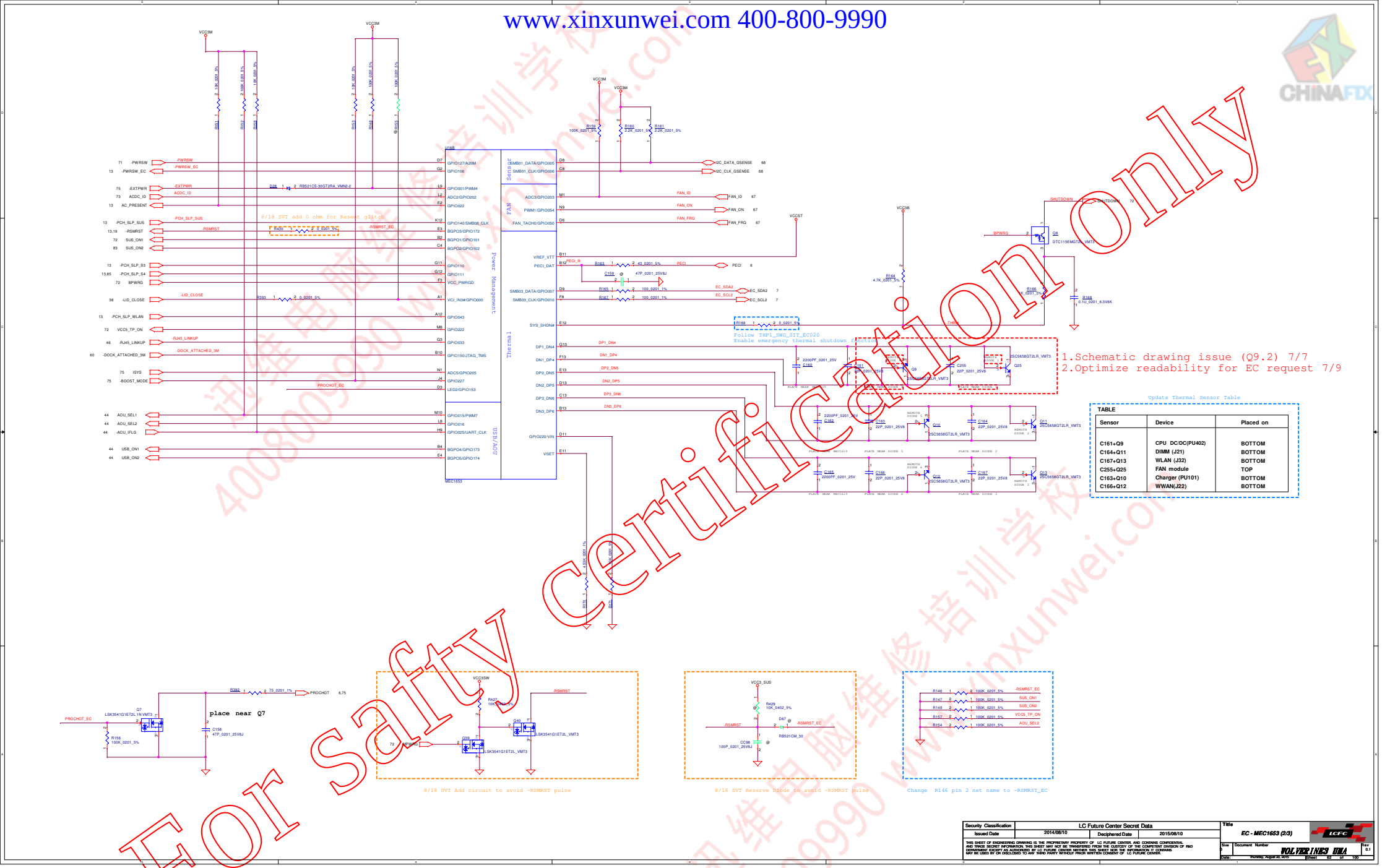

Update Thermal Sensor Table

TABLE

Sensor	Device	Placed on
C161+Q9	CPU DC/DC(PU402)	BOTTOM
C164+Q11	DIMM (J21)	BOTTOM
C167+Q13	WLAN (J32)	BOTTOM
C255+Q25	FAN module	TOP
C163+Q10	Charger (PU101)	BOTTOM
C166+Q12	WWAN(J22)	BOTTOM

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Issued Date	2014/08/10	Deciphered Date	2015/08/10

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Title: EC - MEC1653 (2/3)

Size: B | Document Number: | Rev: 0.1

Date: Monday, August 10, 2015 | Sheet 62 of 100

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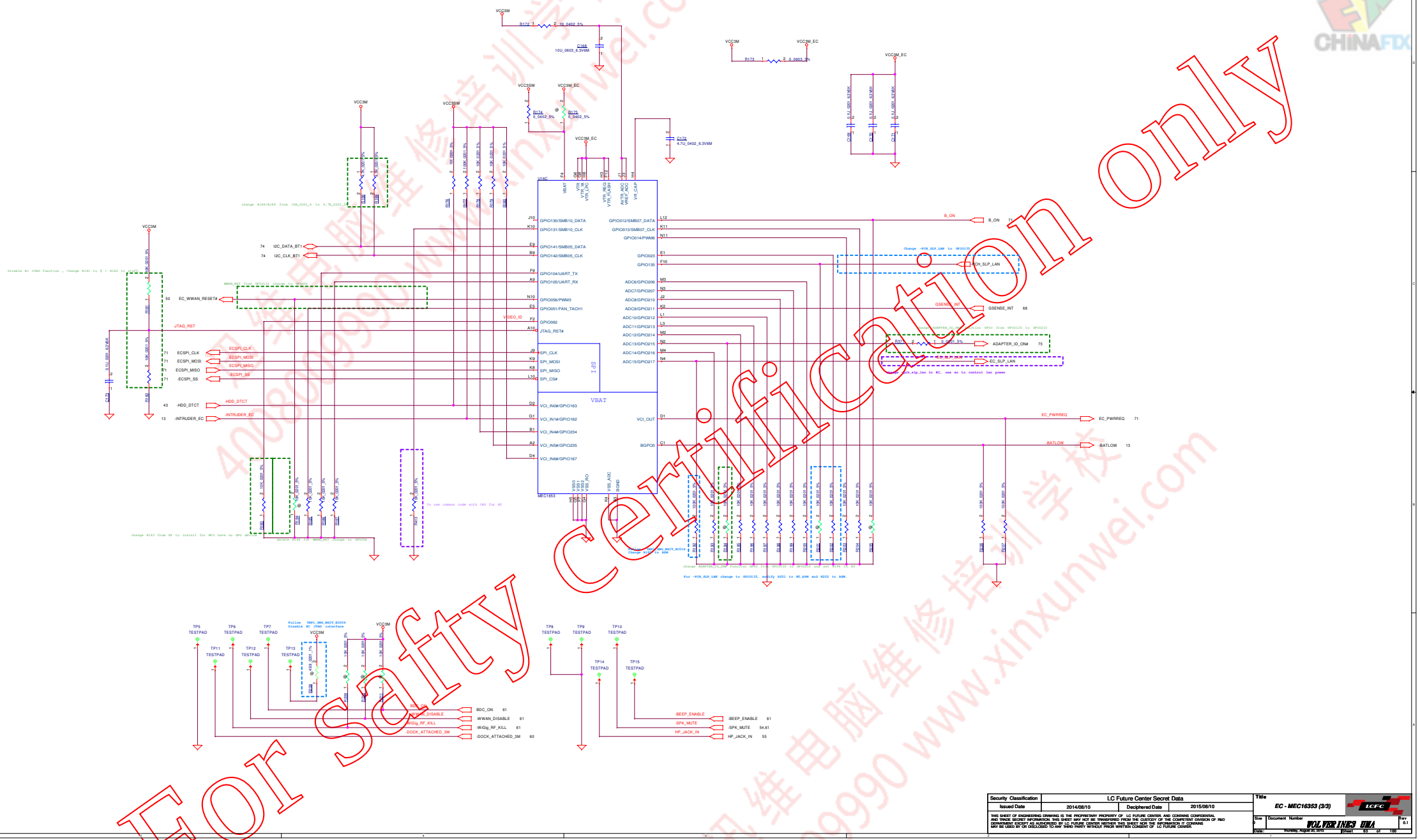

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Title: EC - MEC16353 (3/3)

Size: D | Document Number: WOLVERINES UMA | Rev: 0.1

Date: Thursday, August 20, 2015 | Sheet 63 of 100

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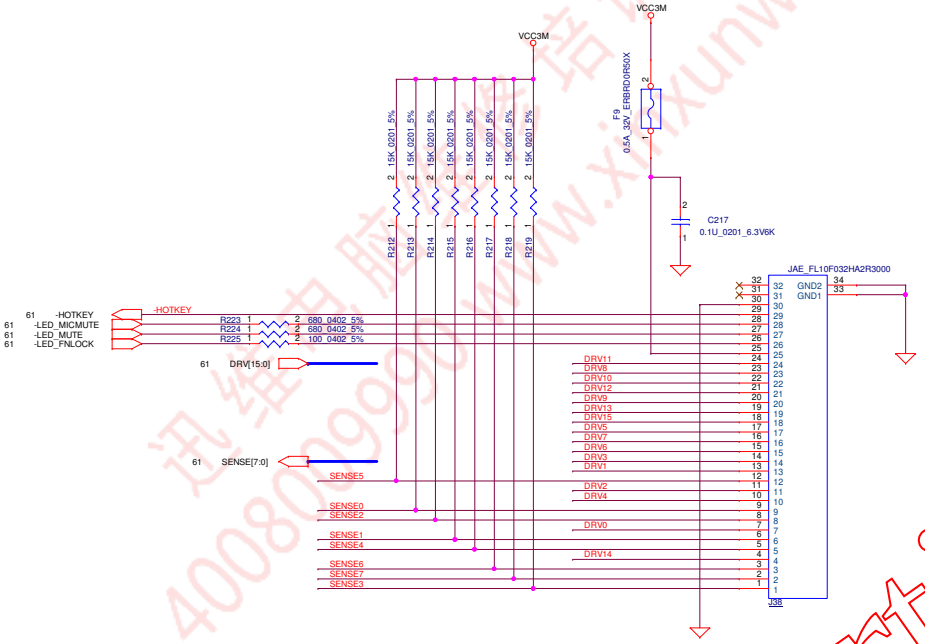

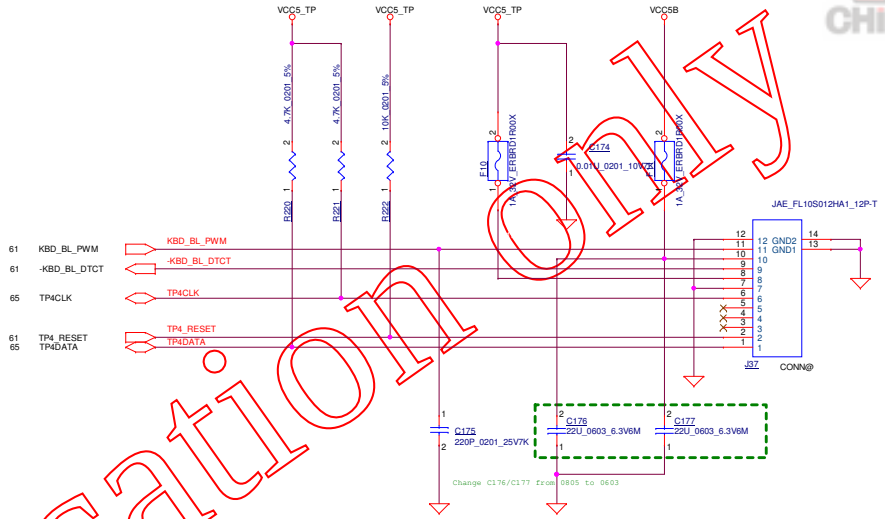

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Title	KEYBOARD/TRACK POINT	
Size: Custom	Document Number: WOLVERINE3 UMA	Rev: 0.1
Date: Thursday, August 20, 2015	Sheet 64 of 100	

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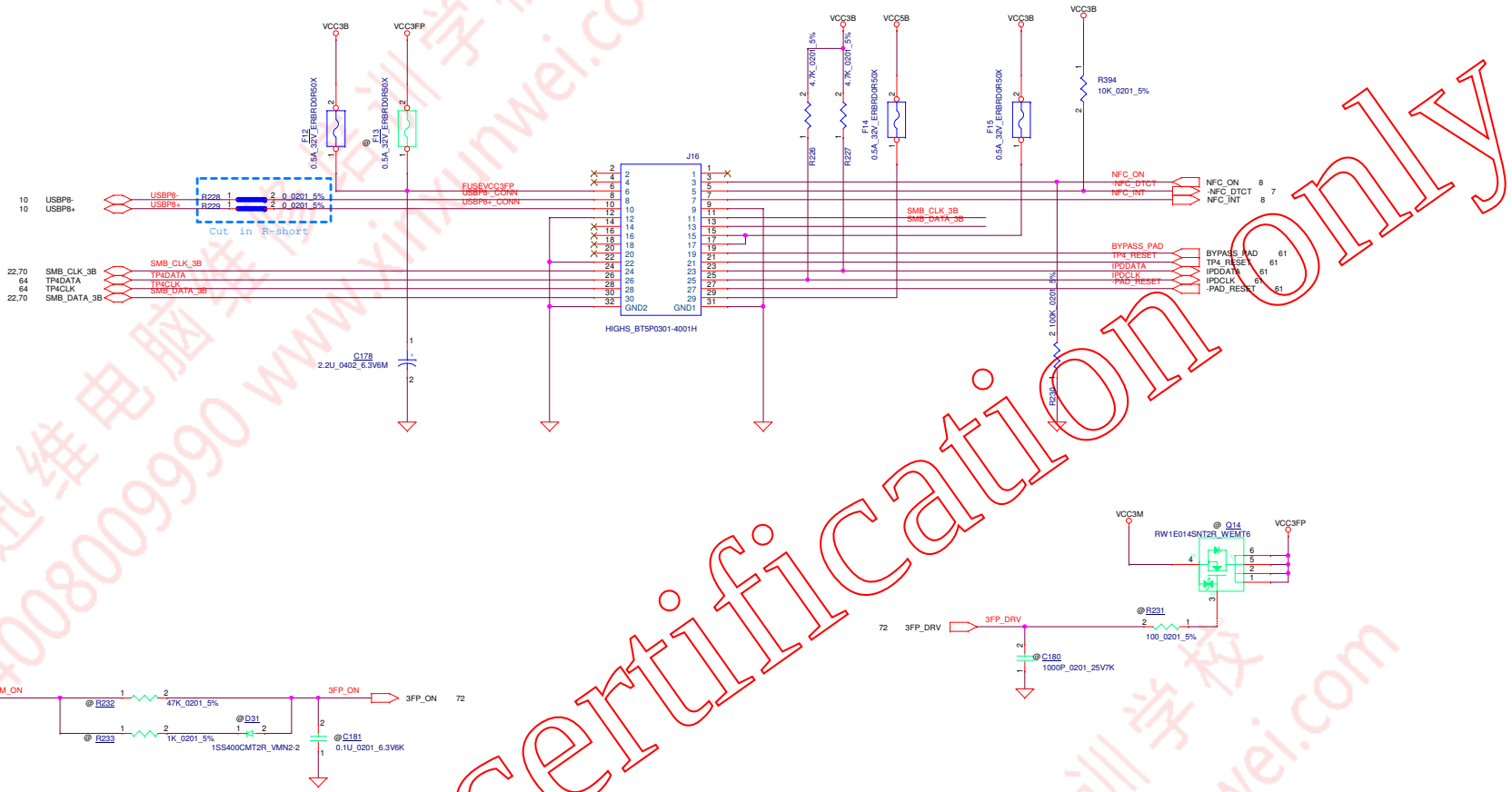

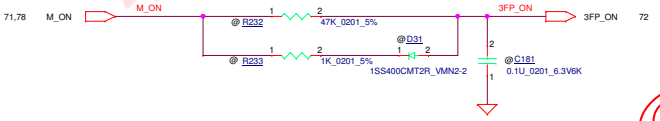

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Title: TOUCH PAD/NFC/FPR

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 65 of 100

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Size: Custom	Document Number	WOLVERINE3 UMA	Rev 0.1
Date: Thursday, August 20, 2015	Sheet 66 of 100		

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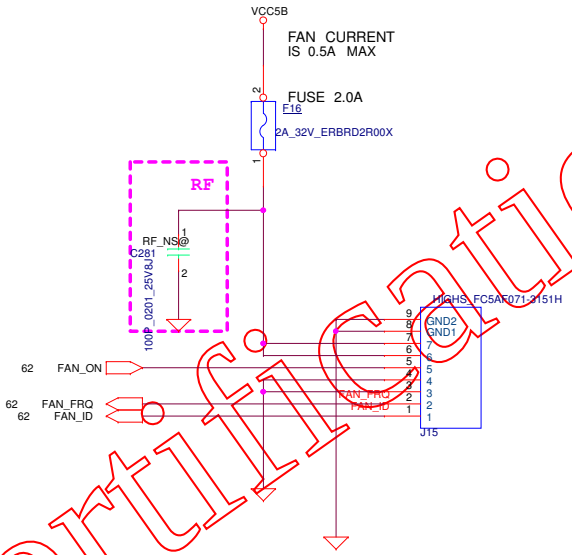

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Title: FAN CONNECTOR

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

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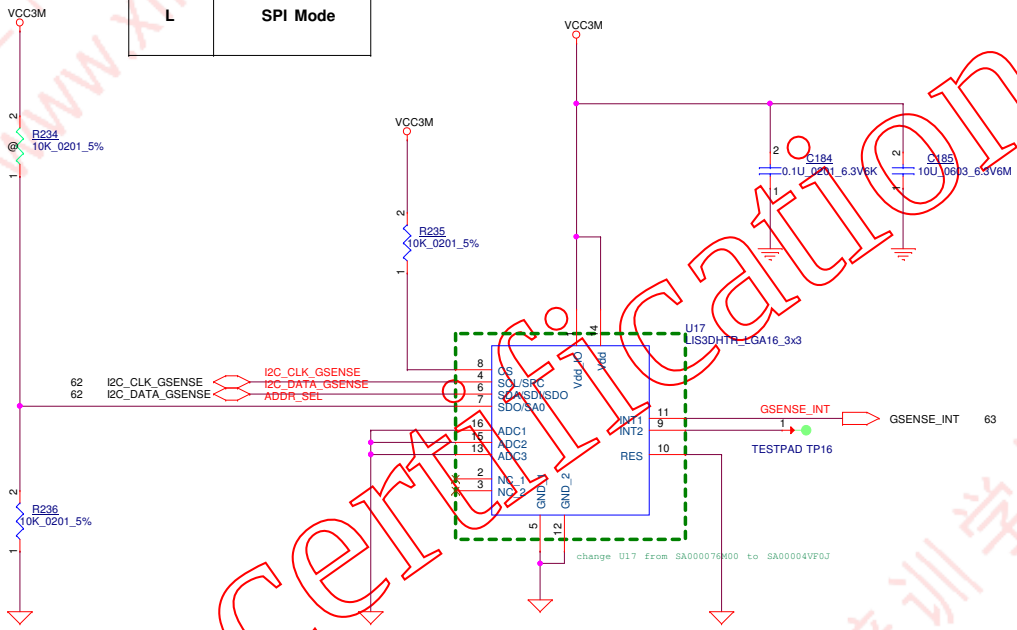
TABLE

P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



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Title: G-SENSOR

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 68 of 100

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TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table

change TPM power rail from VCC3_SUS_SPI to VCC_SUS for TPM VDD SPEC

change R238 / R397 pull high power rail from VCC3_SUS_SPI to VCC3_SUS

Follow Thorpe schematic
R397 to Non-ASM
R396 to ASM

Reserve circuit for use NPCT650LA0 to improve power consumption in S0

8/20 SVT Change TPM to SA00007H110

S IC NPCT650LB0YX QFN 32P DISCRETE TPM

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Title	TPM		
Size	Document Number		Rev
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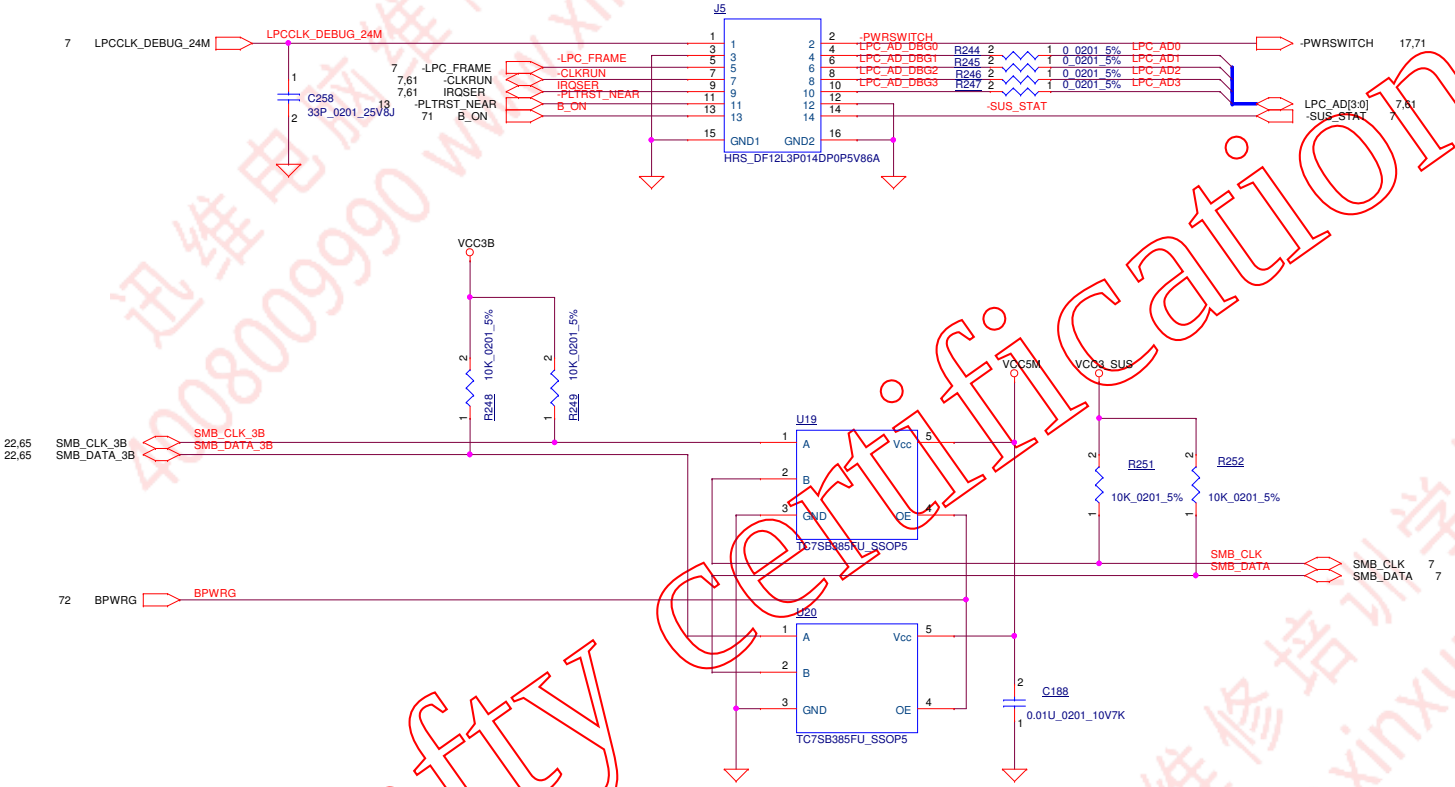
LPC Debug port

	Planner Only	BOX
J5	ASM	NO_ASM
RC29	ASM	ASM



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Title: SMBUS SW/LPC DEBUG PORT

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 70 of 100

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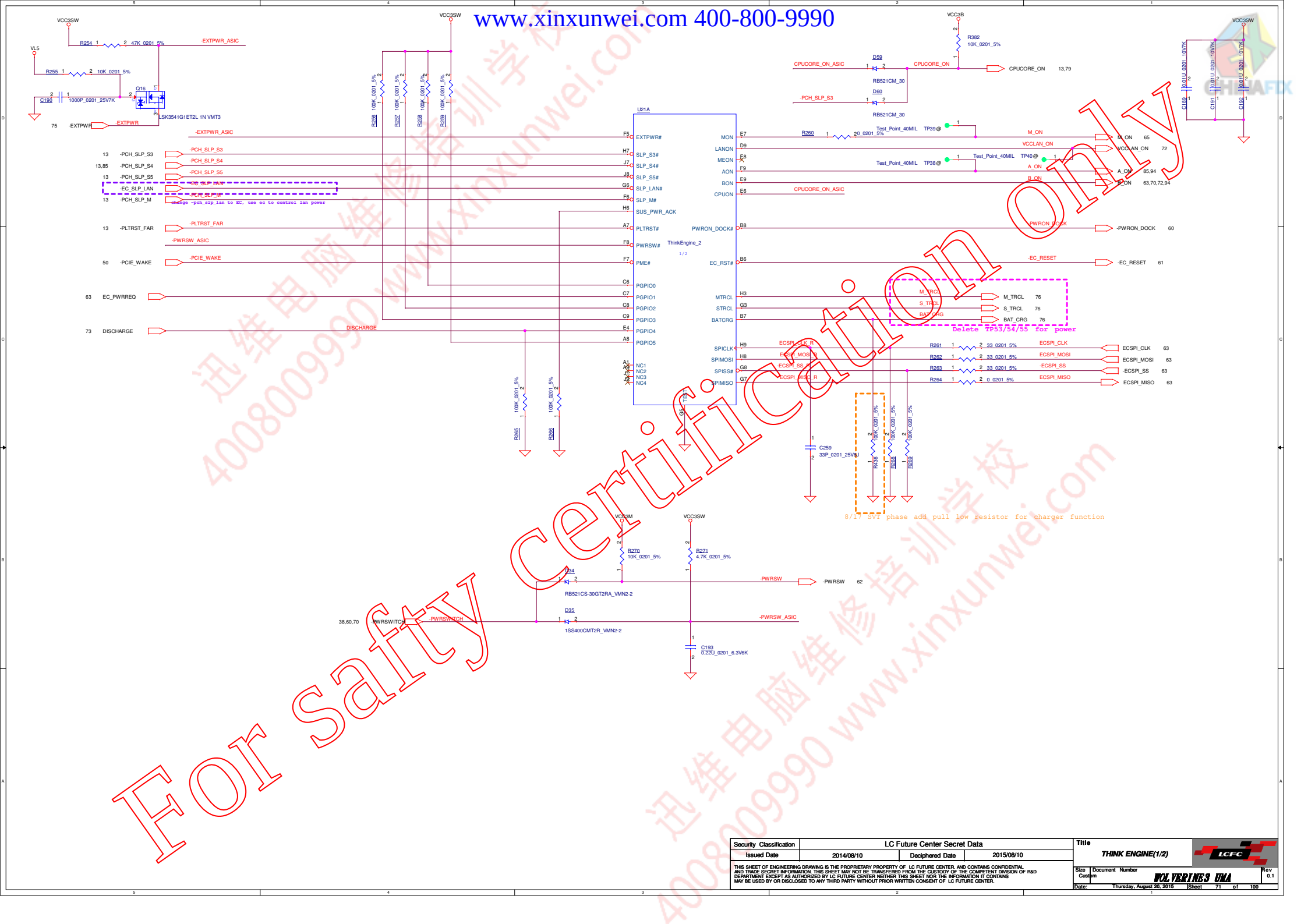

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Title	THINK ENGINE(1/2)		
Size	Document Number		Rev
Custom	WOLVERINE3 UMA		0.1
Date:	Thursday, August 20, 2015	Sheet	71 of 100

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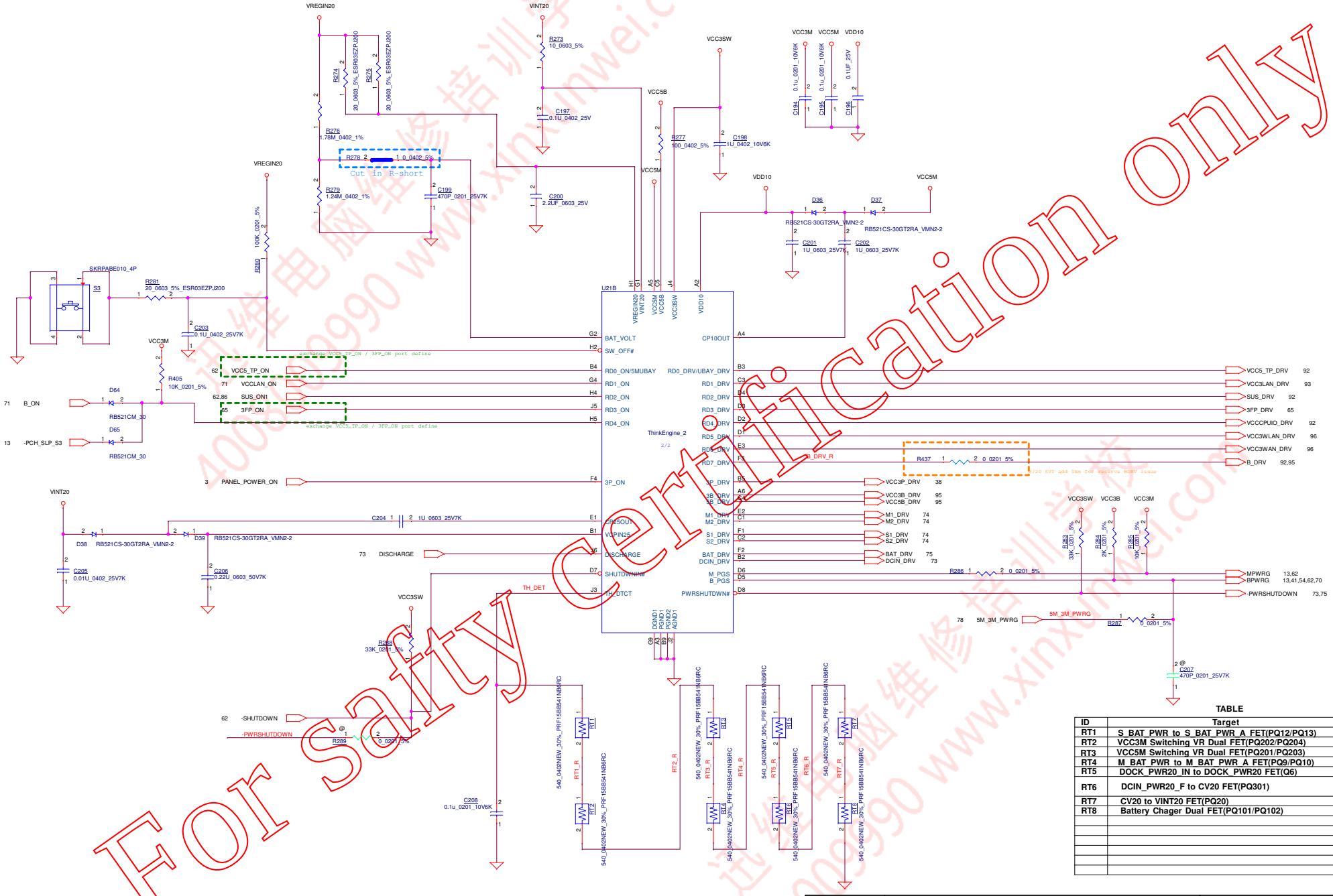

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TABLE

ID	Target
RT1	S_BAT_PWR_to_S_BAT_PWR_A_FET(PQ12/PQ13)
RT2	VCC3M Switching VR Dual FET(PQ202/PQ204)
RT3	VCC5M Switching VR Dual FET(PQ201/PQ203)
RT4	M_BAT_PWR_to_M_BAT_PWR_A_FET(PQ9/PQ10)
RT5	DOCK_PWR20_IN to DOCK_PWR20 FET(Q6)
RT6	DCIN_PWR20_F to CV20 FET(PQ301)
RT7	CV20 to VINT20 FET(PQ20)
RT8	Battery Chager Dual FET(PQ101/PQ102)

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Title: THINK ENGINE(2/2)

Size: Custom | Document Number: DOL VERLINE3 UMA | Rev: 0.1

Date: Thursday, August 20, 2015 | Sheet 72 of 100

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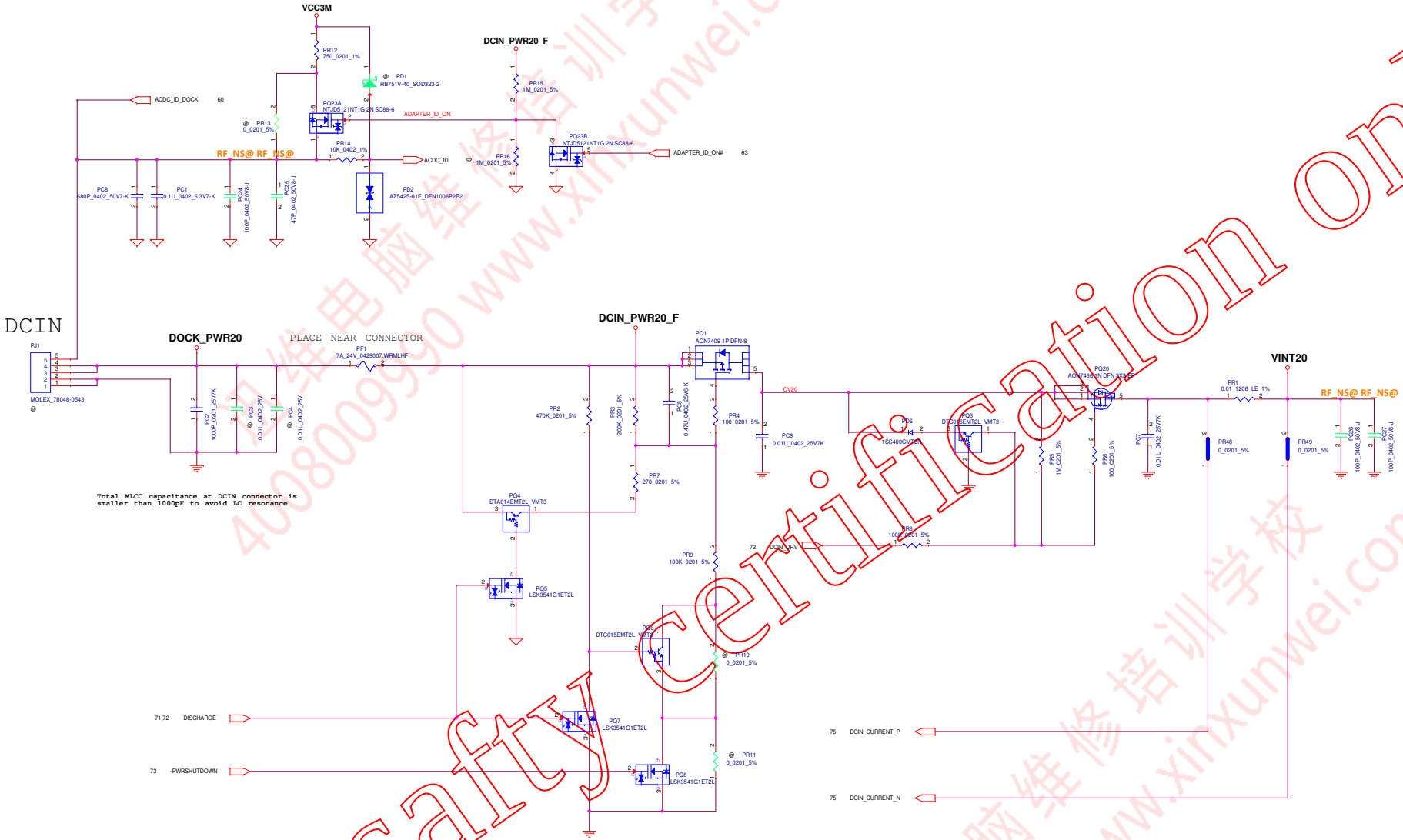
confirm with EE



TABLE

PEAK SHIFT	YES	NO
PR10	NO-ASM	ASM
PR2	ASM	NO-ASM
PQ7	ASM	NO-ASM
PQ6	ASM	NO-ASM

LOGIC

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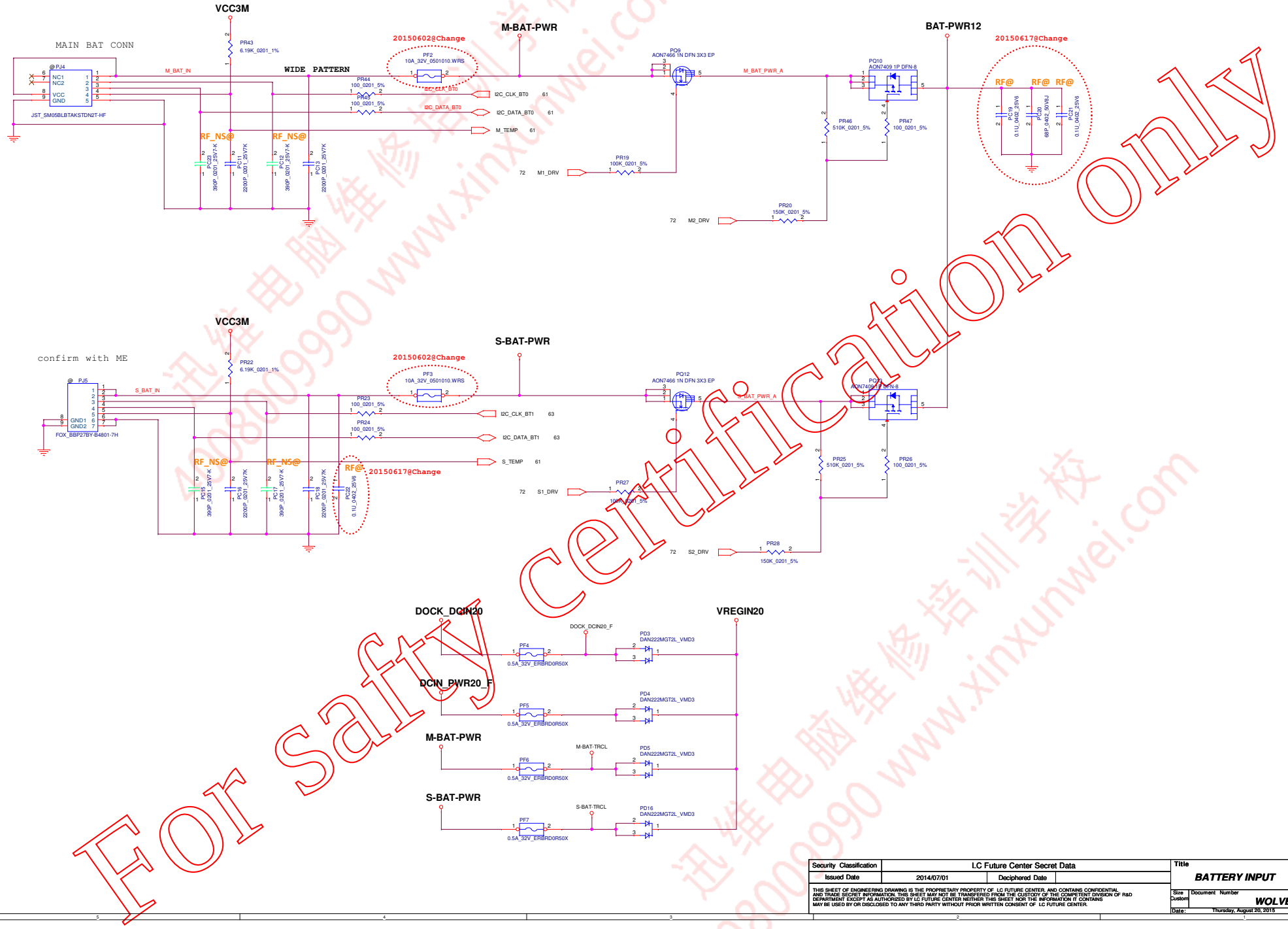

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Title: **BATTERY INPUT**

Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1

Date: Thursday, August 20, 2015 Sheet 74 of 100

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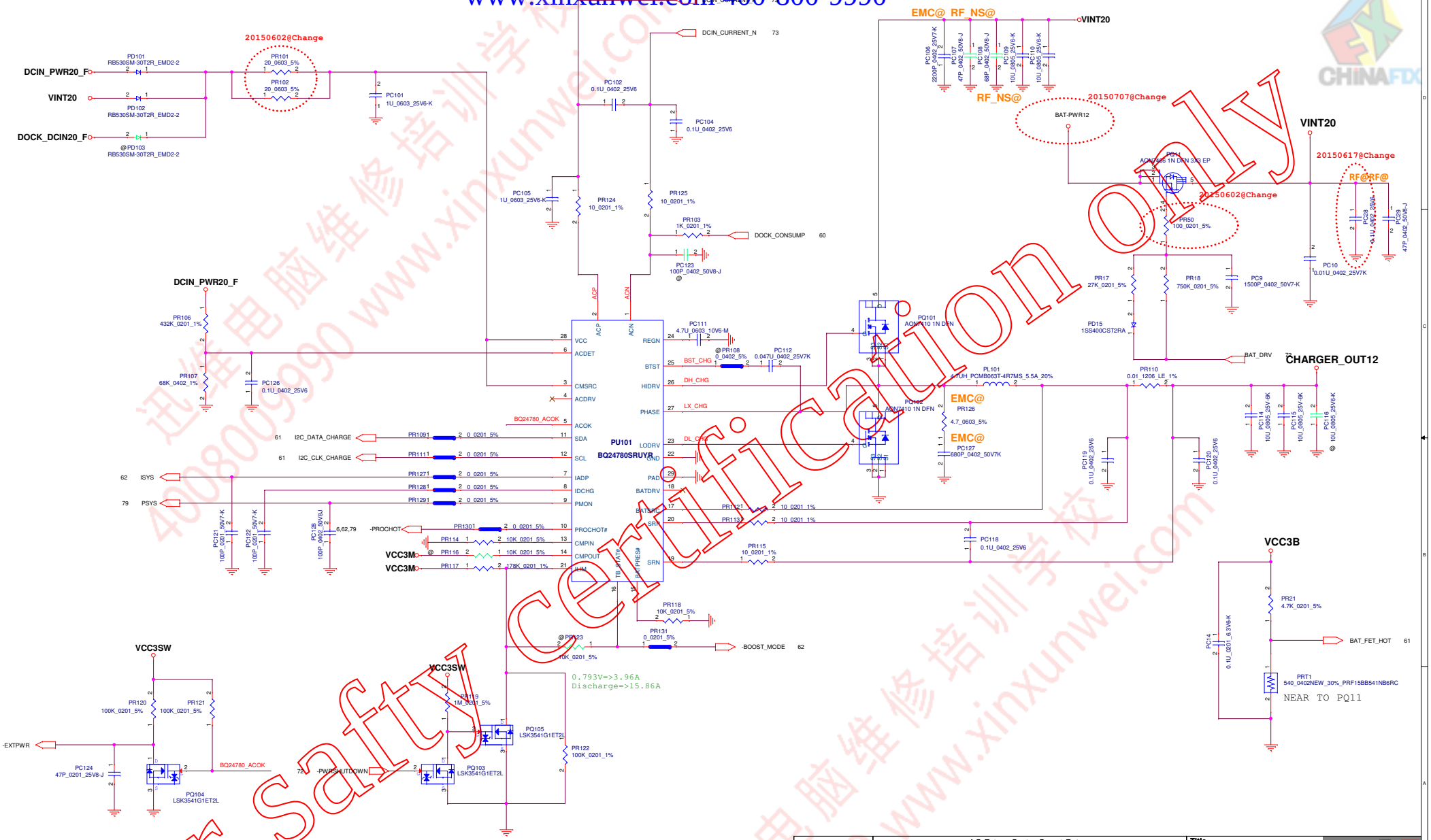

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Size	Document Number	Rev
Custom	WOLVERINE3 UMA	0.1
Date: Thursday, August 20, 2015	Sheet 75 of 100	

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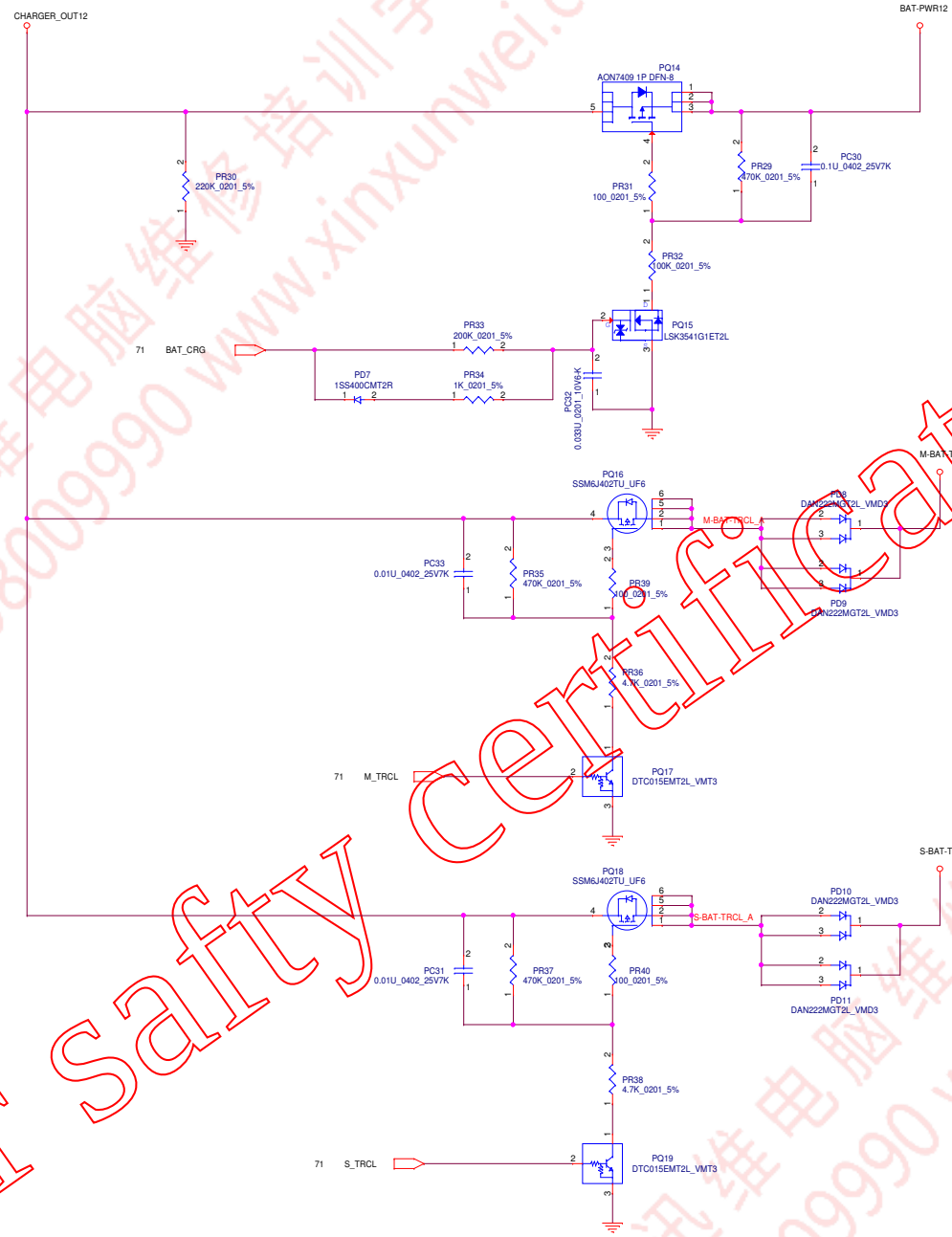

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Title: **CHARGER SELECTOR**

Size	Document Number	Rev
C	WOLVERINE3 UMA	0.1

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Size: C	Document Number: WOLVERINE3 UMA	Rev: 0.1
Date: Thursday, August 20, 2015	Sheet 77 of 100	

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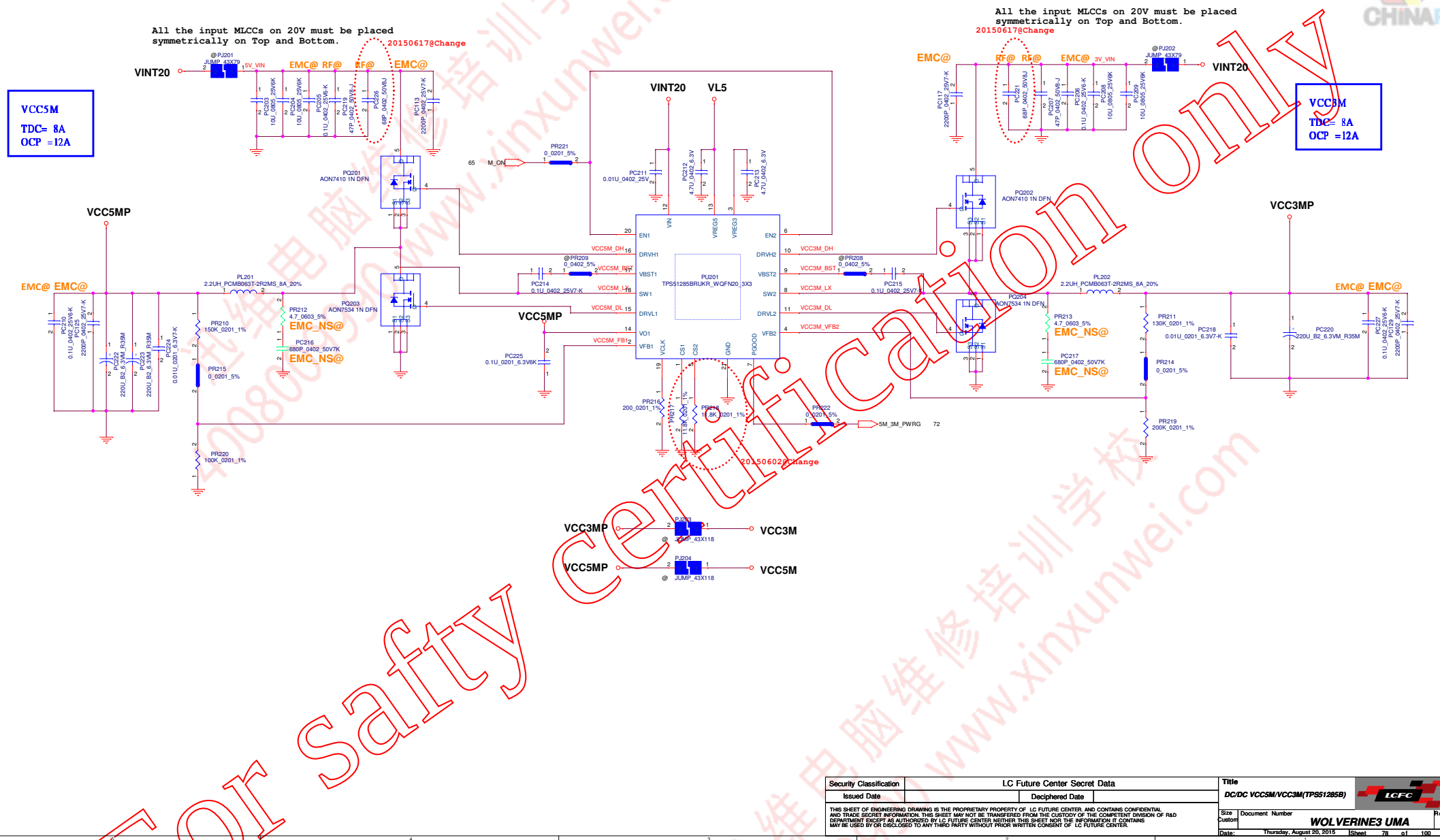

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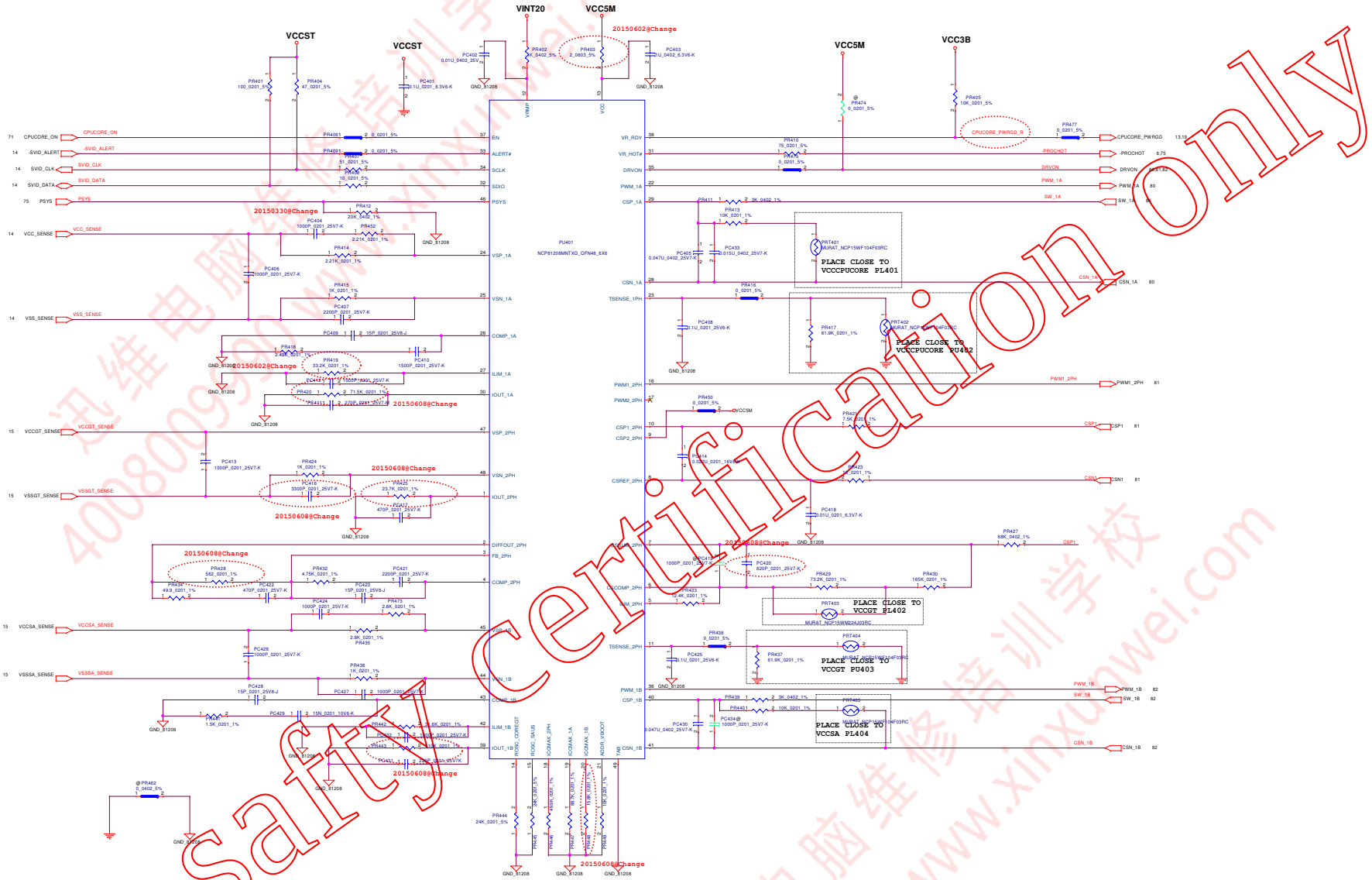

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Title	DC/DC IMVP8(NCP81208)	
Size: D	Document Number: WOLVERINE3 UMA	Rev: 0.1
Date: Monday, August 03, 2015	Sheet 79 of 100	

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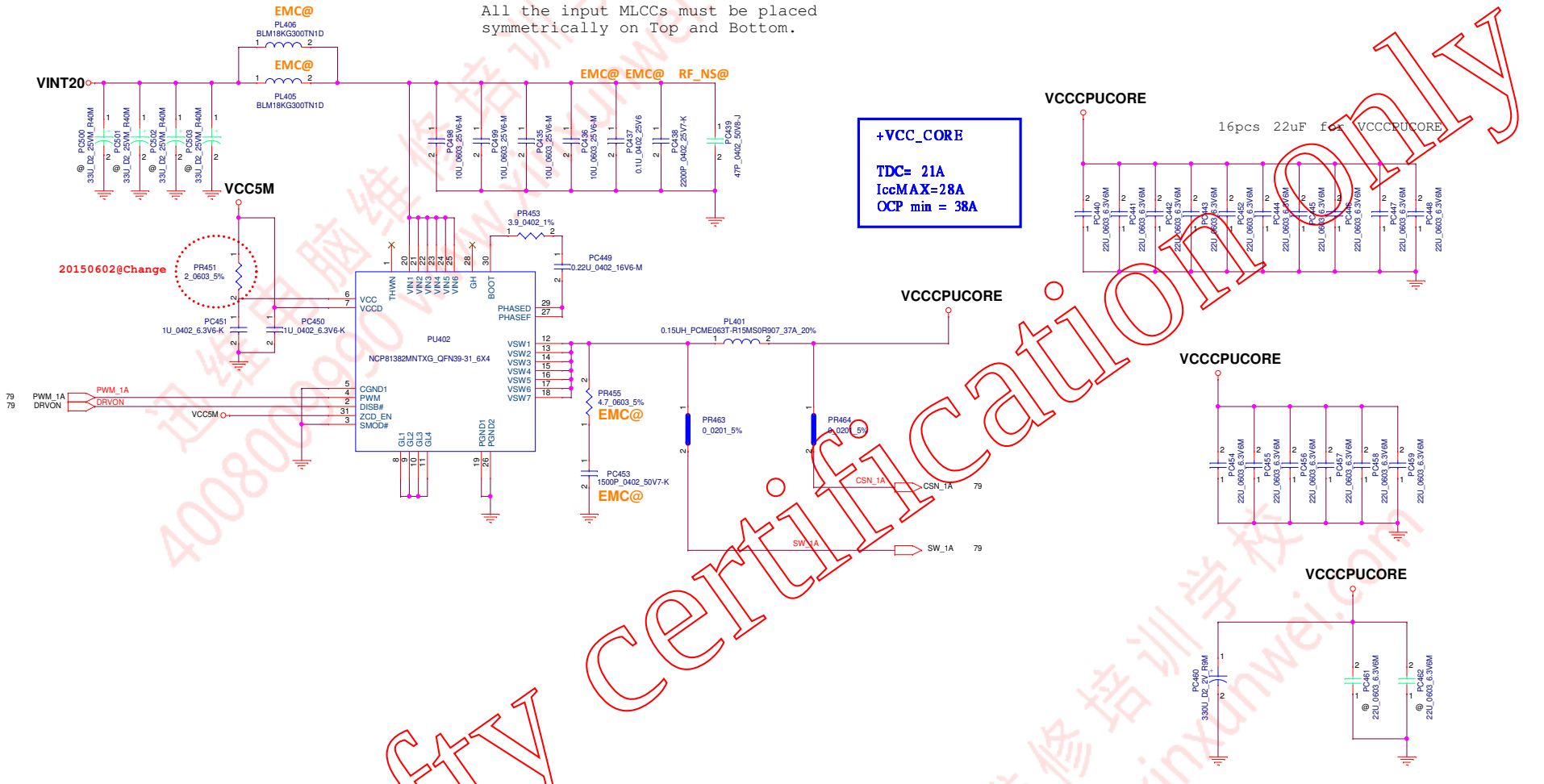
All the input MLCCs must be placed symmetrically on Top and Bottom.

+VCC_CORE

TDC= 21A
IccMAX=28A
OCP min = 38A

16pcs 22uF for VCCCPUCORE



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Title	DC/DC CPUCORE(NCP81382)	
Size: Custom	Document Number: WOLVERINE3 UMA	Rev: 0.1
Date: Thursday, August 20, 2015	Sheet 80 of 100	

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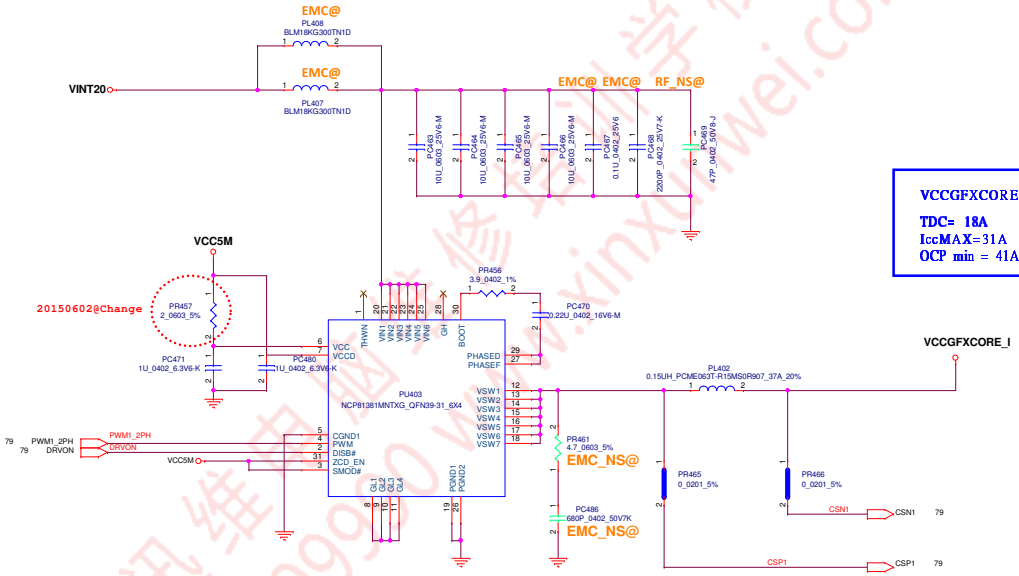

VCCGFXCORE_I
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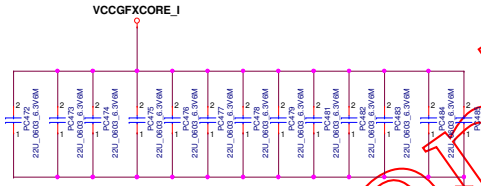
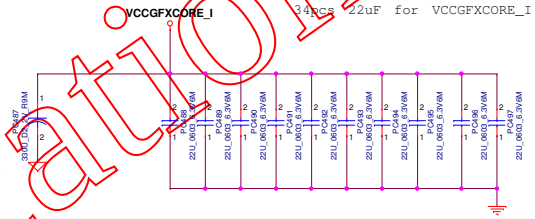
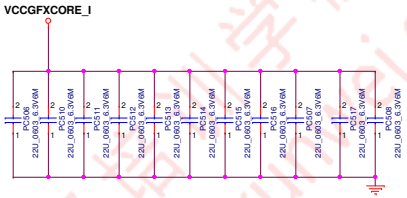
IccMAX=31A
OCP min = 41A







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Issued Date		Deciphered Date	

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Date: Thursday, August 20, 2015	Sheet 81 of 100		

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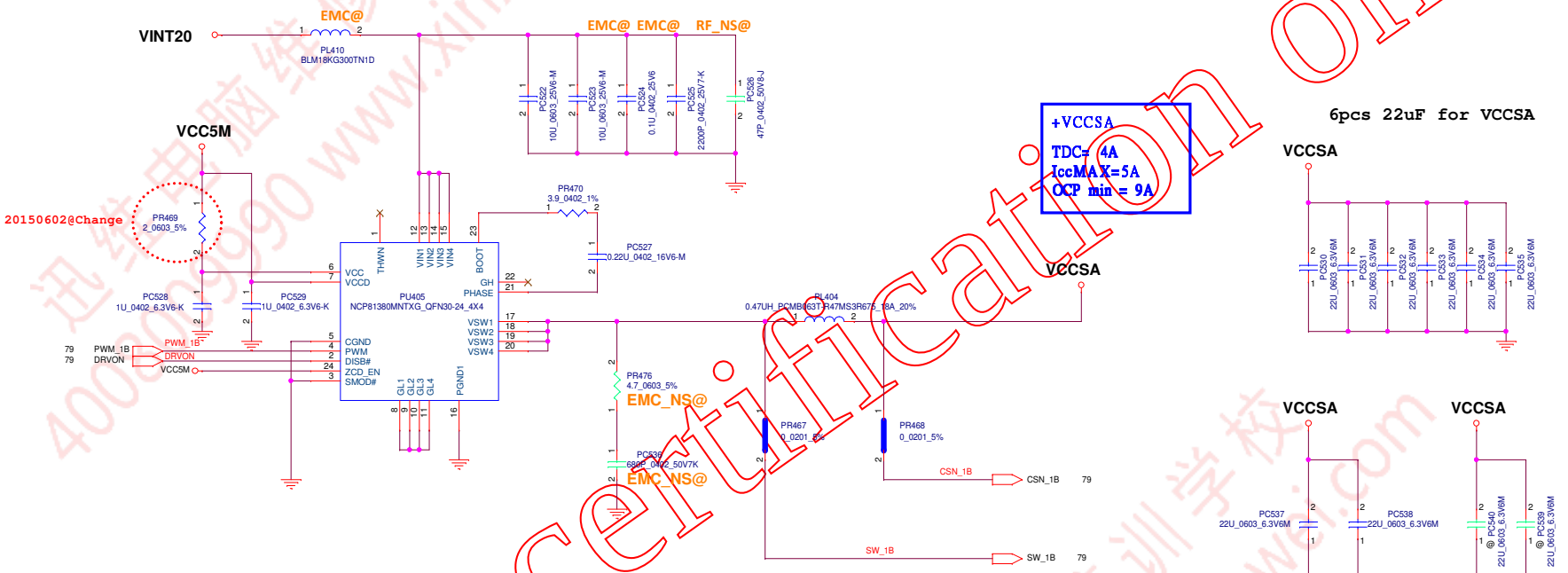
symmetrically on Top and Bottom.



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Title	DC/DC VCCSA(NCP81380)	
Size: Custom	Document Number: WOLVERINE3 UMA	Rev: 0.1
Date: Thursday, August 20, 2015	Sheet 82 of 100	

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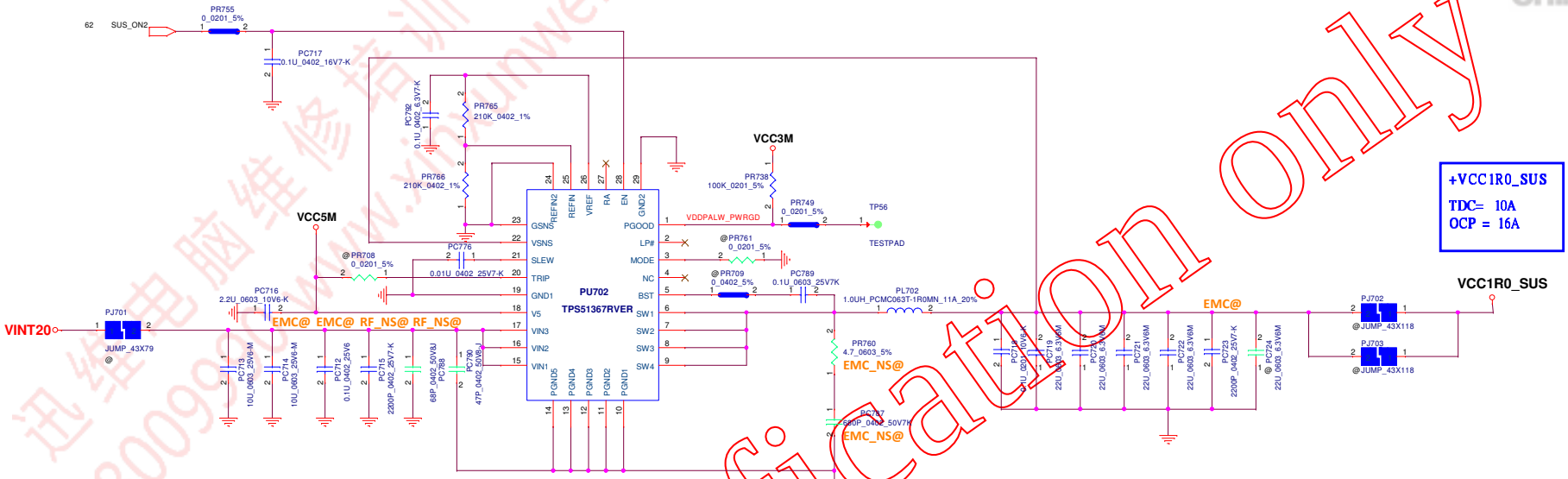

+VCC1R0_SUS
TDC= 10A
OCP = 16A

Mode	Frequency
GND	400KHz
Float	800KHz

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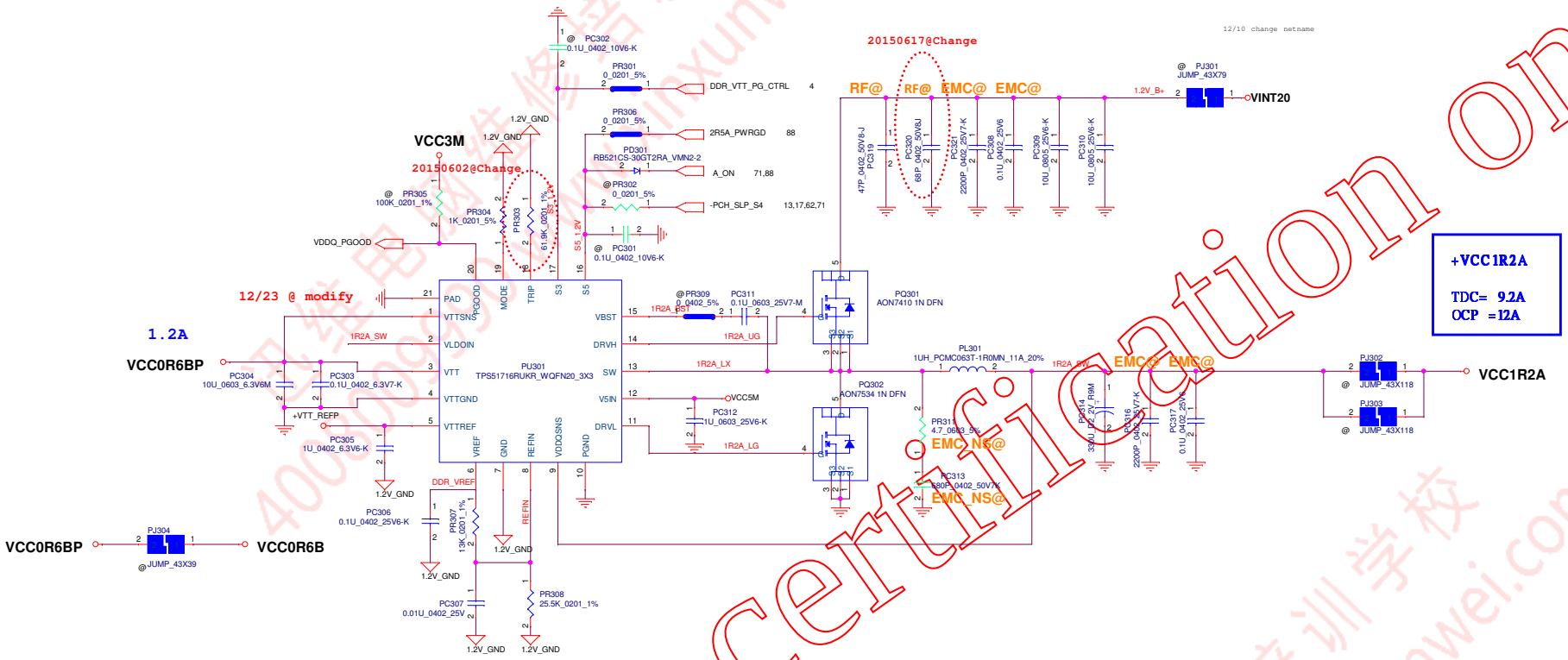

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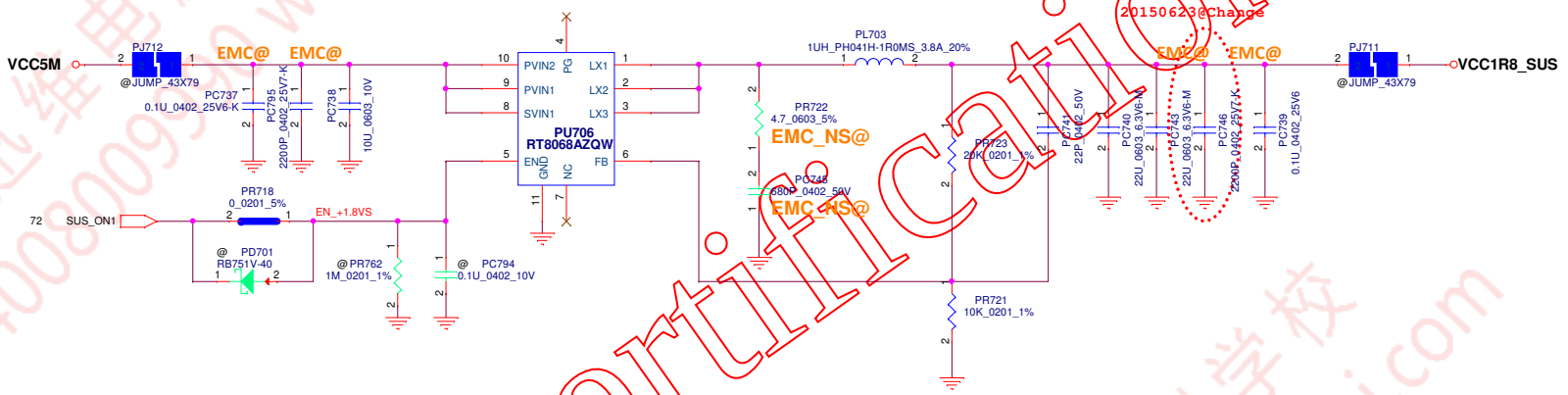

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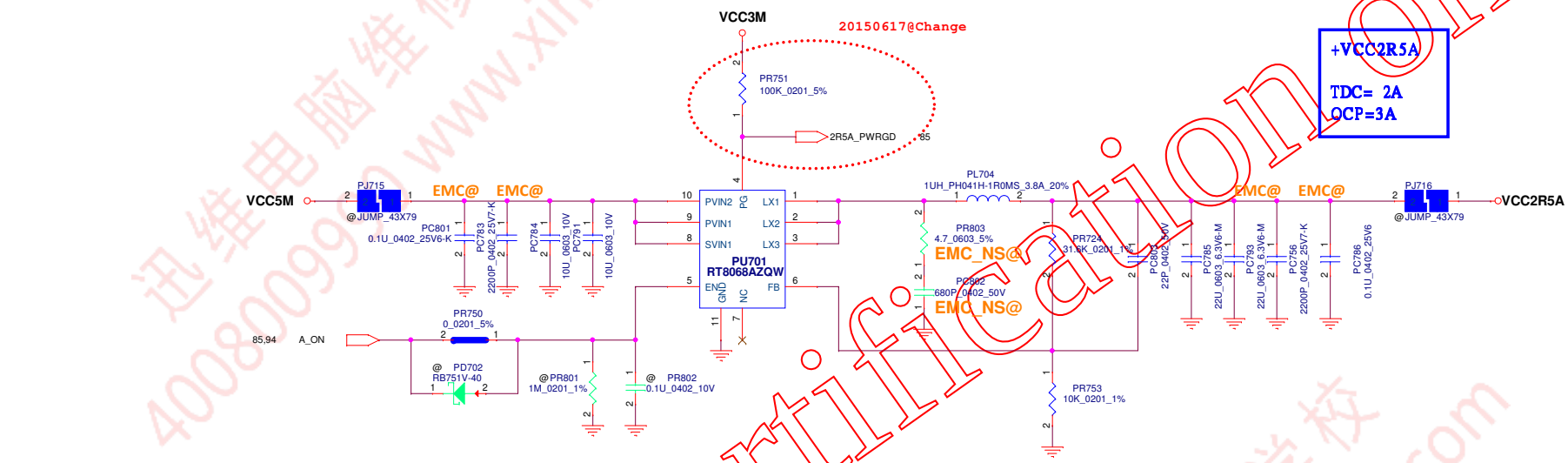

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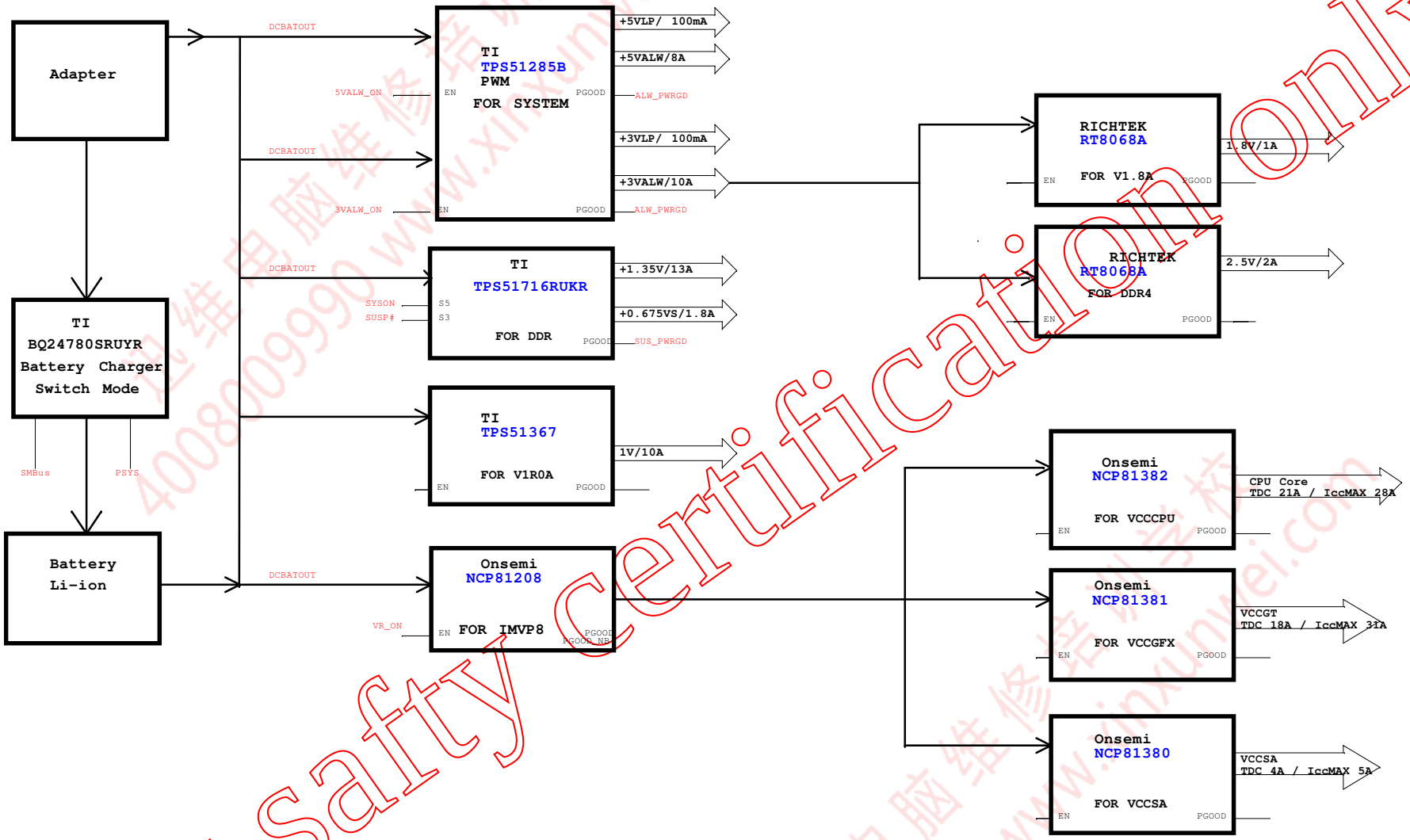

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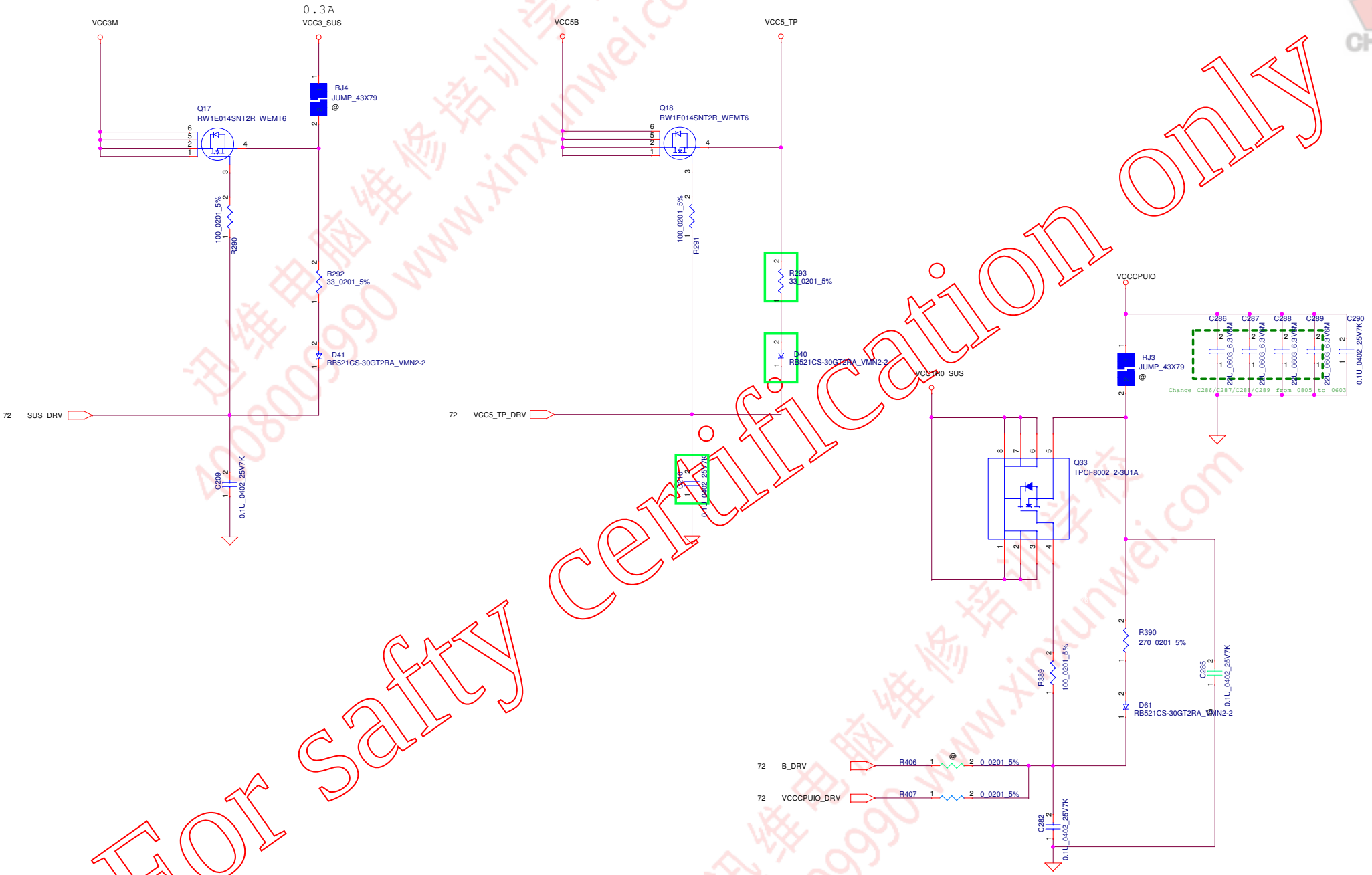

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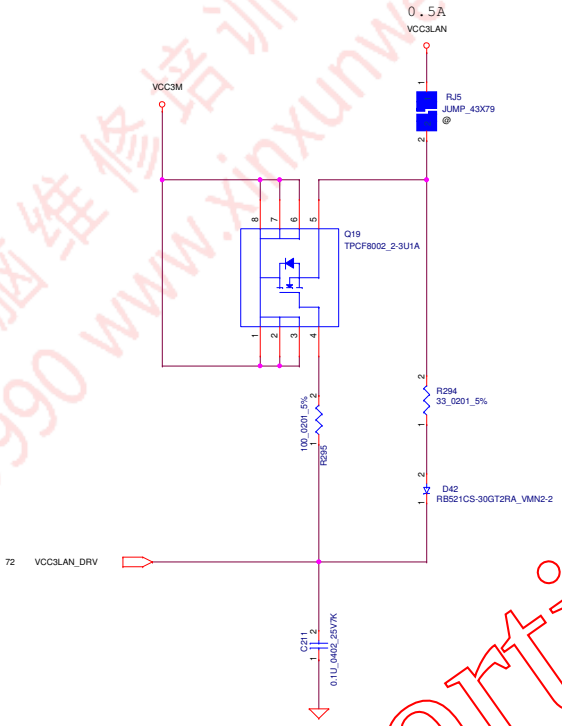

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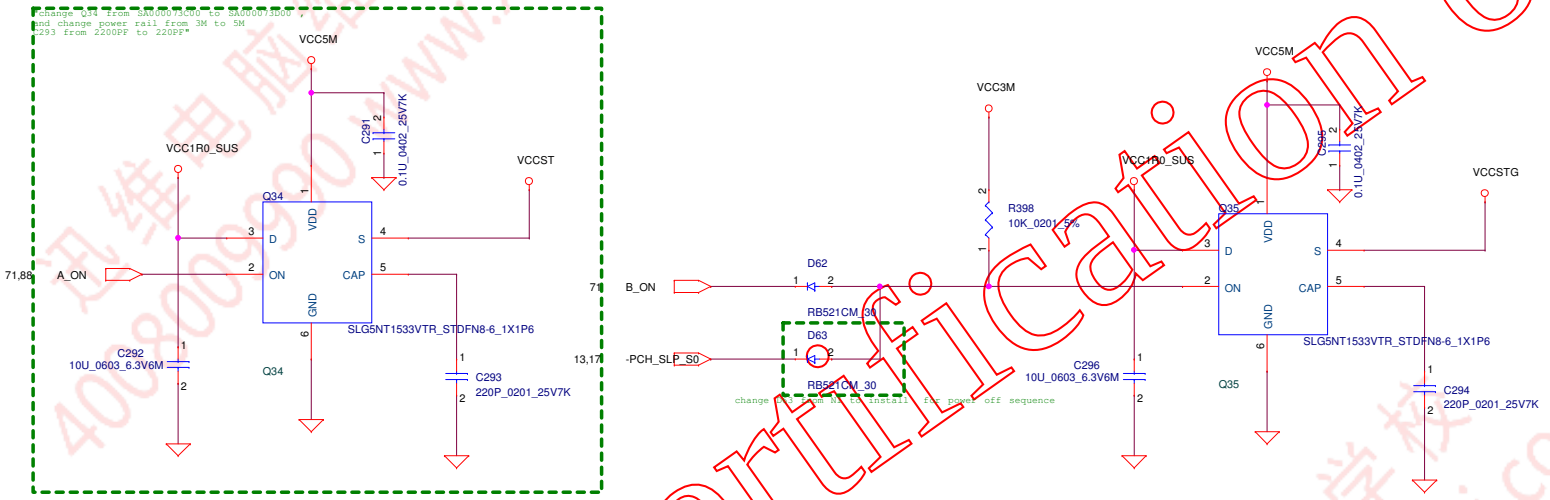

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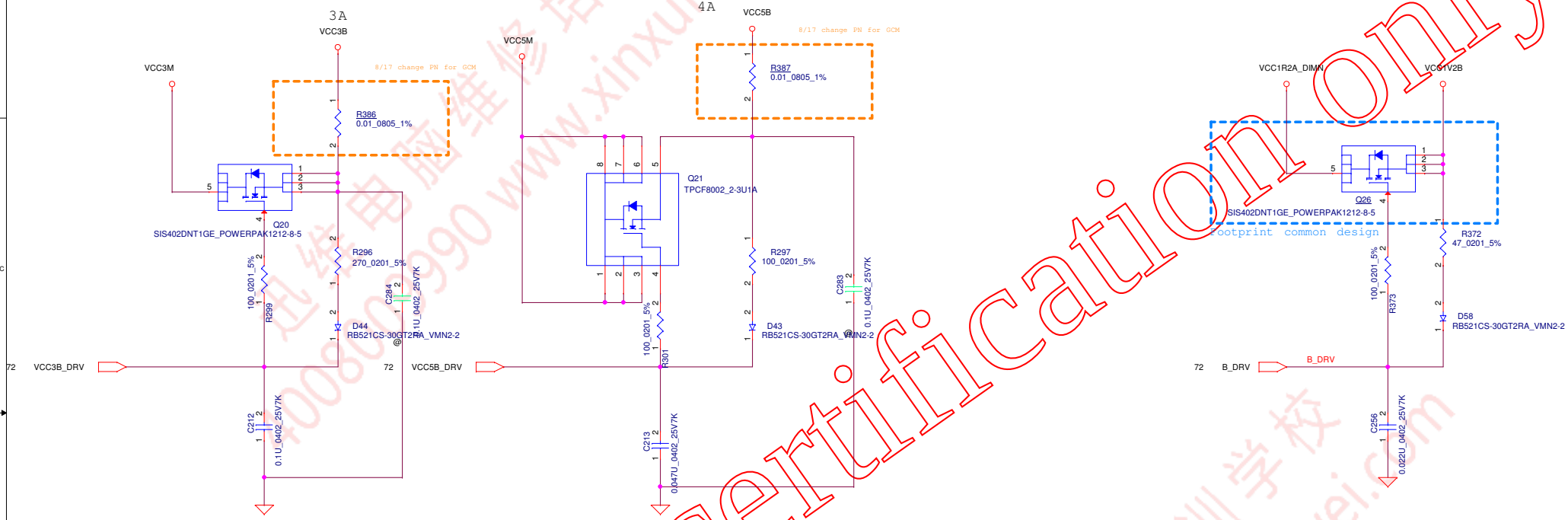

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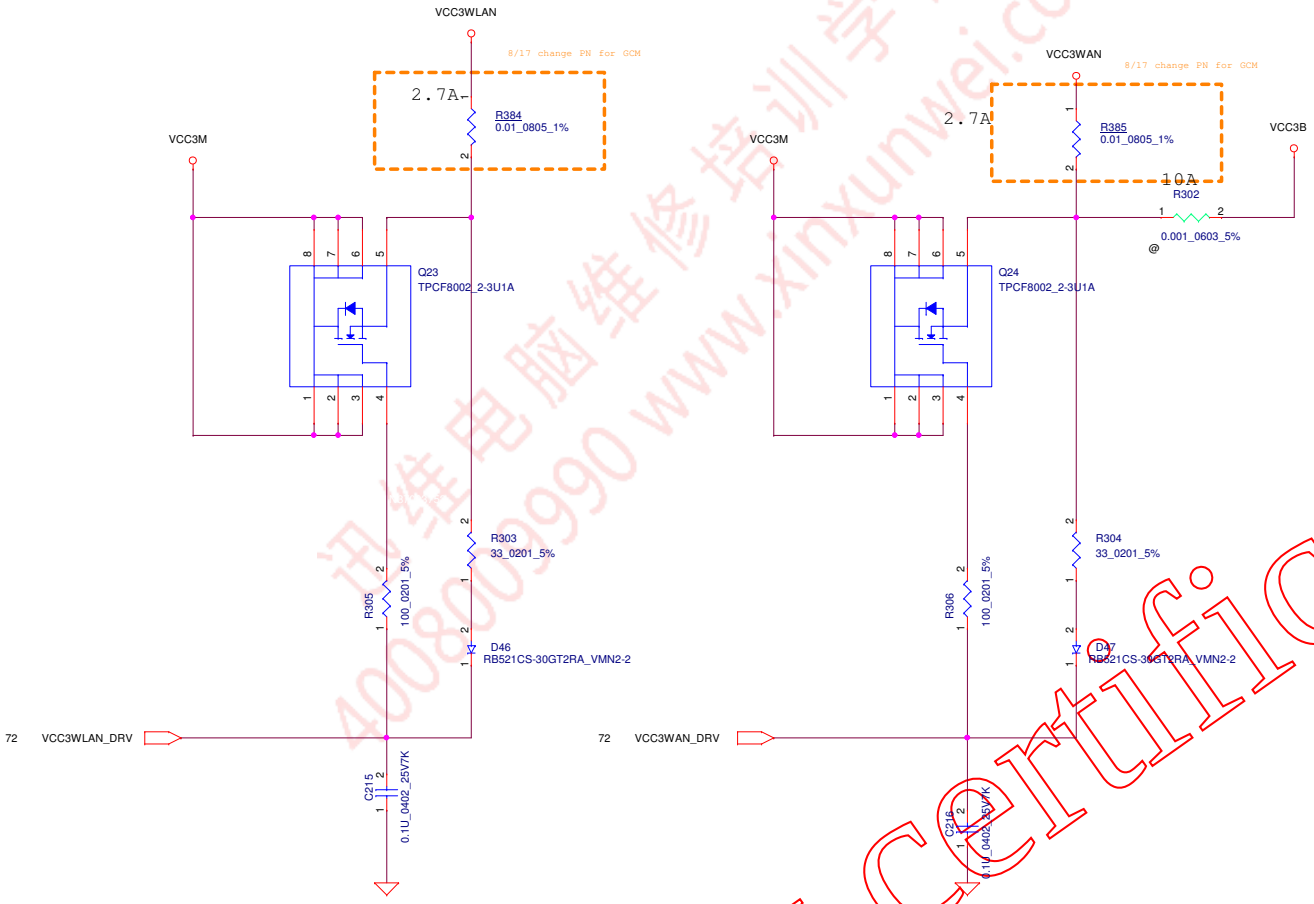

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R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R8924	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

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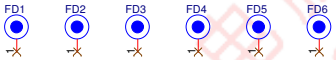

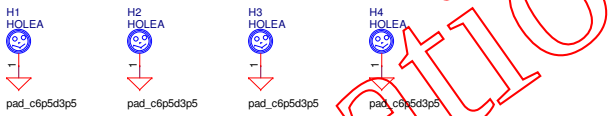

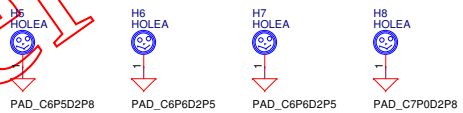

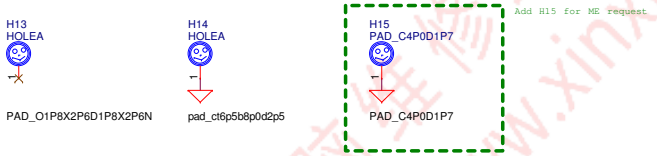

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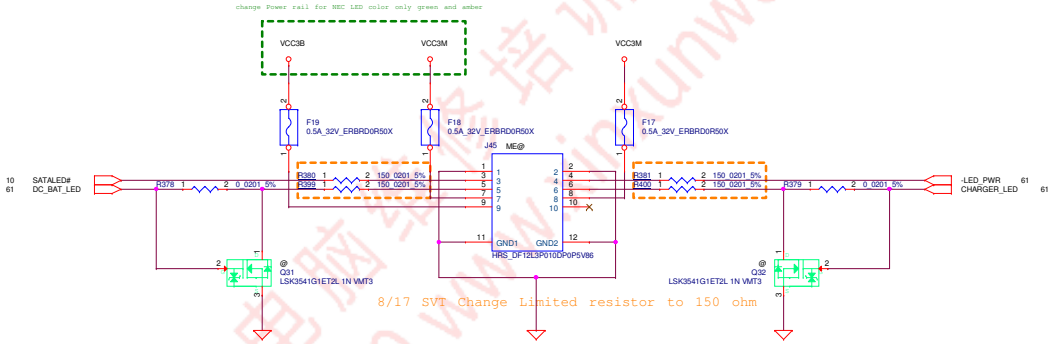

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