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CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

<Core Design>

Title:	Table of Contents	
Engineer:	*Surface*	
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 1 of 76	

Schematics Change History

Rev.	Date	Comments
0p9	28 Oct 2014	1. Starting with G_EV1_1021-1630.DSN 2. Added SL schematic from page 72 ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 3. Added External USB3 schematic from ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 4. Added external DP ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 5. Added IR_CAMERA from Front Camera...put in page 49 6. Removed page 73 PCIe GPU 7. Added Blade from T 8. Removed P72 T2B Pwr Transistors
0p10	3 Nov 2014	1. Changing to NVDC 2. Replaced GTX with GT, kept bypass caps 3. Replaced Charger with BQ24770
0p11	3 Nov 2014	1. Replace SKL-U with SKL-Y
0p12	11 Nov 2014	1. Model DDR connection from Intel SDS
0p13	18 Nov 2014	1. Added FUB information to all components 2. Changed Decretes.. sizing caps
0p14	20 Nov 2014	1. Added +5VA_SHA 2. Added T Cost Down/XCN's 3. Added SL +5V load Switch & Caps 4. Added Blade +5V load Switch & Caps
0p15	26 Nov 2014	1. Removed Boost 2. Re-adjusted usb ports on CPU 3. Removed Audio DSP
0p16	03 Dec 2014	1. changed +1VSB regulator 2. changed IR Camera/added diode 3. added power numbers from 0.91 PDG, Oct14 4. changed BLADE connector 5. cpu decoupling caps changed 6. changed +5V/+3V inductors (place holder)
0p17	05 Dec 2014	1. swapped M_A_CAA with MA_CAB on U1601/U1602 2. added two SAR chips, P32 3. remove tp's from csi lines on (p23) 4. change from 10 ceramic to 3 tantalum-poly on usb3 typeA (p45) 5. remove the RSENSE from output of +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) 6. change RSENSE input to 0402 from 0603 for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) input regulator 7. change inductor for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58) to HMLE20161B-1R0MDR-01 8. change RSENSE input to 0402 from 0603 for +5V_TS,+5V_SDXC,+5V_AUDIO,+5V, +5V_FAN(p64) 9. change RSENSE input to 0402 from 0603 for +3P3V_PANEL,+3P3V,+3P3V_SENSOR,+1P8V_DMIC (p65) 10. Replacing the SL connector with X908351-001 11. Replace PL5901 and PL5902 with CMLE042T-2R2MS-01 12. Replace 0402 1uf 6.3V with 0201 1uF 6.3V X5R 13. Replace L7201 with TOKO #A919CY-100M 14. Added VSYS -> BLADE FANG supply (p73)
0p18	09 Dec 2014	1. Reduced sizes of parts for Cameras (Resistors/Caps/Regulators)
0p19	12 Dec 2014	1. All 47uF caps become 0805/1mmZ 2. All 10uF caps become 0402...4V/6.3V
0p20	15 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x4 2. Shui Changes 3. more Shui Changes
0p21	16 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x5 2. changes from EV_schematic_issue_check_1216_JDM1.xlsx 3. changed name of +6_12 to +V_ALWAYS_ON 4. Removed 2 Mikes & Front Mike & added FPC conn 5. Added 2nd BLADE connector
0p22	17 Dec 2014	1. Replaced SD connector with AY531465T 2. changes from EV_schematic_issue_check_viola_1217_JDM1.xlsx
0p23 - current		1. See apexUfixes_revXpXX.xlsx

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors

S = Short after design fixed

Property: BUILD-OPT

DNP = Not Installed Part.

Title:	CHANGE HISTORY-1		
Engineer:	*Surface*		
Size: A3	Project Name: U -- EV 1.90		Rev: 1.90.2
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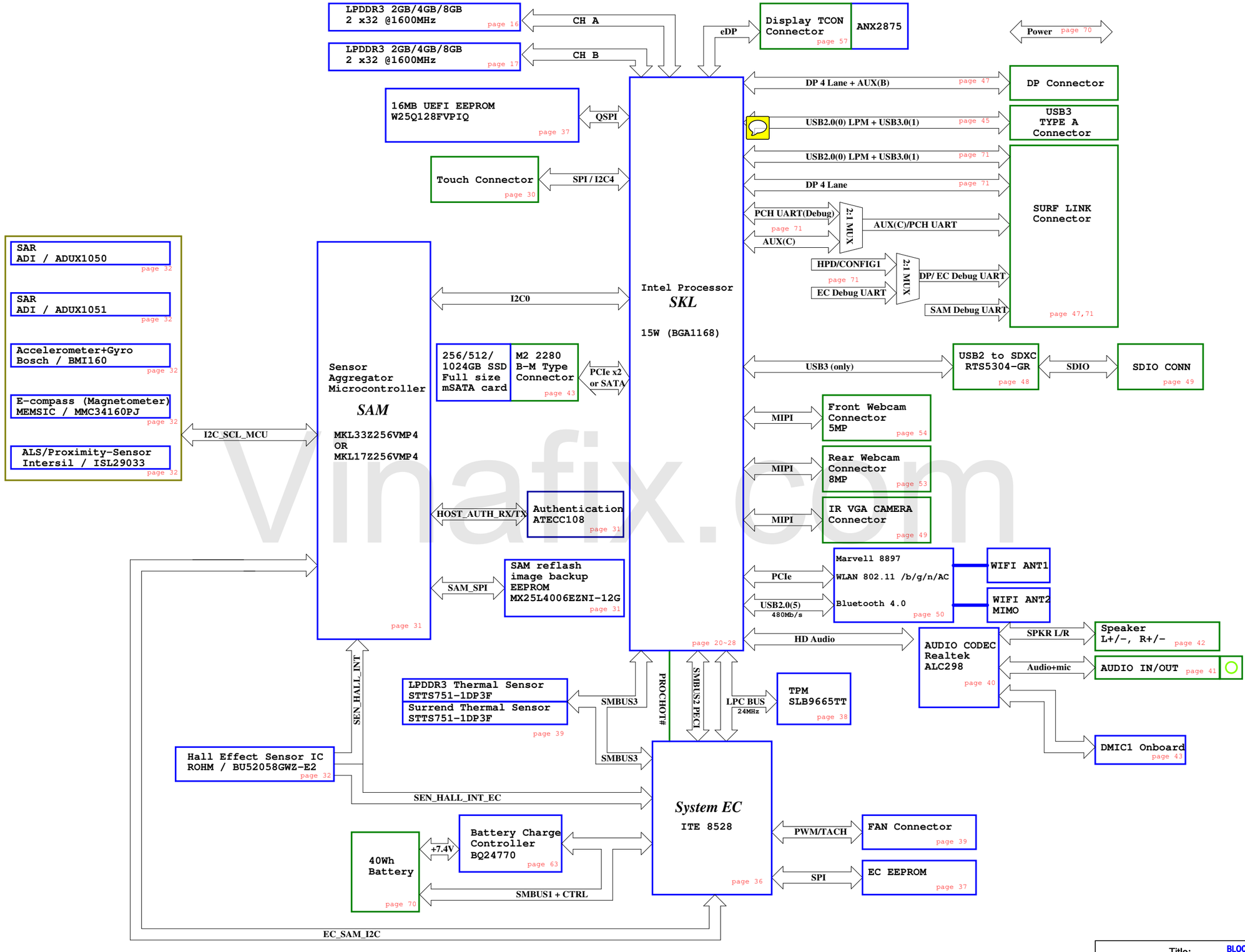

Title: BLOCK DIAGRAM

Microsoft Engineer: Surface

Size: Custom | Project Name: U -- EV 1.90 | Rev: 1.90.2

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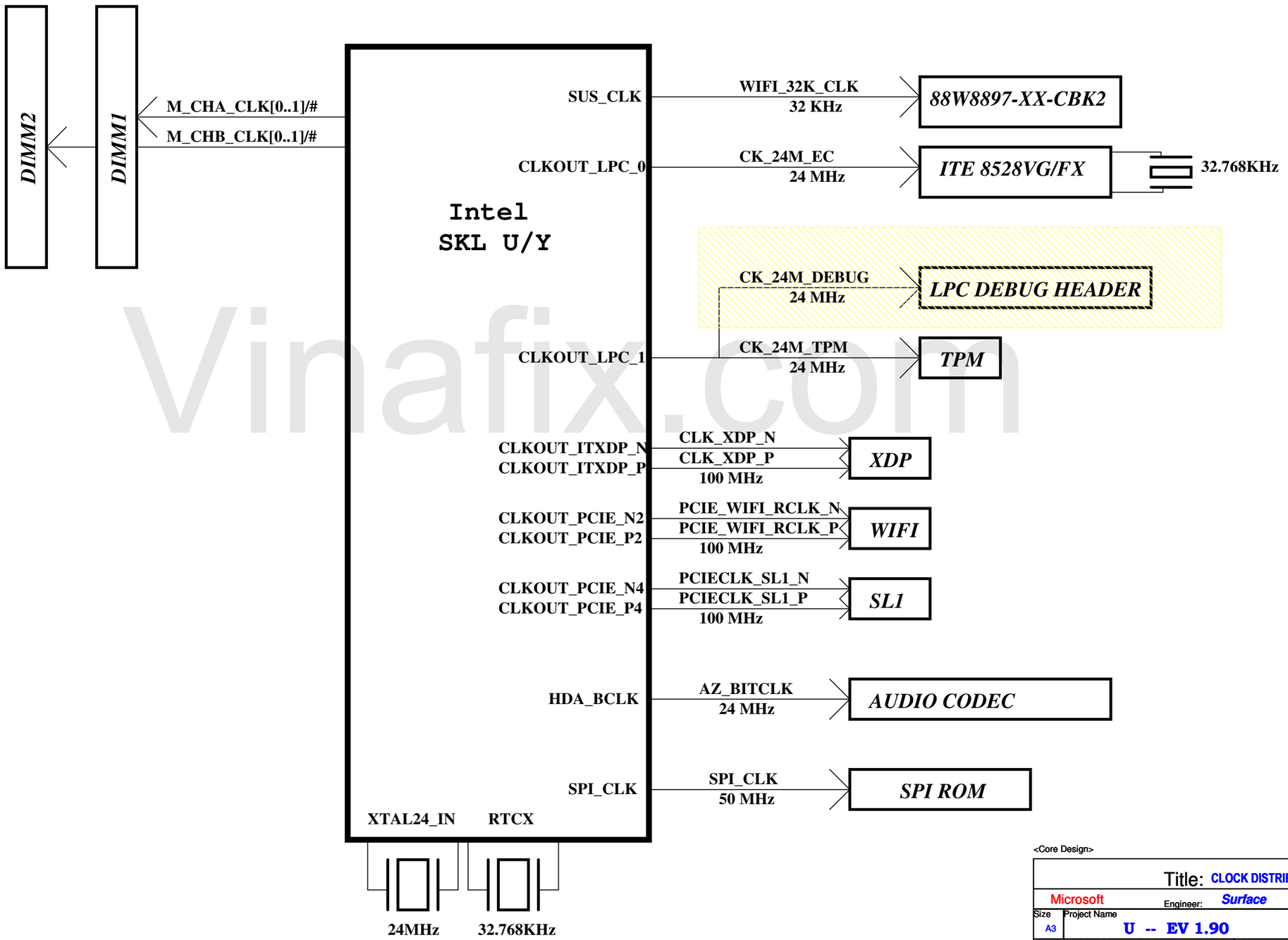
HSW Buffer Through Mode for Pre-Silicon



<Core Design>

Title: CLOCK DISTRIBUTION(TBD)

Microsoft Engineer: Surface

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

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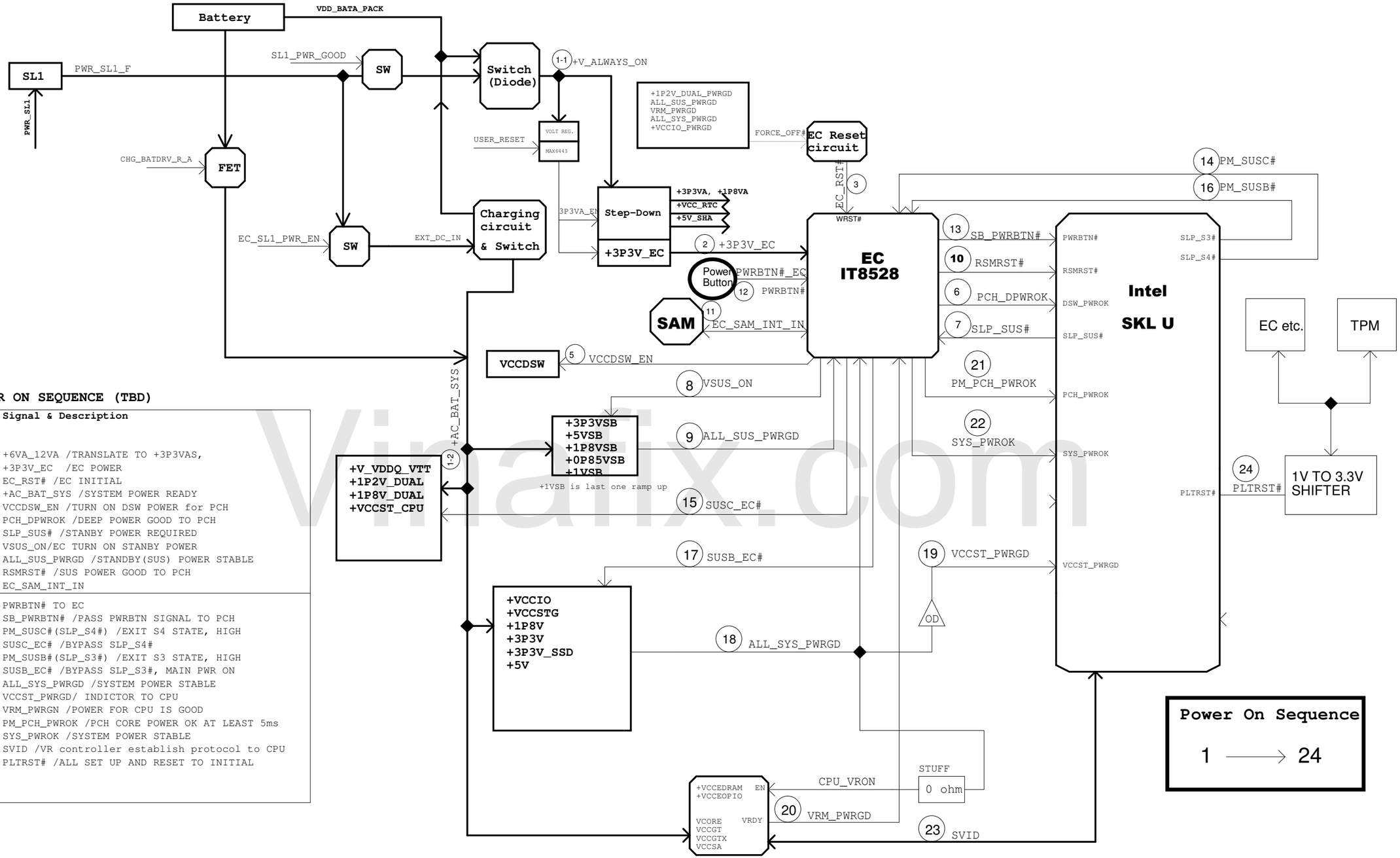
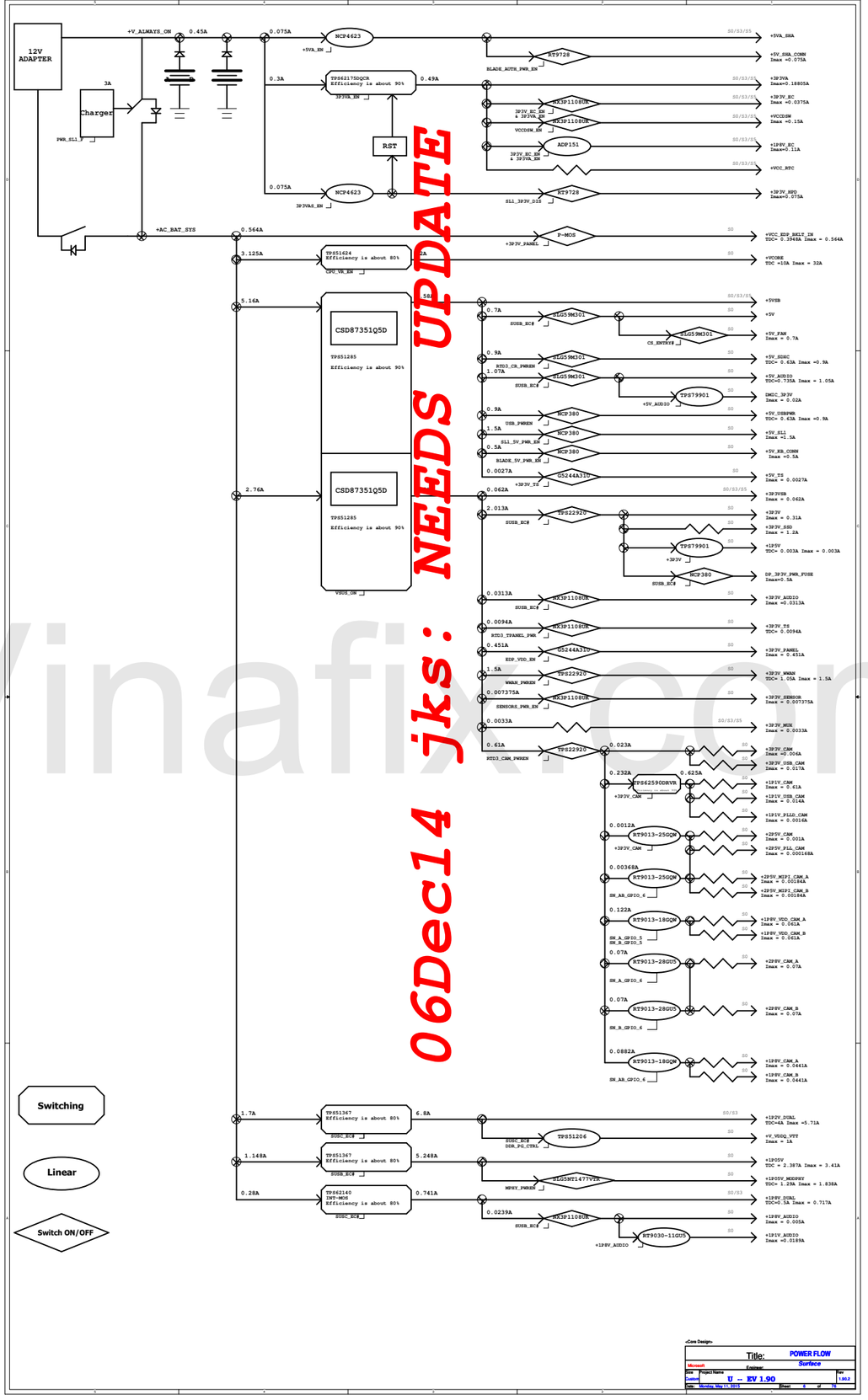


POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4.	+AC_BAT_SYS /SYSTEM POWER READY
5.	VCCDSW_EN /TURN ON DSW POWER for PCH
6.	PCH_DPWROK /DEEP POWER GOOD TO PCH
7.	SLP_SUS# /STANBY POWER REQUIRED
8.	VSUS_ON/EC TURN ON STANBY POWER
9.	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10.	RSMRST# /SUS POWER GOOD TO PCH
11.	EC_SAM_INT_IN
12	PWRBTN# TO EC
13.	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14.	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15.	SUSC_EC# /BYPASS SLP_S4#
16.	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17.	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18.	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19.	VCCST_PWRGD/ INDICTOR TO CPU
20.	VRM_PWRGN /POWER FOR CPU IS GOOD
21.	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
22.	SYS_PWROK /SYSTEM POWER STABLE
23.	SVID /VR controller establish protocol to CPU
24.	PLTRST# /ALL SET UP AND RESET TO INITIAL

<Core Design>

Title:	SIGNAL&RESET MAP
Microsoft	Surface
Engineer:	
Size: A2	Project Name: U -- EV 1.90
Rev:	1.90.2
Date: Monday, May 11, 2015	Sheet 5 of 76


12V ADAPTER
Charger
3A
PWR_SEL1
+V_ALWAYS_ON
0.45A
+AC_BAT_SYS
0.075A
NCP4623
+5VA_EN
0.3A
TPS62175QCR
Efficiency is about 90%
3P3VA_EN
0.49A
RST
0.075A
NCP4623
3P3VAS_EN
SLI_3P3V_DIS
RT9728
BLADE_AUTH_PWR_EN
MX3P1108UK
3P3V_EC_SW & 3P3VA_EN
VCCDSW_EN
ADP151
3P3V_EC_EN & 3P3VA_EN
+5VA_SHA
+5V_SHA_CONN Imax =0.075A
+3P3VA Imax=0.18805A
+3P3V_EC Imax =0.0375A
+VCCDSW Imax =0.15A
+1P8V_EC Imax=0.11A
+VCC_RTC
+3P3V_SSD Imax=0.075A
0.564A
P-MOS
+3P3V_PANEL
+VCC_EDP_BKLT_IN TDC= 0.3948A Imax = 0.564A
3.125A
TPS51624
Efficiency is about 80%
CPU_VR_EN
+VCORE TDC =10A Imax = 32A
5.16A
CSD87351Q5D
TPS51285
Efficiency is about 90%
+5VSB
0.7A
SUSB_EC#
+5V
+5V_FAN Imax = 0.7A
CS_ENTRY#
0.9A
RTD3_CR_PWREN
1.07A
+5V_SSDC TDC= 0.63A Imax =0.9A
+5V_AUDIO TDC=0.735A Imax = 1.05A
+5V_AUDIO
TPS79901
SMIC_3P3V Imax = 0.02A
0.9A
USB_PWREN
NCP380
+5V_USBPWR TDC= 0.63A Imax =0.9A
1.5A
SLI_5V_PWR_EN
+5V_SLI Imax =1.5A
0.5A
BLADE_5V_PWR_EN
+5V_KB_CONN Imax =0.5A
0.0027A
G5244A3ITG
+3P3V_TS
+5V_TS Imax = 0.0027A
0.062A
+3P3VSB Imax = 0.062A
2.76A
CSD87351Q5D
TPS51285
Efficiency is about 90%
VSUS_ON
2.013A
TPS22920
+3P3V Imax = 0.31A
+3P3V_SSD Imax = 1.2A
TPS79901
+1P5V TDC= 0.003A Imax = 0.003A
DP_3P3V_PWR_FUSE Imax=0.5A
0.0313A
+3P3V_AUDIO Imax =0.0313A
0.0094A
+3P3V_TS TDC= 0.0094A
0.451A
+3P3V_PANEL Imax = 0.451A
1.5A
WWAN_PWREN
+3P3V_WWAN TDC= 1.05A Imax = 1.5A
0.007375A
SENSORS_PWR_EN
+3P3V_SENSOR Imax = 0.007375A
0.0033A
+3P3V_MUX Imax = 0.0033A
0.61A
RTD3_CAM_PWREN
0.023A
+3P3V_CAM Imax =0.004A
+3P3V_USB_CAM Imax = 0.017A
0.232A
TPS62590DRVR
0.625A
+3P3V_CAM
+1P1V_CAM Imax = 0.61A
+1P1V_USB_CAM Imax = 0.014A
+1P1V_PLLD_CAM Imax = 0.0016A
0.0012A
RT9013-25GQW
+2P5V_CAM Imax = 0.001A
+2P5V_PLL_CAM Imax = 0.000168A
0.00368A
RT9013-25GQW
SM_AB_GPIO_4
+2P5V_MIPI_CAM_A Imax = 0.00184A
+2P5V_MIPI_CAM_B Imax = 0.00184A
0.122A
RT9013-18GQW
SM_A_GPIO_5 SM_B_GPIO_5
+1P8V_VDD_CAM_A Imax = 0.061A
+1P8V_VDD_CAM_B Imax = 0.061A
0.07A
RT9013-28GUS
SM_A_GPIO_6
+2P8V_CAM_A Imax = 0.07A
SM_B_GPIO_6
+2P8V_CAM_B Imax = 0.07A
0.0882A
RT9013-18GQW
SM_AB_GPIO_4
+1P8V_CAM_A Imax = 0.0441A
+1P8V_CAM_B Imax = 0.0441A
1.7A
TPS51367
Efficiency is about 80%
SUSC_EC#
6.8A
TPS51206
SUSC_EC# DDR_PG_CTRL
+1P2V_DUAL TDC=4A Imax =5.71A
+V_VDDQ_VTT Imax = 1A
1.148A
TPS51367
Efficiency is about 80%
SUSB_EC#
5.248A
SLG5NT1477VTR
MEMV_PWREN
+1P05V TDC = 2.387A Imax = 3.41A
+1P05V_MODPHY TDC= 1.29A Imax = 1.838A
+1P8V_DUAL TDC=0.5A Imax = 0.717A
0.28A
TPS62140
DWT-MOS
Efficiency is about 80%
SUSC_EC#
0.741A
0.0239A
MX3P1108UK
SUSB_EC#
RT9030-11GUS
+1P8V_AUDIO
+1P2V_AUDIO Imax = 0.005A
+1P1V_AUDIO Imax =0.0189A
Switching
Linear
Switch ON/OFF
NEEDS UPDATE
06Dec14 jks
<Core Design>
Title: POWER FLOW
Surface
Engineer:
Project Name: U -- EV 1.90
Rev: 1.90.2
Monday, May 11, 2015
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CPU Haswell ULT

+VCORE	-> 32A
+1P05V	-> 0.6A
+DDR_V (+1P2V_DUAL)	-> 2.5A
+1P05V	-> 2.81A
+1P05V_MODPHY	-> 1.838A
+1P5V	-> 0.003A
+3P3V	-> 0.200A
+3P3VSB	-> 0.062A
+3P3VA	-> 0.099A

LPDDR3

+1P8V_DUAL	-> 0.717A
+1P2V_DUAL	-> 3.210A
+VTT_DDQ_VTT(0.6V)	-> 1A

mSATA(SSD)

+3P3V	-> 1.2A

EC

+3P3V_EC	-> 0.012A

EC ROM

+3P3V_EC	-> 0.005A
+3P3VA	-> 0.00025A

Temp sensor(STTS751)

+3P3V_EC	-> 0.00025A

Camera

+1P1V_CAM	-> 0.609A
+1P1V_PLLD_CAM	-> 0.0016A
+1P1V_USB_CAM	-> 0.0137A
+1P8V_CAM	-> 0.0882A
+1P8V_VDD_CAM	-> 0.122A
+2P5V_CAM	-> 0.001A
+2P5V_PLL_CAM	-> 0.000168A
+2P5V_MIPI_CAM	-> 0.00368A
+2P8V_CAM	-> 0.14A
+3P3V_CAM	-> 0.006A
+3P3V_USB_CAM	-> 0.0169A

TPM(Infineon SLB9665 ESS2)

+3P3V_TPM (+3P3V)	-> 0.1A

SDXC

+5V_SDXC	-> 0.9A

WiFi&BT

+3P3V_WWAN	-> 1.5A

DMIC

DMIC_+3P3V/+3P3V_AUDIO	-> 0.02A

FAN

+5V_FAN	-> 0.7A

UEFI_SPI_BIOS_ROM

+3P3V	-> 0.04A

Panel

VCC_EDP_BKLT_IN	-> 0.564A
+3P3V_PANEL	-> 0.2A

Authentication IC (ECC108)

+3P3VA	-> 0.005A

Touch Interface

+3P3V_TS	-> 0.0094A
+5V_TS	-> 0.0027A

ALC3264 CODEC

+3P3V_AUDIO	-> 0.005A
+5V_AUDIO	-> 1.05A
+1P8V_AUDIO	-> 0.005A

DSP (ES320)

+3P3V_AUDIO	-> 0.0063A
+1P1V_AUDIO	-> 0.0189A

Sensor uC(ATUC256L3U-Z3UR)

+3P3VA	-> 0.061A

SL1

+3P3V_HPD	->0.075A
+5V_SL1	-> 1.5A

BLADE

+5V_KB_CONN	-> 0.5A

Hall effect sensor(BU52058GWZ-E2)

+3P3VA	->0.0028A

Compass(MMC3416XMA)

+3P3V_SENSOR	->0.0012A

Acceleromte&Gyro(LSM330TR)

+3P3V_SENSOR	-> 0.0061A

ALS(ISL29033ROZ-T7) FPC CON

+3P3V_SENSOR	-> 0.000075A

MUX

+3P3V_MUX	-> 0.033A

mini DP

+3P3V	-> 0.5A

USB 3.0 connector

+5VUSBPWR	-> 0.9A

Transceiver SN74AVCT245

+1P8V_EC	-> 0.11A

Battery Charger BQ24735

+V_ALWAYS_ON	-> 0.003A

06Dec14 jks: NEEDS UPDATE

<Core Design>

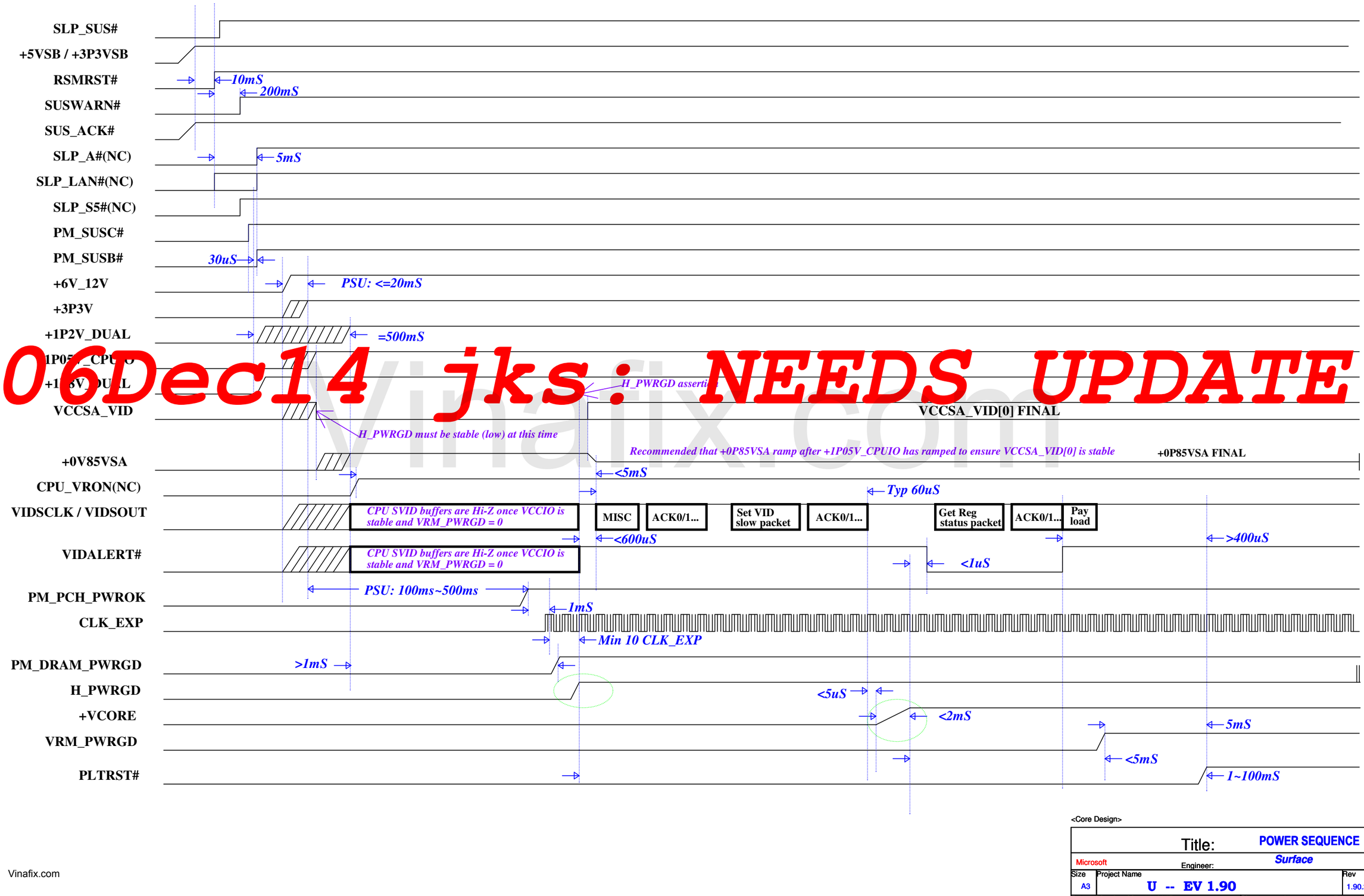
Title: POWER DISTRIBUTION

Microsoft Engineer: Surface

Size: Custom | Project Name: U -- EV 1.90 | Rev: 1.90.2

Date: Monday, May 11, 2015 Sheet 7 of 76

S5 to S0 Power Sequence



06Dec14 jks: NEEDS UPDATE

<Core Design>

Title:	POWER SEQUENCE	
Microsoft	Engineer:	Surface
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 8 of 76	

I2C & SMBUS Map

SML1_PCH_DATA
SML1_PCH_CLK

Q3501
Q3504

PCH
U1001

S
M
M
0x4D

PCH_I2C1_SDA_3V3
PCH_I2C1_SCL_3V3

R3001
R3003

TS_A_I2C_SDA_CON
TS_A_I2C_SCL_CON

Touch Connector
CON3001 0x60

Surrend
TEMP Sensor
U3901 0x4B

Skin
TEMP Sensor
U3902 0x3B

Skin
TEMP Sensor
U3903 0x3A

Skin
TEMP Sensor
U3904 0x4A

SML3_EC_DATA
SML3_EC_CLK

SH_I2C_SDA
SH_I2C_SCL

Debug Connector
CON3302

U3501

SML0_EC_DATA
SML0_EC_CLK

M
S
EC
U3601
M 0x4E

SAM
U3105
S
M
0x28

I2C_SDA_MCU_R
I2C_SCL_MCU_R

R3122
R3124

I2C_SDA_MCU
I2C_SCL_MCU

TEMP Sensor
U3211 0x3A

R3229
R3230

R3266
R3267

R3210
R3211

ADUX1050
U3206 0x2D

ADUX6

R3285
R3287

R3212
R3213

MAG2_X_SDA
MAG2_X_SCL

Accel & Gyro
U3202 0x68

MAG2_SCL_3V3
MAG2_SDA_3V3

Magnetometer
U3203 0x30

SML1_EC_DATA
SML1_EC_CLK

CHG_SDA_A
CHG_SCL_A

Charger
U6301 0x12

PR6309
PR6310
0 ohm

R7032/L7005
R7033/L7006

EC_SMCLK_BAT
EC_SMDATA_BAT

Battery
Connector
CON7001 0x16

ADUX1050
U3207 0x2C

ADUX7

R3286
R3288

Vinafix.com

Title: 09. I2C MAP
Engineer: Surface
Size: A3
Project Name: U -- EV 1.90
Rev: 1.90.2
Date: Monday, May 11, 2015
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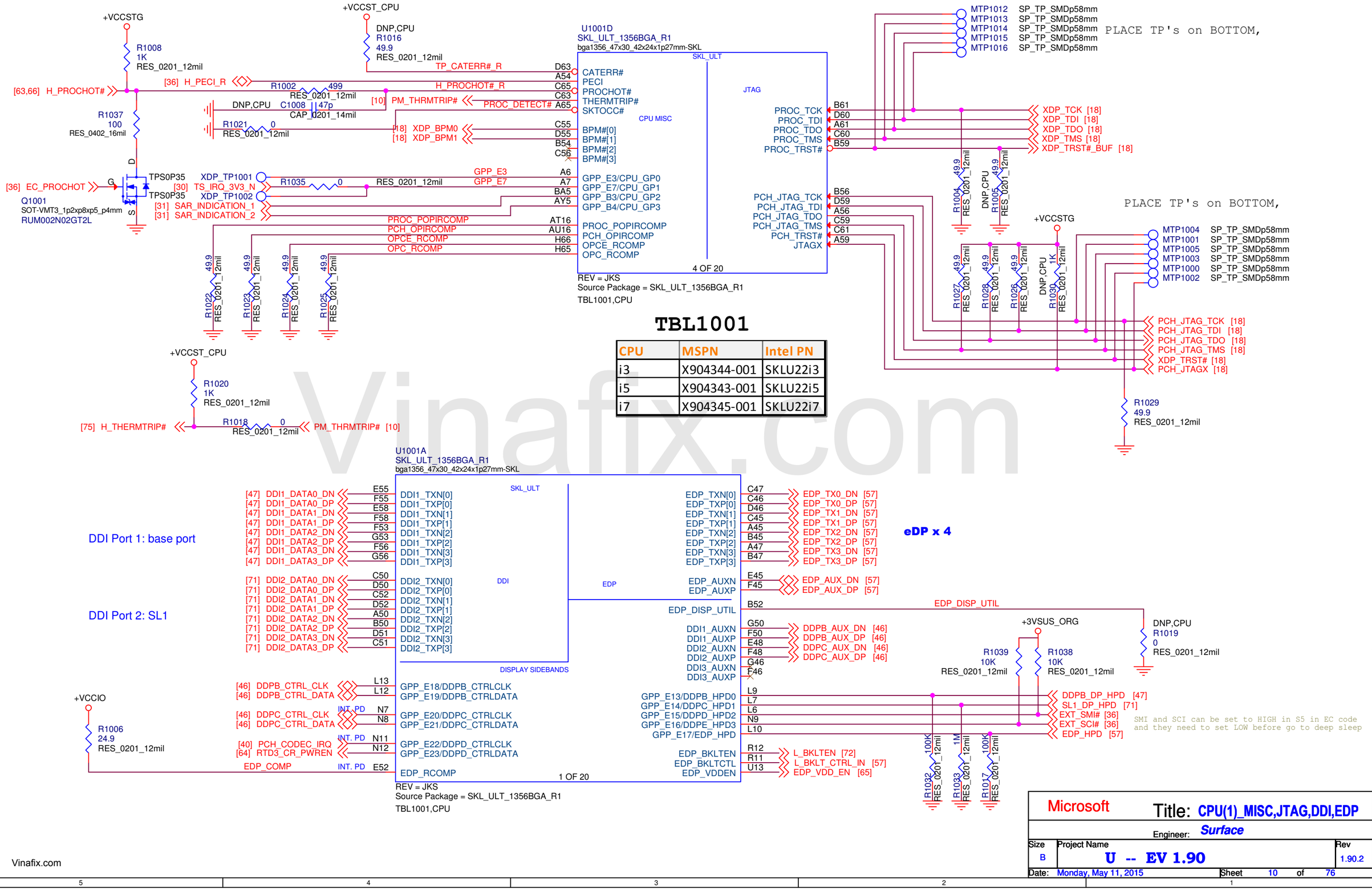
+VCCSTG
R1008
1K
RES_0201_12mil
[63,66] H_PROHOT#
R1037
100
RES_0402_16mil
[36] EC_PROHOT
Q1001
SOT-VMT3_1p2xp8xp5_p4mm
RUM002N02GT2L
TPS0P35
TPS0P35
+VCCST_CPU
DNP,CPU
R1016
49.9
RES_0201_12mil
[36] H_PECI_R
R1002
499
RES_0201_12mil
H_PROCHOT#_R
DNP,CPU
C1008
47p
CAP_0201_14mil
[10] PM_THRMTRIP#
R1021
0
RES_0201_12mil
[18] XDP_BPM0
[18] XDP_BPM1
XDP_TP1001
XDP_TP1002
[30] TS_IRQ_3V3_N
[31] SAR_INDICATION_1
[31] SAR_INDICATION_2
R1035
0
RES_0201_12mil
TP_CATERR#_R
PROC_DETECT#
GPP_E3
GPP_E7
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
R1022
R1023
R1024
R1025
49.9
RES_0201_12mil
U1001D
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
CPU MISC
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
4 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
TBL1001,CPU
JTAG
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST#
JTAGX
MTP1012 SP_TP_SMDp58mm
MTP1013 SP_TP_SMDp58mm
MTP1014 SP_TP_SMDp58mm
MTP1015 SP_TP_SMDp58mm
MTP1016 SP_TP_SMDp58mm
PLACE TP's on BOTTOM,
XDP_TCK [18]
XDP_TDI [18]
XDP_TDO [18]
XDP_TMS [18]
XDP_TRST#_BUF [18]
R1004
R1005
DNP,CPU
PLACE TP's on BOTTOM,
+VCCSTG
MTP1004 SP_TP_SMDp58mm
MTP1001 SP_TP_SMDp58mm
MTP1005 SP_TP_SMDp58mm
MTP1003 SP_TP_SMDp58mm
MTP1000 SP_TP_SMDp58mm
MTP1002 SP_TP_SMDp58mm
R1027
R1028
R1026
DNP,CPU
1K
R1030
PCH_JTAG_TCK [18]
PCH_JTAG_TDI [18]
PCH_JTAG_TDO [18]
PCH_JTAG_TMS [18]
XDP_TRST# [18]
PCH_JTAGX [18]
R1029
49.9
RES_0201_12mil
TBL1001
CPU
MSPN
Intel PN
i3
X904344-001
SKLU22i3
i5
X904343-001
SKLU22i5
i7
X904345-001
SKLU22i7
+VCCST_CPU
R1020
1K
RES_0201_12mil
[75] H_THERMTRIP#
R1018
0
RES_0201_12mil
PM_THRMTRIP# [10]
U1001A
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
DDI1_TXN[0]
DDI1_TXP[0]
DDI1_TXN[1]
DDI1_TXP[1]
DDI1_TXN[2]
DDI1_TXP[2]
DDI1_TXN[3]
DDI1_TXP[3]
DDI2_TXN[0]
DDI2_TXP[0]
DDI2_TXN[1]
DDI2_TXP[1]
DDI2_TXN[2]
DDI2_TXP[2]
DDI2_TXN[3]
DDI2_TXP[3]
DDI
DISPLAY SIDEBANDS
GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA
EDP_RCOMP
1 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
TBL1001,CPU
DDI Port 1: base port
DDI Port 2: SL1
[47] DDI1_DATA0_DN
[47] DDI1_DATA0_DP
[47] DDI1_DATA1_DN
[47] DDI1_DATA1_DP
[47] DDI1_DATA2_DN
[47] DDI1_DATA2_DP
[47] DDI1_DATA3_DN
[47] DDI1_DATA3_DP
[71] DDI2_DATA0_DN
[71] DDI2_DATA0_DP
[71] DDI2_DATA1_DN
[71] DDI2_DATA1_DP
[71] DDI2_DATA2_DN
[71] DDI2_DATA2_DP
[71] DDI2_DATA3_DN
[71] DDI2_DATA3_DP
[46] DDPB_CTRL_CLK
[46] DDPB_CTRL_DATA
[46] DDPC_CTRL_CLK
[46] DDPC_CTRL_DATA
[40] PCH_CODEC_IRQ
[64] RTD3_CR_PWREN
INT. PD
EDP_COMP
+VCCIO
R1006
24.9
RES_0201_12mil
EDP_TXN[0]
EDP_TXP[0]
EDP_TXN[1]
EDP_TXP[1]
EDP_TXN[2]
EDP_TXP[2]
EDP_TXN[3]
EDP_TXP[3]
EDP_AUXN
EDP_AUXP
EDP_DISP_UTIL
DDI1_AUXN
DDI1_AUXP
DDI2_AUXN
DDI2_AUXP
DDI3_AUXN
DDI3_AUXP
GPP_E13/DDPB_HPD0
GPP_E14/DDPC_HPD1
GPP_E15/DDPD_HPD2
GPP_E16/DDPE_HPD3
GPP_E17/EDP_HPD
EDP_BKLTEN
EDP_BKLTCTL
EDP_VDDEN
EDP
eDP x 4
EDP_TX0_DN [57]
EDP_TX0_DP [57]
EDP_TX1_DN [57]
EDP_TX1_DP [57]
EDP_TX2_DN [57]
EDP_TX2_DP [57]
EDP_TX3_DN [57]
EDP_TX3_DP [57]
EDP_AUX_DN [57]
EDP_AUX_DP [57]
EDP_DISP_UTIL
+3VSUS_ORG
DNP,CPU
R1019
0
RES_0201_12mil
R1039
10K
RES_0201_12mil
R1038
10K
RES_0201_12mil
DDPB_AUX_DN [46]
DDPB_AUX_DP [46]
DDPC_AUX_DN [46]
DDPC_AUX_DP [46]
DDPB_DP_HPD [47]
SL1_DP_HPD [71]
EXT_SMI# [36]
EXT_SCI# [36]
EDP_HPD [57]
SMI and SCI can be set to HIGH in S5 in EC code
and they need to set LOW before go to deep sleep
L_BKLTEN [72]
L_BKLT_CTRL_IN [57]
EDP_VDD_EN [65]
100K
1M
100K
R1032
R1033
R1017
Microsoft
Title: CPU(1)_MISC,JTAG,DDI,EDP
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
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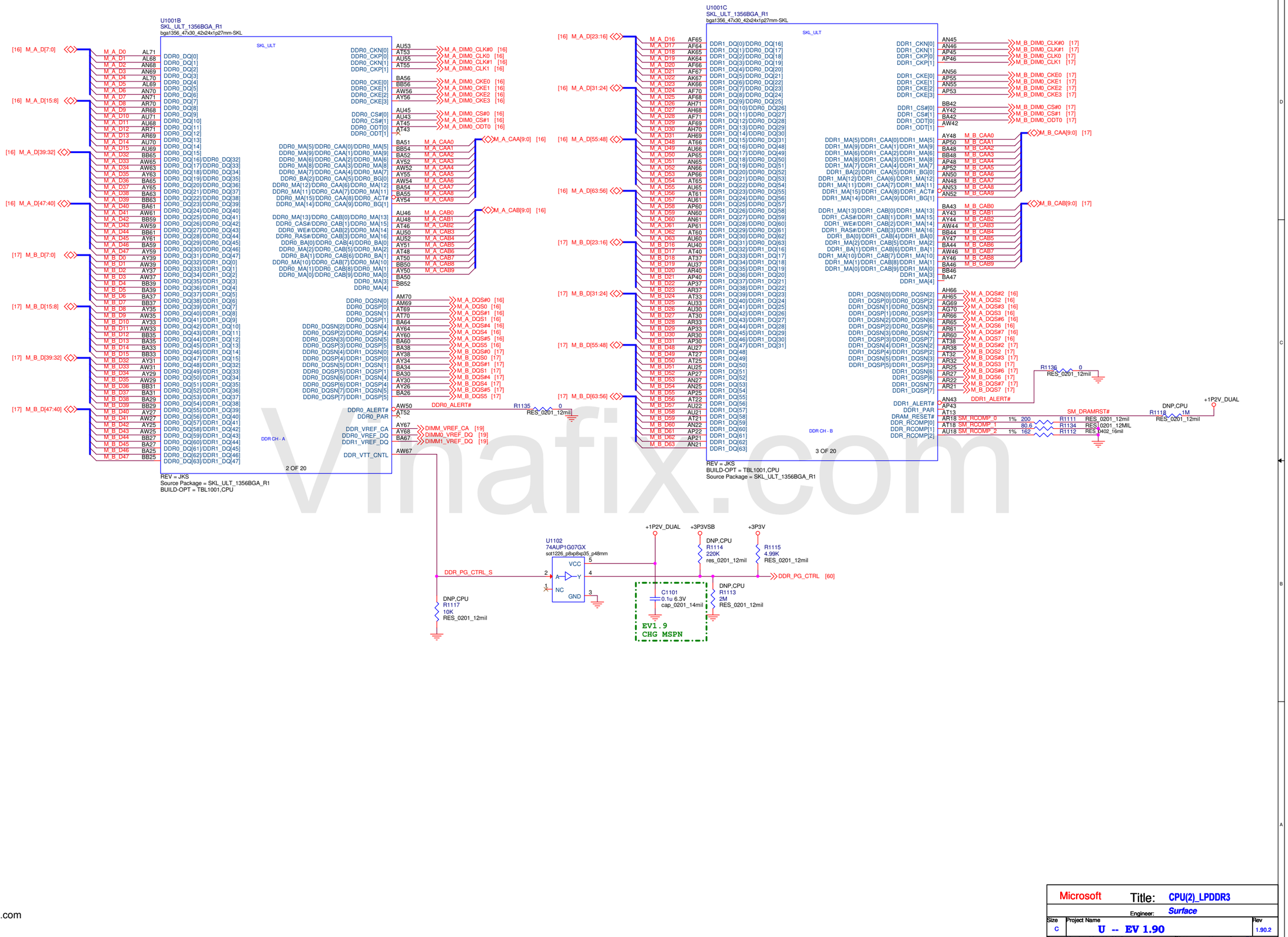
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bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
[16] M_A_D[7:0]
[16] M_A_D[15:8]
[16] M_A_D[39:32]
[16] M_A_D[47:40]
[17] M_B_D[7:0]
[17] M_B_D[15:8]
[17] M_B_D[39:32]
[17] M_B_D[47:40]
M_A_D0 AL71
M_A_D1 AL68
M_A_D2 AN68
M_A_D3 AN69
M_A_D4 AL70
M_A_D5 AL69
M_A_D6 AN70
M_A_D7 AN71
M_A_D8 AR70
M_A_D9 AR68
M_A_D10 AU71
M_A_D11 AU68
M_A_D12 AR71
M_A_D13 AR69
M_A_D14 AU70
M_A_D15 AU69
M_A_D32 BB65
M_A_D33 AW65
M_A_D34 AW63
M_A_D35 AY63
M_A_D36 BA65
M_A_D37 AY65
M_A_D38 BA63
M_A_D39 BB63
M_A_D40 BA61
M_A_D41 AW61
M_A_D42 BB59
M_A_D43 AW59
M_A_D44 BB61
M_A_D45 AY61
M_A_D46 BA59
M_A_D47 AY59
M_B_D0 AY39
M_B_D1 AW39
M_B_D2 AY37
M_B_D3 AW37
M_B_D4 BB39
M_B_D5 BA39
M_B_D6 BA37
M_B_D7 BB37
M_B_D8 AY35
M_B_D9 AW35
M_B_D10 AY33
M_B_D11 AW33
M_B_D12 BB35
M_B_D13 BA35
M_B_D14 BA33
M_B_D15 BB33
M_B_D32 AY31
M_B_D33 AW31
M_B_D34 AY29
M_B_D35 AW29
M_B_D36 BB31
M_B_D37 BA31
M_B_D38 BB29
M_B_D39 BB29
M_B_D40 AY27
M_B_D41 AW27
M_B_D42 AY25
M_B_D43 AW25
M_B_D44 BB27
M_B_D45 BA27
M_B_D46 BA25
M_B_D47 BB25
DDR0_DQ[0] DDR0_DQ[1] DDR0_DQ[2] DDR0_DQ[3] DDR0_DQ[4] DDR0_DQ[5] DDR0_DQ[6] DDR0_DQ[7] DDR0_DQ[8] DDR0_DQ[9] DDR0_DQ[10] DDR0_DQ[11] DDR0_DQ[12] DDR0_DQ[13] DDR0_DQ[14] DDR0_DQ[15]
DDR0_DQ[16]/DDR0_DQ[32] DDR0_DQ[17]/DDR0_DQ[33] DDR0_DQ[18]/DDR0_DQ[34] DDR0_DQ[19]/DDR0_DQ[35] DDR0_DQ[20]/DDR0_DQ[36] DDR0_DQ[21]/DDR0_DQ[37] DDR0_DQ[22]/DDR0_DQ[38] DDR0_DQ[23]/DDR0_DQ[39] DDR0_DQ[24]/DDR0_DQ[40] DDR0_DQ[25]/DDR0_DQ[41] DDR0_DQ[26]/DDR0_DQ[42] DDR0_DQ[27]/DDR0_DQ[43] DDR0_DQ[28]/DDR0_DQ[44] DDR0_DQ[29]/DDR0_DQ[45] DDR0_DQ[30]/DDR0_DQ[46] DDR0_DQ[31]/DDR0_DQ[47]
DDR0_DQ[32]/DDR1_DQ[0] DDR0_DQ[33]/DDR1_DQ[1] DDR0_DQ[34]/DDR1_DQ[2] DDR0_DQ[35]/DDR1_DQ[3] DDR0_DQ[36]/DDR1_DQ[4] DDR0_DQ[37]/DDR1_DQ[5] DDR0_DQ[38]/DDR1_DQ[6] DDR0_DQ[39]/DDR1_DQ[7] DDR0_DQ[40]/DDR1_DQ[8] DDR0_DQ[41]/DDR1_DQ[9] DDR0_DQ[42]/DDR1_DQ[10] DDR0_DQ[43]/DDR1_DQ[11] DDR0_DQ[44]/DDR1_DQ[12] DDR0_DQ[45]/DDR1_DQ[13] DDR0_DQ[46]/DDR1_DQ[14] DDR0_DQ[47]/DDR1_DQ[15]
DDR0_DQ[48]/DDR1_DQ[32] DDR0_DQ[49]/DDR1_DQ[33] DDR0_DQ[50]/DDR1_DQ[34] DDR0_DQ[51]/DDR1_DQ[35] DDR0_DQ[52]/DDR1_DQ[36] DDR0_DQ[53]/DDR1_DQ[37] DDR0_DQ[54]/DDR1_DQ[38] DDR0_DQ[55]/DDR1_DQ[39] DDR0_DQ[56]/DDR1_DQ[40] DDR0_DQ[57]/DDR1_DQ[41] DDR0_DQ[58]/DDR1_DQ[42] DDR0_DQ[59]/DDR1_DQ[43] DDR0_DQ[60]/DDR1_DQ[44] DDR0_DQ[61]/DDR1_DQ[45] DDR0_DQ[62]/DDR1_DQ[46] DDR0_DQ[63]/DDR1_DQ[47]
DDR0_CKN[0] DDR0_CKP[0] DDR0_CKN[1] DDR0_CKP[1]
DDR0_CKE[0] DDR0_CKE[1] DDR0_CKE[2] DDR0_CKE[3]
DDR0_CS#[0] DDR0_CS#[1] DDR0_ODT[0] DDR0_ODT[1]
AU53 AT53 AU55 AT55
BA56 BB56 AW56 AY56
AU45 AU43 AT45 AT43
M_A_DIM0_CLK#0 [16]
M_A_DIM0_CLK0 [16]
M_A_DIM0_CLK#1 [16]
M_A_DIM0_CLK1 [16]
M_A_DIM0_CKE0 [16]
M_A_DIM0_CKE1 [16]
M_A_DIM0_CKE2 [16]
M_A_DIM0_CKE3 [16]
M_A_DIM0_CS#0 [16]
M_A_DIM0_CS#1 [16]
M_A_DIM0_ODT0 [16]
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]
BA51 BB54 BA52 AW52 AW54 BA54 BB55 AY54
M_A_CAA0 M_A_CAA1 M_A_CAA2 M_A_CAA3 M_A_CAA4 M_A_CAA5 M_A_CAA6 M_A_CAA7 M_A_CAA8 M_A_CAA9
M_A_CAA[9:0] [16]
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]
DDR0_MA[3]
DDR0_MA[4]
AU46 AU48 AT46 AU50 AU52 AY51 AT48 AT50 BB50 AY50 BA50 BB52
M_A_CAB0 M_A_CAB1 M_A_CAB2 M_A_CAB3 M_A_CAB4 M_A_CAB5 M_A_CAB6 M_A_CAB7 M_A_CAB8 M_A_CAB9
M_A_CAB[9:0] [16]
DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1] DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5] DDR0_DQSN[1] DDR0_DQSP[1] DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]
AM70 AM69 AT70 BA64 AY64 AY60 BA60 BA38 AY38 AY34 BA34 BA30 AY30 AY26 BA26
M_A_DQS#0 [16]
M_A_DQS0 [16]
M_A_DQS#1 [16]
M_A_DQS1 [16]
M_A_DQS#4 [16]
M_A_DQS4 [16]
M_A_DQS#5 [16]
M_A_DQS5 [16]
M_B_DQS#0 [17]
M_B_DQS0 [17]
M_B_DQS#1 [17]
M_B_DQS1 [17]
M_B_DQS#4 [17]
M_B_DQS4 [17]
M_B_DQS#5 [17]
M_B_DQS5 [17]
DDR0_ALERT#
DDR0_PAR
AW50 AT52
DDR0_ALERT#
R1135 0 RES_0201_12mil
DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ
AY67 AY68 BA67
DIMM_VREF_CA [19]
DIMM0_VREF_DQ [19]
DIMM1_VREF_DQ [19]
DDR_VTT_CNTL
AW67
DDR CH - A
2 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU
U1001C
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
[16] M_A_D[23:16]
[16] M_A_D[31:24]
[16] M_A_D[55:48]
[16] M_A_D[63:56]
[17] M_B_D[23:16]
[17] M_B_D[31:24]
[17] M_B_D[55:48]
[17] M_B_D[63:56]
M_A_D16 AF65
M_A_D17 AF64
M_A_D18 AK65
M_A_D19 AK64
M_A_D20 AF66
M_A_D21 AF67
M_A_D22 AK67
M_A_D23 AK66
M_A_D24 AF70
M_A_D25 AF68
M_A_D26 AH71
M_A_D27 AH68
M_A_D28 AF71
M_A_D29 AF69
M_A_D30 AH70
M_A_D31 AH69
M_A_D48 AT66
M_A_D49 AU66
M_A_D50 AP65
M_A_D51 AN65
M_A_D52 AN66
M_A_D53 AP66
M_A_D54 AT65
M_A_D55 AU65
M_A_D56 AT61
M_A_D57 AU61
M_A_D58 AP60
M_A_D59 AN60
M_A_D60 AN61
M_A_D61 AP61
M_A_D62 AT60
M_A_D63 AU60
M_B_D16 AU40
M_B_D17 AT40
M_B_D18 AT37
M_B_D19 AU37
M_B_D20 AR40
M_B_D21 AP40
M_B_D22 AP37
M_B_D23 AR37
M_B_D24 AT33
M_B_D25 AU33
M_B_D26 AU30
M_B_D27 AT30
M_B_D28 AR33
M_B_D29 AP33
M_B_D30 AR30
M_B_D31 AP30
M_B_D48 AU27
M_B_D49 AT27
M_B_D50 AT25
M_B_D51 AU25
M_B_D52 AP27
M_B_D53 AN27
M_B_D54 AN25
M_B_D55 AP25
M_B_D56 AT22
M_B_D57 AU22
M_B_D58 AU21
M_B_D59 AT21
M_B_D60 AN22
M_B_D61 AP22
M_B_D62 AP21
M_B_D63 AN21
DDR1_DQ[0]/DDR0_DQ[16] DDR1_DQ[1]/DDR0_DQ[17] DDR1_DQ[2]/DDR0_DQ[18] DDR1_DQ[3]/DDR0_DQ[19] DDR1_DQ[4]/DDR0_DQ[20] DDR1_DQ[5]/DDR0_DQ[21] DDR1_DQ[6]/DDR0_DQ[22] DDR1_DQ[7]/DDR0_DQ[23] DDR1_DQ[8]/DDR0_DQ[24] DDR1_DQ[9]/DDR0_DQ[25] DDR1_DQ[10]/DDR0_DQ[26] DDR1_DQ[11]/DDR0_DQ[27] DDR1_DQ[12]/DDR0_DQ[28] DDR1_DQ[13]/DDR0_DQ[29] DDR1_DQ[14]/DDR0_DQ[30] DDR1_DQ[15]/DDR0_DQ[31]
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DDR1_DQ[32]/DDR1_DQ[16] DDR1_DQ[33]/DDR1_DQ[17] DDR1_DQ[34]/DDR1_DQ[18] DDR1_DQ[35]/DDR1_DQ[19] DDR1_DQ[36]/DDR1_DQ[20] DDR1_DQ[37]/DDR1_DQ[21] DDR1_DQ[38]/DDR1_DQ[22] DDR1_DQ[39]/DDR1_DQ[23] DDR1_DQ[40]/DDR1_DQ[24] DDR1_DQ[41]/DDR1_DQ[25] DDR1_DQ[42]/DDR1_DQ[26] DDR1_DQ[43]/DDR1_DQ[27] DDR1_DQ[44]/DDR1_DQ[28] DDR1_DQ[45]/DDR1_DQ[29] DDR1_DQ[46]/DDR1_DQ[30] DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48] DDR1_DQ[49] DDR1_DQ[50] DDR1_DQ[51] DDR1_DQ[52] DDR1_DQ[53] DDR1_DQ[54] DDR1_DQ[55] DDR1_DQ[56] DDR1_DQ[57] DDR1_DQ[58] DDR1_DQ[59] DDR1_DQ[60] DDR1_DQ[61] DDR1_DQ[62] DDR1_DQ[63]
DDR1_CKN[0] DDR1_CKP[0] DDR1_CKN[1] DDR1_CKP[1]
DDR1_CKE[0] DDR1_CKE[1] DDR1_CKE[2] DDR1_CKE[3]
DDR1_CS#[0] DDR1_CS#[1] DDR1_ODT[0] DDR1_ODT[1]
AN45 AN46 AP45 AP46
AN56 AP55 AN55 AP53
BB42 AY42 BA42 AW42
M_B_DIM0_CLK#0 [17]
M_B_DIM0_CLK#1 [17]
M_B_DIM0_CLK0 [17]
M_B_DIM0_CLK1 [17]
M_B_DIM0_CKE0 [17]
M_B_DIM0_CKE1 [17]
M_B_DIM0_CKE2 [17]
M_B_DIM0_CKE3 [17]
M_B_DIM0_CS#0 [17]
M_B_DIM0_CS#1 [17]
M_B_DIM0_ODT0 [17]
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]
AY48 AP50 BA48 BB48 AP48 AP52 AN50 AN48 AN53 AN52
M_B_CAA0 M_B_CAA1 M_B_CAA2 M_B_CAA3 M_B_CAA4 M_B_CAA5 M_B_CAA6 M_B_CAA7 M_B_CAA8 M_B_CAA9
M_B_CAA[9:0] [17]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[3]
DDR1_MA[4]
BA43 AY43 AY44 AW44 BB44 AY47 BA44 AW46 AY46 BA46 BB46 BA47
M_B_CAB0 M_B_CAB1 M_B_CAB2 M_B_CAB3 M_B_CAB4 M_B_CAB5 M_B_CAB6 M_B_CAB7 M_B_CAB8 M_B_CAB9
M_B_CAB[9:0] [17]
DDR1_DQSN[0]/DDR0_DQSN[2] DDR1_DQSP[0]/DDR0_DQSP[2] DDR1_DQSN[1]/DDR0_DQSN[3] DDR1_DQSP[1]/DDR0_DQSP[3] DDR1_DQSN[2]/DDR0_DQSN[6] DDR1_DQSP[2]/DDR0_DQSP[6] DDR1_DQSN[3]/DDR0_DQSN[7] DDR1_DQSP[3]/DDR0_DQSP[7] DDR1_DQSN[4]/DDR1_DQSN[2] DDR1_DQSP[4]/DDR1_DQSP[2] DDR1_DQSN[5]/DDR1_DQSN[3] DDR1_DQSP[5]/DDR1_DQSP[3] DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]
AH66 AH65 AG69 AG70 AR66 AR65 AR61 AR60 AT38 AR38 AT32 AR32 AR25 AR27 AR22 AR21
M_A_DQS#2 [16]
M_A_DQS2 [16]
M_A_DQS#3 [16]
M_A_DQS3 [16]
M_A_DQS#6 [16]
M_A_DQS6 [16]
M_A_DQS#7 [16]
M_A_DQS7 [16]
M_B_DQS#2 [17]
M_B_DQS2 [17]
M_B_DQS#3 [17]
M_B_DQS3 [17]
M_B_DQS#6 [17]
M_B_DQS6 [17]
M_B_DQS#7 [17]
M_B_DQS7 [17]
DDR1_ALERT#
DDR1_PAR
DRAM_RESET#
DDR_RCOMP[0]
DDR_RCOMP[1]
DDR_RCOMP[2]
AN43 AP43 AT13 AR18 AT18 AU18
R1136 0 RES_0201_12mil
SM_DRAMRST#
SM_RCOMP_0 1% 200 R1111 RES_0201_12mil
SM_RCOMP_1 1% 80.6 R1134 RES_0201_12MIL
SM_RCOMP_2 1% 162 R1112 RES_0402_16mil
DNP,CPU
R1118 1M RES_0201_12mil
+1P2V_DUAL
DDR CH - B
3 OF 20
REV = JKS
BUILD-OPT = TBL1001,CPU
Source Package = SKL_ULT_1356BGA_R1
U1102
74AUP1G07GX
sot1226_p8xp8xp35_p48mm
VCC A Y NC GND
DDR_PG_CTRL_S
DDR_PG_CTRL [60]
+1P2V_DUAL +3P3VSB +3P3V
DNP,CPU R1117 10K RES_0201_12mil
DNP,CPU R1114 220K res_0201_12mil
R1115 4.99K RES_0201_12mil
C1101 0.1u 6.3V cap_0201_14mil
DNP,CPU R1113 2M RES_0201_12mil
EV1..9
CHG MSPN
Microsoft
Title: CPU(2)_LPDDR3
Engineer: Surface
Size C
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 11 of 76

+1P2V_DUAL

C13017 22u 4V cap_0603_40mil
C13018 22u 4V cap_0603_40mil
C13019 22u 4V cap_0603_40mil

C1241 10u 6.3V CAP_0402_28mil
C1240 10u 6.3V CAP_0402_28mil
C1239 10u 6.3V CAP_0402_28mil
C1238 10u 6.3V CAP_0402_28mil

Place on secondary side, underneath the package

C1237 10u 4V cap_0402_0p65mm
C1236 10u 4V cap_0402_0p65mm
C1244 1u 6.3V CAP_0201_14mil
C1243 1u 6.3V CAP_0201_14mil
C1242 1u 6.3V CAP_0201_14mil
C1232 1u 6.3V CAP_0201_14mil

R1201 0 RES_0402_16mil

C13020 10u 4V cap_0402_0p65mm

Place on secondary side, underneath the package

C1245 1u 6.3V CAP_0201_14mil

+VCCST_CPU

C1246 1u 6.3V CAP_0402_22mil

from lVSB, control SLP_S4 (S3 rail)

+VCCSTG

Place on secondary side, underneath the package

C1247 1u 6.3V CAP_0402_22mil

+VCCST_CPU

C1249 1u 6.3V CAP_0402_22mil

C1248 1u 6.3V CAP_0402_22mil

+VCCPLL_OC

R1202 0 RES_0402_16mil

U1001N
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
CPU POWER 3 OF 4

AU23	VDDQ_AU23
AU28	VDDQ_AU28
AU35	VDDQ_AU35
AU42	VDDQ_AU42
BB23	VDDQ_BB23
BB32	VDDQ_BB32
BB41	VDDQ_BB41
BB47	VDDQ_BB47
BB51	VDDQ_BB51
AM40	VDDQC
A18	VCCST
A22	VCCSTG_A22
AL23	VCCPLL_OC
K20	VCCPLL_K20
K21	VCCPLL_K21
AM23	VCCIO_SENSE
AM22	VSSIO_SENSE
H21	VSSSA_SENSE
H20	VCCSA_SENSE

14 OF 20

REV = JKS

VCCIO_SENSE [56]
VSSSA_SENSE [66]
VCCSA_SENSE [66]

Place on secondary side, underneath the package

C1262 10u 4V cap_0402_0p65mm
C1261 10u 4V cap_0402_0p65mm
C1259 1u 6.3V CAP_0201_14mil
C1258 1u 6.3V CAP_0201_14mil
C1257 1u 6.3V CAP_0201_14mil
C1260 1u 6.3V CAP_0201_14mil
C1265 1u 6.3V CAP_0402_22mil
C1266 1u 6.3V CAP_0402_22mil
C1263 1u 6.3V CAP_0402_22mil
C1264 1u 6.3V CAP_0402_22mil

+VCCIO

AK28	VCCIO
AK30	VCCIO
AL30	VCCIO
AL42	VCCIO
AM28	VCCIO
AM30	VCCIO
AM42	VCCIO
AK23	VCCSA
AK25	VCCSA
G23	VCCSA
G25	VCCSA
G27	VCCSA
G28	VCCSA
J22	VCCSA
J23	VCCSA
J27	VCCSA
K23	VCCSA
K25	VCCSA
K27	VCCSA
K28	VCCSA
K30	VCCSA

Place on secondary side, underneath the package

C1273 1u 6.3V CAP_0201_14mil
C1274 1u 6.3V CAP_0201_14mil
C1275 1u 6.3V CAP_0201_14mil
C1268 1u 6.3V CAP_0201_14mil
C1269 1u 6.3V CAP_0201_14mil
C1267 1u 6.3V CAP_0201_14mil
C1271 1u 6.3V CAP_0201_14mil
C1272 10u 4V cap_0402_0p65mm
C1270 10u 4V cap_0402_0p65mm
C1277 10u 4V cap_0402_0p65mm
C1276 10u 4V cap_0402_0p65mm
C1278 10u 4V cap_0402_0p65mm
C1279 10u 4V cap_0402_0p65mm
C1280 10u 4V cap_0402_0p65mm

+VCCSA

C1281 10u 4V cap_0402_0p65mm
C1282 10u 4V cap_0402_0p65mm
C1283 10u 4V cap_0402_0p65mm
C1284 10u 4V cap_0402_0p65mm
C1286 10u 4V cap_0402_0p65mm
C1285 10u 4V cap_0402_0p65mm

EV1.9
was:X867508-004

U1001L
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
CPU POWER 1 OF 4

+VCC_CORE

A30	VCC_A30
A34	VCC_A34
A39	VCC_A39
A44	VCC_A44
AK33	VCC_AK33
AK35	VCC_AK35
AK37	VCC_AK37
AK38	VCC_AK38
AK40	VCC_AK40
AL33	VCC_AL33
AL37	VCC_AL37
AL40	VCC_AL40
AM32	VCC_AM32
AM33	VCC_AM33
AM35	VCC_AM35
AM37	VCC_AM37
AM38	VCC_AM38
G30	VCC_G30
K32	RSVD_K32
AK32	RSVD_AK32
AB62	VCCOPC_AB62
P62	VCCOPC_P62
V62	VCCOPC_V62
H63	VCC_OPC_1P8_H63
G61	VCC_OPC_1P8_G61
AC63	VCCOPC_SENSE
AE63	VSSOPC_SENSE
AE62	VCCEOPIO
AG62	VCCEOPIO
AL63	VCCEOPIO_SENSE
AJ62	VSSEOPIO_SENSE

12 OF 20

REV = JKS
BUILD-OPT = TBL1001,CPU
Source Package = SKL_ULT_1356BGA_R1

+VCC_CORE

G32	VCC_G32
G33	VCC_G33
G35	VCC_G35
G37	VCC_G37
G38	VCC_G38
G40	VCC_G40
G42	VCC_G42
J30	VCC_J30
J33	VCC_J33
J37	VCC_J37
J40	VCC_J40
K33	VCC_K33
K35	VCC_K35
K37	VCC_K37
K38	VCC_K38
K40	VCC_K40
K42	VCC_K42
K43	VCC_K43
E32	VCC_SENSE
E33	VSS_SENSE
B63	VIDALERT#
A63	VIDSCK
D64	VIDSOUT
G20	VCCSTG_G20

VCC_CORE_SENSE [66]
VSS_CORE_SENSE [66]

H_CPU_SVIDALERT# R1216 220 res_0201_12mil
H_CPU_SVIDCLK R1209 0 RES_0201_12mil
H_CPU_SVIDDAT R1207 0 RES_0201_12mil

VIDALERT# [66]
VIDSCLK [66]
VIDSOUT [66]

+VCCST_CPU

R1215 56 res_0201_12mil
R1212 100 RES_0201_12mil

+VCCSTG +VCCSTG is control by SLP_S0, but it can overwrite by XDP, that means it need power for XDP intrafece

Place on secondary side, underneath the package

+VCCEDRAM

C1228 10u 4V cap_0402_0p65mm
C1252 1u 6.3V CAP_0201_14mil
C1253 1u 6.3V CAP_0201_14mil
C1250 1u 6.3V CAP_0201_14mil
C1254 1u 6.3V CAP_0201_14mil
C1255 1u 6.3V CAP_0201_14mil
C1256 1u 6.3V CAP_0201_14mil

+1P8V

C1251 6.3V 1u CAP_0201_14mil

[58] VCCOPC_SENSE

+VCCEOPIO

C1231 10u 4V cap_0402_0p65mm
C1230 10u 4V cap_0402_0p65mm

[58] VCCOPIO_SENSE

Place on secondary side, underneath the package

Vinafix.com

Microsoft

Title: CPU(3)_SKL POWER1

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 12 of 76

U1001M
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
CPU POWER 2 OF 4

+VCCGT

VCCGT: A48, A53, A58, A62, A66, AA63, AA64, AA66, AA67, AA69, AA70, AA71, AC64, AC65, AC66, AC67, AC68, AC69, AC70, AC71, J43, J45, J46, J48, J50, J52, J53, J55, J56, J58, J60, K48, K50, K52, K53, K55, K56, K58, K60, L62, L63, L64, L65, L66, L67, L68, L69, L70, L71, M62, N63, N64, N66, N67, N69, N70, N71, R63, R64, R65, R66, R67, R68, R69, R70, R71, T62, U65, U68, U71, W63, W64, W65, W66, W67, W68, W69, W70, W71, Y62

+VCCGT

VCCGTX_AK42, VCCGTX_AK43, VCCGTX_AK45, VCCGTX_AK46, VCCGTX_AK48, VCCGTX_AK50, VCCGTX_AK52, VCCGTX_AK53, VCCGTX_AK55, VCCGTX_AK56, VCCGTX_AK58, VCCGTX_AK60, VCCGTX_AK70, VCCGTX_AL43, VCCGTX_AL46, VCCGTX_AL50, VCCGTX_AL53, VCCGTX_AL56, VCCGTX_AL60, VCCGTX_AM48, VCCGTX_AM50, VCCGTX_AM52, VCCGTX_AM53, VCCGTX_AM56, VCCGTX_AM58, VCCGTX_AU58, VCCGTX_AU63, VCCGTX_BB57, VCCGTX_BB66
AK42, AK43, AK45, AK46, AK48, AK50, AK52, AK53, AK55, AK56, AK58, AK60, AK70, AL43, AL46, AL50, AL53, AL56, AL60, AM48, AM50, AM52, AM53, AM56, AM58, AU58, AU63, BB57, BB66

[66] VCCGT_SENSE — J70 VCCGT_SENSE — AK62 VCCGTX_SENSE
[66] VSSGT_SENSE — J69 VSSGT_SENSE — AL61 VSSGTX_SENSE

13 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

THIS IS PLACE ON VCCGTX pins (they are connected to +VCCGT)
Place on secondary side, underneath the package
only for 23e
U23E,CPU C1390 10u 4V cap_0402_0p65mm
U23E,CPU C1391 10u 4V cap_0402_0p65mm
U23E,CPU C1389 10u 4V cap_0402_0p65mm
U23E,CPU C1393 10u 4V cap_0402_0p65mm
U23E,CPU C1392 10u 4V cap_0402_0p65mm
U23E,CPU C1394 10u 4V cap_0402_0p65mm
U23E,CPU C1395 10u 4V cap_0402_0p65mm
U23E,CPU C1396 10u 4V cap_0402_0p65mm
EV1.9
was:X867508-004

only for 23e
U23E,CPU C13101 22u 4V cap_0603_40mil
U23E,CPU C1376 22u 4V cap_0603_40mil
U23E,CPU C1397 22u 4V cap_0603_40mil
U23E,CPU C1398 22u 4V cap_0603_40mil
U23E,CPU C1399 22u 4V cap_0603_40mil
U23E,CPU C1308 22u 4V cap_0603_40mil
U23E,CPU C13100 22u 4V cap_0603_40mil
U23E,CPU C13102 22u 4V cap_0603_40mil

+VCCGT
Place on secondary side, underneath the package
C1355 10u 4V cap_0402_0p65mm
C1353 10u 4V cap_0402_0p65mm
C1352 10u 4V cap_0402_0p65mm
C1351 10u 4V cap_0402_0p65mm
C1350 10u 4V cap_0402_0p65mm
C1358 10u 4V cap_0402_0p65mm
C1354 10u 4V cap_0402_0p65mm
C1368 10u 4V cap_0402_0p65mm
C1369 10u 4V cap_0402_0p65mm
C1370 10u 4V cap_0402_0p65mm
C13122 10u 4V cap_0402_0p65mm
C13123 10u 4V cap_0402_0p65mm
EV1.9
was:X867508-004
C1361 1u 6.3V CAP_0201_14mil
C1360 1u 6.3V CAP_0201_14mil
C1357 1u 6.3V CAP_0201_14mil
C1359 1u 6.3V CAP_0201_14mil
C1349 1u 6.3V CAP_0201_14mil
C1356 1u 6.3V CAP_0201_14mil
C13196 1u 6.3V CAP_0201_14mil
C1366 1u 6.3V CAP_0201_14mil
C1367 1u 6.3V CAP_0201_14mil
C1364 1u 6.3V CAP_0201_14mil
C1365 1u 6.3V CAP_0201_14mil
C1363 1u 6.3V CAP_0201_14mil
C1362 1u 6.3V CAP_0201_14mil
C13197 1u 6.3V CAP_0201_14mil

DNP_CPU C13124 10u 4V cap_0402_0p65mm
DNP_CPU C13125 10u 4V cap_0402_0p65mm
DNP_CPU C13126 10u 4V cap_0402_0p65mm
DNP_CPU C13127 10u 4V cap_0402_0p65mm
DNP_CPU C13128 10u 4V cap_0402_0p65mm
DNP_CPU C13129 10u 4V cap_0402_0p65mm
DNP_CPU C13130 10u 4V cap_0402_0p65mm
DNP_CPU C13131 10u 4V cap_0402_0p65mm
DNP_CPU C13132 10u 4V cap_0402_0p65mm
DNP_CPU C13133 10u 4V cap_0402_0p65mm
DNP_CPU C13134 10u 4V cap_0402_0p65mm
DNP_CPU C13135 10u 4V cap_0402_0p65mm
DNP_CPU C13136 10u 4V cap_0402_0p65mm
DNP_CPU C13137 10u 4V cap_0402_0p65mm
DNP_CPU C13138 10u 4V cap_0402_0p65mm
DNP_CPU C13139 10u 4V cap_0402_0p65mm
DNP_CPU C13140 10u 4V cap_0402_0p65mm
DNP_CPU C13141 10u 4V cap_0402_0p65mm
DNP_CPU C13142 10u 4V cap_0402_0p65mm
DNP_CPU C13143 10u 4V cap_0402_0p65mm
EV1.9
was:X867508-003

Place on secondary side, underneath the package
DNP_CPU C13144 1u 6.3V CAP_0201_14mil
DNP_CPU C13145 1u 6.3V CAP_0201_14mil
DNP_CPU C13146 1u 6.3V CAP_0201_14mil
DNP_CPU C13147 1u 6.3V CAP_0201_14mil
DNP_CPU C13148 1u 6.3V CAP_0201_14mil
DNP_CPU C13149 1u 6.3V CAP_0201_14mil
DNP_CPU C13177 1u 6.3V CAP_0201_14mil
DNP_CPU C13151 1u 6.3V CAP_0201_14mil
DNP_CPU C13152 1u 6.3V CAP_0201_14mil
DNP_CPU C13153 1u 6.3V CAP_0201_14mil
DNP_CPU C13154 1u 6.3V CAP_0201_14mil
DNP_CPU C13155 1u 6.3V CAP_0201_14mil
DNP_CPU C13156 1u 6.3V CAP_0201_14mil
DNP_CPU C13157 1u 6.3V CAP_0201_14mil
DNP_CPU C13158 1u 6.3V CAP_0201_14mil
DNP_CPU C13159 1u 6.3V CAP_0201_14mil
DNP_CPU C13160 1u 6.3V CAP_0201_14mil
DNP_CPU C13161 1u 6.3V CAP_0201_14mil
DNP_CPU C13162 1u 6.3V CAP_0201_14mil
DNP_CPU C13163 1u 6.3V CAP_0201_14mil

C1371 47u 6.3V cap_0805_36mil
C1373 47u 6.3V cap_0805_36mil
C1372 47u 6.3V cap_0805_36mil
C1374 47u 6.3V cap_0805_36mil
C1375 47u 6.3V cap_0805_36mil
C1382 22u 6.3V cap_0603_38mil
C1381 22u 6.3V cap_0603_38mil
C1384 22u 6.3V cap_0603_38mil
C1383 22u 6.3V cap_0603_38mil
C1377 22u 6.3V cap_0603_38mil
C1378 22u 6.3V cap_0603_38mil
C1379 22u 6.3V cap_0603_38mil
EV19
WAS: 0402

C13165 47u 6.3V cap_0805_36mil
C13166 47u 6.3V cap_0805_36mil
C13164 47u 6.3V cap_0805_36mil
C1380 22u 6.3V cap_0603_38mil
C1385 22u 6.3V cap_0603_38mil
C1386 22u 6.3V cap_0603_38mil
C1387 22u 6.3V cap_0603_38mil
C1388 22u 6.3V cap_0603_38mil
EV19
WAS: 0402

DNP_CPU C13167 10u 4V cap_0402_0p65mm
DNP_CPU C13168 10u 4V cap_0402_0p65mm
DNP_CPU C13169 10u 4V cap_0402_0p65mm
DNP_CPU C13170 10u 4V cap_0402_0p65mm
DNP_CPU C13171 10u 4V cap_0402_0p65mm
DNP_CPU C13172 10u 4V cap_0402_0p65mm
DNP_CPU C13173 10u 4V cap_0402_0p65mm
DNP_CPU C13174 10u 4V cap_0402_0p65mm
DNP_CPU C13175 10u 4V cap_0402_0p65mm
DNP_CPU C13176 10u 4V cap_0402_0p65mm
EV1.9
was:X867508-002

+VCC_CORE
C1338 10u 4V cap_0402_0p65mm
C1337 10u 4V cap_0402_0p65mm
C1336 10u 4V cap_0402_0p65mm
C1320 10u 4V cap_0402_0p65mm
C1321 10u 4V cap_0402_0p65mm
C1319 10u 4V cap_0402_0p65mm
C1339 10u 4V cap_0402_0p65mm
C1340 10u 4V cap_0402_0p65mm
EV1.9
was:X867508-001

C1341 47u 6.3V cap_0603_40mil
C1342 47u 6.3V cap_0603_40mil
C1343 47u 6.3V cap_0603_40mil
C1344 47u 6.3V cap_0603_40mil
C1345 47u 6.3V cap_0603_40mil
C1346 47u 6.3V cap_0603_40mil
C1347 47u 6.3V cap_0603_40mil
C1348 47u 6.3V cap_0603_40mil
EV1.9 was:0805

+VCC_CORE
Place on secondary side, underneath the package
C1315 10u 4V cap_0402_0p65mm
C1314 10u 4V cap_0402_0p65mm
C1317 10u 4V cap_0402_0p65mm
C1316 10u 4V cap_0402_0p65mm
C1310 10u 4V cap_0402_0p65mm
C1311 10u 4V cap_0402_0p65mm
C1312 10u 4V cap_0402_0p65mm
C1313 10u 4V cap_0402_0p65mm
C1318 10u 4V cap_0402_0p65mm
C13179 10u 4V cap_0402_0p65mm
C13182 10u 4V cap_0402_0p65mm
C13180 10u 4V cap_0402_0p65mm
C13184 10u 4V cap_0402_0p65mm
C13178 10u 4V cap_0402_0p65mm
C13183 10u 4V cap_0402_0p65mm
C13181 10u 4V cap_0402_0p65mm
C13185 10u 4V cap_0402_0p65mm
C13186 10u 4V cap_0402_0p65mm
C13188 10u 4V cap_0402_0p65mm
C13191 10u 4V cap_0402_0p65mm
C13189 10u 4V cap_0402_0p65mm
C13193 10u 4V cap_0402_0p65mm
C13187 10u 4V cap_0402_0p65mm
C13192 10u 4V cap_0402_0p65mm
C13190 10u 4V cap_0402_0p65mm
C13194 10u 4V cap_0402_0p65mm
C13195 10u 4V cap_0402_0p65mm
C1328 10u 4V cap_0402_0p65mm
C1327 10u 4V cap_0402_0p65mm
C1326 10u 4V cap_0402_0p65mm
C1325 10u 4V cap_0402_0p65mm
C1324 10u 4V cap_0402_0p65mm
C1331 10u 4V cap_0402_0p65mm
C1329 10u 4V cap_0402_0p65mm
EV1.9
was:X867508-004
C1334 1u 6.3V CAP_0201_14mil
C1335 1u 6.3V CAP_0201_14mil
C1332 1u 6.3V CAP_0201_14mil
C1333 1u6.3V CAP_0201_14mil
C1323 1u6.3V CAP_0201_14mil
C1330 1u 6.3V CAP_0201_14mil
C1301 1u 6.3V CAP_0201_14mil
C1300 1u 6.3V CAP_0201_14mil
C1306 1u 6.3V CAP_0201_14mil
C1307 1u 6.3V CAP_0201_14mil
C1304 1u 6.3V CAP_0201_14mil
C1305 1u 6.3V CAP_0201_14mil
C1302 1u 6.3V CAP_0201_14mil
C1303 1u 6.3V CAP_0201_14mil
C1309 1u 6.3V CAP_0201_14mil
C13108 1u 6.3V CAP_0201_14mil
C1322 1u 6.3V CAP_0201_14mil
C13104 1u 6.3V CAP_0201_14mil
C13103 1u 6.3V CAP_0201_14mil
C13106 1u 6.3V CAP_0201_14mil
C13105 1u 6.3V CAP_0201_14mil
C13107 1u 6.3V CAP_0201_14mil
C13115 1u 6.3V CAP_0201_14mil
C13109 1u 6.3V CAP_0201_14mil
C13111 1u 6.3V CAP_0201_14mil
C13110 1u 6.3V CAP_0201_14mil
C13113 1u 6.3V CAP_0201_14mil
C13112 1u 6.3V CAP_0201_14mil
C13114 1u 6.3V CAP_0201_14mil
C13121 1u 6.3V CAP_0201_14mil
C13116 1u 6.3V CAP_0201_14mil
C13119 1u 6.3V CAP_0201_14mil
C13117 1u 6.3V CAP_0201_14mil
C13120 1u 6.3V CAP_0201_14mil
C13118 1u 6.3V CAP_0201_14mil

Microsoft
Title: CPU(4)_SKL_POWER2
Engineer: Surface
Size C | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 | Sheet 13 of 76

U1001P
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
GND 1 OF 3

A5	VSS	VSS	AL65
A67	VSS	VSS	AL66
A70	VSS	VSS	AM13
AA2	VSS	VSS	AM21
AA4	VSS	VSS	AM25
AA65	VSS	VSS	AM27
AA68	VSS	VSS	AM43
AB15	VSS	VSS	AM45
AB16	VSS	VSS	AM46
AB18	VSS	VSS	AM55
AB21	VSS	VSS	AM60
AB8	VSS	VSS	AM61
AD13	VSS	VSS	AM68
AD16	VSS	VSS	AM71
AD19	VSS	VSS	AM8
AD20	VSS	VSS	AN20
AD21	VSS	VSS	AN23
AD62	VSS	VSS	AN28
AD8	VSS	VSS	AN30
AE64	VSS	VSS	AN32
AE65	VSS	VSS	AN33
AE66	VSS	VSS	AN35
AE67	VSS	VSS	AN37
AE68	VSS	VSS	AN38
AE69	VSS	VSS	AN40
AF1	VSS	VSS	AN42
AF10	VSS	VSS	AN58
AF15	VSS	VSS	AN63
AF17	VSS	VSS	AP10
AF2	VSS	VSS	AP18
AF4	VSS	VSS	AP20
AF63	VSS	VSS	AP23
AG16	VSS	VSS	AP28
AG17	VSS	VSS	AP32
AG18	VSS	VSS	AP35
AG19	VSS	VSS	AP38
AG20	VSS	VSS	AP42
AG21	VSS	VSS	AP58
AG71	VSS	VSS	AP63
AH13	VSS	VSS	AP68
AH6	VSS	VSS	AP70
AH63	VSS	VSS	AR11
AH64	VSS	VSS	AR15
AH67	VSS	VSS	AR16
AJ15	VSS	VSS	AR20
AJ18	VSS	VSS	AR23
AJ20	VSS	VSS	AR28
AJ4	VSS	VSS	AR35
AK11	VSS	VSS	AR42
AK16	VSS	VSS	AR43
AK18	VSS	VSS	AR45
AK21	VSS	VSS	AR46
AK22	VSS	VSS	AR48
AK27	VSS	VSS	AR5
AK63	VSS	VSS	AR50
AK68	VSS	VSS	AR52
AK69	VSS	VSS	AR53
AK8	VSS	VSS	AR55
AL2	VSS	VSS	AR58
AL28	VSS	VSS	AR63
AL32	VSS	VSS	AR8
AL35	VSS	VSS	AT2
AL38	VSS	VSS	AT20
AL4	VSS	VSS	AT23
AL45	VSS	VSS	AT28
AL48	VSS	VSS	AT35
AL52	VSS	VSS	AT4
AL55	VSS	VSS	AT42
AL58	VSS	VSS	AT56
AL64	VSS	VSS	AT58

16 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

U1001Q
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
GND 2 OF 3

AT63	VSS	VSS	BA49
AT68	VSS	VSS	BA53
AT71	VSS	VSS	BA57
AU10	VSS	VSS	BA6
AU15	VSS	VSS	BA62
AU20	VSS	VSS	BA66
AU32	VSS	VSS	BA71
AU38	VSS	VSS	BB18
AV1	VSS	VSS	BB26
AV68	VSS	VSS	BB30
AV69	VSS	VSS	BB34
AV70	VSS	VSS	BB38
AV71	VSS	VSS	BB43
AW10	VSS	VSS	BB55
AW12	VSS	VSS	BB6
AW14	VSS	VSS	BB60
AW16	VSS	VSS	BB64
AW18	VSS	VSS	BB67
AW21	VSS	VSS	BB70
AW23	VSS	VSS	C1
AW26	VSS	VSS	C25
AW28	VSS	VSS	C5
AW30	VSS	VSS	D10
AW32	VSS	VSS	D11
AW34	VSS	VSS	D14
AW36	VSS	VSS	D18
AW38	VSS	VSS	D22
AW41	VSS	VSS	D25
AW43	VSS	VSS	D26
AW45	VSS	VSS	D30
AW47	VSS	VSS	D34
AW49	VSS	VSS	D39
AW51	VSS	VSS	D44
AW53	VSS	VSS	D45
AW55	VSS	VSS	D47
AW57	VSS	VSS	D48
AW6	VSS	VSS	D53
AW60	VSS	VSS	D58
AW62	VSS	VSS	D6
AW64	VSS	VSS	D62
AW66	VSS	VSS	D66
AW8	VSS	VSS	D69
AY66	VSS	VSS	E11
B10	VSS	VSS	E15
B14	VSS	VSS	E18
B18	VSS	VSS	E21
B22	VSS	VSS	E46
B30	VSS	VSS	E50
B34	VSS	VSS	E53
B39	VSS	VSS	E56
B44	VSS	VSS	E6
B48	VSS	VSS	E65
B53	VSS	VSS	E71
B58	VSS	VSS	F1
B62	VSS	VSS	F13
B66	VSS	VSS	F2
B71	VSS	VSS	F22
BA1	VSS	VSS	F23
BA10	VSS	VSS	F27
BA14	VSS	VSS	F28
BA18	VSS	VSS	F32
BA2	VSS	VSS	F33
BA23	VSS	VSS	F35
BA28	VSS	VSS	F37
BA32	VSS	VSS	F38
BA36	VSS	VSS	F4
F68	VSS	VSS	F40
BA45	VSS	VSS	F42
	VSS	VSS	BA41

17 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

U1001R
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
GND 3 OF 3

F8	VSS	VSS	L18
G10	VSS	VSS	L2
G22	VSS	VSS	L20
G43	VSS	VSS	L4
G45	VSS	VSS	L8
G48	VSS	VSS	N10
G5	VSS	VSS	N13
G52	VSS	VSS	N19
G55	VSS	VSS	N21
G58	VSS	VSS	N6
G6	VSS	VSS	N65
G60	VSS	VSS	N68
G63	VSS	VSS	P17
G66	VSS	VSS	P19
H15	VSS	VSS	P20
H18	VSS	VSS	P21
H71	VSS	VSS	R13
J11	VSS	VSS	R6
J13	VSS	VSS	T15
J25	VSS	VSS	T17
J28	VSS	VSS	T18
J32	VSS	VSS	T2
J35	VSS	VSS	T21
J38	VSS	VSS	T4
J42	VSS	VSS	U10
J8	VSS	VSS	U63
K16	VSS	VSS	U64
K18	VSS	VSS	U66
K22	VSS	VSS	U67
K61	VSS	VSS	U69
K63	VSS	VSS	U70
K64	VSS	VSS	V16
K65	VSS	VSS	V17
K66	VSS	VSS	V18
K67	VSS	VSS	W13
K68	VSS	VSS	W6
K70	VSS	VSS	W9
K71	VSS	VSS	Y17
L11	VSS	VSS	Y19
L16	VSS	VSS	Y20
L17	VSS	VSS	Y21
	VSS	VSS	

18 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

Microsoft

Title: CPU(5)_GND

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 14 of 76

CFG4	
0 **Default**	enable eDP
1	Disable eDP

TP1516

[18] CFG0
[18] CFG1
[18] CFG2
[18] CFG3
[18] CFG4
[18] CFG5
[18] CFG6
[18] CFG7
[18] CFG8
[18] CFG9
[18] CFG10
[18] CFG11
[18] CFG12
[18] CFG13
[18] CFG14
[18] CFG15

[18] CFG16
[18] CFG17

[18] CFG18
[18] CFG19

R1507 49.9 RES_0201_12mil — CFG_RCOMP

[18] ITP_PMODE

R1501 1K RES_0201_12mil

U1001S
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
RESERVED SIGNALS-1

E68	CFG[0]	RSVD_TP_BB68	BB68
B67	CFG[1]	RSVD_TP_BB69	BB69
D65	CFG[2]		
D67	CFG[3]	RSVD_TP_AK13	AK13 — RSVD_TP_AK13 — TP1503 SP_TP_SMDp58mm
E70	CFG[4]	RSVD_TP_AK12	AK12 — RSVD_TP_AK12 — TP1502 SP_TP_SMDp58mm
C68	CFG[5]		
D68	CFG[6]	RSVD_BB2	BB2
C67	CFG[7]	RSVD_BA3	BA3
F71	CFG[8]		
G69	CFG[9]	TP5	AU5
F70	CFG[10]	TP6	AT5
G68	CFG[11]		
H70	CFG[12]		
G71	CFG[13]	RSVD_D5	D5
H69	CFG[14]	RSVD_D4	D4
G70	CFG[15]	RSVD_B2	B2
		RSVD_C2	C2
E63	CFG[16]	RSVD_B3	B3
F63	CFG[17]	RSVD_A3	A3
		RSVD_AW1	AW1
E66	CFG[18]	RSVD_E1	E1
F66	CFG[19]	RSVD_E2	E2
E60	CFG_RCOMP	RSVD_BA4	BA4
E8	ITP_PMODE	RSVD_BB4	BB4
AY2	RSVD_AY2	RSVD_A4	A4
AY1	RSVD_AY1	RSVD_C4	C4
D1	RSVD_D1	TP4	BB5
D3	RSVD_D3	RSVD_A69	A69
K46	RSVD_K46	RSVD_B69	B69
K45	RSVD_K45	RSVD_AY3	AY3 — RSVD_AY3 — R1502 0 RES_0201_12mil DNP,CPU
AL25	RSVD_AL25	RSVD_D71	D71
AL27	RSVD_AL27	RSVD_C70	C70
C71	RSVD_C71	RSVD_C54	C54
B70	RSVD_B70	RSVD_D54	D54
F60	RSVD_F60	TP1	AY4
A52	RSVD_A52	TP2	BB3
BA70	RSVD_TP_BA70	VSS_AY71	AY71
BA68	RSVD_TP_BA68	ZVM#	AR56 — ZVM# [58]
J71	RSVD_J71	RSVD_TP_AW71	AW71
J68	RSVD_J68	RSVD_TP_AW70	AW70
F65	VSS_F65	MSM#	AP56 — MSM# [58]
G65	VSS_G65	PROC_SELECT#	C64 — PROC_SELECT#
F61	RSVD_F61		
E61	RSVD_E61		

19 OF 20

REV = JKS
TBL1001,CPU
Source Package = SKL_ULT_1356BGA_R1

MFang 8Jan15: [Intel] used in the HVM testing should be left not connected.

ZVM# and MSM# may need to control the VCCOPC and VCCEOPIO

+VCCST_CPU
R1540 100K RES_0201_12mil DNP,CPU

100k ohm resistor only needed for Cannonlake

U1001T
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
SPARE

AW69	RSVD_AW69	RSVD_F6	F6
AW68	RSVD_AW68	RSVD_E3	E3
AU56	RSVD_AU56	RSVD_C11	C11
AW48	RSVD_AW48	RSVD_B11	B11
C7	RSVD_C7	RSVD_A11	A11
U12	RSVD_U12	RSVD_D12	D12
U11	RSVD_U11	RSVD_C12	C12
H11	RSVD_H11	RSVD_F52	F52

20 OF 20

REV = JKS
TBL1001,CPU
Source Package = SKL_ULT_1356BGA_R1

+1P8VSUS_ORG
DNP,CPU
C1501 1u CAP_0402_22mil 6.3V

Microsoft	Title: CPU(6)_CFG_RESERVED		
	Engineer: Surface		
Size B	Project Name U -- EV 1.90		Rev 1.90.2
Date: Monday, May 11, 2015		Sheet 15 of 76	

U1601
H9CCNNN8JTALAR-NTD
bga178_13x17_11x11p5x1_p8xp65mm

U1602
H9CCNNN8JTALAR-NTD
bga178_13x17_11x11p5x1_p8xp65mm

TBL1601,DDR

TBL1601,DDR

TBL2301,DDR

TBL2301,DDR

Title: LPDDR3(1)_MEMORY DOWN

Microsoft Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 16 of 76

U1701
H9CCNNN8JTALAR-NTD
bga178_13x17_11x11p5x1_p8xp65mm

U1702
H9CCNNN8JTALAR-NTD
bga178_13x17_11x11p5x1_p8xp65mm

TBL1601,DDR

TBL2301,DDR

EV1.9

Title: LPDDR3(2)_MEMORY DOWN

Microsoft Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 17 of 76

PRIMARY XDP connector

[15,18] CFG3
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<3>
DB,XDP R1841 1K RES_0201_12mil
DB,XDP RES_0201_12mil R1840 0
+1VSB_XDP
DNP,XDP R1803 49.9 RES_0201_12mil
XDP_PIN1
+1VSB
DB,XDP R1838 0 RES_0201_12mil
+1VSB_XDP
DB,XDP J1801 X869110-001
B2B 60P
conn_b2b-r_60_4mtg_14p2x2p54xp88_p4mm
RECEPTACLE

[24] XDP_PREQ#
[24] XDP_PRDY#
[15,18] CFG0
[15] CFG1
[15] CFG2
[15,18] CFG3
[10] XDP_BPM0
[10] XDP_BPM1
[15] CFG4
[15] CFG5
[15] CFG6
[15] CFG7
CFG17 [15]
CFG16 [15]
CFG8 [15]
CFG9 [15]
CFG10 [15]
CFG11 [15]
CFG19 [15]
CFG18 [15]
CFG12 [15]
CFG13 [15]
CFG14 [15]
CFG15 [15]

+1VSB_XDP
DNP,XDP C1803 1u 6.3V CAP_0201_14mil
GND
+3P3VSB
DB,XDP R1826 1.5K RES_0201_12mil

+1VSB_XDP
DB,XDP R1844 1K RES_0201_12mil
+1VSB_XDP
DB,XDP R1823 1K RES_0201_12mil
+3P3V

+VCCSTG
DNP,XDP R1825 49.9 RES_0201_12mil
Place R1825 within 1100mil from CPU

[22,36] RSMRST#
[22] PCH_PWRBTN#
[30,32,33] PWR_SW_N
R1842 DB,XDP 1K RES_0201_12mil
R1807 DB,XDP 0 RES_0201_12mil
R1804 DNP,XDP 0 RES_0201_12mil
PM_RSMRST_PWRGD_XDP
PM_PWRBTN#_XDP

[21] SPI0_MOSI_XDP
R1846 DB,XDP 0 RES_0201_12mil
[15,18] CFG0
R1843 DNP,XDP 0 XDP_CFG0
XDP_MOSI_R
RES_0201_12mil

CLK_XDP_R_DP
CLK_XDP_R_DN
XDP_RST#_R
XDP_DBRESET#_R
XDP_TDO_BUF
XDP_TDI_R
XDP_PIN60

R1805 DB,XDP 0 RES_0201_12mil
R1806 DB,XDP 0 RES_0201_12mil
R1837 DB,XDP 0 RES_0201_12mil
R1808 DNP,XDP 1K RES_0201_12mil
R1810 DB,XDP 0 RES_0201_12mil
R1809 DB,XDP 0 RES_0201_12mil
R1849 DB,XDP 0 RES_0201_12mil
R1851 DB,XDP 0 RES_0201_12mil

CLK_XDP_DP [20]
CLK_XDP_DN [20]
ITP_PMODE [15]
PLT_RST#_BUF [22,36,38,43,75]
PCH_SYS_RST# [22]
XDP_TRST#_BUF [10]
XDP_TDO [10]
XDP_TRST# [10]
XDP_TDI [10]
XDP_TMS [10]

DB,XDP PC1804 0.1u 6.3V cap_0201_14mil
GND
DB,XDP PC1805 0.1u 6.3V cap_0201_14mil
GND

[21] SMBDATA
[21] SMBCLK
XDP_TCK1
[10] PCH_JTAG_TCK
[10] XDP_TCK
R1821 DB,XDP 0 RES_0201_12mil
R1853 DNP,XDP 0 RES_0201_12mil
R1811 DB,XDP 0 RES_0201_12mil
[10] PCH_JTAGX

DB,XDP C1801 0.01u 10V CAP_0201_14mil
GND
DNP,XDP R1852 0 RES_0201_12mil

R1822 DB,XDP 0 RES_0201_12mil
PCH_JTAG_TDI [10]
R1848 DB,XDP 0 RES_0201_12mil
PCH_JTAG_TMS [10]
R1847 DB,XDP 0 RES_0201_12mil
PCH_JTAG_TDO [10]

GND
MTG1 MTG2
MTG3 MTG4
GND
GND

[21] XDP_SPI0_IO2
R1845 DB,XDP 0 RES_0201_12mil

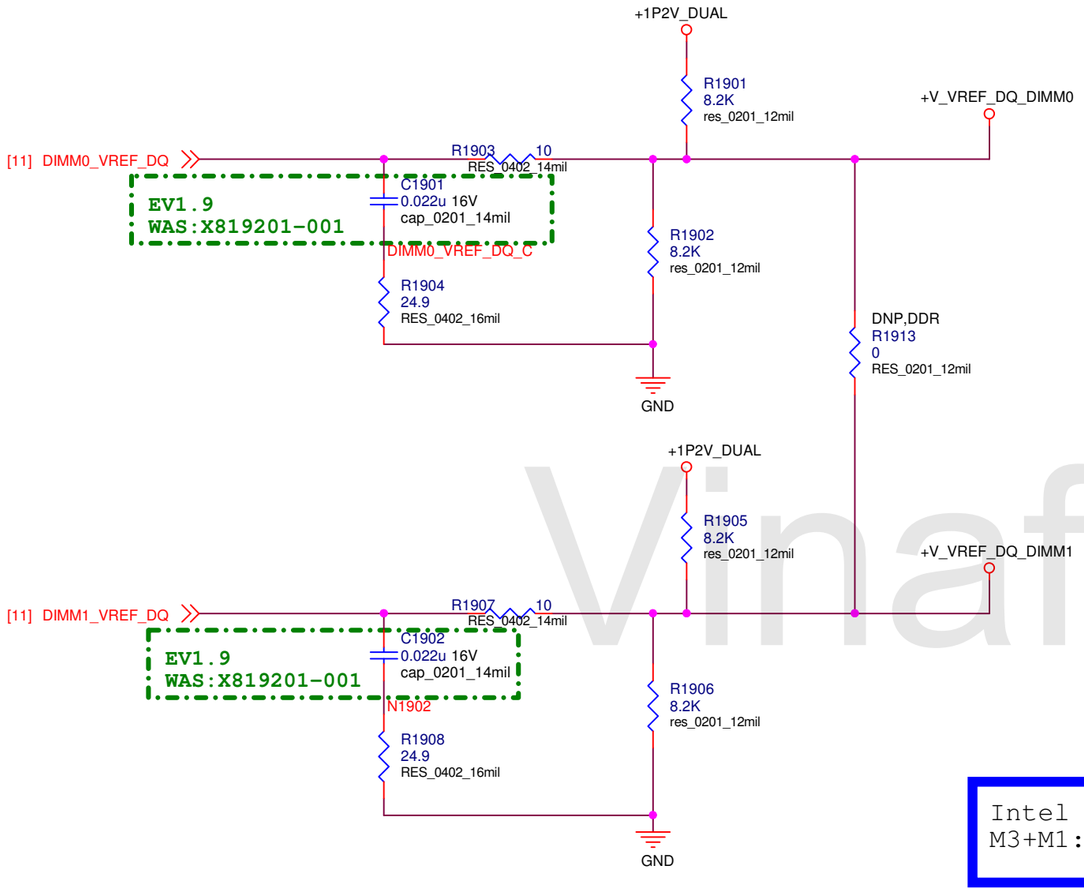
R1854 DNP,XDP 0 RES_0201_12mil

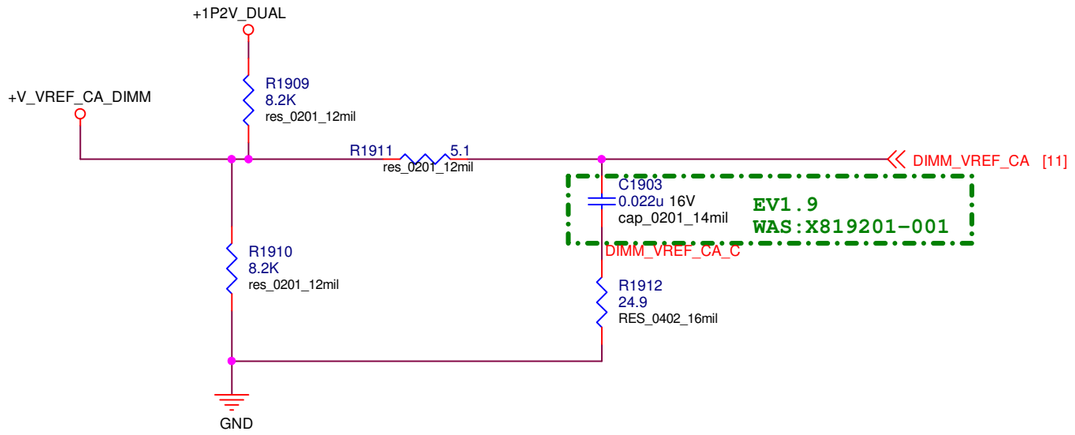
For the signals only go to XDP, the 0R should be close to XDP connector.
For the signals to both XDP and target circuit, the option resistor locaction should follow the target signal routing.

Title: XDP		
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 18 of 76	

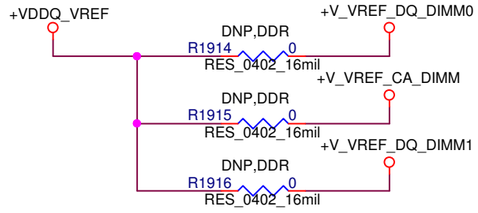
LPDDR3 Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off





Intel 0203
M3+M1: Default Recommendation



Title:	LPDDR3(3)_CA/DQ Voltage		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 19 of 76		

+3P3V

R2052 10K RES_0201_12mil

R2048 10K RES_0201_12mil

[43] SSD_PCIECLK_REQ_N

[50] PCIE_WIFI_CLKREQ_N

U1001J
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
CLOCK SIGNALS

D42	CLKOUT_PCIE_N0	
C42	CLKOUT_PCIE_P0	
AR10	GPP_B5/SRCCLKREQ0#	
B42	CLKOUT_PCIE_N1	[43] PCIECLK_SSD_DN
A42	CLKOUT_PCIE_P1	[43] PCIECLK_SSD_DP
AT7	GPP_B6/SRCCLKREQ1#	
D41	CLKOUT_PCIE_N2	
C41	CLKOUT_PCIE_P2	
AT8	GPP_B7/SRCCLKREQ2#	
D40	CLKOUT_PCIE_N3	
C40	CLKOUT_PCIE_P3	
AT10	GPP_B8/SRCCLKREQ3#	
B40	CLKOUT_PCIE_N4	
A40	CLKOUT_PCIE_P4	
AU8	GPP_B9/SRCCLKREQ4#	
E40	CLKOUT_PCIE_N5	[50] PCIE_WIFI_RCLK_DN
E38	CLKOUT_PCIE_P5	[50] PCIE_WIFI_RCLK_DP
AU7	GPP_B10/SRCCLKREQ5#	

10 OF 20

CLKOUT_ITPXDP_N	F43	CLK_XDP_DN [18]
CLKOUT_ITPXDP_P	E43	CLK_XDP_DP [18]
GPD8/SUSCLK	BA17	WIFI_32K_CLK_R
XTAL24_IN	E37	XTAL_24M_IN
XTAL24_OUT	E35	XTAL_24M_OUT
XCLK_BIASREF	E42	XCLK_BIASREF
RTCX1	AM18	RTC_X1
RTCX2	AM20	RTC_X2
SRTCRST#	AN18	SRTC_RST# [20]
RTCRST#	AM16	RTC_RST# [20,36]

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

EV1.9 WAS INSTALL

R2010 DNP,CPU 33 RES_0201_12mil

WIFI_32K_CLK [50]

XTAL_24M_IN

XTAL_24M_OUT R2035 1M RES_0201_12mil

xtal_4_3p2x2p5xp8_2p2x1p7mm
24MHZ X2002
EV1.9
WAS:X879083-001

C2007 50V 10p CAP_0201_14mil

C2006 10p 50V CAP_0201_14mil

this need 2.71K 0.5% resistor.
the power rail connector
to the rail of VCCCLK5

+VCCCLK5_R

R2036 1% 2.7K RES_0402_16MIL

EV1.9 CHG MSPN

R2001 10M RES_0201_12mil

R2005 0 CTAL_1 RES_0201_12mil

X2001 32.7 KHz xtal_3p2x1p5xp9_2p5mm

C2001 15p 25V CAP_0201_14mil 2%

C2002 15p 25V CAP_0201_14mil 2%

DNP,CPU R2022 60.4 res_0201_12mil

EV1.9 CHG MSPN

EV1.9 CHG MSPN

HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

2.HDA_SDOwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

DNP,CPU R2009 1K RES_0201_12mil

+3P3VSB

U1001G
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

AUDIO

SKL_ULT

[40] AZ_SYNC_1	RES_0201_12mil R2020 33	HDA_SYNC_R BA22
[40] AZ_BITCLK_1	RES_0201_12mil R2053 33	HDA_BCLK_R AY22
[40] AZ_SDATA_OUT_1	RES_0201_12mil R2054 33	INT. PD HDA_SDO_R BB22
[40] AZ_SDATA_IN0		was HDA_SDI0_R BA21
		AY21
[40] AZ_RST#_1	R2056 33 RES_0201_12mil	HDA_RST#_R AW22
		J5
		AY20
		AW20
		AK7
		AK6
		AK9
		AK10
		H5
		D7
		D8
		C8
		AW5

HDA_SYNC/I2S0_SFRM	
HDA_BLK/I2S0_SCLK	
HDA_SDO/I2S0_TXD	
HDA_SDI0/I2S0_RXD	
HDA_SDI1/I2S1_RXD	
HDA_RST#/I2S1_SCLK	
GPP_D23/I2S_MCLK	
I2S1_SFRM	
I2S1_TXD	
GPP_F1/I2S2_SFRM	
GPP_F0/I2S2_SCLK	
GPP_F2/I2S2_TXD	
GPP_F3/I2S2_RXD	
GPP_D19/DMIC_CLK0	[20,32,40,42] DMIC1_CLK
GPP_D20/DMIC_DATA0	[20,32,40,42] DMIC1_DATA
GPP_D17/DMIC_CLK1	[20] DMIC2_CLK_XDP
GPP_D18/DMIC_DATA1	[20] DMIC2_DATA_XDP
GPP_B14/SPKR	

SDIO/SDXC

GPP_G0/SD_CMD	AB11
GPP_G1/SD_DATA0	AB13
GPP_G2/SD_DATA1	AB12
GPP_G3/SD_DATA2	W12
GPP_G4/SD_DATA3	W11
GPP_G5/SD_CD#	W10
GPP_G6/SD_CLK	W8
GPP_G7/SD_WP	W7
GPP_A17/SD_PWR_EN#/ISH_GP7	BA9
GPP_A16/SD_1P8_SEL	BB9
SD_RCOMP	AB7
GPP_F23	AF13

No SD support

7 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

SD_RCOMP

R2080 200 RES_0201_12mil

+VCC_RTC

R2021 20K RES_0201_12mil

SRTC_RST# [20]

C2003 1u 6.3V CAP_0402_22mil

R2002 20K RES_0201_12mil

RTC_RST# [20,36]

C2004 1u 6.3V CAP_0402_22mil

+3P3V

+3V_EC

R2006 1K RES_0201_12mil

TOP_SWAP_1A

DNP,CPU R2003 100K RES_0201_12mil

U2001A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm

A1 1A
B2 EN
VCC A2
1B B1
GND D1

+3V_EC

C2005 0.1u 25V CAP_0402_22mil

TOP_SWAP

INT. PD

U2001B
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm

TOP_SWAP_2A D2
TOP_SWAP_EN# C1
2A
2EN
2B C2

R2007 49.9K RES_0201_12mil

[20,32,40,42] DMIC1_CLK
[20,32,40,42] DMIC1_DATA

TPS0P35 XDP_TP2001
TPS0P35 XDP_TP2002
TPS0P35 XDP_TP2003
TPS0P35 XDP_TP2004

DMIC2_CLK_XDP [20]
DMIC2_DATA_XDP [20]

to EC PIN D9

[36] EC_UEFI_TOP_SWAP

DNP,CPU Q2001 RUM002N02GT2L SOT-VMT3_1p2xp8xp5_p4mm

R2004 100K RES_0201_12mil

DNP,CPU R2008 100K RES_0201_12mil

STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper

High=Enabled A16 swap override/ Top-Block swap override
Low=Default

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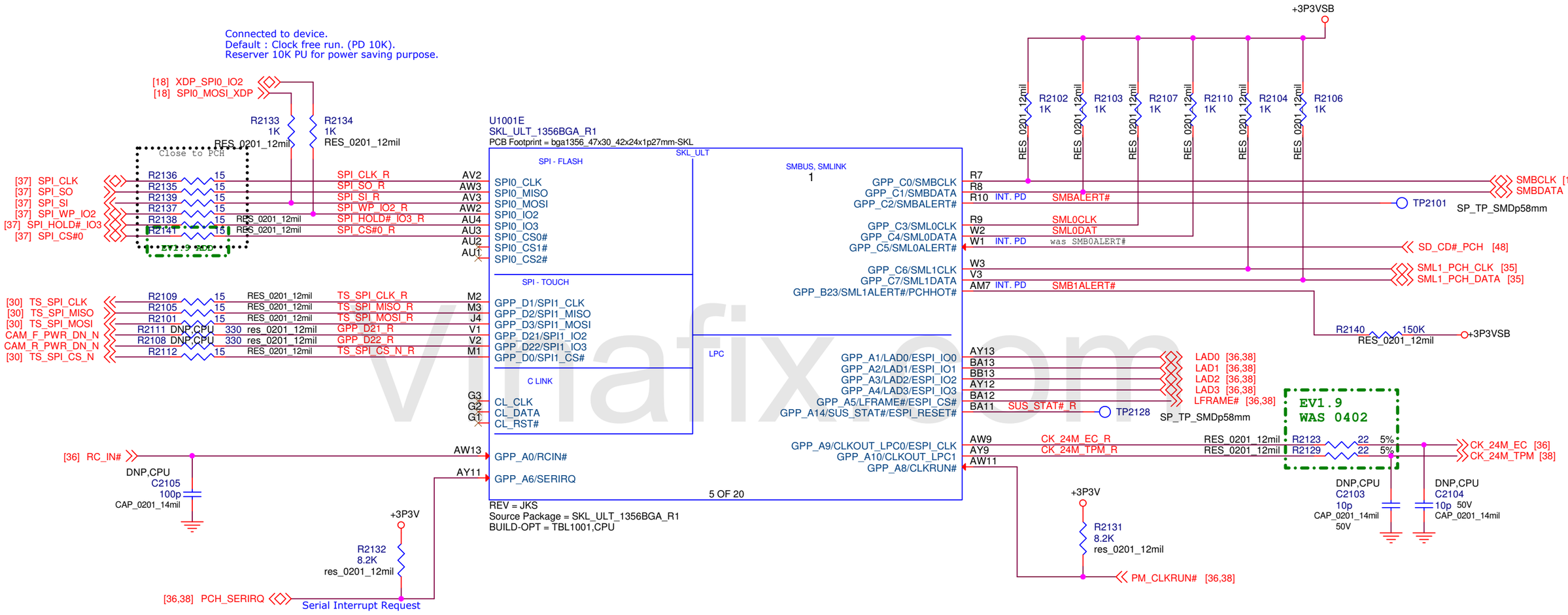
Title:	PCH(1)_SD,HDA,RTC,CLK		
Engineer:	*Surface*		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 20 of 76	



GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

Vinafix.com

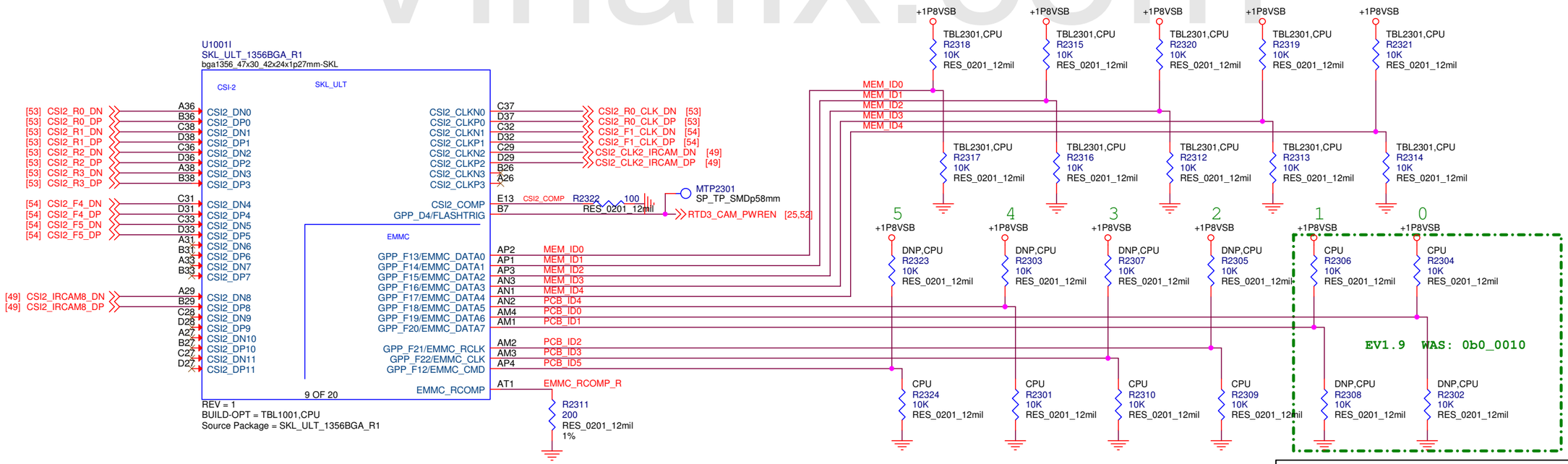
Title:	PCH(2)_CLK,SMB,LPC,SPI	
Engineer:	*Surface*	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 21 of 76	

Vinafix.com

Title: PCH(3)_SYS PWR CONTR		
Engineer: Surface		
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 22 of 76	

Rev 4	EC Processor ID		PCH Processor ID	TPM			EC Board Rev	PCH Board ID[3:0]				DRAM Manufacturer		RAM Speed	RAM Size & Calibration		
Signal	EC_ID1	ED_ID0	PCB_ID5	PCB_ID4			R3619	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0	MEM_ID1	MEM_ID0	MEM_ID4	MEM_ID3	MEM_ID2	ZQ1
	1 = R3642 0 = R3643	1 = R3640 0 = R3641	1 = R2323 0 = R2324	1 = R2303 0 = R2301	R3813 R3815 R3816	R3814		1 = R2307 0 = R2310	1 = R2305 0 = R2309	1 = R2306 0 = R2308	1 = R2304 0 = R2302	1 = R2315 0 = R2316	1 = R2318 0 = R2317	1 = R2321 0 = R2314	1 = R2319 0 = R2313	1 = R2320 0 = R2312	R1602 R1604 R1702 R1704
	U22 = 0 U23E = 1 Y = 0 S = 1	**U22 = 0 U23E=0 Y = 1 S = 1**	U = 0 Y = 1	Infineon = 0 Nation Z = 1	Infineon = DNP NationZ = POP	Infineon = POP NationZ =DNP						**Hynix = 0 Samsung = 0**	**Hynix = 0 Samsung = 1**	1600 LPDDR3 = 0 1866 LPDDR3 = 1	4GB = 0 8GB = 0 16GB = 1	4 GB = 0 8 GB = 1 16 GB = 0	4GB = DNP 8GB = POP 16GB = POP
EV 0.9							80.6 Ω	0	0	0	0						
EV 1.0							169 Ω	0	0	0	1						
EV 1.5							698 Ω	0	0	1	0						
EV 1.9							909 Ω	0	0	1	1						

TBL2301



Vinafix.com

Title:	PCH(4)_CCI, HWID	
Engineer:	Surface	
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 23 of 76	

U1001H
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT

PCIE/USB3/SATA

H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP

G11 PCIE2_RXN/USB3_6_RXN
F11 PCIE2_RXP/USB3_6_RXP
D16 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

H16 PCIE3_RXN
G16 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP

G15 PCIE4_RXN
F15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP

G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

[43] PCIE_SSD_RX7_DN
[43] PCIE_SSD_RX7_DP
[43] PCIE_SSD_TX7_DN
[43] PCIE_SSD_TX7_DP
F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

[43] PCIE_SSD_RX8_DN
[43] PCIE_SSD_RX8_DP
[43] PCIE_SSD_TX8_DN
[43] PCIE_SSD_TX8_DP
G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

PCIE WIFI
[50] PCIE_WIFI_RX9_DN
[50] PCIE_WIFI_RX9_DP
[50] PCIE_WIFI_TX9_DN
[50] PCIE_WIFI_TX9_DP
E22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP

F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

SP_TP_SMDp58mm TP2417
SP_TP_SMDp58mm TP2418

PCIE_RCOMPN F5
R2401 100 PCIE_RCOMPP E5
RES_0201_12mil
PCIE_RCOMPN
PCIE_RCOMPP

[18] XDP_PRDY# D56 PROC_PRDY#
[18] XDP_PREQ# D61 PROC_PREQ#
TP2419 PIRQA# BB11 GPP_A7/PIRQA#
SP_TP_SMDp58mm

E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP
E30 PCIE12_RXN/SATA2_RXN
F30 PCIE12_RXP/SATA2_RXP
A25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP

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SSIC / USB3

USB3_1_RXN H8
USB3_1_RXP G8
USB3_1_TXN C13
USB3_1_TXP D13
USB3_CONN_RX_DN [45]
USB3_CONN_RX_DP [45]
USB3_CONN_TX_DN [45]
USB3_CONN_TX_DP [45]
USB Type A

USB3_2_RXN/SSIC_1_RXN J6
USB3_2_RXP/SSIC_1_RXP H6
USB3_2_TXN/SSIC_1_TXN B13
USB3_2_TXP/SSIC_1_TXP A13
USB3_SL1_RX_DN [71]
USB3_SL1_RX_DP [71]
USB3_SL1_TX_DN [71]
USB3_SL1_TX_DP [71]
USB SL1

USB3_3_RXN/SSIC_2_RXN J10
USB3_3_RXP/SSIC_2_RXP H10
USB3_3_TXN/SSIC_2_TXN B15
USB3_3_TXP/SSIC_2_TXP A15

USB3_4_RXN E10
USB3_4_RXP F10
USB3_4_TXN C15
USB3_4_TXP D15
USB3_SDXC_RX_DN [48]
USB3_SDXC_RX_DP [48]
USB3_SDXC_TX_DN [48]
USB3_SDXC_TX_DP [48]
USB3.0 SDXC

USB2

USB2N_1 AB9
USB2P_1 AB10
USB2_CONN_DN [45]
USB2_CONN_DP [45]
USB Type A

USB2N_2 AD6
USB2P_2 AD7
USB2_SL1_DN [71]
USB2_SL1_DP [71]
USB SL2

USB2N_3 AH3
USB2P_3 AJ3

USB2N_4 AD9
USB2P_4 AD10

USB2N_5 AJ1
USB2P_5 AJ2
USB2_BT_DN [50]
USB2_BT_DP [50]
BT

USB2N_6 AF6
USB2P_6 AF7

USB2N_7 AH1
USB2P_7 AH2
USB2_BLADE_DN [74]
USB2_BLADE_DP [74]
BLADE

USB2N_8 AF8
USB2P_8 AF9

USB2N_9 AG1
USB2P_9 AG2

USB2N_10 AH7
USB2P_10 AH8

USB2_COMP AB6
USB2_ID AG3
USB2_VBUSSENSE AG4
USB2_COMP R2402 113 res_0201_12mil
GND

GPP_E9/USB2_OC0# A9
GPP_E10/USB2_OC1# C9
GPP_E11/USB2_OC2# D9
GPP_E12/USB2_OC3# B9
GPP_E10
GPP_E11
GPP_E12

GPP_E4/DEVSLP0 J1
GPP_E5/DEVSLP1 J2
GPP_E6/DEVSLP2 J3
GPP_E4
GPP_E5
GPP_E6

GPP_E0/SATAXPCIE0/SATAGP0 H2
GPP_E1/SATAXPCIE1/SATAGP1 H3
GPP_E2/SATAXPCIE2/SATAGP2 G4
GPP_E0
GPP_E1
GPP_E2

GPP_E8/SATALED# H1
GPP_E8

+3VSUS_ORG
R2417 10K RES_0201_12mil DNP,CPU
R2418 10K RES_0201_12mil DNP,CPU
R2420 10K RES_0201_12mil DNP,CPU
R2419 10K RES_0201_12mil CPU

USB_CONN_OC# [45]

XDP_TP2400 TPS0P35
XDP_TP2401 TPS0P35
XDP_TP2402 TPS0P35
XDP_TP2403 TPS0P35
XDP_TP2404 TPS0P35
XDP_TP2405 TPS0P35
XDP_TP2406 TPS0P35
XDP_TP2407 TPS0P35
XDP_TP2408 TPS0P35
XDP_TP2409 TPS0P35
XDP_TP2410 TPS0P35

R2403 0 RES_0201_12mil DEVSLP_SSD [43]
R2409 0 RES_0201_12mil SSD_SATA_PCIE_DET_N [43]

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

Title: PCH(5)_PCIE,USB
Engineer: Surface
Size A3 | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 | Sheet 24 of 76

No reboot strap
Low: Disable (Default)
High:Enable

U1001F
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT

LPSS

+3P3V — DNP,CPU R2543 1K RES_0201_12mil — SKL_NO_REBOOT — INT. PD

AN8 GPP_B15/GSPI0_CS#
AP7 GPP_B16/GSPI0_CLK
AP8 GPP_B17/GSPI0_MISO
AR7 GPP_B18/GSPI0_MOSI

[31] PCH_SAM_INT — AM5 GPP_B19/GSPI1_CS#
AN7 GPP_B20/GSPI1_CLK
AP5 GPP_B21/GSPI1_MISO
[25] BBS_BIT0 — INT. PD — AN5 GPP_B22/GSPI1_MOSI

+3P3V
[33,71] PCH_UART0_RXD — AB1 GPP_C8/UART0_RXD
[33,71] PCH_UART0_TXD — AB2 GPP_C9/UART0_TXD
[31,33] SWD_CLK — DNP,CPU R2525 0 — SWD_CLK_R — W4 GPP_C10/UART0_RTS#
[31,33] SWD_DIO — DNP,CPU R2526 0 — SWD_DIO_R — AB3 GPP_C11/UART0_CTS#
RES_0201_12mil
RES_0201_12mil
[25,62,64] RTD3_AUD_PWR — AD1 GPP_C20/UART2_RXD
AD2 GPP_C21/UART2_TXD
AD3 GPP_C22/UART2_RTS#
[25,31] LID_CLOSED — AD4 GPP_C23/UART2_CTS#

EV19
WAS: INSTALL

+3P3V
RES_0201_12mil 499 R2589
RES_0201_12mil 499 R2590

TO SAM
[31,33] SH_I2C_SDA — U7 GPP_C16/I2C0_SDA
[31,33] SH_I2C_SCL — U6 GPP_C17/I2C0_SCL

[28] PMI_I2C_SDA — U8 GPP_C18/I2C1_SDA
[28] PMI_I2C_SCL — U9 GPP_C19/I2C1_SCL

[54] I2C_SDA_FCAM — R2522 0 RES_0201_12mil — I2C_SDA_FCAM_R — AH9 GPP_F4/I2C2_SDA
[54] I2C_SCL_FCAM — R2523 0 RES_0201_12mil — I2C_SCL_FCAM_R — AH10 GPP_F5/I2C2_SCL

[53] I2C_SDA_RCAM — R2520 0 RES_0201_12mil — I2C_SDA_REAR_IR_CAM — AH11 GPP_F6/I2C3_SDA
[53] I2C_SCL_RCAM — R2521 0 RES_0201_12mil — I2C_SCL_REAR_IR_CAM — AH12 GPP_F7/I2C3_SCL
AF11 GPP_F8/I2C4_SDA
AF12 GPP_F9/I2C4_SCL

[49] I2C_SDA_IRCAM — 0 R2527 RES_0201_12mil
[49] I2C_SCL_IRCAM — 0 R2528 RES_0201_12mil

4.99K RES_0201_2mil R2504 — +1P8V_CAM_F
4.99K RES_0201_2mil R2506
4.99K RES_0201_2mil R2507 — +1P8V_CAM_R
4.99K RES_0201_2mil R2508

I2C PU can be placed anywhere along the net

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REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

ISH

GPP_D9 P2 TPANEL_RST#_R — R2511 0 RES_0201_12mil — TPANEL_RST# [25,30]
GPP_D10 P3 — RTD3_TPANEL_PWR [25,62,64]
GPP_D11 P4 — CAM_R_XO_EN [25,53]
GPP_D12 P1 — CAM_F_XO_EN [25,54]

GPP_D5/ISH_I2C0_SDA — M4 CAM_F_PWR_DN_N_R — R2512 330 res_0201_12mil — MTP2531 — CAM_F_PWR_DN_N [21,53,54]
GPP_D6/ISH_I2C0_SCL — N3 CAM_R_PWR_DN_N_R — R2513 CPU 330 res_0201_12mil — MTP2530 — CAM_R_PWR_DN_N [21,53,54]

GPP_D7/ISH_I2C1_SDA — N1
GPP_D8/ISH_I2C1_SCL — N2 CAM_IR_PWR_DN_N_R — R2509 1K RES_0201_12mil — CAM_IRCAM_XO_EN [49]; CAM_IR_PWR_DN_N [49]; MTP2501 SP_TP_SMDp58mm

GPP_F10/I2C5_SDA/ISH_I2C2_SDA — AD11
GPP_F11/I2C5_SCL/ISH_I2C2_SCL — AD12 FLASH_PROTECT_N_R — R2598 0 RES_0201_12mil — FLASH_PROTECT_N [30]

GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA — U1 — TS_BRD_REV[0] [25,30]
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL — U2 — TS_BRD_REV[1] [25,30]
GPP_D15/ISH_UART0_RTS# — U3 — TCON_BRD_REV [25,57]
GPP_D16/ISH_UART0_CTS#/SML0BALERT# — U4 — TCON_VENDOR_ID [25,57]

GPP_C12/UART1_RXD/ISH_UART1_RXD — AC1
GPP_C13/UART1_TXD/ISH_UART1_TXD — AC2 *was PCIE_GPU_PERST#* — SL1_CONN [25,31]
GPP_C14/UART1_RTS#/ISH_UART1_RTS# — AC3 — SH_INT [25,31,33]
GPP_C15/UART1_CTS#/ISH_UART1_CTS# — AB4 — PCIE_WIFI_WAKE_N [25,50]
TP2514 SP_TP_SMDp58mm

GPP_A18/ISH_GP0 — AY8 — WLAN_PWD_N [25,50]
GPP_A19/ISH_GP1 — BA8 — DISPLAY_OFF# [25,36,64]
GPP_A20/ISH_GP2 — BB7 — PCIE_WIFI_DISABLE_N [25,50]
GPP_A21/ISH_GP3 — BA7 — PCIE_WIFI_PERST_N [25,50]
GPP_A22/ISH_GP4 — AY7
GPP_A23/ISH_GP5 — AW7
GPP_A12/BM_BUSY#/ISH_GP6 — AP13 PCIE_SSD_PERST#_R — R2599 0 RES_0201_12mil — WWAN_PWREN [25,65]; PCIE_SSD_PERST# [43]

TP2513 SP_TP_SMDp58mm
TP2521 SP_TP_SMDp58mm
TP2515 SP_TP_SMDp58mm
TP2516 SP_TP_SMDp58mm

EV1.9 SWAP PCIE_WIFI_WAKE_N and DISPLAY_OFF#

+3VSUS_ORG

R2532 DNP,CPU 10K RES_0201_12mil
R2567 DNP,CPU 49.9K RES_0201_12mil — PCIE_WIFI_DISABLE_N [25,50]
R2531 DNP,CPU 10K RES_0201_12mil
R2573 DNP,CPU 49.9K RES_0201_12mil — PCIE_WIFI_PERST_N [25,50]
R2591 DNP,CPU 10K RES_0201_12mil — SH_INT [25,31,33]
R2530 49.9K RES_0201_12mil
R2552 DNP,CPU 10K RES_0201_12mil — RTD3_CAM_PWREN [23,52]
R2592 49.9K RES_0201_12mil
R2577 CPU 10K RES_0201_12mil — PCIE_WIFI_WAKE_N [25,50]
R2535 DNP,CPU 49.9K RES_0201_12mil

[30] PCH_I2C1_SDA_TS
[30] PCH_I2C1_SCL_TS

RES_0201_12mil 1.21K R2586
RES_0201_12mil 1.21K R2587 — +1P8V_TS

+1P8V
RES_0201_12mil R2560 49.9K — TCON_BRD_REV [25,57]
RES_0201_12mil R2561 49.9K — TCON_VENDOR_ID [25,57]
RES_0201_12mil R2562 49.9K — TS_BRD_REV[0] [25,30]
RES_0201_12mil R2563 49.9K — TS_BRD_REV[1] [25,30]

R2539 DNP,CPU 49.9K RES_0201_12mil — DISPLAY_OFF# [25,36,64]
R2572 49.9K RES_0201_12mil — WWAN_PWREN [25,65]
R2595 49.9K RES_0201_12mil — RTD3_AUD_PWR [25,62,64]
R2559 49.9K RES_0201_12mil — RTD3_TPANEL_PWR [25,62,64]
R2596 10K RES_0201_12mil — TPANEL_RST# [25,30]
R2578 49.9K RES_0201_12mil — LID_CLOSED [25,31]
R2502 49.9K RES_0201_12mil — CAM_R_XO_EN [25,53]
R2503 49.9K RES_0201_12mil — CAM_F_XO_EN [25,54]
R2548 49.9K RES_0201_12mil — WLAN_PWD_N [25,50]
R2514 49.9K RES_0201_12mil — SL1_CONN [25,31]

BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap	
BBS_BIT0	Boot BIOS Location
1	LPC
0	SPI **(PCH)**

Sampled on rising edge of PWROK.

[25] BBS_BIT0 — +3P3V — RES_0201_12mil R2501 DNP,CPU 10K; R2574 DNP,CPU 49.9K RES_0201_12mil

Vinafix.com

Title:	PCH(6)_CPU,GPIO,MISC		
Engineer:	*Surface*		
Size: B	Project Name: **U -- EV 1.90**		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 25 of 76	

U1001O
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
CPU POWER 4 OF 4

VCCPRIM_1P0 AB19
VCCPRIM_1P0 AB20
VCCPRIM_1P0 P18
VCCPRIM_CORE AF18
VCCPRIM_CORE AF19
VCCPRIM_CORE V20
VCCPRIM_CORE V21
DCPDSW_1P0 AL1
VCCMPHYAON_1P0 K17
VCCMPHYAON_1P0 L1
VCCMPHYGT_1P0_N15 N15
VCCMPHYGT_1P0_N16 N16
VCCMPHYGT_1P0_N17 N17
VCCMPHYGT_1P0_P15 P15
VCCMPHYGT_1P0_P16 P16
VCCAMPHYPLL_1P0 K15
VCCAMPHYPLL_1P0 L15
VCCAPLL_1P0 V15
VCCPRIM_1P0_AB17 AB17
VCCPRIM_1P0_Y18 Y18
VCCDSW_3P3_AD17 AD17
VCCDSW_3P3_AD18 AD18
VCCDSW_3P3_AJ17 AJ17
VCCHDA AJ19
VCCSPI AJ16
VCCSRAM_1P0 AF20
VCCSRAM_1P0 AF21
VCCSRAM_1P0 T19
VCCSRAM_1P0 T20
VCCPRIM_3P3_AJ21 AJ21
VCCPRIM_1P0_AK20 AK20
VCCAPLLEBB N18

15 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

VCCPGPPA AK15
VCCPGPPB AG15
VCCPGPPC Y16
VCCPGPPD Y15
VCCPGPPE T16
VCCPGPPF AF16
VCCPGPPG AD15
VCCPRIM_3P3_V19 V19
VCCPRIM_1P0_T1 T1
VCCATS_1P8 AA1
VCCRTCPRIM_3P3 AK17
VCCRTC_AK19 AK19
VCCRTC_BB14 BB14
DCPRTC BB10
VCCCLK1 A14
VCCCLK2 K19
VCCCLK3 L21
VCCCLK4 N20
VCCCLK5 L19
VCCCLK6 A10
GPP_B0/CORE_VID0 AN11
GPP_B1/CORE_VID1 AN13

+1VSB
DNP,CPU C2622 1u 6.3V CAP_0402_22mil
+0P85VSB 2.57A
DNP,CPU C2612 1u 6.3V CAP_0402_22mil
C2613 1u 6.3V CAP_0402_22mil
+1V_MODPHY
L2605 0 res_0603_24mil
DNP,CPU CE2601 47u 6.3V cap_0603_40mil
C2614 1u 6.3V CAP_0402_22mil
L2601 0 res_0603_24mil
DNP,CPU CE2639 47u 6.3V cap_0603_40mil
DNP,CPU C2632 1u 6.3V CAP_0402_22mil
C2615 1u 6.3V CAP_0402_22mil
DCPDSW_1P0
VCCMPHYGT_1P0
VCCAMPHYPLL_1P0
VCCAPLL_1P0
VCCAPLLEBB
VCCPLL (VCCSFR) = 0.12A
+1VSB
L2607
EV1.9 Add C2637 6.3V 0.1u cap_0201_14mil
ind_0402_22mil
EV1.9 Was 0ohm,0603
DNP,CPU CE2635 47u 6.3V cap_0603_40mil
+VCCDSW
+1P8VSUS_ORG
L2611
+3VSUS_ORG
ind_0402_22mil
EV1.9 Add C2636 6.3V 0.1u cap_0201_14mil
EV1.9 Add
DNP,CPU C2617 1u 6.3V CAP_0402_22mil
+1V_MODPHY
R2622 0 RES_0402_16mil
DNP,CPU C2619 1u 6.3V CAP_0402_22mil
+1VSB
+1V_MODPHY
R2623 0 RES_0402_16mil
C2625 1u 6.3V CAP_0402_22mil
+3VSUS_ORG
+1P8VSUS_ORG
+1VSB
+3VSUS_ORG
+1P8VSUS_ORG
+VCC_RTC
+1VSB
+1P8VSUS_ORG
+3VSUS_ORG
+VCCCLK5_R
for B, C E port
DNP,CPU C2620 1u 6.3V CAP_0402_22mil
DNP,CPU C2634 1u 6.3V CAP_0402_22mil
DNP,CPU C2635 1u 6.3V CAP_0402_22mil
DNP,CPU C2621 1u 6.3V CAP_0402_22mil
C2627 1u 6.3V CAP_0402_22mil
C2629 1u 6.3V CAP_0402_22mil
C2628 0.1u 25V CAP_0402_22mil
C2630 0.1u 25V CAP_0402_22mil
C2633 1u 6.3V CAP_0402_22mil
DCPRTC
C2631 0.1u 25V CAP_0402_22mil
VCCCLK2_R
VCCCLK4_R
+VCCCLK5_R
CORE_VID0 [56]
CORE_VID1 [56]
L2610 0 res_0603_24mil
DNP,CPU CE2636 47u 6.3V cap_0603_40mil
L2609 0 res_0603_24mil
DNP,CPU CE2637 47u 6.3V cap_0603_40mil
L2608 0 res_0603_24mil
DNP,CPU CE2638 47u 6.3V cap_0603_40mil
DNP,CPU C2623 1u 6.3V CAP_0402_22mil
+1P8VSB
DB,CPU R2624 0.01 res_0402_22mil
PMTP2605 SP-tp-c0p381
PMTP2606 SP-tp-c0p381
+1P8VSUS_ORG
CE2641 47u 6.3V cap_0603_40mil
+0P85VSB
CE2643 47u 6.3V cap_0603_40mil
+1VSB
CE2642 47u 6.3V cap_0603_40mil
+3P3VSB
DB,CPU R2612 0.01 res_0402_22mil
PMTP2607 SP-tp-c0p381
PMTP2608 SP-tp-c0p381
+3VSUS_ORG
CE2640 47u cap_0603_40mil 6.3V

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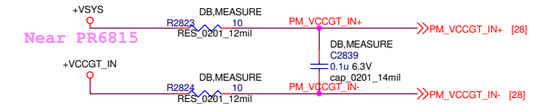
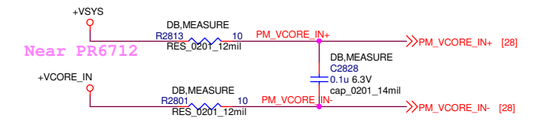
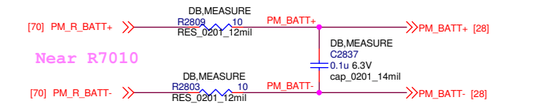
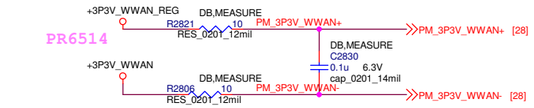
Title: PCH(7)_POWER
Engineer: Surface
Size A3 | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 | Sheet 26 of 76

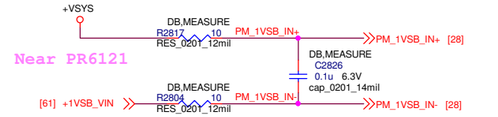
Title:	PCH(8)_empty
Engineer:	Surface
Size: B	Project Name: U -- EV 1.90
Rev:	1.90.2
Date:	Monday, May 11, 2015
Sheet	27 of 76

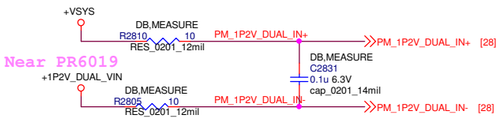


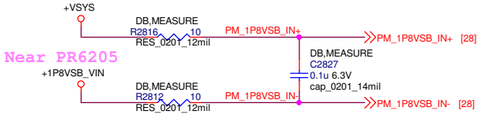


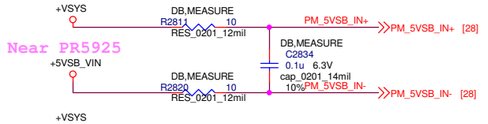


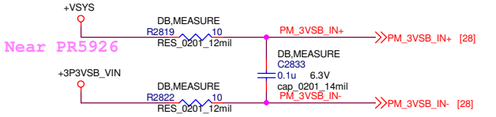


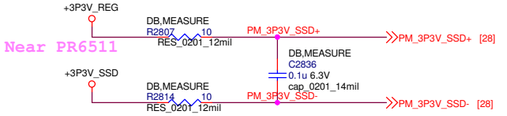


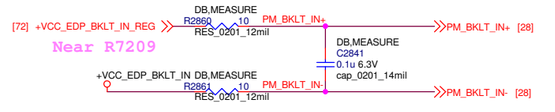


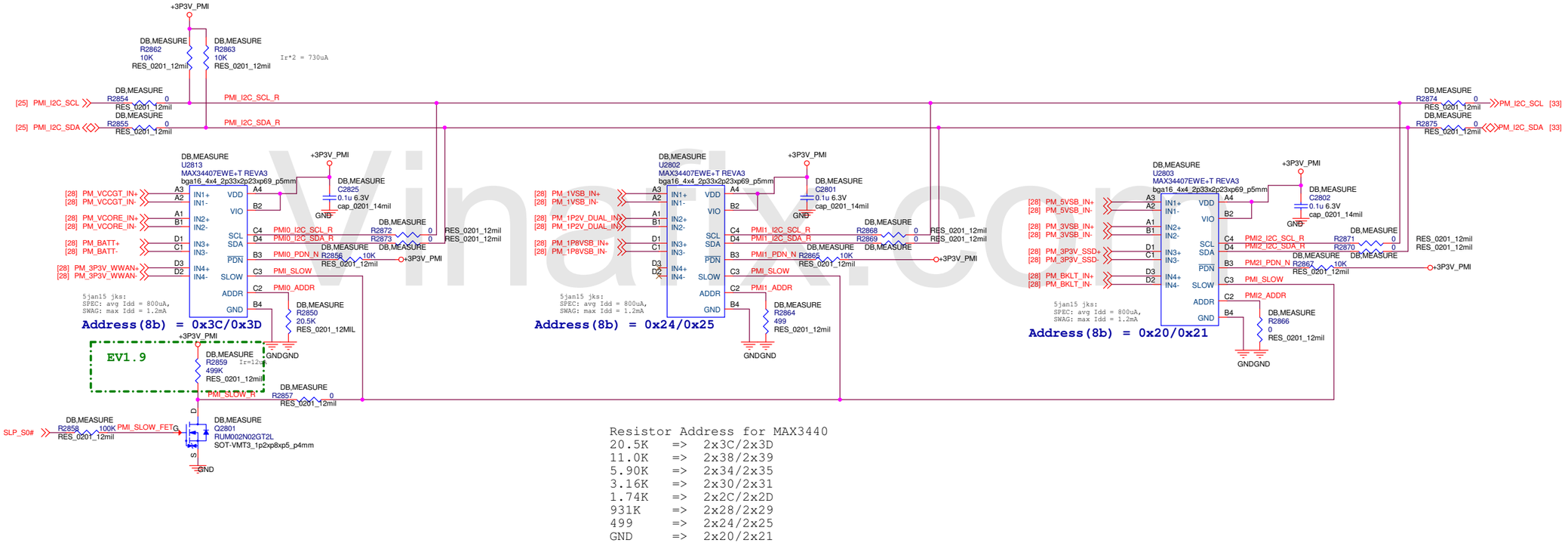












Resistor Address for MAX3440
20.5K => 2x3C/2x3D
11.0K => 2x38/2x39
5.90K => 2x34/2x35
3.16K => 2x30/2x31
1.74K => 2x2C/2x2D
931K => 2x28/2x29
499 => 2x24/2x25
GND => 2x20/2x21

Title: Power Monitor
Engineer: Surface
Size: C
Project Name: U -- EV 1.90
Rev: 1.90.2
Date: Monday, May 11, 2015
Sheet 28 of 76

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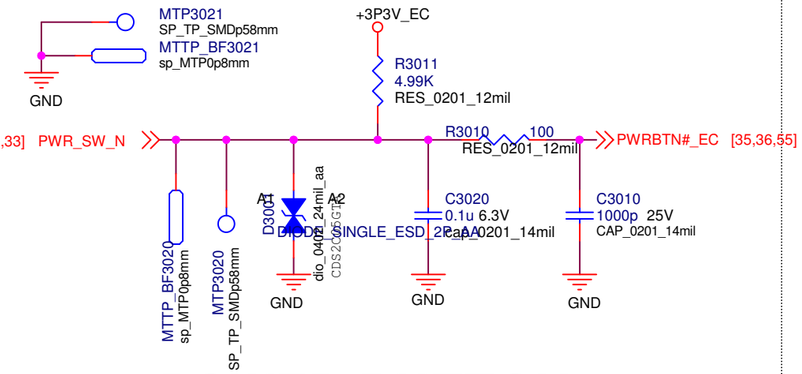
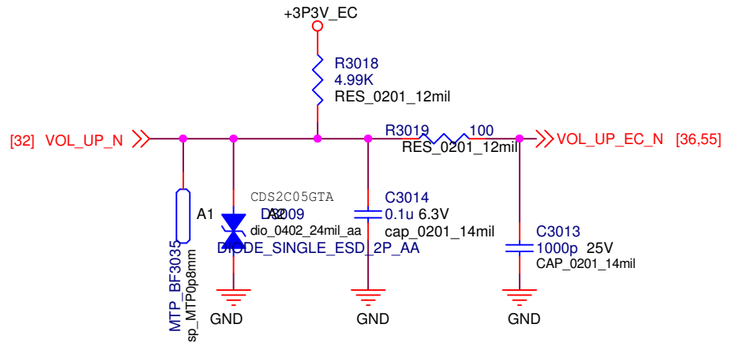
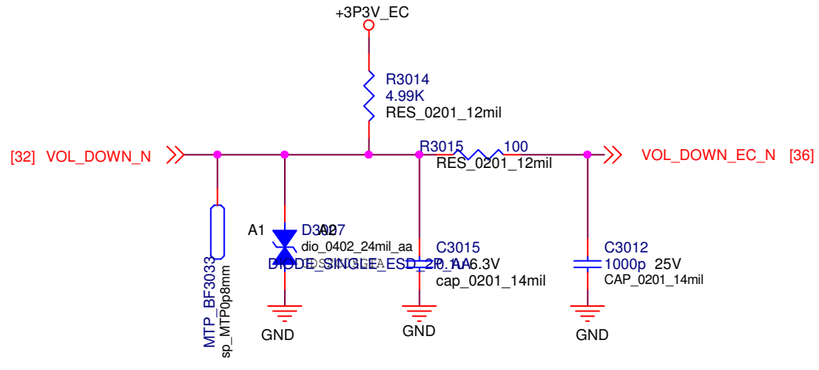
Title:	EMPTY		
Engineer:	*Surface*		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 29 of 76	



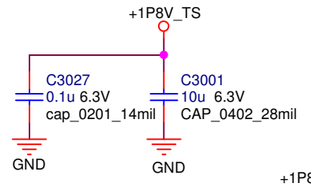
POWER BUTTON

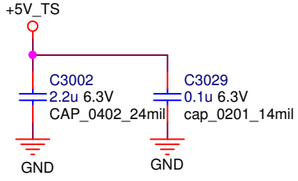


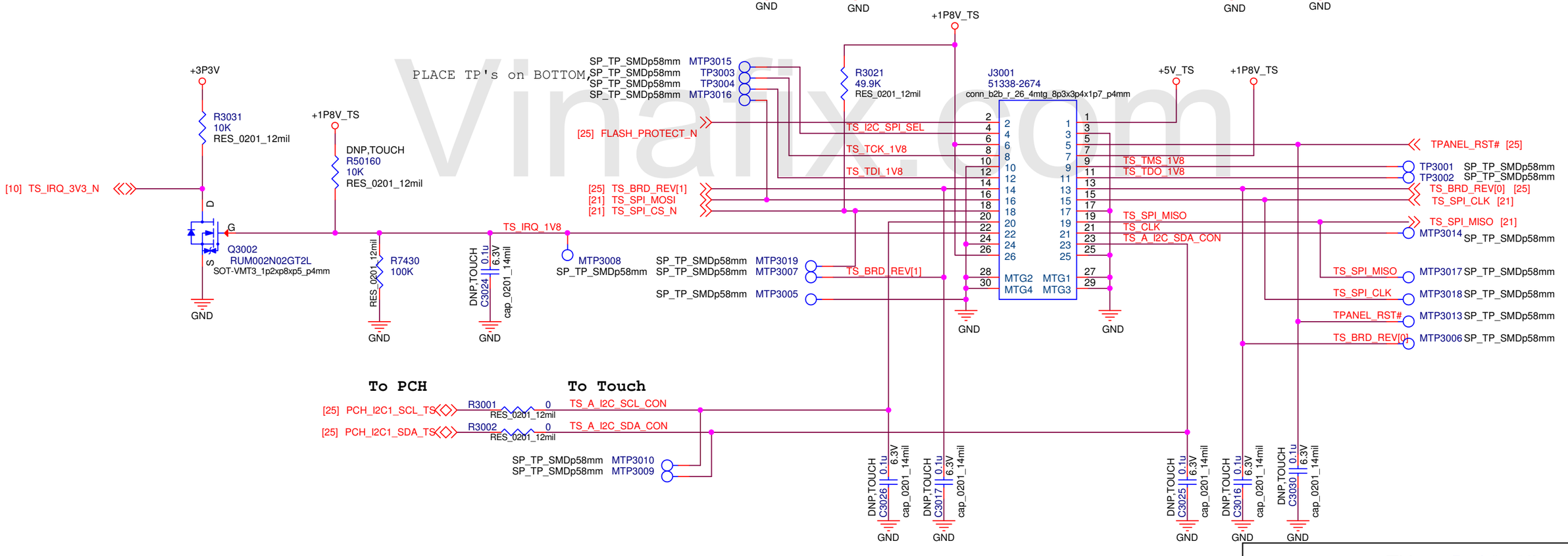
VOL_UP BUTTON



VOL_DOWN BUTTON







Title:	Touch Con & Key	
Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 30 of 76	

SENSOR MCU

Authentication

Address 0x28

+3P3VA
L3101 30 OHMS
IND_0603_38mil
1A
+1P8VA
Idda_adc<=1.7mA
R3172 0 RES_0402_16mil
VREFH
C3114 2.2u 6.3V CAP_0402_24mil
C3105 0.1u 6.3V cap_0201_14mil
GND
+3P3VA_F
C3110 10u 6.3V CAP_0402_28mil
C3107 0.1u 6.3V cap_0201_14mil
C3108 0.1u 6.3V cap_0201_14mil
C3109 0.1u 6.3V cap_0201_14mil
C3106 0.1u 6.3V cap_0201_14mil
D3101 RB520CS3002L dio_sod882_1x6x5_p7mm 30V 200mA
DNP,SENSOR
R3160 150K RES_0201_12mil
BLADE_AUTH_DATA [31,74]
SAM_X2_OUT
SAM_X2_IN R3171 10M RES_0201_12mil
R3112 0 RES_0402_16mil
SAM_CTAL_1
32.7 KHz
xtal_3p2x1p5xp9_2p5mm
X3101
C3113 18p 25V CAP_0201_14mil
C3112 25V 18p CAP_0201_14mil
GND
U3105
MKL17Z256VMP4
bga64_8x8_5x5x1p23_p5mm
G4 VREFH
G3 VREFL
VDD1 G7
VDD2 E4
VDDA F4
R3104 4.99K RES_0201_12mil
HOST_AUTH_TXRX_R R3105 100 RES_0201_12mil
One Wire UART
[31] SAM_SPI_NPCS[0] C3
[70] SL1_ADC_RD_EN A4
[32] ALS_IRQ_N C2
HOST_AUTH_TXRX B3
PTD0
PTD1
PTD2
PTD3
U3102
ATECC108A-MAHUT-T
son9_3x2xp6_p5mm-2
VCC NC1
SDA NC2
SCL NC3
GND NC7
X906888-001
SP_TP_SMDp58mm TP3146
R3179 100 RES_0201_12mil
BLADE_DET_N
[31,74] BLADE_AUTH_DATA A3
[71] EC_PCH_DBG_EN C1
[74] BLADE_UART_RX B2
[74] BLADE_UART_TX A2
PTD4/LLWU_P14
PTD5
PTD6/LLWU_P15
PTD7
C3130 0.1u 6.3V cap_0201_14mil
C3131 1u 6.3V CAP_0201_14mil
SP_TP_SMDp58mm TP3144
MTP_BF3145 sp_MTP0p8mm
R3181 10K RES_0201_12mil
PTA0 D3
PTA1 D4 BLADE_AUTH_RX R3177 100 RES_0201_12mil SWD_CLK [25,33]
PTA2 E5 BLADE_AUTH_TX R3178 100 RES_0201_12mil
MTP_BF3154 sp_MTP0p8mm
PTA3 D5
PTA4 G5 SAM_BOOT_TRAP SWD_DIO [25,33]
PTA5 F5 LID_CLOSED [25]
RES_0201_12mil
R3182 1K
TP3137 SP_TP_SMDp58mm
PTA12 H6
PTA13 G6 SL1_3P3V_DIS [72]
SAR_CONV [32]
MTP3162 SP_TP_SMDp58mm
PTA18 H8
PTA19 G8
PTA20 F8
R3117 10K RES_0201_12mil
MTP_BF3102 sp_MTP0p8mm
SEN_MCU_NRST [33]
DNP,SENSOR
C3132 100p 25V CAP_0201_14mil
GND
+3P3VA
[25,33] SH_INT
[25] SL1_CONN
SP_TP_SMDp58mm TP3126
A1
B1
PTE0
PTE1
R3103 200K RES_0201_12mil
SP_TP_SMDp58mm TP3121
SP_TP_SMDp58mm MTP3149
R3173 100K RES_0201_12mil
PTB0/LLWU_P5 F7
PTB1 F6
PTB2 E7 BLADE_UART_USB_N_R R3180 1K RES_0201_12mil
PTB3 E8
PCH_SAM_INT [25]
SENSORS_PWR_EN [65]
BLADE_UART_USB_N [74]
DBG_LED0 [33]
TP3101 SP_TP_SMDp58mm
SP_TP_SMDp58mm TP3116
[70] SL1_ADC E1
[31,33] SAM_SPI_SPCK D1
[31,33] SAM_SPI_MOSI E2
[31,33] SAM_SPI_MISO D2
PTE16
PTE17
PTE18
PTE19
PTE20
PTE21
PTE22
PTE23
TP3163 SP_TP_SMDp58mm
TP3120 SP_TP_SMDp58mm
SL1_UART_TX_SEL_N [70]
BLADE_+5V_KB_CONN_EN [64]
SAR_INDICATION_2 [10]
SL1_5V_OC# [64]
+3P3VA
[33,71] SEN_MCU_UART_TXD
[33,71] SEN_MCU_UART_RXD
R3143 33 SEN_MCU_UART_TXD_R RES_0402_16mil
R3144 33 SEN_MCU_UART_RXD_R RES_0402_16mil
R3152 1K RES_0201_12mil
R3151 1K RES_0201_12mil
[35] EC_SAM_I2C_SDA G2
[35] EC_SAM_I2C_SCL F2
SP_TP_SMDp58mm TP3152
SP_TP_SMDp58mm TP3153
I2C_SCL_MCU_R H4
I2C_SDA_MCU_R H5
PTE24
PTE25
E6 SL1_UART_TX_SEL_R R3113 0 RES_0201_12mil
D7 BLADE_+5V_KB_CONN_EN_R R3183 0 RES_0201_12mil
D6 SAR_INDICATION_2_R R3107 0 RES_0201_12mil
C7 was HINGER1_POS_A
PTB16
PTB17
PTB18
PTB19
TP3155 SP_TP_SMDp58mm
D8
C6
B7
PTC0
PTC1/LLWU_P6/RTC_CLKIN
PTC2
SL1_5V_PWR_EN [64,70]
SH_I2C_SCL [25,33]
SH_I2C_SDA [25,33]
[31,32,33] I2C_SCL_MCU
[31,32,33] I2C_SDA_MCU
R3122 0 RES_0201_12mil
R3124 0 RES_0201_12mil
MTP3104 SP_TP_SMDp58mm
MTP3103 SP_TP_SMDp58mm
SP_TP_SMDp58mm TP3150
SP_TP_SMDp58mm TP3122
[73] BLADE_AUTH_PWR_EN H1
H2
[70] SL1_UART_RX_SEL_N H3
PTE29
PTE30
PTE31
C8 SL1_UART_RX_R R3115 100 RES_0201_12mil
B8 SL1_UART_TX_R R3114 100 RES_0201_12mil
A8 SEN_HALL_INT_S_R R3111 0 RES_0201_12mil
A7
PTC3/LLWU_P7
PTC4/LLWU_P8
PTC5/LLWU_P9
PTC6/LLWU_P10
SL1_UART_RX [33,70]
SL1_UART_TX [33,70]
SEN_HALL_INT [32]
EC_SAM_INT [33,36]
MTP3118
SP_TP_SMDp58mm
[33,36] SAM_EC_INT
R3176 100K RES_0201_12mil
SP_TP_SMDp58mm TP3139
C5 NC
C4
H7 VSS1
E3 VSS2
VSS3
F3 VSSA
SP_TP_SMDp58mm TP3164
B5 SAR_INDICATION_1_R R3106 0 RES_0201_12mil
A6 was HGR2_PWR_EN
B6
PTC9
PTC8
PTC7
SAR_INDICATION_1 [10]
TP3160 SP_TP_SMDp58mm
SL1_BUF_EN [47,71]
TP3136 SP_TP_SMDp58mm
B4 was HINGER2_POS_B
A5
PTC10
PTC11
I2C_ADUX_MUX [32]
AGYRO_INT1 [32]
TP3159 SP_TP_SMDp58mm
+3P3VA
R3127 10K RES_0201_12mil
R3126 10K RES_0201_12mil
[31] SAM_SPI_NPCS[0]
[31,33] SAM_SPI_MISO
SAM_SPI_NPCS[0] 1
SAM_SPI_MISO 2
FLASH_WP_N 3
4
U3104
W25X40CLUXIG
son9_2x3xp6_p5mm
/CS
DO(IO1)
/WP
GND
GND_PAD 9
VCC 8
/HOLD 7
CLK 6
DI(IO0) 5
MSPN = X893206-001
SAM_FLASH_VCC
SAM_HOLD#
SAM_SPI_SPCK
SAM_SPI_MOSI
SAM_SPI_SPCK [31,33]
SAM_SPI_MOSI [31,33]
SAM_HOLD#
TP3130 SP_TP_SMDp58mm
TP3133 SP_TP_SMDp58mm
R3102 0 RES_0402_16mil
R3125 10K RES_0201_12mil
C3119 0.1u 6.3V cap_0201_14mil
SAM_SPI_NPCS[0]
FLASH_WP_N
TP3127 SP_TP_SMDp58mm
TP3129 SP_TP_SMDp58mm

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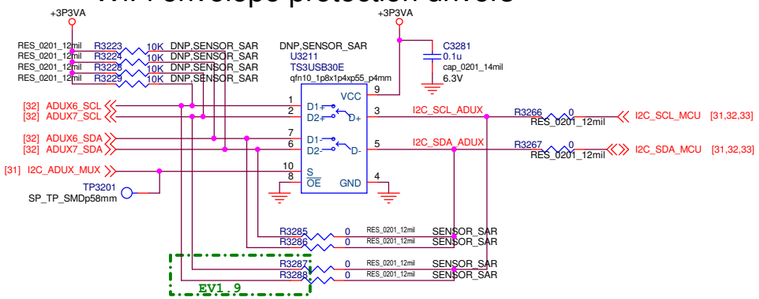
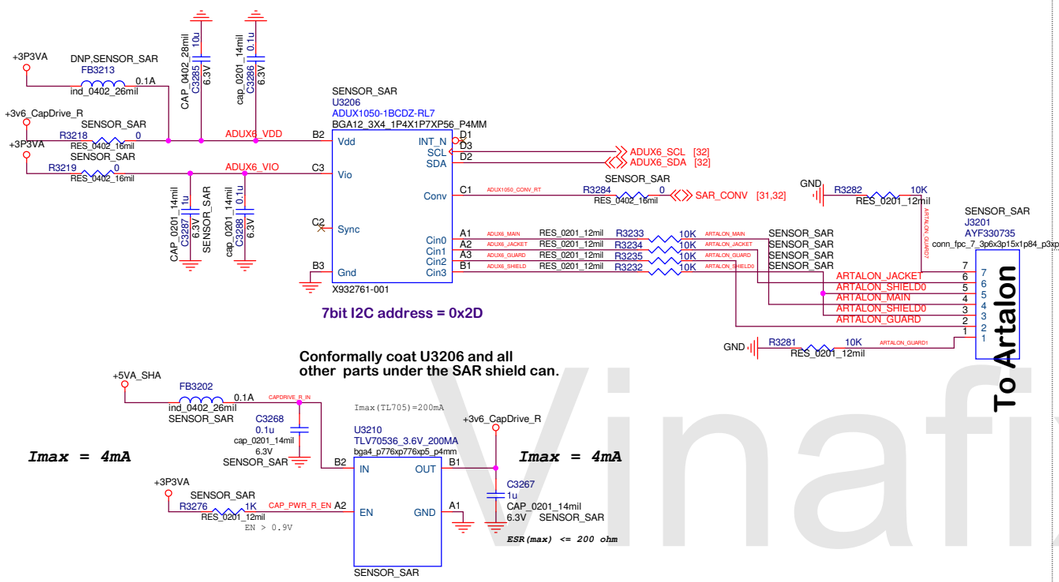
Title:	Sensor-uC
Engineer:	Surface
Size	B
Project Name	
Rev	1.90.2
Date:	Monday, May 11, 2015
Sheet	31 of 76

WiFi envelope protection drivers



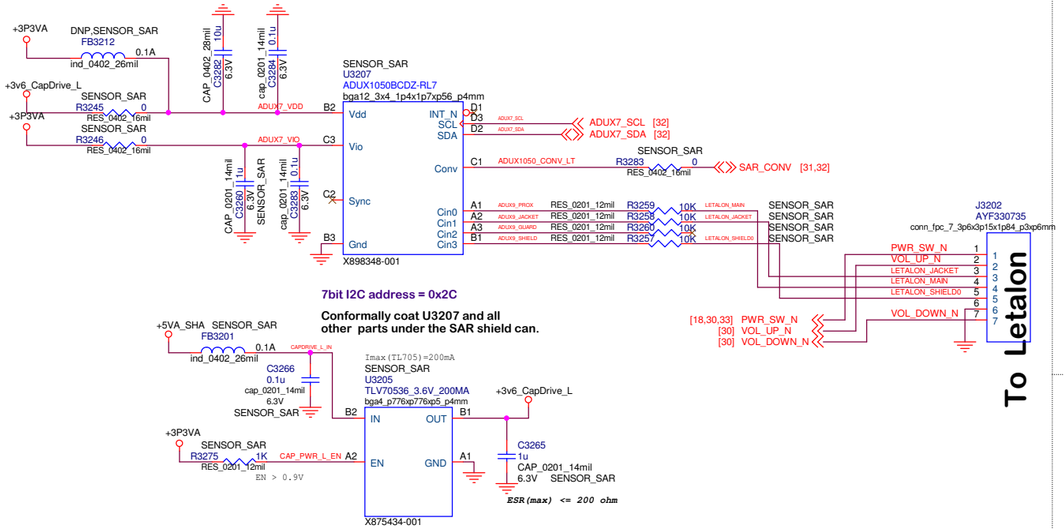


7bit I2C address = 0x2D

Conformally coat U3206 and all other parts under the SAR shield can.

Imax = 4mA

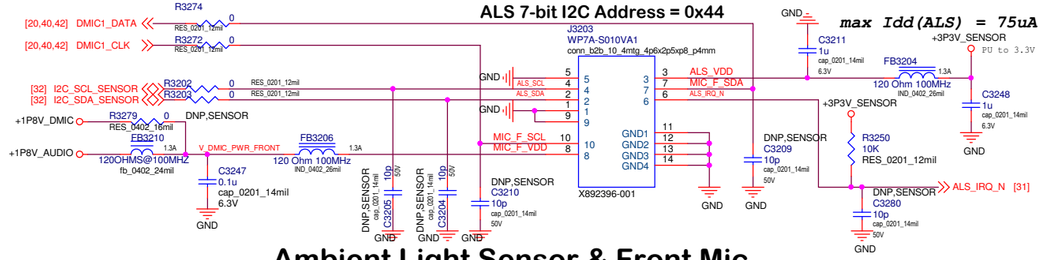
Imax = 4mA



7bit I2C address = 0x2C

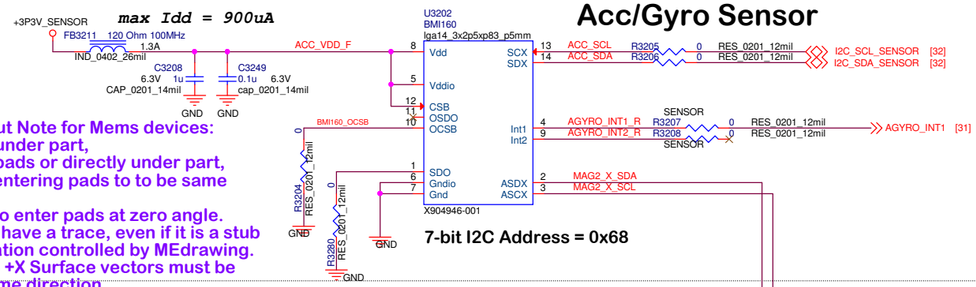
Conformally coat U3207 and all other parts under the SAR shield can.

ALS 7-bit I2C Address = 0x44



Ambient Light Sensor & Front Mic

Acc/Gyro Sensor

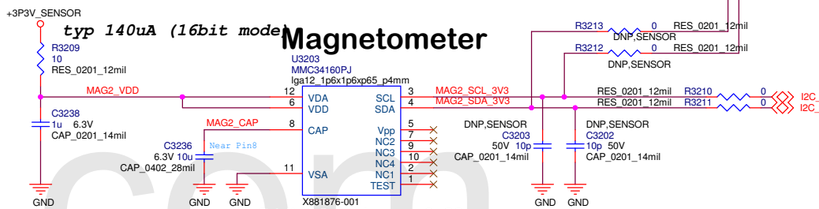


Critical Layout Note for Mems devices:
- No traces under part,
- No vias in pads or directly under part,
- All traces entering pads to to be same width,
- All traces to enter pads at zero angle.
- All pads to have a trace, even if it is a stub

Clocking rotation controlled by MEdrawing. (+X Device & +X Surface vectors must be parallel w/same direction

7-bit I2C Address = 0x68

Magnetometer

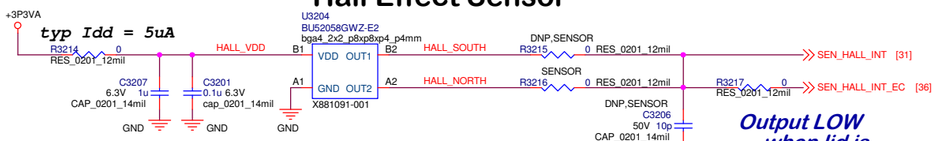


7-bit I2C Address = 0x30

Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm ... on any layer.
Clocking rotation controlled by MEdrawing.

This change, putting the MAG behind the AGyro allows us to take advantage of the time-stamped FIFO in the AGyro to reduce power consumption and address load on the I2C bus -- in addition to improving jitter filtering in post processing. Eventually this will enable IR range camera frame syncing.

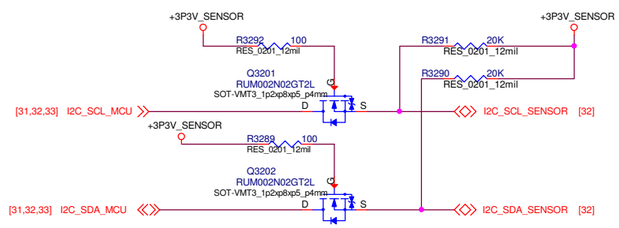
Hall Effect Sensor



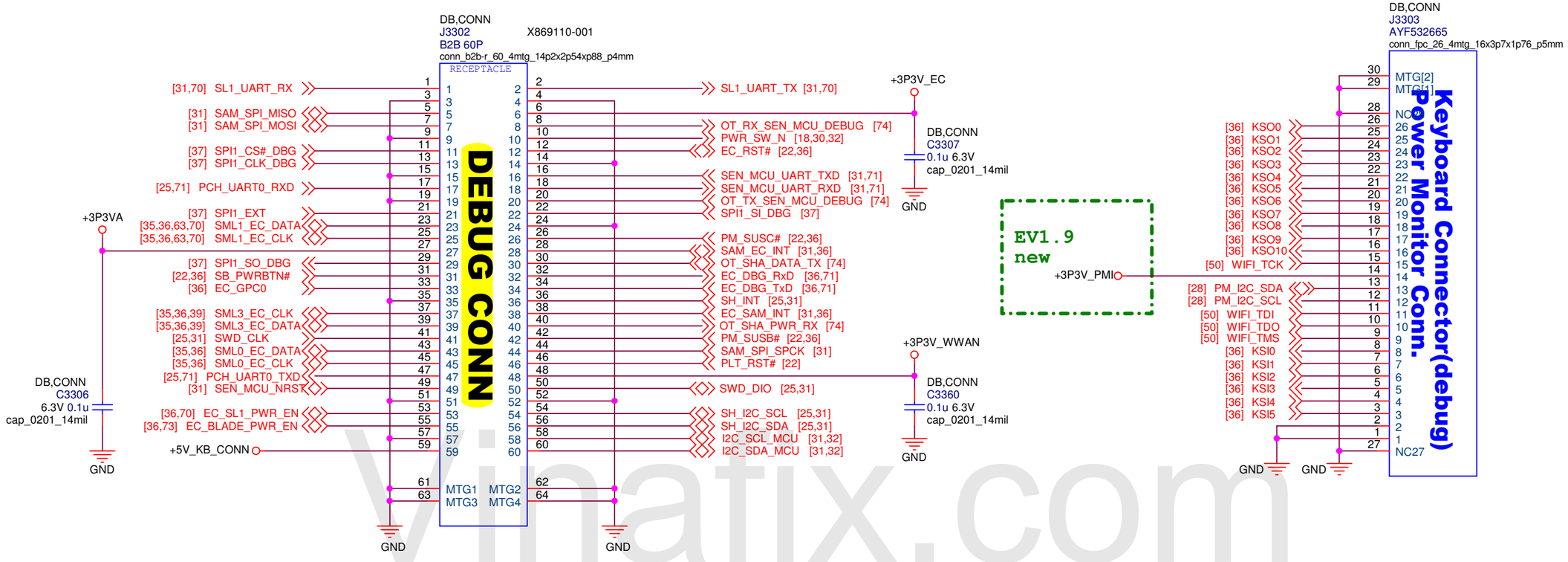
Output LOW ...when lid is closed

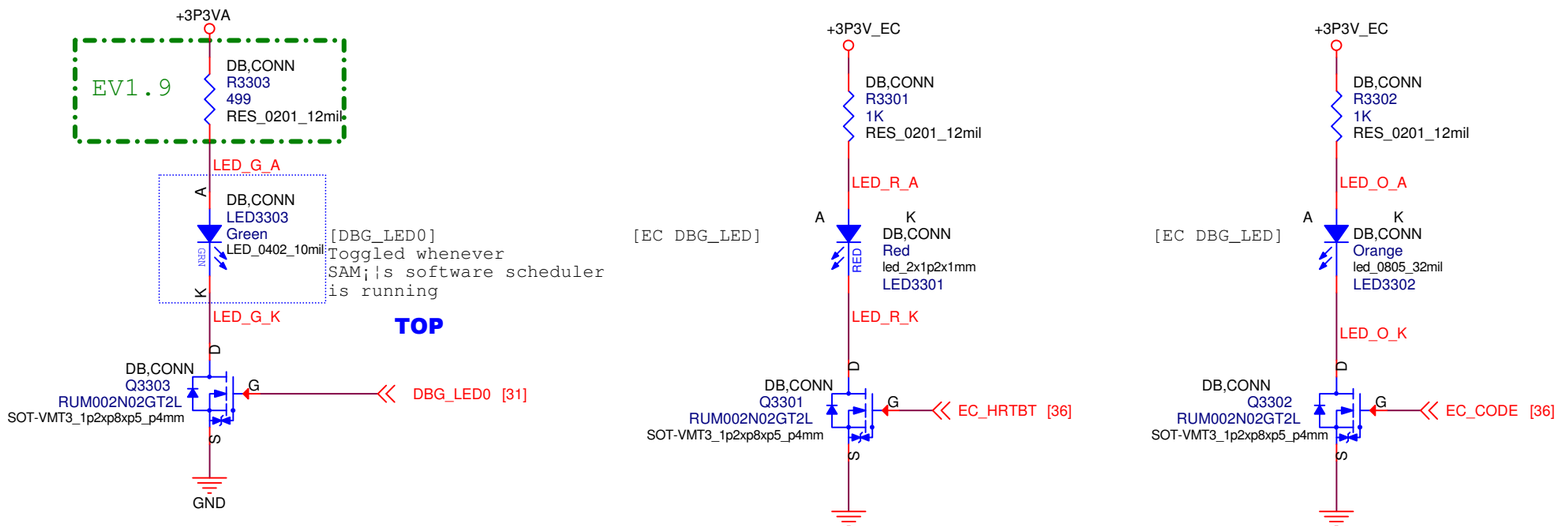
typ Idd(en) = 2.8mA (startup)

Critical Layout Note:
Sensitive to ferrous materials
Do not mount under a steel shield can
If mounted on Glass side of board,
Trigger may occur as early as 30Gauss North B-field or as late as 50Gauss North B-field
Be careful not to mount within 15mm of speaker autofocus camera or other magnet.
X-Y location controlled by MEdrawing.



Title: On Board-Sensors
Engineer: Surface
Size C | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 | Sheet 32 of 76





<Core Design>

Title: Debug Conn / LPC

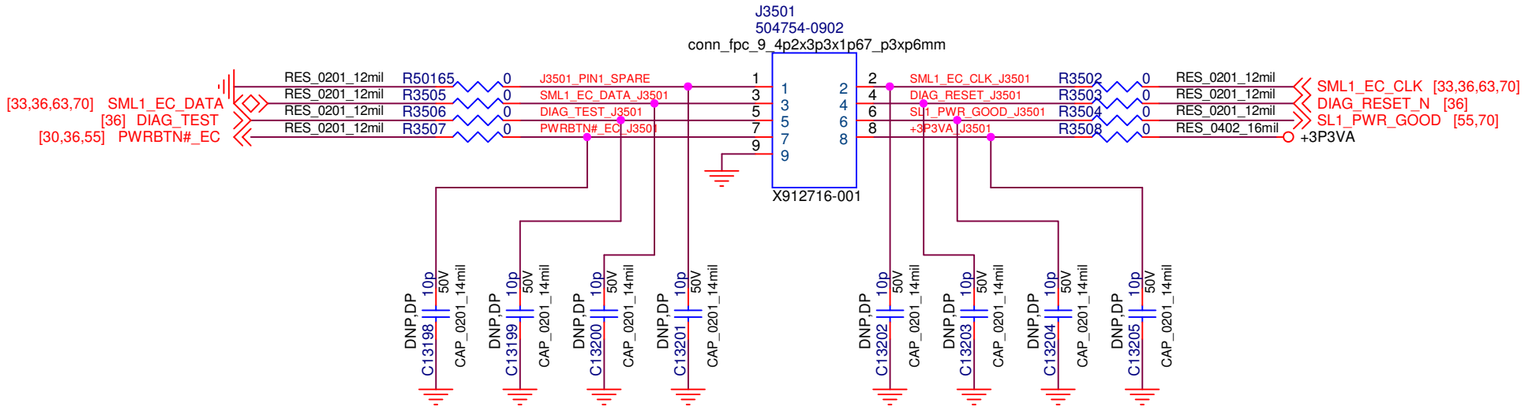
Microsoft Engineer: Surface

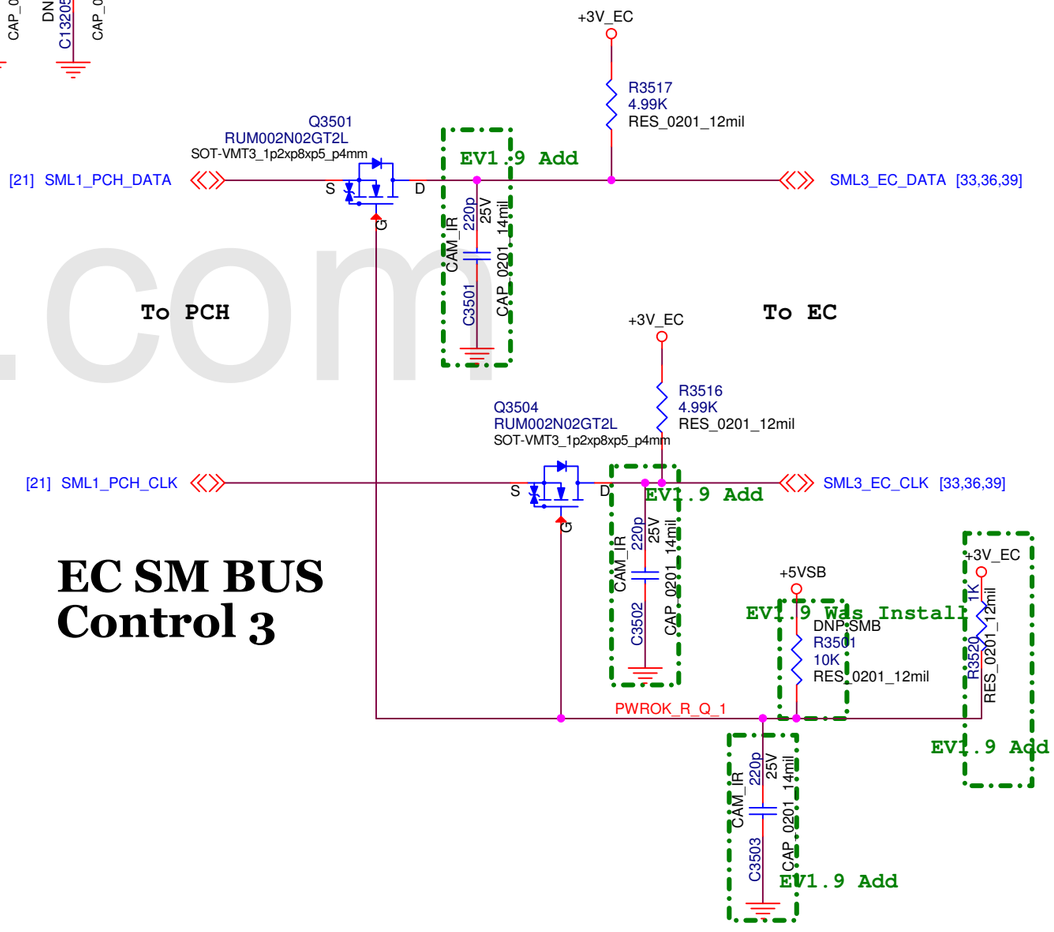
Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

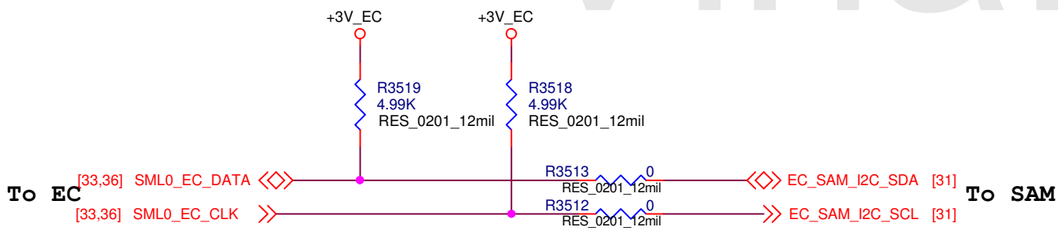
Date: Monday, May 11, 2015 Sheet 33 of 76

Title:	Empty
Microsoft	Engineer: Surface
Size: A	Project Name: U -- EV 1.90
Rev:	1.90.2
Date:	Monday, May 11, 2015
Sheet	34 of 76

DIAGNOSTIC CONNECTOR

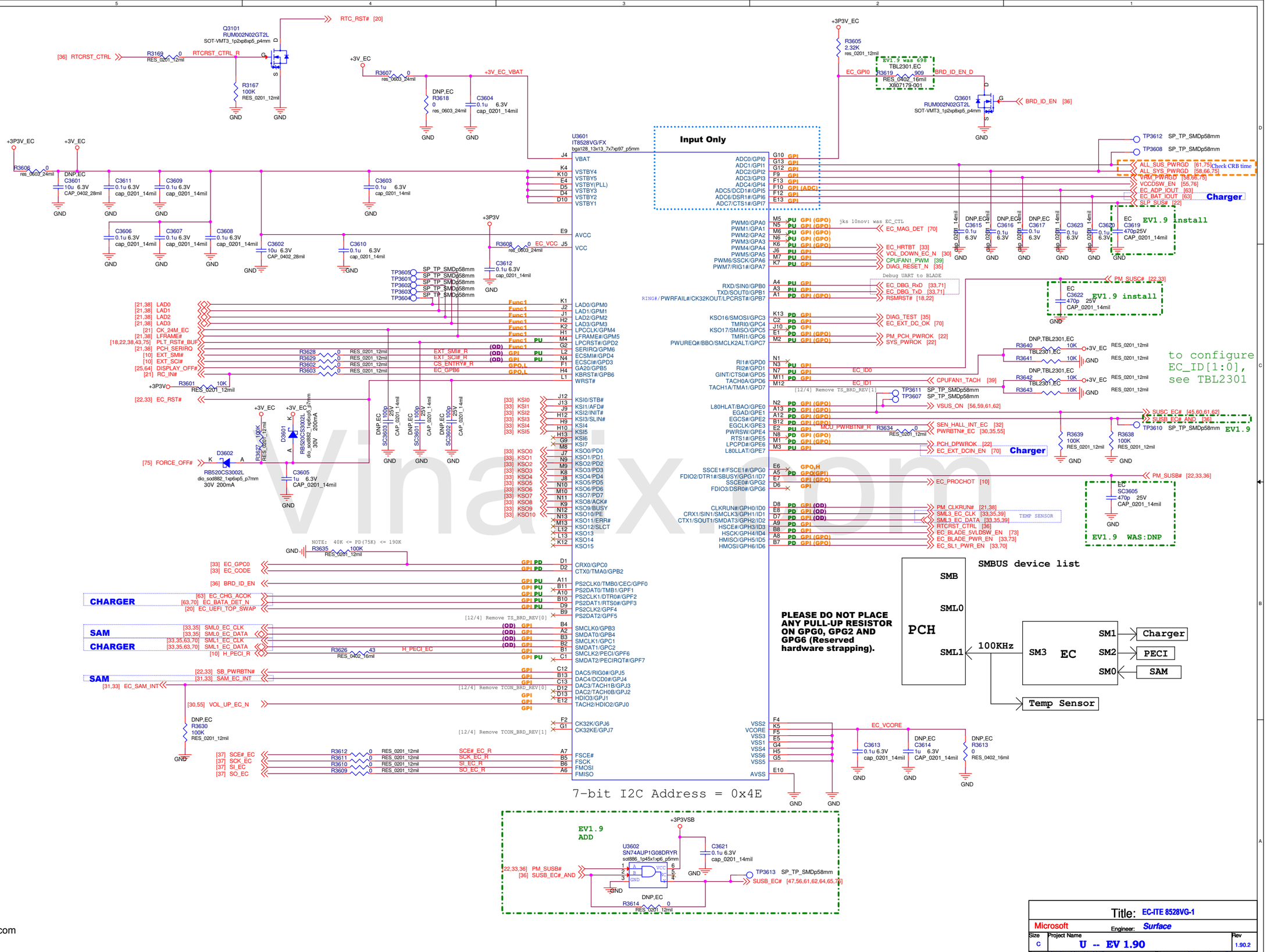






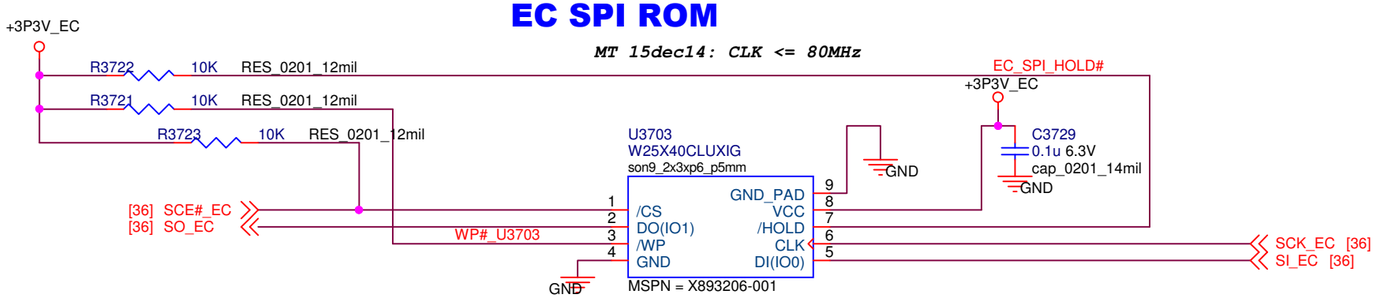
EC SM BUS Control 3

Title:	SM BUS/DIAG CONN	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 35 of 76	

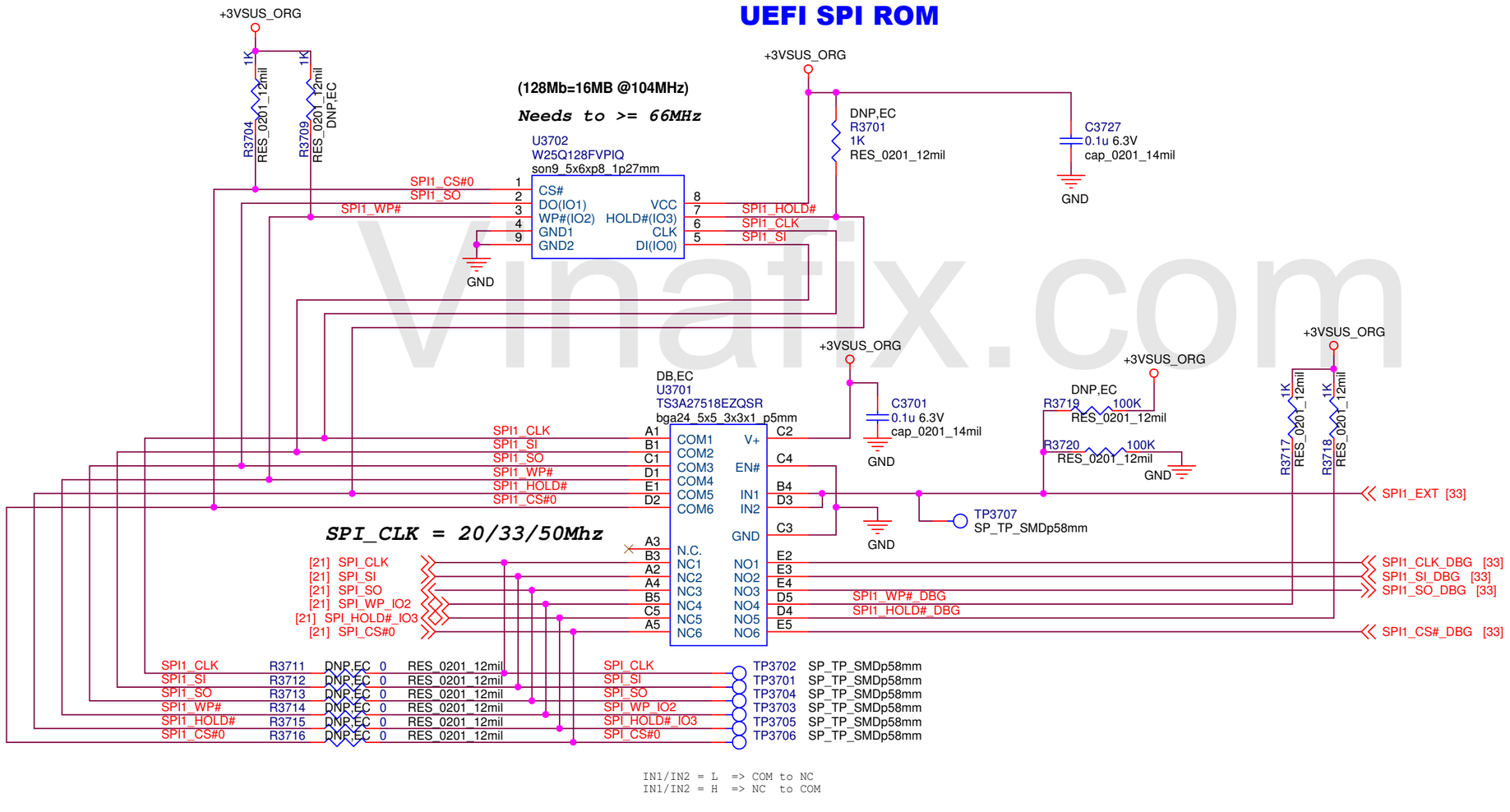

Q3101
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
RTC_RST# [20]
[36] RTCRST_CTRL
R3169 0 RES_0201_12mil
RTCRST_CTRL_R
R3167 100K RES_0201_12mil
GND
+3V_EC
R3607 0 res_0603_24mil
+3V_EC_VBAT
DNP,EC R3618 res_0603_24mil
C3604 0.1u 6.3V cap_0201_14mil
+3P3V_EC
R3606 0 res_0603_24mil
DNP,EC C3601 10u 6.3V CAP_0402_28mil
C3611 0.1u 6.3V cap_0201_14mil
C3609 0.1u 6.3V cap_0201_14mil
C3606 0.1u 6.3V cap_0201_14mil
C3607 0.1u 6.3V cap_0201_14mil
C3608 0.1u 6.3V cap_0201_14mil
C3602 10u 6.3V CAP_0402_28mil
C3610 0.1u 6.3V cap_0201_14mil
C3603 0.1u 6.3V cap_0201_14mil
U3601
IT8528VG/FX
bga128_13x13_7x7xp97_p5mm
VBAT
VSTBY4
VSTBY5
VSTBY(PLL)
VSTBY3
VSTBY2
VSTBY1
AVCC
VCC
+3P3V
R3608 0 res_0603_24mil EC_VCC
C3612 0.1u 6.3V cap_0201_14mil
TP3605 TP3601 TP3602 TP3603 TP3604 SP_TP_SMDp58mm
[21,38] LAD0
[21,38] LAD1
[21,38] LAD2
[21,38] LAD3
[21] CK_24M_EC
[21,38] LFRAME#
[18,22,38,43,75] PLT_RST#_BUF
[21,38] PCH_SERIRQ
[10] EXT_SMI#
[10] EXT_SCI#
[25,64] DISPLAY_OFF#
[21] RC_IN#
LAD0/GPM0
LAD1/GPM1
LAD2/GPM2
LAD3/GPM3
LPCCLK/GPM4
LFRAME#/GPM5
LPCRST#/GPD2
SERIRQ/GPM6
ECSMI#/GPD4
ECSCI#/GPD3
GA20/GPB5
KBRST#/GPB6
WRST#
+3P3VO
R3601 10K RES_0201_12mil
[22,33] EC_RST#
R3628 0 RES_0201_12mil EXT_SMI#_R
R3629 0 RES_0201_12mil EXT_SCI#_R
R3602 0 RES_0201_12mil CS_ENTRY#_R
R3603 0 RES_0201_12mil EC_GPB6
+3V_EC
D3601 RB520CS30V2L dio_sod882_1xp6xp5_p7mm 30V 200mA
R3627 100K RES_0201_12mil
D3602 RB520CS30V2L
C3605 1u 6.3V CAP_0201_14mil
[75] FORCE_OFF#
SC3603 SC3601 SC3602 100p 25V CAP_0201_14mil
[33] KSI0
[33] KSI1
[33] KSI2
[33] KSI3
[33] KSI4
[33] KSI5
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7
[33] KSO0
[33] KSO1
[33] KSO2
[33] KSO3
[33] KSO4
[33] KSO5
[33] KSO6
[33] KSO7
[33] KSO8
[33] KSO9
[33] KSO10
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
NOTE: 40K <= PD(75K) <= 190K
GND R3635 100K RES_0201_12mil
[33] EC_GPC0
[33] EC_CODE
CRX0/GPC0
CTX0/TMA0/GPB2
[36] BRD_ID_EN
CHARGER
[63] EC_CHG_ACOK
[63,70] EC_BATA_DET_N
[20] EC_UEFI_TOP_SWAP
PS2CLK0/TMB0/CEC/GPF0
PS2DAT0/TMB1/GPF1
PS2CLK1/DTR0#/GPF2
PS2DAT1/RTS0#/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5
SAM
CHARGER
[33,35] SML0_EC_CLK
[33,35] SML0_EC_DATA
[33,35,63,70] SML1_EC_CLK
[33,35,63,70] SML1_EC_DATA
[10] H_PECI_R
R3626 43 RES_0402_16mil H_PECI_EC
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/PECI/GPF6
SMDAT2/PECIRQT#/GPF7
[12/4] Remove TS_BRD_REV[0]
[12/4] Remove TCON_BRD_REV[0]
[12/4] Remove TCON_BRD_REV[1]
SAM
[22,33] SB_PWRBTN#
[31,33] SAM_EC_INT
[31,33] EC_SAM_INT
DAC5/RIG0#/GPJ5
DAC4/DCD0#/GPJ4
DAC3/TACH1B/GPJ3
DAC2/TACH0B/GPJ2
HDIO3/GPJ1
TACH2/HDIO2/GPJ0
[30,55] VOL_UP_EC_N
DNP,EC R3630 100K RES_0201_12mil
CK32K/GPJ6
CK32KE/GPJ7
[37] SCE#_EC
[37] SCK_EC
[37] SI_EC
[37] SO_EC
R3612 0 RES_0201_12mil SCE#_EC_R
R3611 0 RES_0201_12mil SCK_EC_R
R3610 0 RES_0201_12mil SI_EC_R
R3609 0 RES_0201_12mil SO_EC_R
FSCE#
FSCK
FMOSI
FMISO
7-bit I2C Address = 0x4E
Input Only
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/DCD1#/GPI5
ADC6/DSR1#/GPI6
ADC7/CTS1#/GPI7
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/SSCK/GPA6
PWM7/RIG1#/GPA7
RXD/SIN0/GPB0
TXD/SOUT0/GPB1
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
KSO16/SMOSI/GPC3
TMRI0/GPC4
KSO17/SMISO/GPC5
TMRI1/GPC6
PWUREQ#/BBO/SMCLK2ALT/GPC7
RI1#/GPD0
RI2#/GPD1
GINT/CTS0#/GPD5
TACH0A/GPD6
TACH1A/TMA1/GPD7
L80HLAT/BAO/GPE0
EGAD/GPE1
EGCS#/GPE2
EGCLK/GPE3
PWRSW/GPE4
RTS1#/GPE5
LPCPD#/GPE6
L80LLAT/GPE7
SSCE1#/FSCE1#/GPG0
FDIO2/DTR1#/SBUSY/GPG1/ID7
SSCE0#/GPG2
FDIO3/DSR0#/GPG6
CLKRUN#/GPH0/ID0
CRX1/SIN1/SMCLK3/GPH1/ID1
CTX1/SOUT1/SMDAT3/GPH2/ID2
HSCE#/GPH3/ID3
HSCK/GPH4/ID4
HMISO/GPH5/ID5
HMOSI/GPH6/ID6
VSS2
VCORE
VSS3
VSS1
VSS4
VSS6
VSS5
AVSS
+3P3V_EC
R3605 2.32K res_0201_12mil
EC_GPI0
EV1.9 was 698
TBL2301,EC R3619 909 RES_0402_16mil X807179-001
BRD_ID_EN_D
Q3601 RUM002N02GT2L SOT-VMT3_1p2xp8xp5_p4mm
BRD_ID_EN [36]
TP3612 TP3608 SP_TP_SMDp58mm
ALL_SUS_PWRGD [61,75] Check CRB time
ALL_SYS_PWRGD [58,66,75]
VRM_PWRGD [58,66,75]
VCCDSW_EN [55,76]
EC_ADP_IOUT [63]
EC_BAT_IOUT [63]
SLP_SUS# [22]
Charger
DNP,EC C3615 C3616 C3617 C3623 C3620 0.1u 6.3V cap_0201_14mil
EC C3619 470p25V CAP_0201_14mil
EV1.9 install
jks 10nov: was EC_CTL
EC_MAG_DET [70]
EC_HRTBT [33]
VOL_DOWN_EC_N [30]
CPUFAN1_PWM [39]
DIAG_RESET_N [35]
Debug UART to BLADE
EC_DBG_RxD [33,71]
EC_DBG_TxD [33,71]
RSMRST# [18,22]
PM_SUSC# [22,33]
EC C3622 470p 25V CAP_0201_14mil
EV1.9 install
DIAG_TEST [35]
EC_EXT_DC_OK [70]
PM_PCH_PWROK [22]
SYS_PWROK [22]
EC_ID0
EC_ID1
CPUFAN1_TACH [39]
DNP,TBL2301,EC R3640 R3641 R3642 R3643 10K
TBL2301,EC
+3V_EC
GND
RES_0201_12mil
to configure EC_ID[1:0], see TBL2301
TP3611 TP3607 SP_TP_SMDp58mm
VSUS_ON [56,59,61,62]
SUSC_EC# [45,60,61,62]
SUSB_EC# AND [36]
TP3610 SP_TP_SMDp58mm
EV1.9
MCU_PWRBTN#_R R3634 0 RES_0201_12mil
SEN_HALL_INT_EC [32]
PWRBTN#_EC [30,35,55]
PCH_DPWROK [22]
EC_EXT_DCIN_EN [70]
Charger
R3639 100K RES_0201_12mil
R3638 100K RES_0201_12mil
EC_PROCHOT [10]
PM_SUSB# [22,33,36]
EC SC3605 470p 25V CAP_0201_14mil
EV1.9 WAS:DNP
PM_CLKRUN# [21,38]
SML9_EC_CLK [33,35,39]
SML9_EC_DATA [33,35,39]
TEMP SENSOR
RTCRST_CTRL [36]
EC_BLADE_5VLDSW_EN [73]
EC_BLADE_PWR_EN [33,73]
EC_SL1_PWR_EN [33,70]
PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG0, GPG2 AND GPG6 (Reserved hardware strapping).
SMBUS device list
SMB
SML0
PCH
SML1
100KHz
SM3
EC
SM1
SM2
SM0
Charger
PECI
SAM
Temp Sensor
EC_VCORE
C3613 0.1u 6.3V cap_0201_14mil
DNP,EC C3614 1u 6.3V CAP_0201_14mil
DNP,EC R3613 0 RES_0402_16mil
EV1.9 ADD
+3P3VSB
U3602
SN74AUP1G08DRYR
sot886_1p45x1xp6_p5mm
C3621 0.1u 6.3V cap_0201_14mil
[22,33,36] PM_SUSB#
[36] SUSB_EC#_AND
TP3613 SP_TP_SMDp58mm
SUSB_EC# [47,56,61,62,64,65,75]
DNP,EC R3614 0 RES_0201_12mil
Title: EC-ITE 8528VG-1
Microsoft
Engineer: Surface
Size C
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 38 of 76

EC SPI ROM

MT 15dec14: CLK <= 80MHz

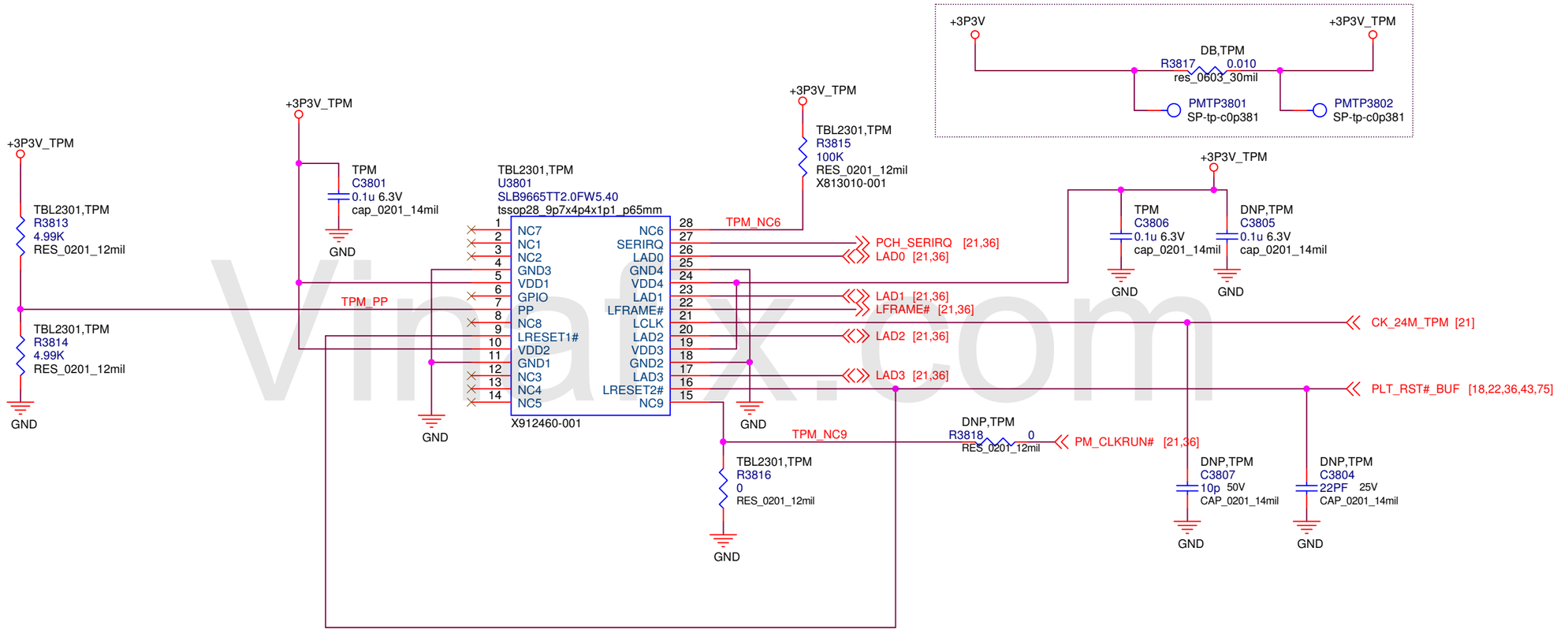


UEFI SPI ROM



Title:	EC-ITE 8528VG-2/SPI ROM		
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 37 of 76	

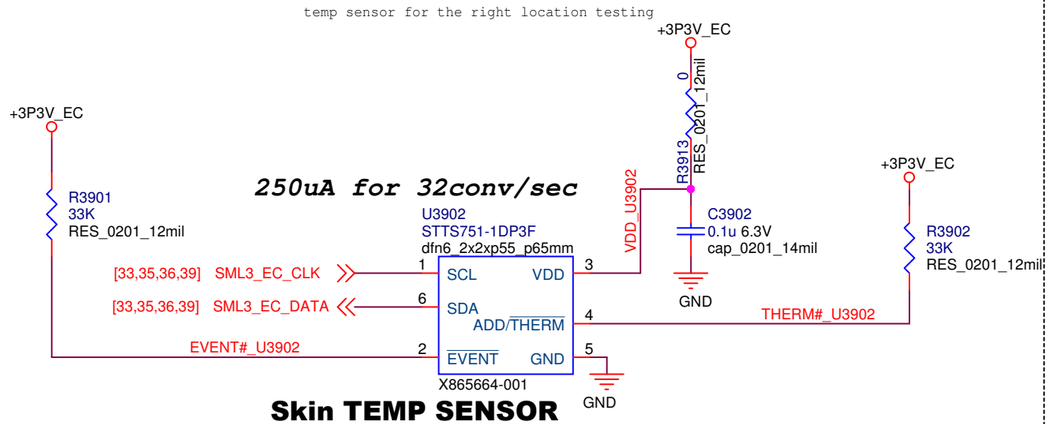
Trusted Platform Module

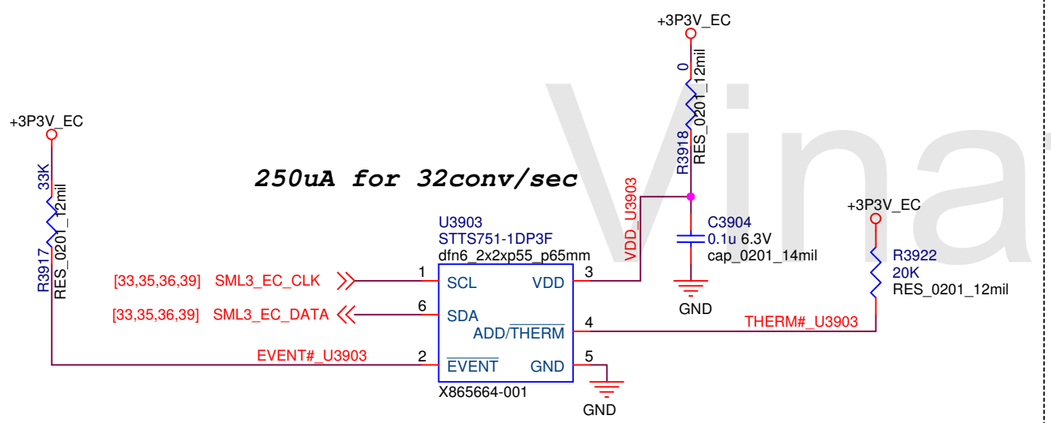


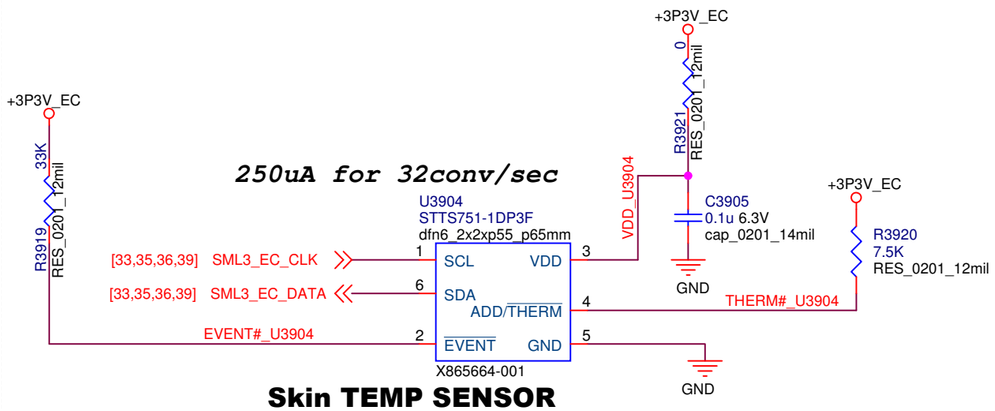
Title: TPM		
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 38 of 76	

jks 6dec14: Only one sensor will be used for final product

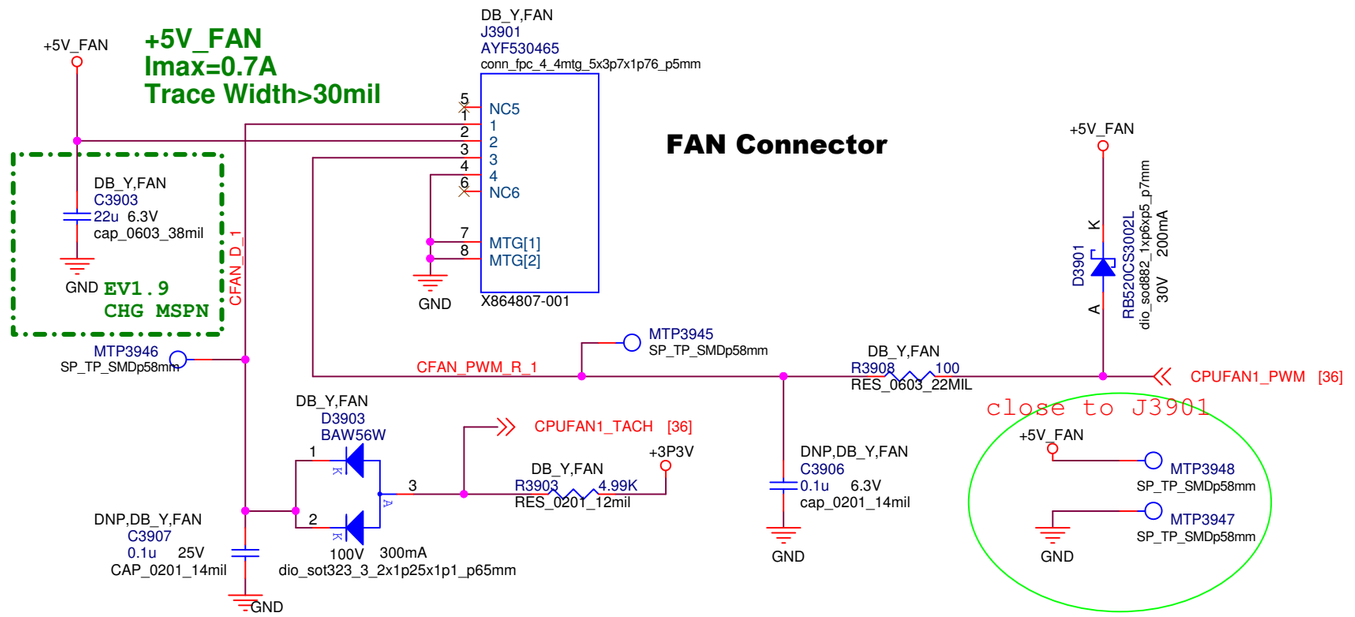
temp sensor for the right location testing

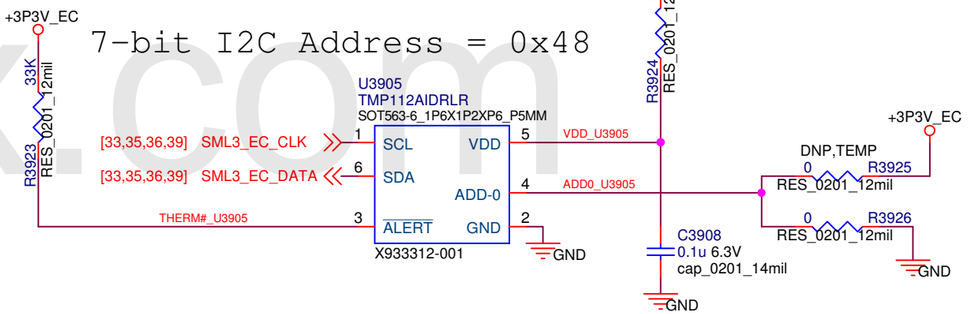


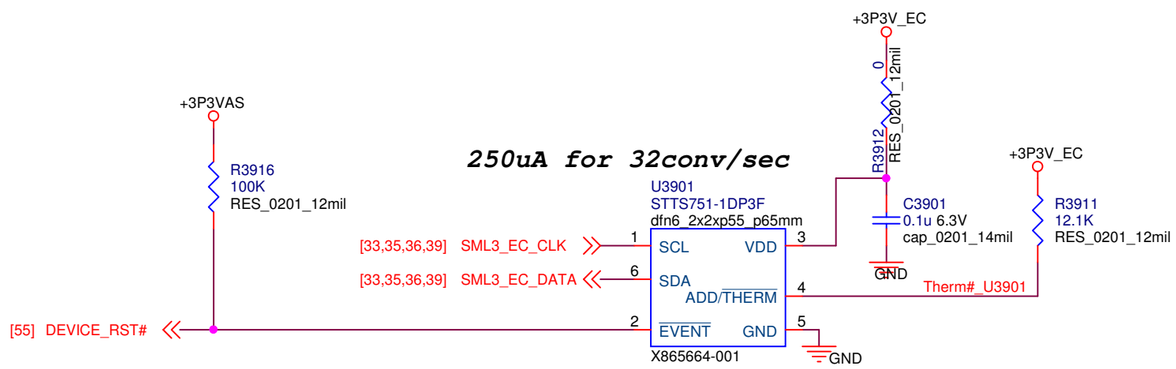




Vinafix.com







Title:	Temp Sensor/System Fan		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 39 of 76		

SPK Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

AUDIO_VREF
AC4019 2.2u CAP_0402_24mil 6.3V
AC4002 0.1u 6.3V cap_0201_14mil
AUDIO_VREF1
C4011 10u 6.3V CAP_0402_28mil
AC4010 0.1u 6.3V cap_0201_14mil
AGND

+5V_AUDIO
AR4034 0 res_0603_24mil
+5V_AUIDO_AVDD
C4010 10u 6.3V CAP_0402_28mil
AC4005 0.1u 6.3V cap_0201_14mil
L4010 600 OHM 2A ind_0805_44mil
+5V_AUIDO_PVDD
C4012 10u 10V cap_0603_36mil
AC4039 0.1u 6.3V cap_0201_14mil
C4014 10u 6.3V CAP_0402_28mil
AC4040 0.1u 6.3V cap_0201_14mil
GND

+1P8V_AUDIO
AR4014 0 res_0603_24mil
C4013 10u 6.3V CAP_0402_28mil
AC4021 0.1u 6.3V cap_0201_14mil
C4015 10u 6.3V CAP_0402_28mil
AC4041 0.1u 6.3V cap_0201_14mil
+1P8V_AUDIO_DVDD
EV1.9 WAS:10V

+1P8V_AUDIO
AR4008 10K RES_0201_12mil
CODEC_PD#_G
AR4007 10K RES_0201_12mil
Q4001 MMBT3904WT1G sot323_2x1p25x1p1_p65mm
[20,40] AZ_RST#_1
+1P8V_AUDIO
AR4018 100K RES_0201_12mil
[10] PCH_CODEC_IRQ

C4016 10u 6.3V CAP_0402_28mil
AC4003 0.1u 6.3V cap_0201_14mil
AC4014 2.2u 6.3V CAP_0402_22mil
AC4046 2.2u 6.3V CAP_0402_22mil
C4017 10u 6.3V CAP_0402_28mil
AGND

EV1.9 WAS:10V
AC4017 2.2u 6.3V CAP_0402_22mil
AC4018 2.2u 6.3V CAP_0402_22mil

DNP,AUDIO
AR4002 0 RES_0201_12mil
AR4001 0 RES_0201_12mil
GND AGND

TP4031 SP_TP_SMDp58mm
AGND
close to audio

U4009
ALC3269-CG
qfn57_7x7xp9_p4mm

43	VREF	
21	VREF1	
45	AVDD1	
23	PCBEEP	
46	PVDD1	
51	PVDD2	
7	DVDD	
19	DVDD_IO	
24	CPVDD/AVDD2	
31	CPVEE	CPVEE
29	CPVPP	CPVPP
30	CPVREF	
53	DMIC_CLK	[20,32,42] DMIC1_CLK
54	DMIC_DATA1	[20,32,42] DMIC1_DATA
41	MIC1_CAP	ALC298_MIC1_CAP
52	EAPD+PD#/GPIO11	CODEC_PD#
6	HD_I2S_SEL/IRQOUT/GPIO0	
5	I2S_IN/GPIO5	was I2S_IN (DSP)
3	I2S_OUT/GPIO6	was I2S_OUT (DSP)
56	I2S_BCLK/GPIO7	was I2S_BCLK (DSP)
55	I2S_MCLK/SPDIF_IN/GPIO8	was AUD_RESET (DSP)
1	I2S_LRCK/GPIO9	was I2S_LCLK (DSP)
2	GPIO1/DMIC_CLK2/SPDIF_OUT/I2S_IN_JD	
4	GPIO2/DMIC_DATA2/I2S_OUT_JD	
28	CBN1	CODEC_CBN1_R
25	CNB2	
27	CBP1	CODEC_CBP1_R
26	CBP2	CODEC_CBN2_R / CODEC_CBP2_R

TP4001 TP4002 SP_TP_SMDp58mm SP_TP_SMDp58mm

13	HDA_BCLK/I2S_BCLK	AZ_BITCLK_1 [20]
15	HDA_RESETB/I2S_MCLK	AZ_RST#_1 [20,40]
16	HDA_SDATA_IN/I2S_SDO	SDATA_IN_R → AR4004 33 RES_0201_12mil; AZ_SDATA_IN0 [20]
17	HDA_SDATA_OUT/I2S_SDI	AZ_SDATA_OUT_1 [20]
14	HAD_SYNC/I2S_LRCK	AZ_SYNC_1 [20]
9	HP_JD/LINE1_JD	HPOUT_JD_R
32	HP_OUT_L	HPOUT_L [41]
33	HP_OUT_R	HPOUT_R [41]
12	I2C_CLK	
11	I2C_DATA	
8	I2S_OUT_JD/MIC_JD	COMBO_JACK [41]
44	LDO1_CAP	CODEC_LDO1
22	LDO2_CAP	CODEC_LDO2
18	LDO3_CAP	CODEC_LDO3
35	LINE1_L	DSP
34	LINE1_R	DSP
40	LINE1_VREFO	
36	MIC1_L/RING2	MIC1_L [41]
37	MIC1_R/SLEEVE	MIC1_R [41]
38	MIC1_VREFO_L/AGPO_0	MIC1_VREFO_L [41]
39	MIC1_VREFO_R/AGPO_1	
48	SPK_OUT_LN	SPK_L- [41]
47	SPK_OUT_LP	SPK_L+ [41]
49	SPK_OUT_RN	SPK_R- [41]
50	SPK_OUT_RP	SPK_R+ [41]
42	AVSS1	
20	AVSS2	
10	VD33STB	ALC298_VD22STB
57	E_PAD	

+1P8V_AUDIO
AR4019 100K RES_0201_12mil
HPOUT_JD_R
AR4006 200K RES_0201_12mil HPOUT_JD [41]
DNP,AUDIO AR4033 100K RES_0201_12mil
DNP,AUDIO AC4038 0.1u 6.3V cap_0201_14mil
DNP,AUDIO AC4012 22PF 25V CAP_0201_14mil
DNP,AUDIO AC4011 22PF 25V CAP_0201_14mil
GND AGND

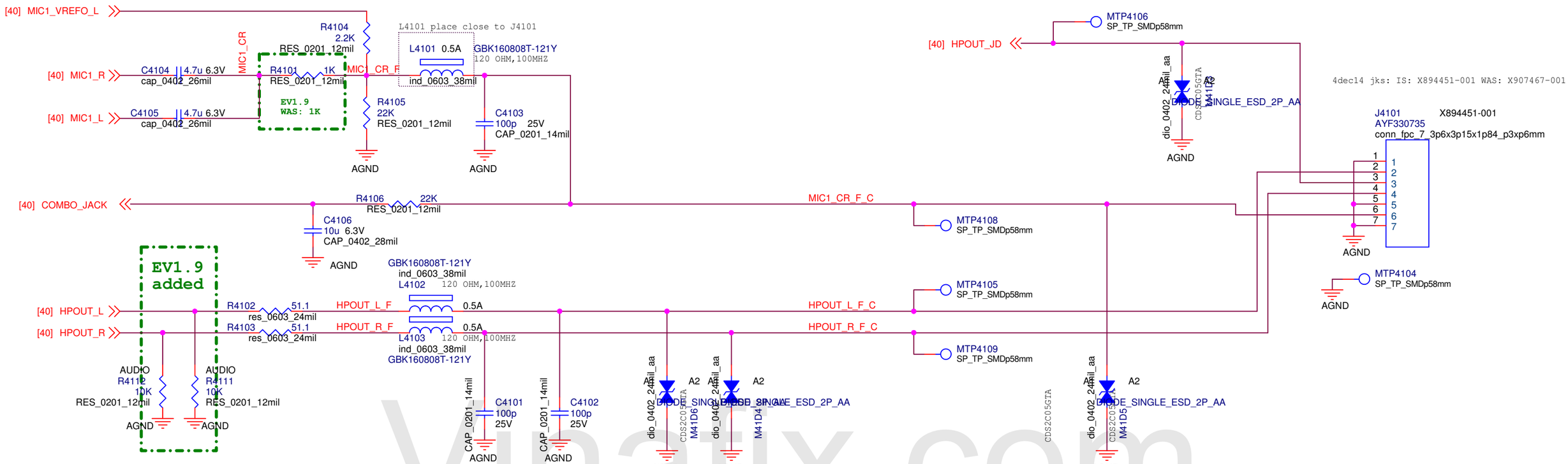
+5V_AUDIO
AR4035 10K RES_0201_12mil
DNP,AUDIO AR4036 100K RES_0201_12mil
GND AGND

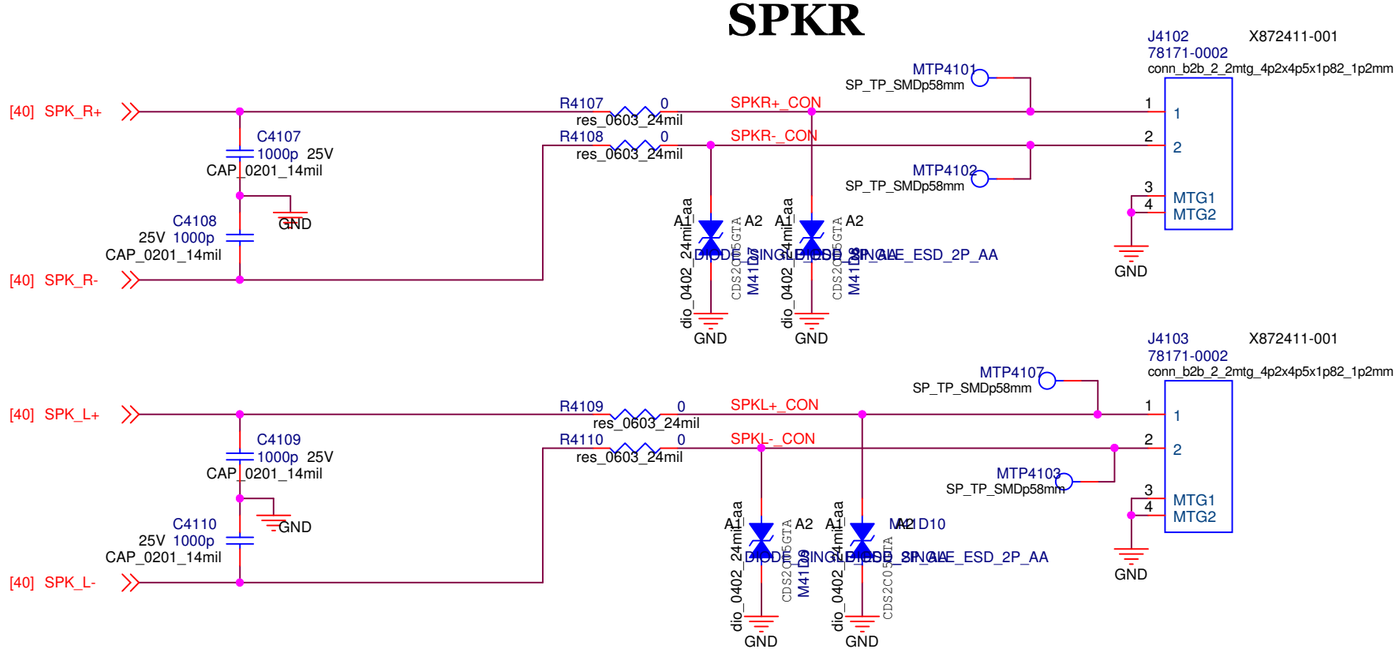
AC4023 0.1u 6.3V cap_0201_14mil
AC4016 10u 6.3V CAP_0402_28mil
AC4024 0.1u 6.3V cap_0201_14mil
AC4025 10u 6.3V CAP_0402_28mil
AC4026 0.1u 6.3V cap_0201_14mil
AC4027 10u 6.3V CAP_0402_28mil
GND AGND

Vinafix.com

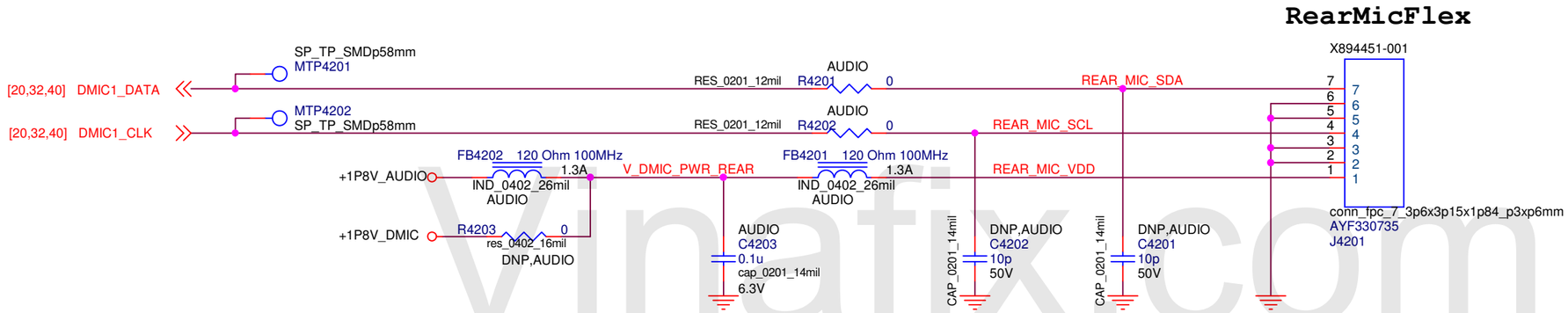
Title: REALTEK ALC3269 CODEC
Microsoft Engineer: Surface
Size A3 | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 | Sheet 40 of 76

Audio Jack/MIC1 Combo Jack





Title:	Audio Jack/Speaker	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 41 of 76	



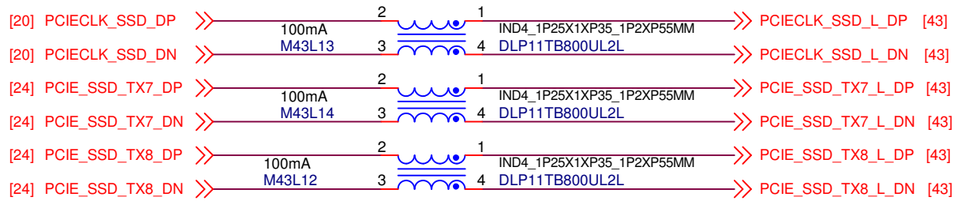
Vinafix.com

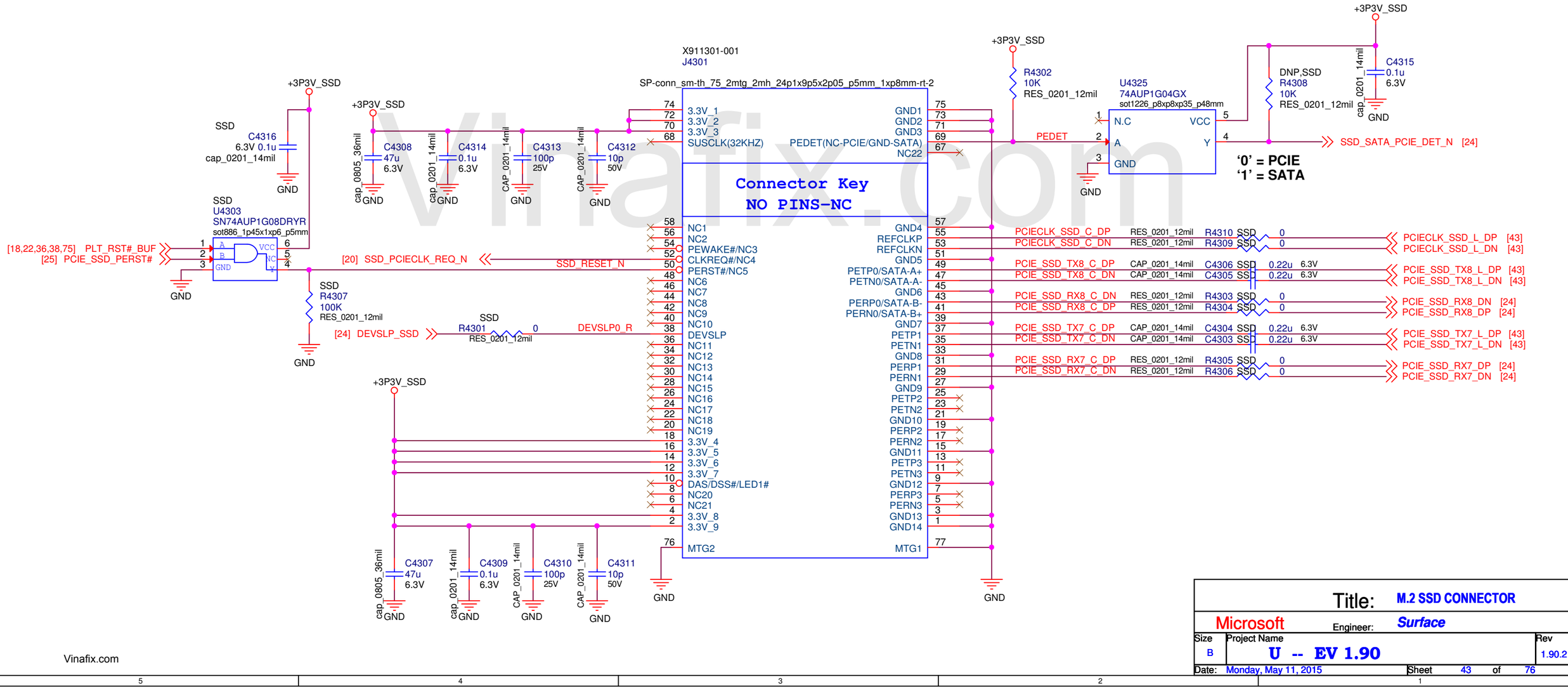
Title: Microphones			
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 42 of 76		

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen2/SATA	PCI Express* Gen3/SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF [2]	None	None [3]

2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.

3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.

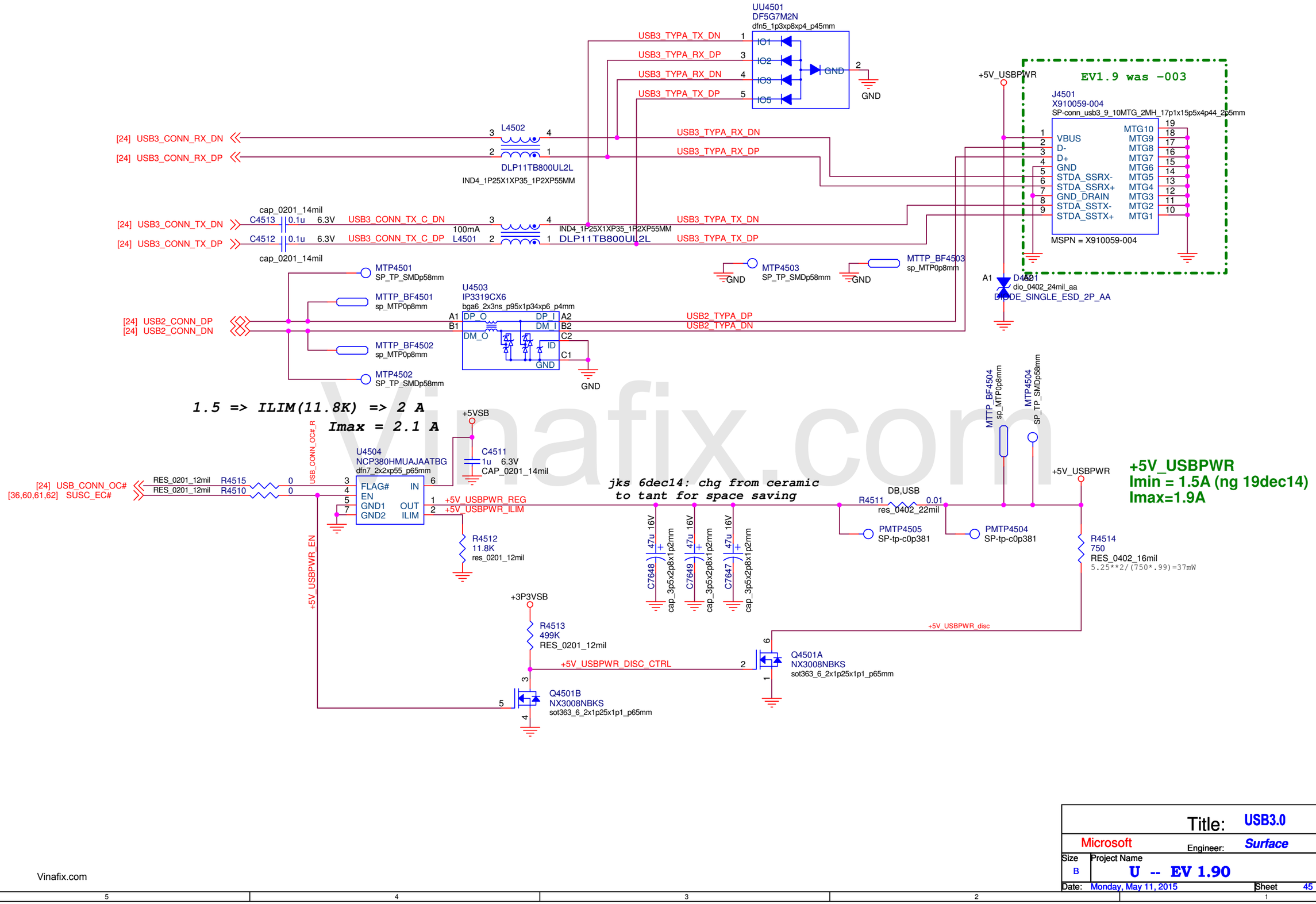




Vinafix.com

Title:	M.2 SSD CONNECTOR		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 43 of 76		

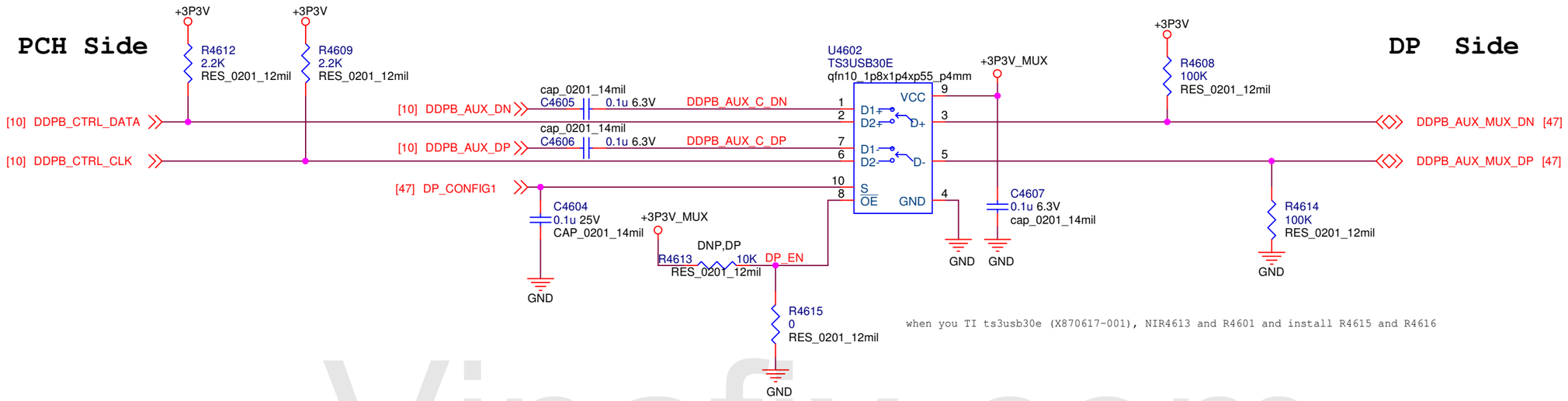
Title:	Empty	
Microsoft	Engineer:	*Surface*
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 44 of 76	



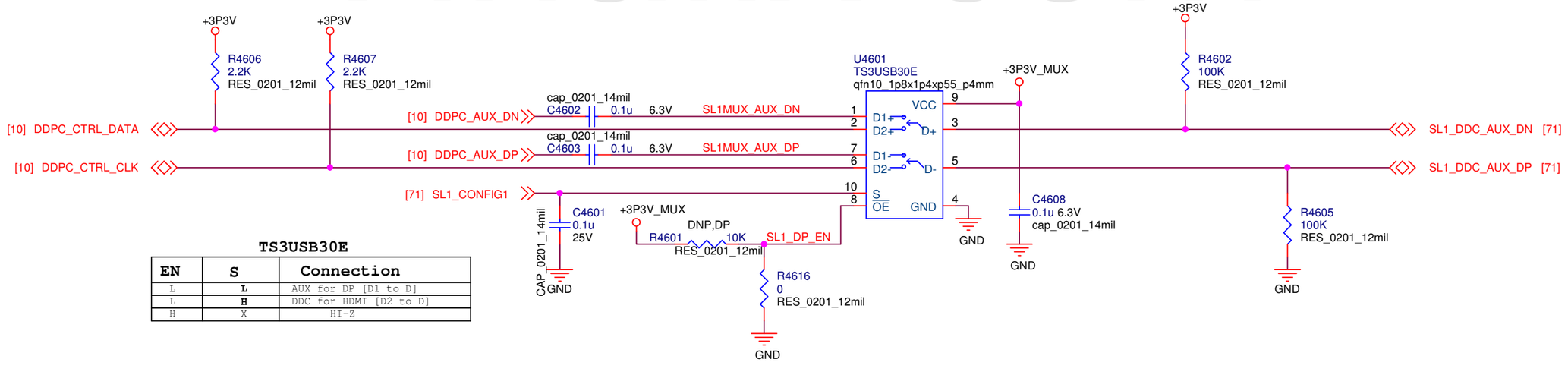
Vinafix.com

Title:	USB3.0	
Microsoft	Engineer:	Surface
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 45 of 76	

mDP mux to HDMI/DVI Dongle control



SL1 DP mux to HDMI/DVI Dongle control



TS3USB30E

EN	S	Connection
L	L	AUX for DP [D1 to D]
L	H	DDC for HDMI [D2 to D]
H	X	HI-Z

Title:	DP Dongle Control	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 46 of 76	

NOTE:
Pass gate to prevent back-drive when sink device is on and PCH is powered down.

NOTE:
Place D4701 near to DP connector

NOTE:
Place those AC Caps near to DP connector.

EV1.9 was -003

+3P3V
mDP conn
Imax = 0.5A

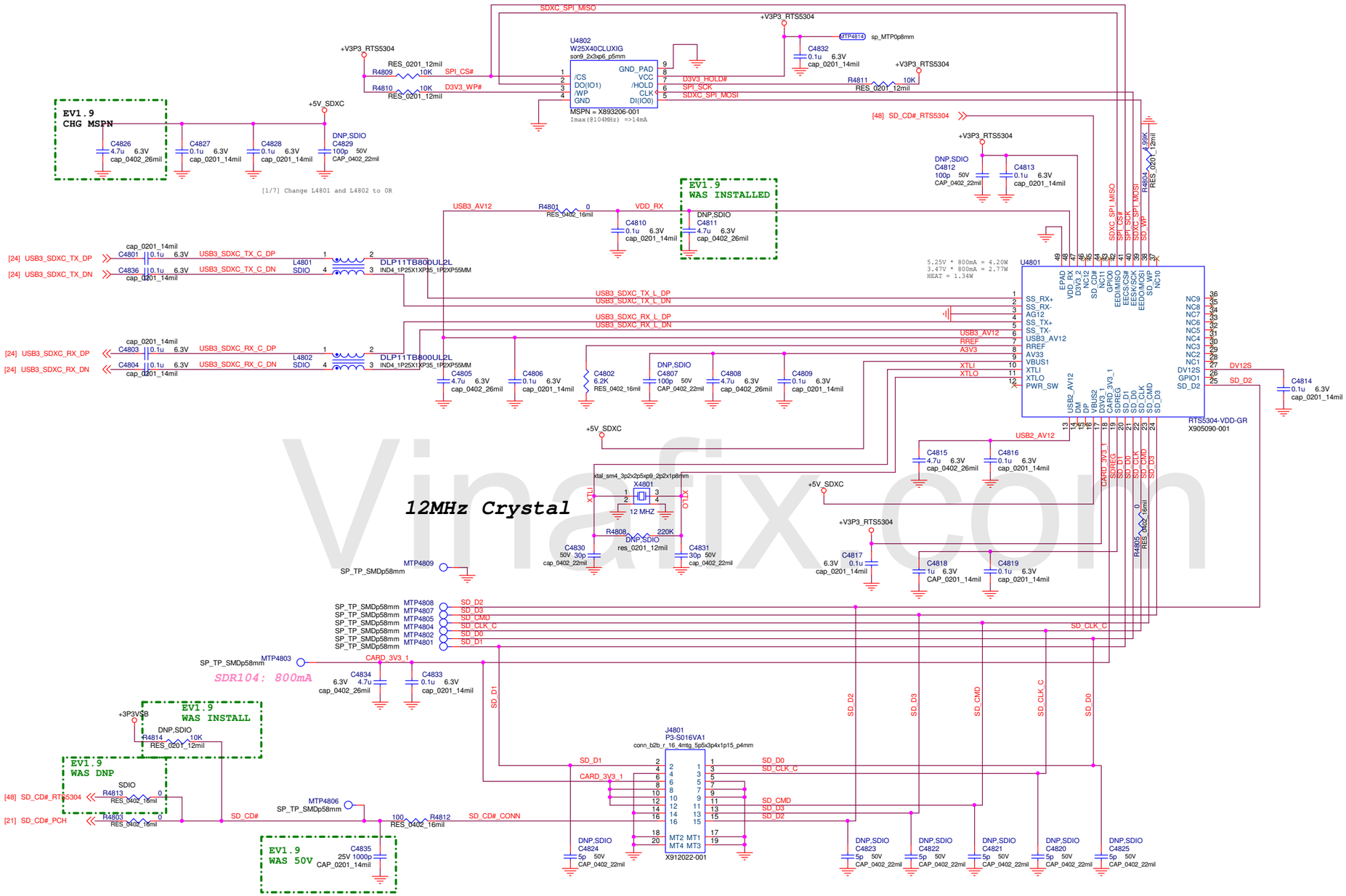
EV1.9 WAS:+3P3V

ILIM(33K) ~ 0.8A
meet VESA spec

EV1.9
was:16V

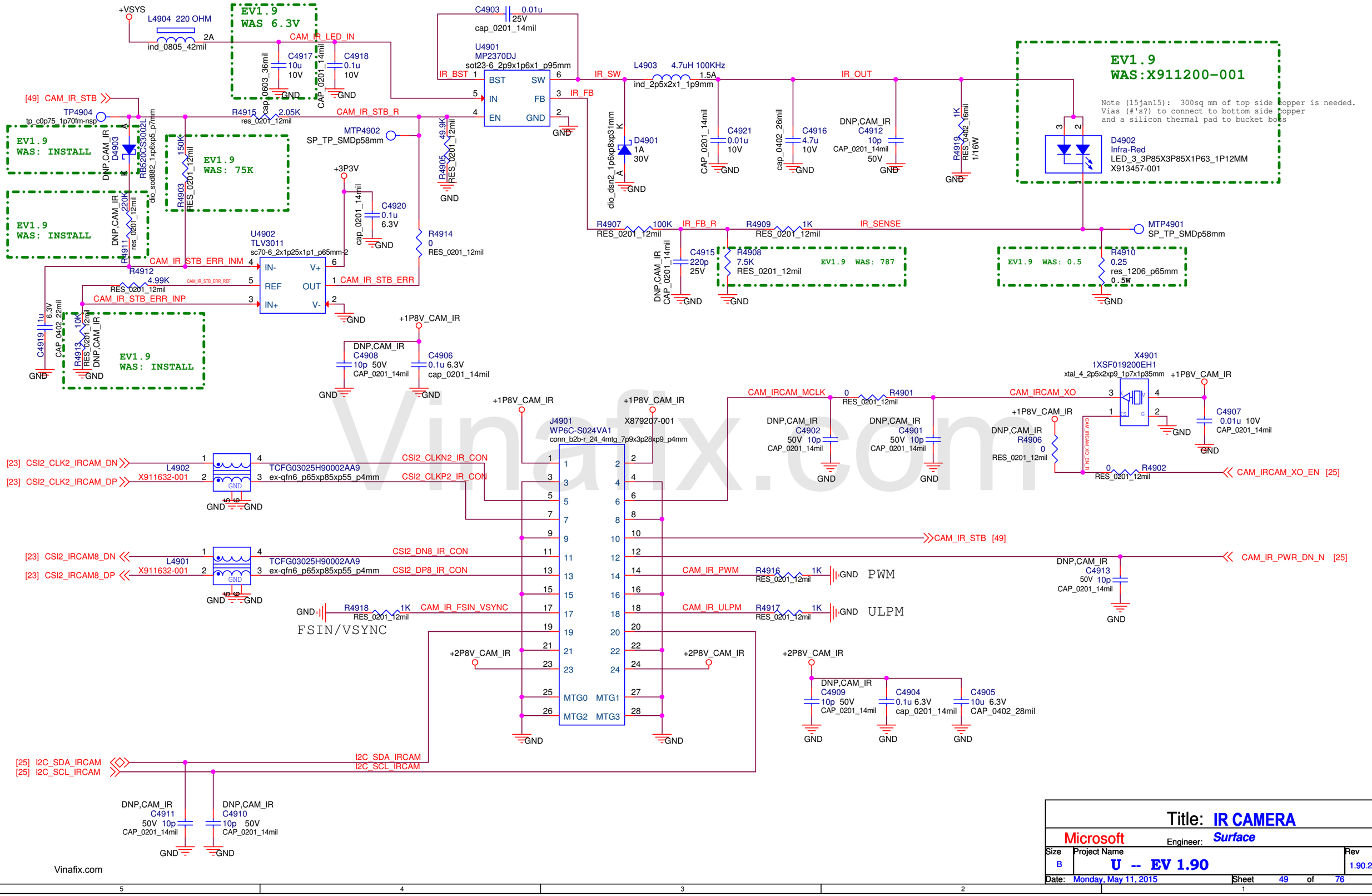
MSPN = X909561-004

Title:	mDP		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 47 of 76		



Vinafix.com

Title: SDXC			
Microsoft	Engineer: Surface		
Size: C	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 48 of 76	


+VSYS
L4904 220 OHM
2A
ind_0805_42mil
EV1.9
WAS 6.3V
CAM_IR_LED_IN
C4917
10u
10V
cap_0603_36mil
C4918
0.1u
10V
CAP_0201_14mil
GND
C4903
0.01u
25V
cap_0201_14mil
U4901
MP2370DJ
sot23-6_2p9x1p6x1_p95mm
IR_BST
BST
SW
IN
FB
EN
GND
IR_SW
IR_FB
L4903
4.7uH 100KHz
1.5A
ind_2p5x2x1_1p9mm
IR_OUT
[49] CAM_IR_STB
TP4904
tp_c0p75_1p70fm-nsp
R4915
2.05K
res_0201_12mil
CAM_IR_STB_R
MTP4902
SP_TP_SMDp58mm
49.9K
RES_0201_12mil
R4905
D4901
1A
30V
dio_dsn2_1p6xp8xp31mm
C4921
0.01u
10V
CAP_0201_14mil
C4916
4.7u
10V
cap_0402_26mil
DNP,CAM_IR
C4912
10p
50V
CAP_0201_14mil
R4919
1K
RES_0402_6mil
1/16W
EV1.9
WAS:X911200-001
Note (15jan15): 300sq mm of top side copper is needed.
Vias (#'s?) to connect to bottom side copper
and a silicon thermal pad to bucket boss
D4902
Infra-Red
LED_3_3P85X3P85X1P63_1P12MM
X913457-001
EV1.9
WAS: INSTALL
DNP,CAM_IR
D4903
RB520CS3002L
dio_sod882_1xp6xp5_p7mm
EV1.9
WAS: 75K
150K
RES_0201_12mil
R4903
+3P3V
C4920
0.1u
6.3V
cap_0201_14mil
EV1.9
WAS: INSTALL
DNP,CAM_IR
R4911
220K
res_0201_12mil
U4902
TLV3011
sc70-6_2x1p25x1p1_p65mm-2
R4914
0
RES_0201_12mil
R4907
100K
RES_0201_12mil
IR_FB_R
R4909
1K
RES_0201_12mil
IR_SENSE
MTP4901
SP_TP_SMDp58mm
CAM_IR_STB_ERR_INM
IN-
V+
REF
OUT
IN+
V-
CAM_IR_STB_ERR
R4912
4.99K
RES_0201_12mil
CAM_IR_STB_ERR_REF
CAM_IR_STB_ERR_INP
C4915
220p
25V
DNP,CAM_IR
CAP_0201_14mil
R4908
7.5K
RES_0201_12mil
EV1.9 WAS: 787
EV1.9 WAS: 0.5
R4910
0.25
res_1206_p65mm
0.5W
C4919
1u
6.3V
CAP_0402_22mil
R4913
10K
RES_0201_12mil
DNP,CAM_IR
EV1.9
WAS: INSTALL
+1P8V_CAM_IR
DNP,CAM_IR
C4908
10p 50V
CAP_0201_14mil
C4906
0.1u 6.3V
cap_0201_14mil
X4901
1XSF019200EH1
xtal_4_2p5x2xp9_1p7x1p35mm
CAM_IRCAM_MCLK
0
R4901
RES_0201_12mil
CAM_IRCAM_XO
C4907
0.01u 10V
CAP_0201_14mil
DNP,CAM_IR
C4902
50V 10p
CAP_0201_14mil
DNP,CAM_IR
C4901
50V 10p
CAP_0201_14mil
DNP,CAM_IR
R4906
0
RES_0201_12mil
CAM_IRCAM_XO_EN
R4902
RES_0201_12mil
CAM_IRCAM_XO_EN [25]
J4901
WP6C-S024VA1
conn_b2b-r_24_4mtg_7p9x3p28xp9_p4mm
X879207-001
[23] CSI2_CLK2_IRCAM_DN
[23] CSI2_CLK2_IRCAM_DP
L4902
X911632-001
TCFG03025H90002AA9
ex-qfn6_p65xp85xp55_p4mm
CSI2_CLKN2_IR_CON
CSI2_CLKP2_IR_CON
[23] CSI2_IRCAM8_DN
[23] CSI2_IRCAM8_DP
L4901
X911632-001
TCFG03025H90002AA9
ex-qfn6_p65xp85xp55_p4mm
CSI2_DN8_IR_CON
CSI2_DP8_IR_CON
CAM_IR_STB [49]
CAM_IR_PWR_DN_N [25]
DNP,CAM_IR
C4913
50V 10p
CAP_0201_14mil
CAM_IR_PWM
R4916
1K
RES_0201_12mil
PWM
CAM_IR_ULPM
R4917
1K
RES_0201_12mil
ULPM
GND
R4918
1K
RES_0201_12mil
CAM_IR_FSIN_VSYNC
FSIN/VSYNC
+2P8V_CAM_IR
MTG0
MTG1
MTG2
MTG3
C4909
10p 50V
CAP_0201_14mil
C4904
0.1u 6.3V
cap_0201_14mil
C4905
10u 6.3V
CAP_0402_28mil
[25] I2C_SDA_IRCAM
[25] I2C_SCL_IRCAM
I2C_SDA_IRCAM
I2C_SCL_IRCAM
DNP,CAM_IR
C4911
50V 10p
CAP_0201_14mil
DNP,CAM_IR
C4910
10p 50V
CAP_0201_14mil
Vinafix.com
Title: IR CAMERA
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
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+1P8V_INT_OUT
VDD1V8_RF_K9
C5011 1u 6.3V CAP_0201_14mil
C5001 3.3p 25V cap_0201_14mil
GND
VDD1V8_RF_K3
C5012 1u 6.3V CAP_0201_14mil
C5002 100p 25V CAP_0201_14mil
VDD1V8_RF_J1
C5003 100p 25V CAP_0201_14mil
VDD1V8_RF_H1
C5005 100p 25V CAP_0201_14mil
VDD1V8_RF_G9
C5013 1u 6.3V CAP_0201_14mil
VDD1V8_RF_F1
C5004 0.1u 6.3V cap_0201_14mil
VDD1V8_RF_M14
C5044 2.2u 6.3V CAP_0402_24mil
C5006 100p 25V CAP_0201_14mil
VDD1V8_RF_NFC_E14
C5038 0.1u 6.3V cap_0201_14mil

+1P8V_INT_OUT
VDD1V8_RF_H16
C5007 100p 25V CAP_0201_14mil
VDD1V8_RF_K16
C5008 100p 25V CAP_0201_14mil
VDD1V8_RF_G16
C5009 100p 25V CAP_0201_14mil
VDD1V8_RF_D2
C5010 100p 25V CAP_0201_14mil
VDD1V8_RF_C1
C5052 100p 25V CAP_0201_14mil
VDD1V8_RF_PCIE_HSIC_A10
C5053 1u 6.3V CAP_0201_14mil
C5054 10p 50V CAP_0201_14mil

+3P3V_RADIO
VDD3V3_RF_M3
C5036 10u 6.3V cap_0603_38mil
C5014 100p 25V CAP_0201_14mil
C5079 3.3p 25V cap_0201_14mil
VDD3V3_RF_M9
C5016 10u 6.3V cap_0603_38mil
C5015 100p 25V CAP_0201_14mil
C5078 3.3p 25V cap_0201_14mil
VDD3V3_RF_B1
C5035 1u 6.3V CAP_0201_14mil
C5034 0.1u 6.3V cap_0201_14mil
VIO_RF_L12
C5017 0.1u 6.3V cap_0201_14mil

+1P8V_INT_OUT
U5001A
88W8897-XX-CBK2
bga150_16x12_7p354x5p4xp545_p45mm
AVDD18_1 AVDD18_10 AVDD18_11 AVDD18_12 AVDD18_13 AVDD18_14 AVDD18_2 AVDD18_3 AVDD18_4 AVDD18_5 AVDD18_6 AVDD18_7 AVDD18_8 AVDD18_9 AVDD33_1 AVDD33_2 AVDD33_3 AVDD33_4
AVSS1 AVSS10 AVSS11 AVSS12 AVSS13 AVSS14 AVSS15 AVSS16 AVSS17 AVSS18 AVSS19 AVSS2 AVSS20 AVSS21 AVSS22 AVSS23 AVSS3 AVSS4 AVSS5 AVSS6 AVSS7 AVSS8 AVSS9
GPIO[0] GPIO[1] GPIO[2] GPIO[3] GPIO[4] GPIO[5] GPIO[6] GPIO[7] GPIO[8]/LED_OUT_WLAN GPIO[9]/LED_OUT_BT GPIO[10]/SER_WB GPIO[11]/LED_OUT_NFC GPIO[12]/PCIE_PERSTn GPIO[13]/PCIE_W_DISABLE GPIO[14] GPIO[15] GPIO[16] GPIO[17] GPIO[18] GPIO[19] GPIO[20] GPIO[21] GPIO[22] GPIO[23] GPIO[24]
CONFIG_HOST[0] CONFIG_HOST[1] CONFIG_HOST[2] CONFIG_HOST[3]
BRF_ANT
BUCK11_SENSE BUCK11_VOUT
BUCK18_SENSE BUCK18_VOUT
C3 WIFI_GPIO0 TP5020 SP_TP_SMDp58mm
D5 WIFI_GPIO1 TP5025 SP_TP_SMDp58mm
B2 WIFI_GPIO2 TP5026 SP_TP_SMDp58mm
PCIE_W_PERST_N
PCIE_W_DISABLE
WF_CNFG_HST0 WF_CNFG_HST1 WF_CNFG_HST2 WF_CNFG_HST3
TP5009 TP5010 TP5011 TP5012 SP_TP_SMDp58mm
M15 BRF_ANT_M15 [50]
A15 WF_BUCK11_VOUT L5001 1.67A ind_2p5x2x1p2_2p4mm 2.2uH
B16 WF_BUCK18_VOUT L5002 2.2uH 1.67A ind_2p5x2x1p2_2p4mm
C5020 10u 6.3V cap_0603_38mil
C5043 0.1u 6.3V cap_0201_14mil

+3P3V_RADIO
TP5007 SP_TP_SMDp58mm VDD3V3_RF_D16
C5018 6.3V 0.1u cap_0201_14mil

EV1.9 RM TP5021
EV1.9 WAS INSTALL DNP,WF
C5075 0.1u 6.3V cap_0201_14mil

EV1.9 RM TP5022
R5043 DNP,WF 49.9K RES_0201_12mil
R5042 49.9K RES_0201_12mil
R5041 49.9K RES_0201_12mil
R5040 49.9K RES_0201_12mil
R5039 49.9K RES_0201_12mil
R5038 DNP,WF 49.9K RES_0201_12mil
R5037 DNP,WF 49.9K RES_0201_12mil
R5036 DNP,WF 49.9K RES_0201_12mil

PCIE_W_PERST_N 0 R5070 RES_0201_12mil PCIE_WIFI_PERST_N [25]
PCIE_W_DISABLE 0 R5064 RES_0201_12mil PCIE_WIFI_DISABLE_N [25]

+1P1V_INT 1.1V +1P1V_INT_OUT
R5015 0 RES_0201_12mil
+1P8V_INT 1.8V +1P8V_INT_OUT
R5016 0 RES_0201_12mil

+1P1V_INT
C5042 0.1u 6.3V cap_0201_14mil
+3P3V_WWAN
R5048 0 RES_0402_16mil
+3P3V_WWAN_ALT
L5007 FERRITE 2.2A ind_0402_22mil 30 Ohm
C5040 0.1u 6.3V cap_0201_14mil
+3P3V_RADIO
C5041 10u 6.3V cap_0603_38mil
C5037 0.1u 6.3V cap_0201_14mil
C5046 10p 50V CAP_0201_14mil

WIFI_TCK [33] WIFI_TDI [33] WIFI_TDO [33] WIFI_TMS [33]
TP5001 SP_TP_SMDp58mm
TP5002 TP5004 SP_TP_SMDp58mm
TP5003 SP_TP_SMDp58mm
PLACE TP's on BOTTOM,

OPTION HOST VIO
+1P8V_INT_OUT +3P3V_RADIO
DNP,WF R5014 0 RES_0201_12mil
R5073 0 RES_0201_12mil
[50] VIO
VIO
C5025 0.1u 6.3V cap_0201_14mil

U5001B
88W8897-XX-CBK2
bga150_16x12_7p354x5p4xp545_p45mm
HSIC_DATA HSIC_STROBE NFC_ANT_N NFC_ANT_P NFC_SWP1_IO NFC_SWP1_VDDIN NFC_SWP1_VDDOUT NFC_SWP2_IO NFC_SWP2_VDDOUT18 NFC_TWSI_SCK NFC_TWSI_SDA NFC_VDDANT NFC_WI_IN
PCIE_CLKREQn PCIE_RCLK_N PCIE_RCLK_P PCIE_RX_N PCIE_RX_P PCIE_TX_N PCIE_TX_P PCIE_WAKEn PDn
RES1 RES10 RES11 RES12 RES13 RES2 RES3 RES4 RES5 RES6 RES7 RES8 RES9
RF_CNTL0_N RF_CNTL1_P RF_TR_2_A RF_TR_2_B RF_TR_5_A RF_TR_5_B
SD_CLK SD_CMD
TCK TDI TDO TMS
USB_DMNS USB_DPLS
VBAT_IN VBLDO33_CNTL VBLDO33_SENSE
VDD11 VDD12
VIO VIO_RF VIO_SD
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8
XTAL_IN XTAL_OUT SLP_CLK_IN SER_DAT SER_CSn SER_CLK SD_DAT[0] SD_DAT[1] SD_DAT[2] SD_DAT[3]

GND C5048 0.1u 6.3V cap_0201_14mil NFC_SWP1_VDDIN

EV1.9 WAS:DNP R5047 WF 49.9K RES_0201_12mil +3P3V_RADIO
R5046 DNP,WF 49.9K RES_0201_12mil GND
EV1.9 RM TP5005,TP5006
D11 USB_DMNS C11 USB_DPLS
R5008 0 R5009 0 RES_0201_12mil
BT -> USB2.0(5)
USB2_BT_DN [24] USB2_BT_DP [24]
wf_vbat_in_sys
+3P3V_RADIO R5017 0 RES_0201_12mil
+1P1V_INT_OUT
C5021 1u 6.3V cap_0201_14mil
C5022 10u 6.3V cap_0603_38mil
GND
B15 F7 F6 A7 B10 A2 L12 A12 A6 A9 A11 A14 B1 C14 C16 D1 E1 E2 A4 E3 F5 D3 D12 C13 B13 A13 B12 C12
VDD11 VDD12_B1 C5039 0.1u 6.3V cap_0201_14mil
VIO [50] +3P3V_RADIO
C5024 0.1u 6.3V cap_0201_14mil
REF_CLK_IN REF_CLK_OUT
EV1.9 RM R5001
TP5034 SP_TP_SMDp58mm
WIFI_32K_CLK [20]
SER_DAT SER_CSn SER_CLK
EV1.9 WAS:DNP R5045 WF 49.9K RES_0201_12mil
R5044 DNP,WF 49.9K RES_0201_12mil
+1P8V_INT_OUT
xtal4_3p25x2p55xp75_2p12x1p6mm
X5002 FL4000023
TP5029 SP_TP_SMDp58mm
TP5031 SP_TP_SMDp58mm
TP5033 SP_TP_SMDp58mm
+1P8V_INT_OUT
R5020 10K RES_0201_12mil
R5019 10K RES_0201_12mil
C5028 0.1u 6.3V cap_0201_14mil
U5002
AT24C16D-MAHM
dfn9_2x3xp6_p5mm-2
NC NC1 NC2 GND PAD Vcc WP SCL SDA
wf_eep_wp
SER_CLK SER_DAT
X912618-001
EEPROM

WIFI > PCIe3
[20] PCIE_WIFI_CLKREQ_N
[20] PCIE_WIFI_RCLK_DN
[20] PCIE_WIFI_RCLK_DP
[24] PCIE_WIFI_TX9_DN
[24] PCIE_WIFI_TX9_DP
[24] PCIE_WIFI_RX9_DN
[24] PCIE_WIFI_RX9_DP
RES_0201_12mil R5027 0 PCIE_WIFI_CLKREQ_N_R
RES_0201_12mil R5028 0 PCIE_WIFI_RCLK_R_DN
RES_0201_12mil R5029 0 PCIE_WIFI_RCLK_R_DP
cap_0201_14mil C5057 0.1u 6.3V PCIE_WIFI_C_TX9_DN
cap_0201_14mil C5058 0.1u 6.3V PCIE_WIFI_C_TX9_DP
cap_0201_14mil C5055 0.1u 6.3V PCIE_WIFI_C_RX9_DN
cap_0201_14mil C5056 0.1u 6.3V PCIE_WIFI_C_RX9_DP
[25] PCIE_WIFI_WAKE_N
R5026 0 RES_0201_12mil PCIE_WAKE_N_R
EV1.9 Add R5076 WF 0 RES_0201_12mil
[25] WLAN_PWD_N
+3P3V_RADIO
EV1.9 was installed R5018 0 RES_0201_12mil
DNP,WF C5073 0.1u cap_0201_14mil
WF C5023 0.1u cap_0201_14mil
sp_MTP0p8mm MTP5019 M_PDN
sp_MTP0p8mm MTP5027 AT0
Done: RF_CNTL0_N = 1 for 40MHz auto calibration
EV1.9 Add R5074 49.9K RES_0201_12mil
sp_MTP0p8mm MTP5039
RF_CNTL0_N RF_CNTL1_P RF_TR_2_A RF_TR_2_B RF_TR_5_A RF_TR_5_B

Antenna spring x5
MP5002 MP5004
10F00B18011-P springclip_2p5x1p1x90mm X902698-001
WF_RF_PATH_A_ANT_FEED WF_RF_PATH_A_ANT
J5001 MM8030-2610RK0 CONN_COAX_4_2P1X2X1P0MM
C5061 1.5nH @ 250MHz 0402
DNP,WF L5005 2.7nH 500MHz ind_0402_18mil 0.22A
DNP,WF L5003 2.7nH 500MHz ind_0402_18mil 0.22A
<HDL_POWER>
WF_RF_PATH_A_POSTCOAX
CON5003 COAX coax_wifi_x911513-002
WF_RF_PATH_A_PRECOAX
U5005 LFD182G45MJ6D431 son6_1p6xp8xp7_p5mm
RF_TR_5_A_P RF_TR_5_A_C C5051 0 RES_0201_12mil C5076 5.6p 25V CAP_0201_14mil RF_TR_5_A
WIFI_RF_2_A_OUT C5072 10p 50V CAP_0201_14mil RF_TR_2_A
DNP,WF C5064 5.6p 25V
DNP,WF C5066 5.6p
DNP,WF C5065 5.6p
A1 D5010 LXES15AAA1-153 X936756-001 esd_0402_14mil
Done: 4.7k 0402 for ESD
EV1.9 WAS 4.7K
MP5007 10F00B18011-P springclip_2p5x1p1x90mm X902698-001
Isolation Element

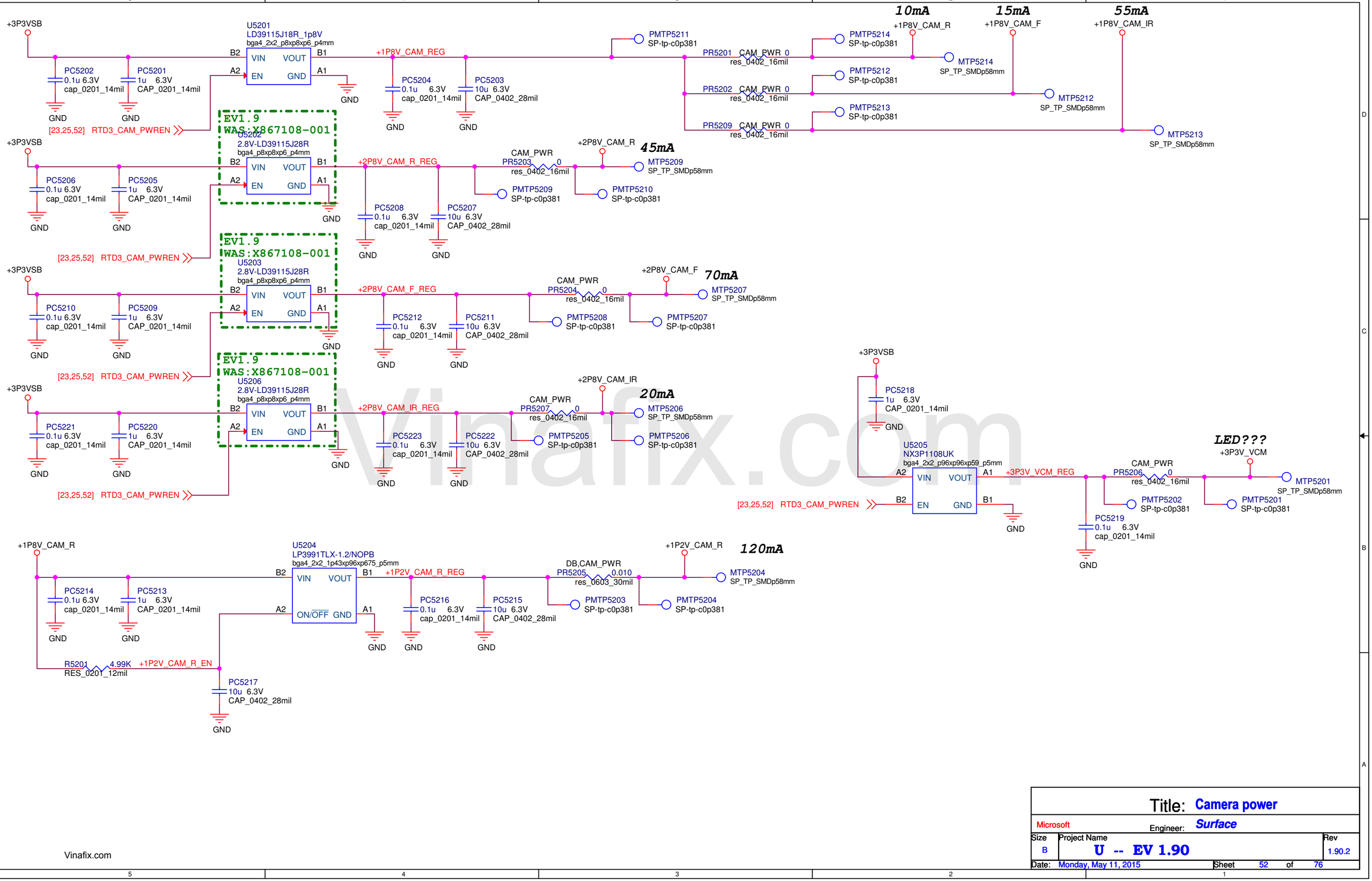
Antenna spring
MP5003 10F00B18011-P springclip_2p5x1p1x90mm X902698-001
MP5006 10F00B18011-P springclip_2p5x1p1x90mm X902698-001
WF_RF_PATH_B_ANT_FEED
C5062 0 RES_0402_16mil 0402
WF_RF_PATH_B_ANT
J5002 MM8030-2610RK0 CONN_COAX_4_2P1X2X1P0MM
L5006 2.7nH 500MHz DNP,WF 0.22A
L5004 2.7nH 500MHz DNP,WF 0.22A
<HDL_POWER>
WF_RF_PATH_B
U5004 LFD182G45MJ6D431 son6_1p6xp8xp7_p5mm
RF_TR_5_B_P RF_TR_5_B_C C5049 0 RES_0201_12mil C5077 5.6p 25V CAP_0201_14mil RF_TR_5_B
WIFI_RF_2_B_FIL_IN
DNP,WF C5067 5.6p 25V
DNP,WF C5068 5.6p 25V
DNP,WF C5069 5.6p
A1 D5011 LXES15AAA1-153 X936756-001 esd_0402_14mil
EV1.9 WAS 4.7K

+3P3V_RADIO
EV1.9 Add R5075 49.9K RES_0201_12mil
R5002 0 RES_0201_12mil
C5033 10p 50V CAP_0201_14mil <HDL_POWER>
DNP,WF C5071 5.6p CAP_0201_14mil 25V
U5003 BGS12SN6 sw_sm_6_1p1xp7xp4_p4mm
VDD RFIN CTRL GND RF1 RF2
WIFI_RF_2_B_FIL_IN_C
RF_CNTL1_P_R
R5003 0 RES_0201_12mil
C5032 10p 50V CAP_0201_14mil <HDL_POWER>
RF_TR_2_B_1 C5030 10p 50V RF_TR_2_B
BRF_ANT_M15_C C5031 10p 50V CAP_0201_14mil BRF_ANT_M15 [50]

Title: WI-FI_BT
Microsoft Engineer: Surface
Size A2 | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 | Sheet 50 of 76

EMPTY

Title:	Empty		
Microsoft	Engineer:	*Surface*	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 51 of 76		

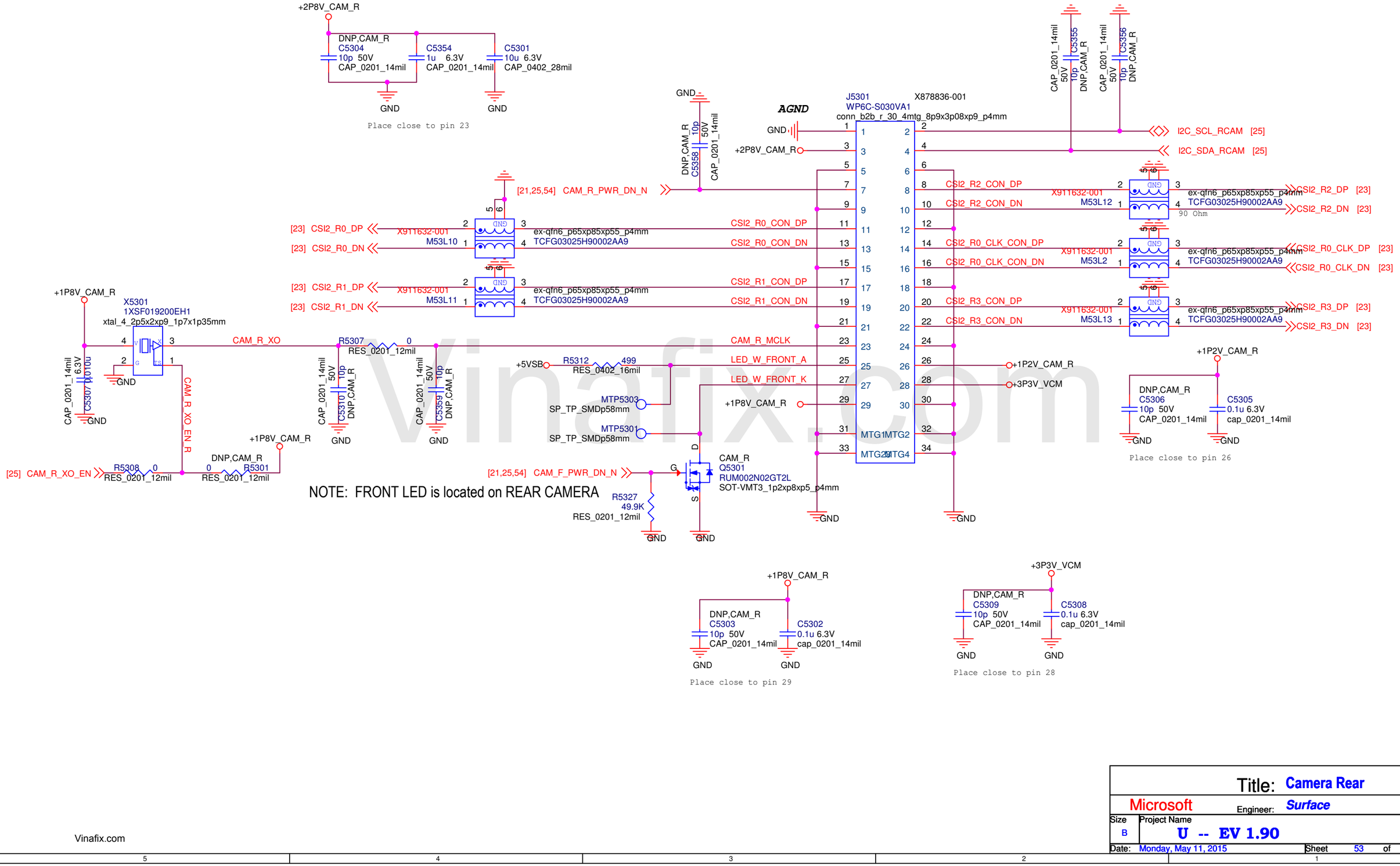


Title: Camera power

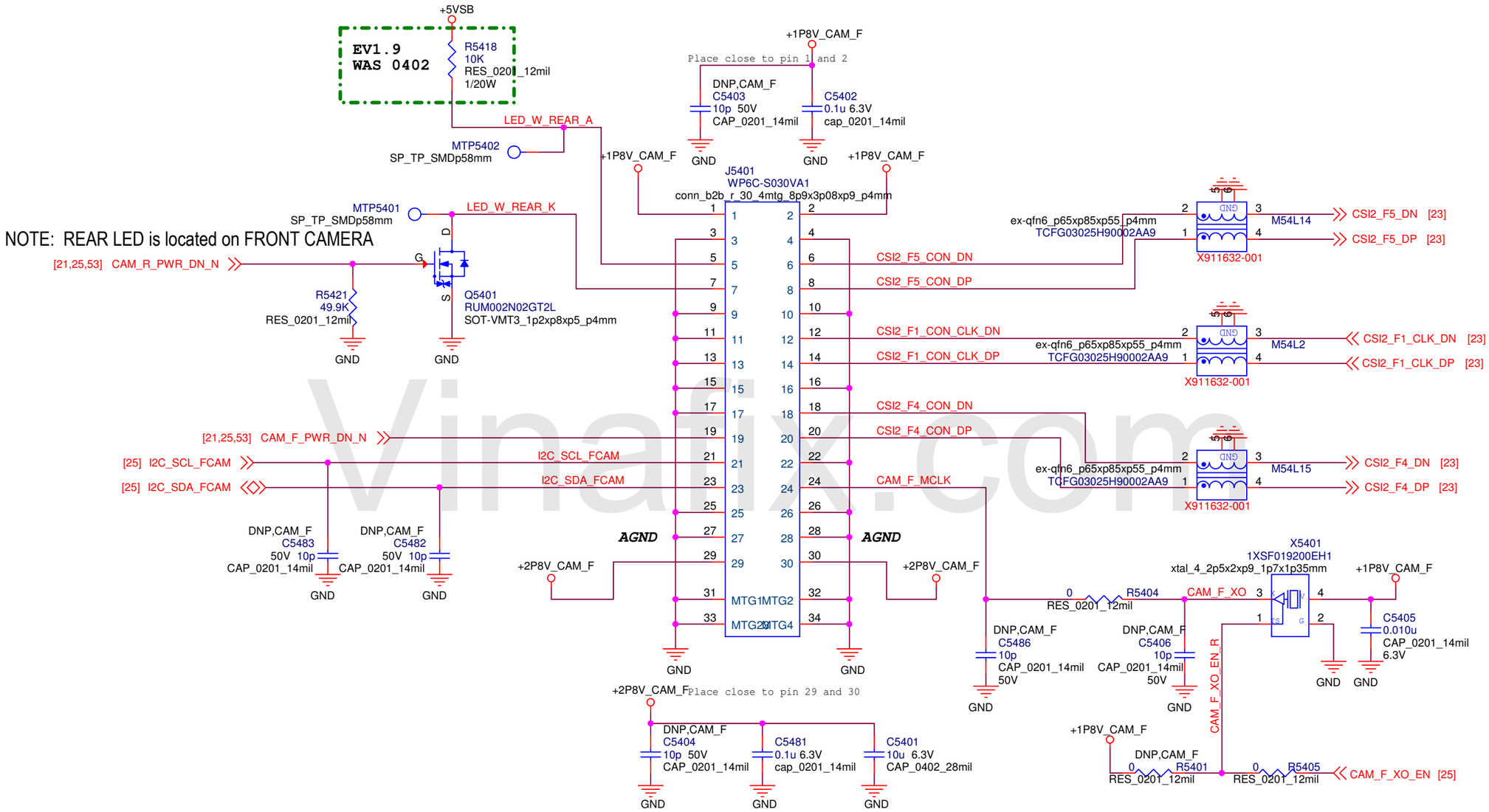
Microsoft Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

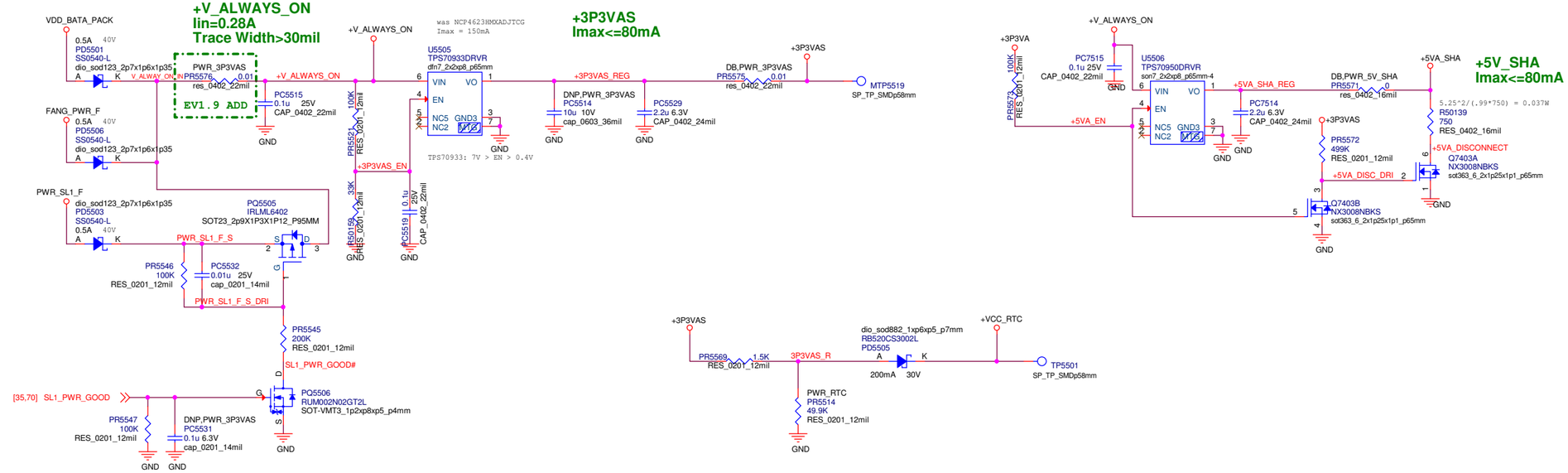
Date: Monday, May 11, 2015 Sheet 52 of 76



Title:	Camera Rear	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 53 of 76	

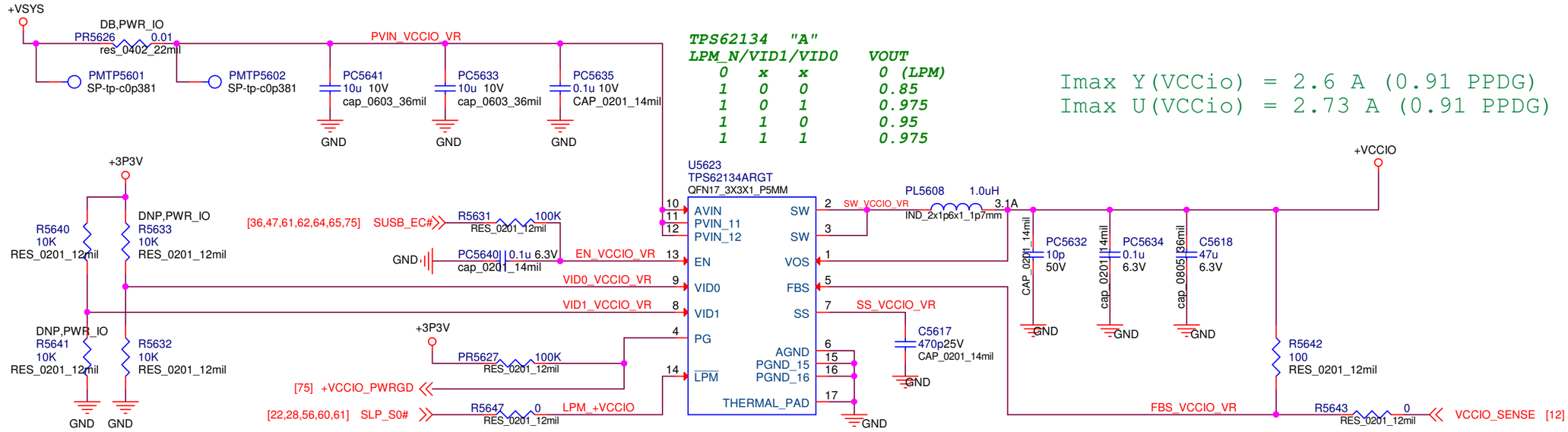


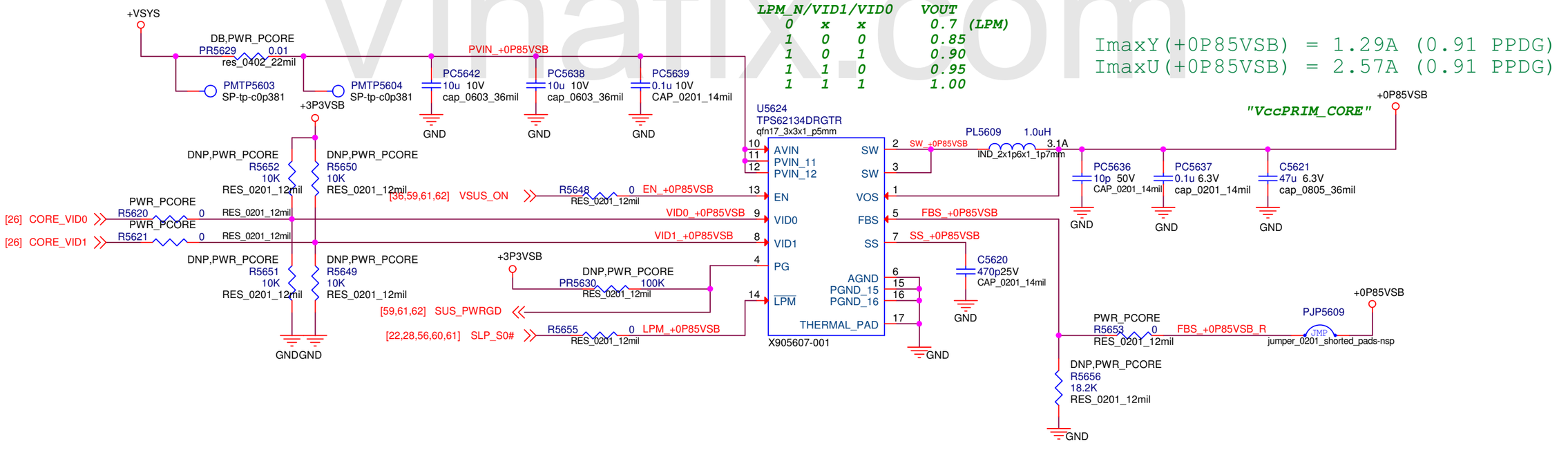
Title:	Camera Front		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 54 of 76		



Vinafix.com

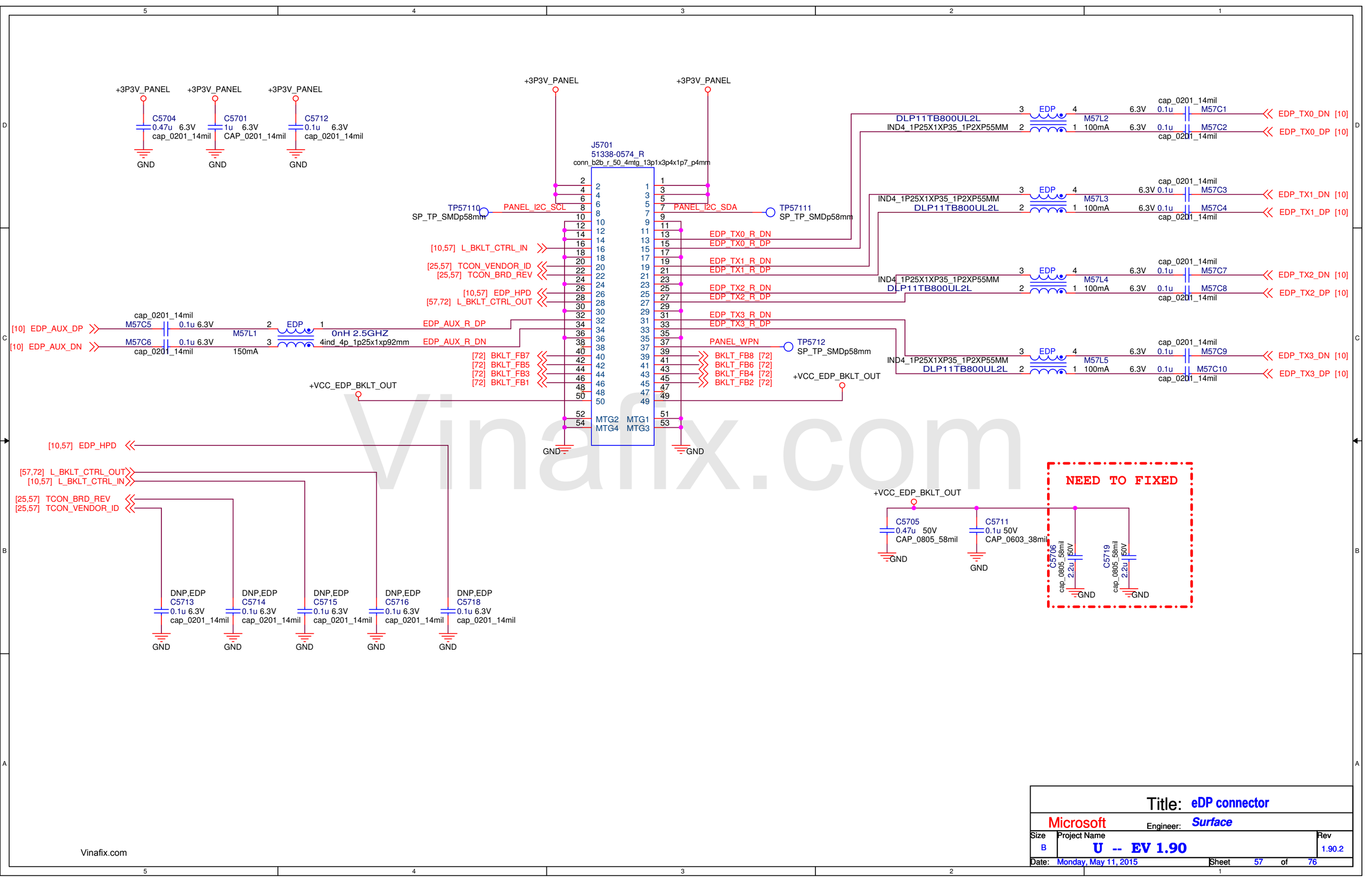
Title:	+3P3VA & +5VA		
Microsoft	Engineer:	Surface	
Size: C	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 55 of 76		





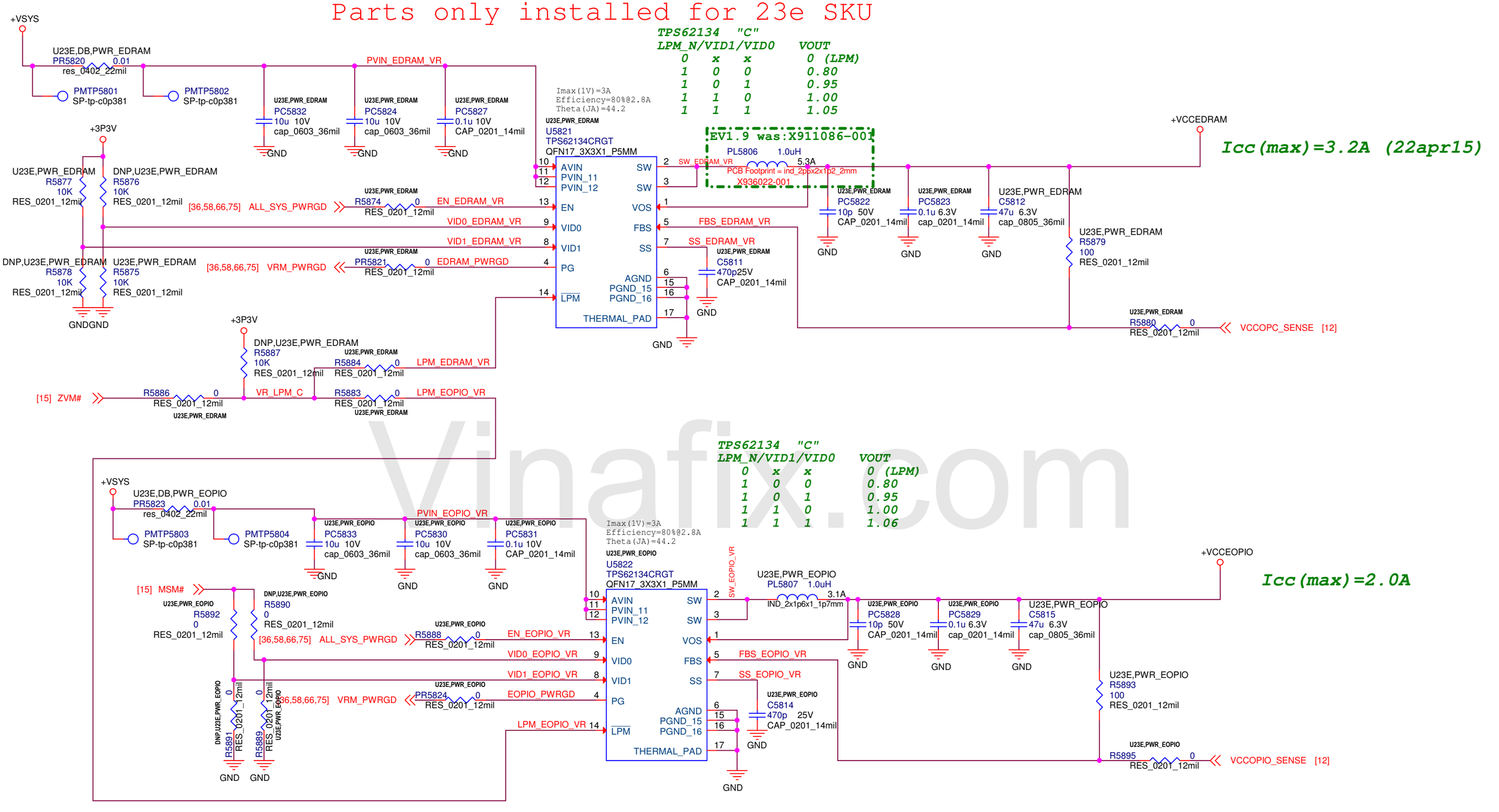
Vinafix.com

Title:	+VCCIO & 0P85VSB	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 56 of 76	

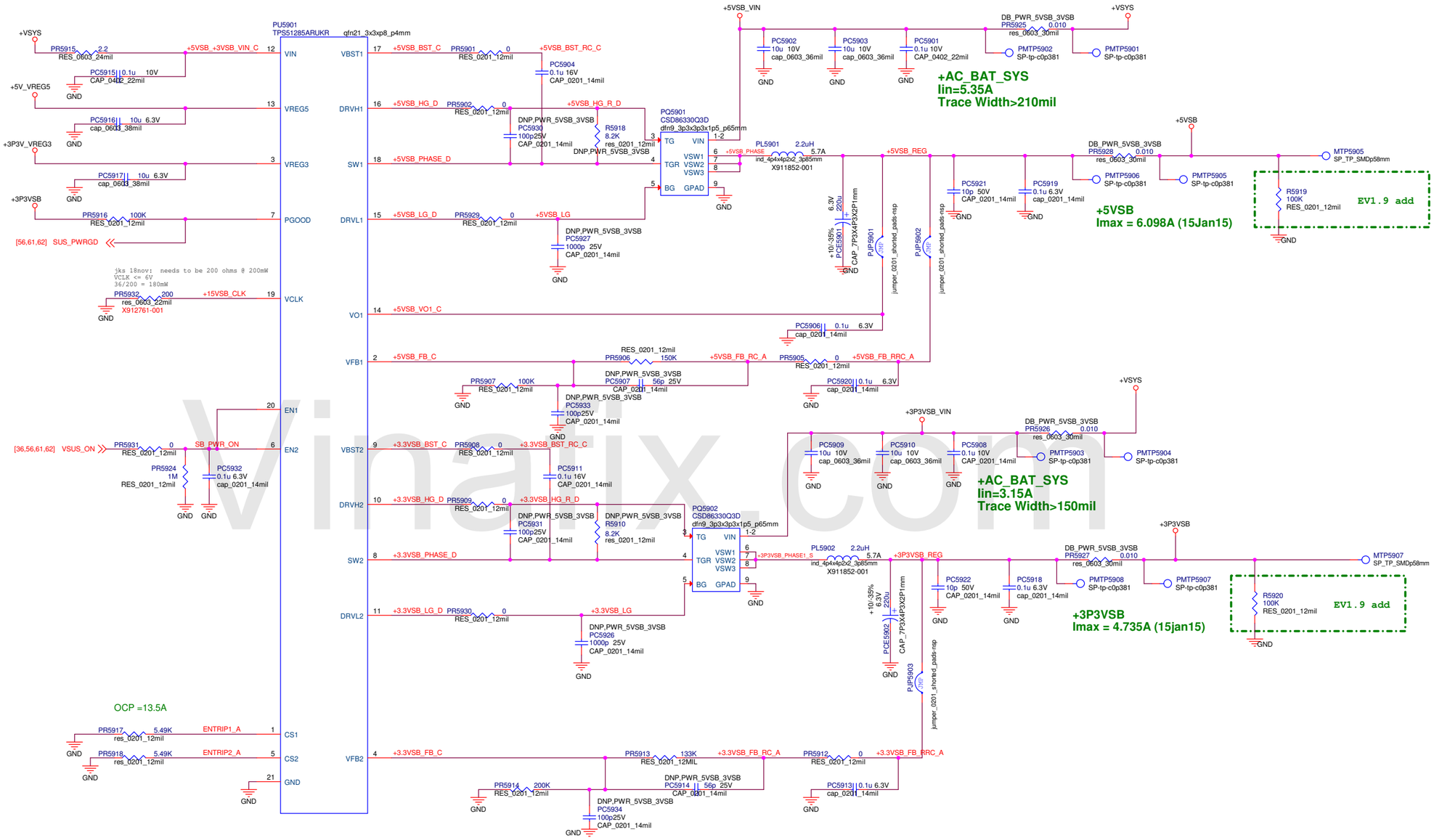


Title:	eDP connector		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 57 of 76		

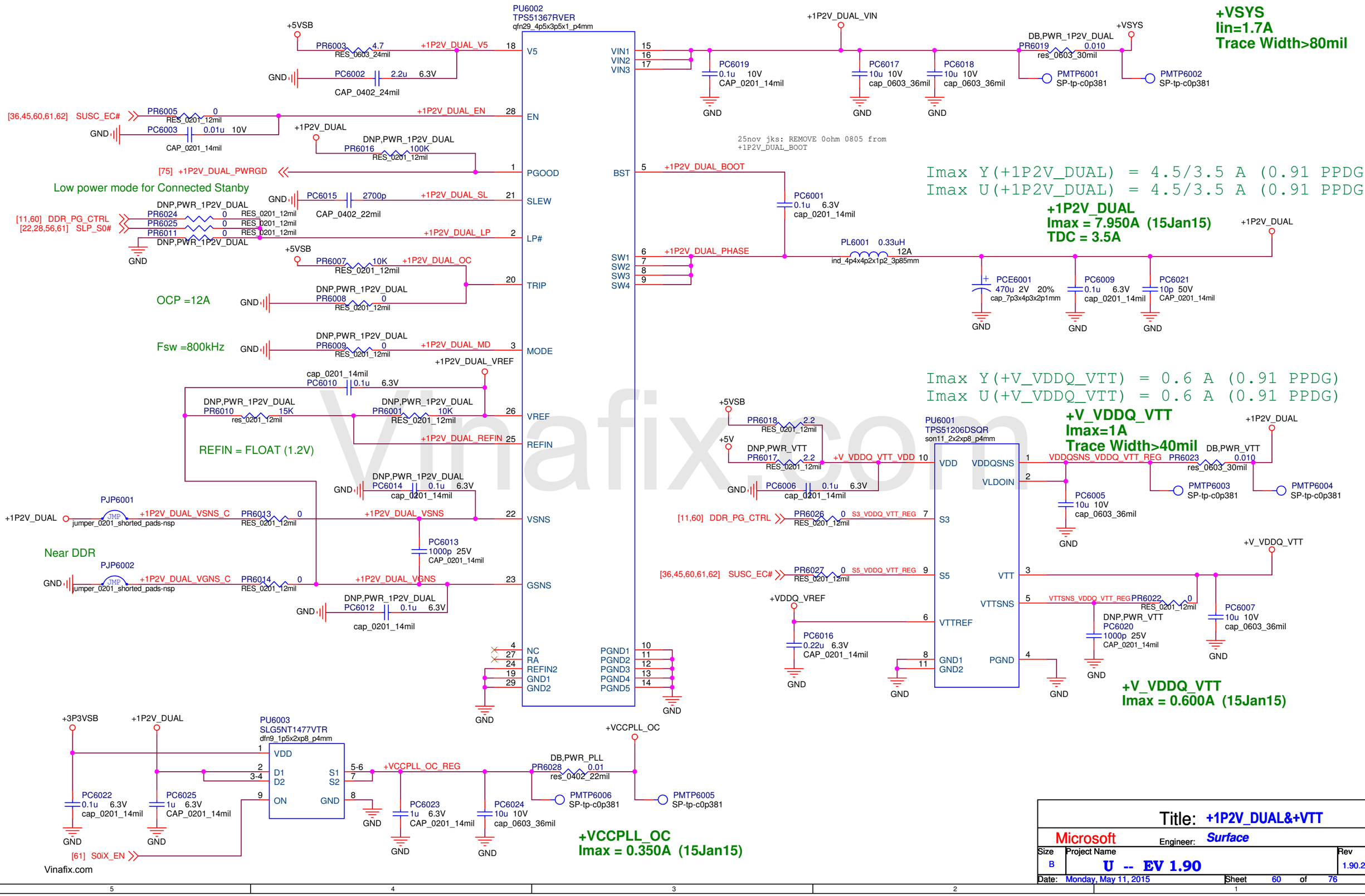
Parts only installed for 23e SKU

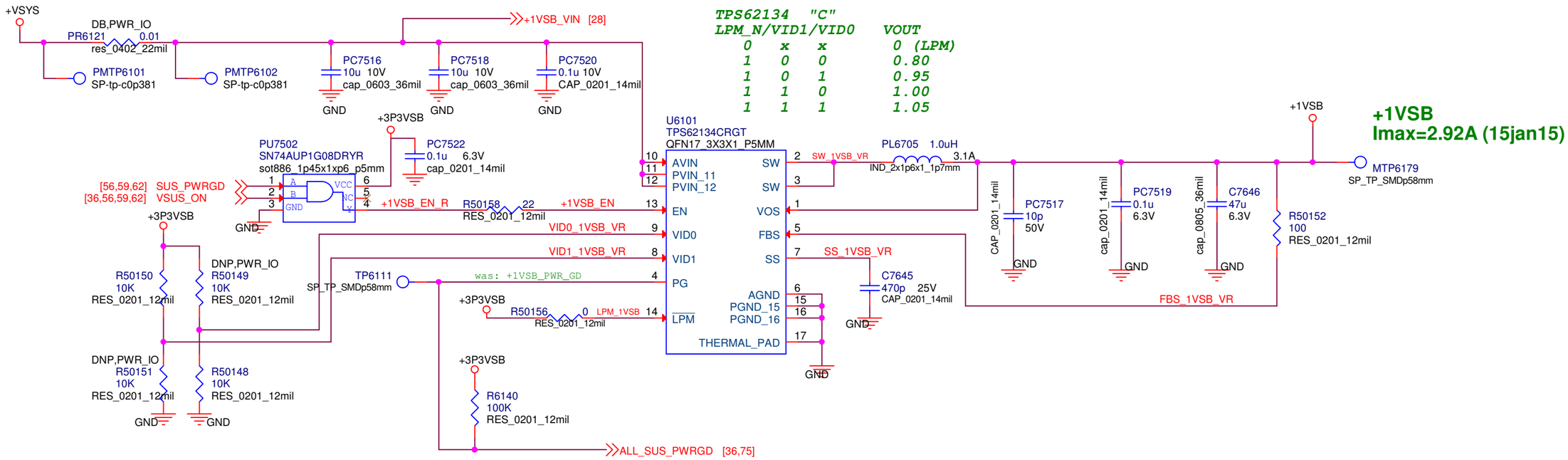


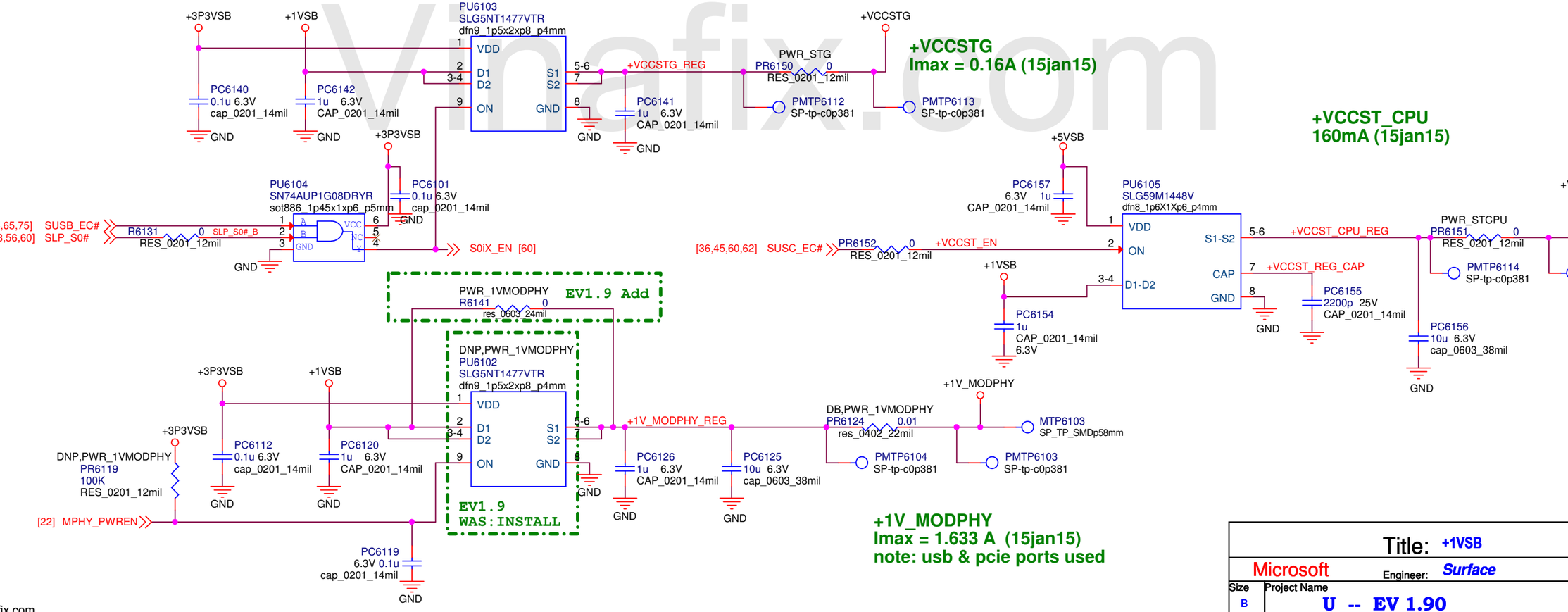
Title:	+VCCEDRAM & +VCCEOPIO		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 58 of 76	



Title:	+5VSB & +3P3VSB		
Microsoft	Engineer: Surface		
Size: C	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 59	of 76	


PU6002
TPS51367RVER
qfn29_4p5x3p5x1_p4mm
+5VSB
PR6003 4.7 RES_0603_24mil
+1P2V_DUAL_V5
PC6002 2.2u 6.3V CAP_0402_24mil
V5
[36,45,60,61,62] SUSC_EC#
PR6005 0 RES_0201_12mil
PC6003 0.01u 10V CAP_0201_14mil
+1P2V_DUAL_EN
EN
+1P2V_DUAL
DNP,PWR_1P2V_DUAL PR6016 100K RES_0201_12mil
[75] +1P2V_DUAL_PWRGD
PGOOD
Low power mode for Connected Stanby
PC6015 2700p CAP_0402_22mil
+1P2V_DUAL_SL
SLEW
[11,60] DDR_PG_CTRL
[22,28,56,61] SLP_S0#
DNP,PWR_1P2V_DUAL
PR6024 0 RES_0201_12mil
PR6025 0 RES_0201_12mil
PR6011 0 RES_0201_12mil
+1P2V_DUAL_LP
LP#
+5VSB
PR6007 10K RES_0201_12mil
+1P2V_DUAL_OC
TRIP
OCP =12A
DNP,PWR_1P2V_DUAL PR6008 0 RES_0201_12mil
Fsw =800kHz
DNP,PWR_1P2V_DUAL PR6009 0 RES_0201_12mil
+1P2V_DUAL_MD
MODE
+1P2V_DUAL_VREF
cap_0201_14mil PC6010 0.1u 6.3V
DNP,PWR_1P2V_DUAL PR6010 15K res_0201_12mil
DNP,PWR_1P2V_DUAL PR6001 10K RES_0201_12mil
VREF
+1P2V_DUAL_REFIN
REFIN
REFIN = FLOAT (1.2V)
DNP,PWR_1P2V_DUAL PC6014 0.1u 6.3V cap_0201_14mil
PJP6001
+1P2V_DUAL
JMP jumper_0201_shorted_pads-nsp
+1P2V_DUAL_VSNS_C
PR6013 0 RES_0201_12mil
+1P2V_DUAL_VSNS
VSNS
PC6013 1000p 25V CAP_0201_14mil
Near DDR
PJP6002
JMP jumper_0201_shorted_pads-nsp
+1P2V_DUAL_VGNS_C
PR6014 0 RES_0201_12mil
+1P2V_DUAL_VGNS
GSNS
DNP,PWR_1P2V_DUAL PC6012 0.1u 6.3V cap_0201_14mil
NC
RA
REFIN2
GND1
GND2
PGND1
PGND2
PGND3
PGND4
PGND5
+1P2V_DUAL_VIN
VIN1
VIN2
VIN3
PC6019 0.1u 10V CAP_0201_14mil
PC6017 10u 10V cap_0603_36mil
PC6018 10u 10V cap_0603_36mil
DB,PWR_1P2V_DUAL PR6019 0.010 res_0603_30mil
+VSYS
PMTP6001 SP-tp-c0p381
PMTP6002 SP-tp-c0p381
+VSYS
lin=1.7A
Trace Width>80mil
25nov jks: REMOVE 0ohm 0805 from +1P2V_DUAL_BOOT
BST
+1P2V_DUAL_BOOT
PC6001 0.1u 6.3V cap_0201_14mil
SW1
SW2
SW3
SW4
+1P2V_DUAL_PHASE
PL6001 0.33uH 12A ind_4p4x4p2x1p2_3p85mm
PCE6001 470u 2V 20% cap_7p3x4p3x2p1mm
PC6009 0.1u 6.3V cap_0201_14mil
PC6021 10p 50V CAP_0201_14mil
+1P2V_DUAL
Imax Y(+1P2V_DUAL) = 4.5/3.5 A (0.91 PPDG)
Imax U(+1P2V_DUAL) = 4.5/3.5 A (0.91 PPDG)
+1P2V_DUAL
Imax = 7.950A (15Jan15)
TDC = 3.5A
Imax Y(+V_VDDQ_VTT) = 0.6 A (0.91 PPDG)
Imax U(+V_VDDQ_VTT) = 0.6 A (0.91 PPDG)
+5VSB
PR6018 2.2 RES_0201_12mil
+5V
DNP,PWR_VTT PR6017 2.2 RES_0201_12mil
+V_VDDQ_VTT_VDD
PC6006 0.1u 6.3V cap_0201_14mil
PU6001
TPS51206DSQR
son11_2x2xp8_p4mm
VDD
VLDOIN
S3
S5
VTTREF
GND1
GND2
VDDQSNS
VTT
VTTSNS
PGND
[11,60] DDR_PG_CTRL
PR6026 0 S3_VDDQ_VTT_REG RES_0201_12mil
[36,45,60,61,62] SUSC_EC#
PR6027 0 S5_VDDQ_VTT_REG RES_0201_12mil
+VDDQ_VREF
PC6016 0.22u 6.3V CAP_0201_14mil
VDDQSNS_VDDQ_VTT_REG
PR6023 0.010 res_0603_30mil
DB,PWR_VTT
PMTP6003 SP-tp-c0p381
PMTP6004 SP-tp-c0p381
PC6005 10u 10V cap_0603_36mil
VTTSNS_VDDQ_VTT_REG
PR6022 0 RES_0201_12mil
DNP,PWR_VTT PC6020 1000p 25V CAP_0201_14mil
PC6007 10u 10V cap_0603_36mil
+V_VDDQ_VTT
Imax=1A
Trace Width>40mil
+V_VDDQ_VTT
Imax = 0.600A (15Jan15)
+3P3VSB
+1P2V_DUAL
PU6003
SLG5NT1477VTR
dfn9_1p5x2xp8_p4mm
VDD
D1
D2
ON
S1
S2
GND
PC6022 0.1u 6.3V cap_0201_14mil
PC6025 1u 6.3V CAP_0201_14mil
[61] S0iX_EN
5-6
+VCCPLL_OC_REG
PC6023 1u 6.3V CAP_0201_14mil
PC6024 10u 10V cap_0603_36mil
DB,PWR_PLL PR6028 0.01 res_0402_22mil
+VCCPLL_OC
PMTP6006 SP-tp-c0p381
PMTP6005 SP-tp-c0p381
+VCCPLL_OC
Imax = 0.350A (15Jan15)
Vinafix.com
Vinafix.com
Title: +1P2V_DUAL&+VTT
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 60 of 76





Title:	+1VSB		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 61 of 76		

+VSYS
Iin=0.274A
Trace Width>30mil

+3P3VSB
DNP,PWR_1P8VSB
PR6201
100K
RES_0201_12mil

PU6202
TPS62140RGT
QFN17_3X3X1_P5MM

[56,59,61] SUS_PWRGD
[36,56,59,61] VSUS_ON
PR6203 0 RES_0201_12mil

+1P8VSB
PR6225 100K RES_0201_12mil

PC6202
3300p 16V
cap_0201_14mil
Tss=1.5ms

GND GND GND GND

+1P8VSB_EN
+1P8VSB_FSW
+1P8VSB_SS
+1P8VSB_SW
+1P8VSB_FB

PG EN FSW SS/TR DEF SW1 SW3 SW2 VOS FB AVIN PVIN3 PVIN2 AGND GND PGND1 PGND2

+1P8VSB_VIN

PC6211 10u 10V cap_0603_36mil
PC6212 10u 10V cap_0603_36mil
PC6205 0.1u 10V CAP_0201_14mil

DB,PWR_1P8VSB
PR6205 0.01 res_0402_22mil
PMTP6202 SP-tp-c0p381
PMTP6201 SP-tp-c0p381

PL6201 2.2uH 1.60A ind_2x1p6x1_1p6mm

PC6218 10p 50V CAP_0201_14mil

EV1.9 was:6V
PC6203 22u 4V cap_0603_40mil
PC6204 22u 4V cap_0603_40mil

PR6211 120K RES_0201_12mil

R1 = R2 {Vout /Vref(0.8) - 1}

+1P8VSB
Imax=1.54A (15jan15)

MTP6211 SP_TP_SMDp58mm
PR6214 100 RES_0201_12mil

+3P3VA
PR6215 499K RES_0201_12mil
+1P8VSB_DISC_CTRL
+1P8VSB_disc
PQ6201A NX3008NBKS sot363_6_2x1p25x1p1_p65mm
PQ6201B NX3008NBKS sot363_6_2x1p25x1p1_p65mm

+1P8V_AUDIO
Imax=0.260A (15jan15)

+5VSB
PC6242 1u 6.3V CAP_0201_14mil

U6202
VDD ON D1-D2 S1-S2 CAP GND
SLG59M1448V
dfn8_1p6X1Xp6_p4mm

DNP,PWR_1P8V_DUAL
[25,64] RTD3_AUD_PWR
PR6226 0 RES_0201_12mil
[36,47,56,61,62,64,65,75] SUSB_EC#
PR6227 0 RES_0201_12mil
+1P8V_AUD_REG_EN
+1P8VSB
C6248 6.3V 1u CAP_0201_14mil

+1P8V_AUD_REG
CAP_+1P8V_AUDIO

PC6210 0.1u 6.3V cap_0201_14mil
C6251 2200p 25V CAP_0201_14mil

+1P8V_AUDIO
DB,PWR_1P8V_DUAL
PR6210 0.01 res_0402_22mil
PMTP6204 SP-tp-c0p381
MTP6203 SP_TP_SMDp58mm
PMTP6203 SP-tp-c0p381

PC6206 1u 6.3V CAP_0201_14mil

PU6201
NX3P1108UK
bga4_2x2_p96xp96xp59_p5mm
VIN VOUT EN GND A2 A1 B2 B1

[36,47,56,61,62,64,65,75] SUSB_EC#
PR6207 0 RES_0201_12mil
+1P8V_REG_EN
+1P8V_REG

PC6207 0.1u 6.3V cap_0201_14mil

DB,PWR_1P8V
PR6202 0.01 res_0402_22mil
PMTP6208 SP-tp-c0p381

+1P8V
Imax=~0 (15jan15)

MTP6207 SP_TP_SMDp58mm
PMTP6207 SP-tp-c0p381

+1P8V_DUAL
Imax=0.620A (15jan15)

+5VSB
PC7526 1u 6.3V CAP_0201_14mil

U6203
VDD ON D1-D2 S1-S2 CAP GND
SLG59M1448V
dfn8_1p6X1Xp6_p4mm

[36,45,60,61] SUSC_EC#
PR6233 0 RES_0201_12mil
+1P8V_DUAL_REG_EN
+1P8VSB
C6249 6.3V 1u CAP_0201_14mil

+1P8V_DUAL_REG
CAP_+1P8V_DUAL

C6250 0.1u 6.3V cap_0201_14mil
C6252 2200p 25V CAP_0201_14mil

+1P8V_DUAL
DB,PWR_1P8V_DUAL
PR6231 0.01 res_0402_22mil
PMTP6206 SP-tp-c0p381
MTP6205 SP_TP_SMDp58mm
PMTP6205 SP-tp-c0p381

[25,64] RTD3_TPANEL_PWR
PR6208 0 RES_0201_12mil
+1P8V_TS_REG_EN

PC6213 1u 6.3V CAP_0201_14mil

PU6205
NX3P1108UK
bga4_2x2_p96xp96xp59_p5mm
VIN VOUT EN GND A2 A1 B2 B1

+1P8V_TS_REG

PC6214 0.1u 6.3V cap_0201_14mil

DB,PWR_1P8_TS
PR6209 0.01 res_0402_22mil
PMTP6210 SP-tp-c0p381
MTP6209 SP_TP_SMDp58mm
PMTP6209 SP-tp-c0p381

+1P8V_TS
Imax=0.452A (15jan15)

Vinafix.com

Title:	+1.8VSB & Load SW	
Microsoft	Engineer: Surface	
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 62 of 76	

CHGR_VIN
Iin=9.731A
Trace Width>389mil

+SYS
Iin=8A
Trace Width>320mil

+SYS
Imax = 12.0A
TDC = 10.0A

*Cgs>=40*Cgd*
Cgs.9 >= 40*Cgd*1.1*
*Cgs >= (1.1/0.9)*40*1nF*
Cgs >= 49nF

CHGR needs 200uF for loop stability
{2*f*pi = 1/sqrt(L*C)}

EffCap@20V=3.22uF*3=9.66uF

I(ripple)=Vin*DutyCycle*(1-DutyCycle)/(FreqSwitch*L)
I(ripple)= 20%~40% I(charge)
Vin(12.6V+/-10%) => I(ripple)@2.2uH => 1.93A, 40.5%
Vin(12.6V+/-10%) => I(ripple)@3.3uH => 1.29A, 27.0%
assuming 60W, DutyCycle=0.5, Freq=1020KHz

EV1.9 CHG MSPN

EV1.9 CHG MSPN

7-bit I2C Address = 0x12

Title:	CHARGER NVDC
Microsoft	Engineer: Surface
Size: A3	Project Name: U -- EV 1.90
Rev:	1.90.2
Date: Monday, May 11, 2015	Sheet 63 of 76

+5V_TS
Imax=0.0027A

R6431 75 RES_0402_16mil
R6430 75 RES_0402_16mil
DSG_+5V_TS
+5VSB
C6423 6.3V 1u CAP_0201_14mil
U6407 G5244A31U dfn6_1p5x1p5xp8_p5mm
1 IN OUT 6
2 NC EN 4
3 DSG GND 5
GND
+5V_TS_REG
C6422 6.3V 10u CAP_0402_28mil
GND
+5V
+5V_TS
DNP,DB,PWR_5V_TS
0.01 R6445 res_0402_22mil
PMTP6419 SP-tp-c0p381
DB,PWR_5V_TS
0.01 R6428 res_0402_22mil
PMTP6413 SP-tp-c0p381
PMTP6420 SP-tp-c0p381
MTP6413 SP_TP_SMDp58mm
PMTP6414 SP-tp-c0p381

G5244A31U
Imax= 2.5A
Rdc=120mOhm

[25,62] RTD3_TPANEL_PWR
R6452 0 RES_0201_12mil
+5V_TS_EN
C6421 0.1u 6.3V cap_0201_14mil
GND

+5V_SDXC
Imax= 880mA

+5VSB
DNP,PWR_5V_SDXC
R6453 0 RES_0402_16mil
C6413 1u 6.3V CAP_0201_14mil
U6402 SLG59M1448V dfn8_1p6X1Xp6_p4mm
1 VDD S1-S2 5-6 +5V_SDXC_REG
[10] RTD3_CR_PWREN
R6413 0 RES_0201_12mil
ON_+5V_SDXC
2 ON CAP 7 CAP_+5V_SDXC
3-4 D1-D2 GND 8
C6411 2200p 25V CAP_0201_14mil
C6412 10u 6.3V CAP_0402_28mil
GND
+5V_SDXC
DB,PWR_5V_SDXC
R6414 0.01 res_0402_22mil
PMTP6404 SP-tp-c0p381
MTP6404 SP_TP_SMDp58mm
PMTP6412 SP-tp-c0p381

SLG59M1448V
Imax= 2.5A
Rdc(@70C)=20mOhm

+5V_AUDIO
Imax=1.05A

+5VSB
C6406 1u 6.3V CAP_0201_14mil
U6404 SLG59M1448V dfn8_1p6X1Xp6_p4mm
1 VDD S1-S2 5-6 +5V_AUDIO_REG
DNP,PWR_5V_AUDIO
[25,62] RTD3_AUD_PWR
R6447 0 RES_0201_12mil
ON_+5V_AUDIO_REG
2 ON CAP 7 CAP_+5V_AUDIO_REG
[36,47,56,61,62,64,65,75] SUSB_EC#
R6448 0 RES_0201_12mil
3-4 D1-D2 GND 8
C6415 2200p 25V CAP_0201_14mil
C6429 10u 6.3V cap_0402_26mil TMAX=0.65mm
EV1.9 WAS:X867508-001
GND
+5V_AUDIO
DB,PWR_5V_AUDIO
R6418 0.010 res_0603_18mil
PMTP6410 SP-tp-c0p381
MTP6410 SP_TP_SMDp58mm
PMTP6411 SP-tp-c0p381

+5V
Imax=0.2A

+5VSB
C6407 1u 6.3V CAP_0201_14mil
U6405 SLG59M1448V dfn8_1p6X1Xp6_p4mm
1 VDD S1-S2 5-6 +5V_REG
[36,47,56,61,62,64,65,75] SUSB_EC#
2 ON CAP 7 CAP_+5V_REG
3-4 D1-D2 GND 8
C6414 2200p 25V CAP_0201_14mil
C6428 10u 6.3V cap_0402_26mil TMAX=0.65mm
EV1.9 WAS:X867508-001
GND
+5V
DB,PWR_5V
R6411 0.01 res_0402_22mil
PMTP6406 SP-tp-c0p381
MTP6406 SP_TP_SMDp58mm
PMTP6407 SP-tp-c0p381

+5V_FAN
Imax=0.7A

+5V
DB_Y,PWR_5V_FAN
C6424 1u 6.3V CAP_0201_14mil
U6408 SLG59M1448V dfn8_1p6X1Xp6_p4mm
1 VDD S1-S2 5-6 +5V_FAN_REG
DB_Y,PWR_5V_FAN
[25,36] DISPLAY_OFF#
R6403 1K RES_0201_12mil
ON_+5V_FAN_REG
2 ON CAP 7 CAP_+5V_FAN_REG
SP_TP_SMDp58mm MTP6402
3-4 D1-D2 GND 8
C6425 2200p 25V CAP_0201_14mil
C6427 10u 6.3V cap_0402_26mil TMAX=0.65mm
EV1.9 WAS:X867508-001
GND
+5V_FAN
DB_Y,DB,PWR_5V_FAN
R6432 0.01 res_0402_22mil
PMTP6408 SP-tp-c0p381
PMTP6409 SP-tp-c0p381

+5V_KB_CONN
Imin=0.5A (ng 18dec14)

EffCap(22uf_0603@5V) = 4.7uF X 6 = 28uF
EffCap(10uf_0.90mm@5V) = 2.7uF
EffCap(10uf_0.95mm@5V) = 4.8uF
EffCap(22uf_0805_1.4mm@5V) = 7.5uF X 6 = 45uF

Close Page 73

+3P3VSB
R6405 100K RES_0201_12mil
[31] BLADE_+5V_KB_CONN_EN
R6419 1K RES_0201_12mil
U6401 NCP380HMUAJAATBG dfn7_2x2xp55_p65mm
3 FLAG# IN 6
4 EN
5 GND1 OUT 1 +5V_BLADE_REG
7 GND2 ILIM 2 5V_BLADE_REG_ILIM
GND
Imax(DFN) <= 2.1A
Imax(DFN) <= 2.1A
1.02A <= ILIM(20K) <= 1.38A
0.5 A <= ILIM(43K) <= 0.65A
+5VSB
C6401 1u 6.3V CAP_0201_14mil
GND
SP-tp-c0p381 PMTP6416
SP-tp-c0p381 PMTP6415
DB,BLADE_PWR
R6402 0.01 res_0402_22mil
+5V_KB_CONN
R6426 44.2K res_0201_12mil
C6402 10u 6.3V CAP_0402_28mil
C6446 22u 6.3V cap_0603_38mil
C6447 22u 6.3V cap_0603_38mil
C6448 22u 6.3V cap_0603_38mil
R6401 1K RES_0201_12mil
BLADE_5V_PWR_EN_R
MTP6405 SP_TP_SMDp58mm
R6404 100K RES_0201_12mil
+3P3VSB
R6442 499K RES_0201_12mil
Q6402B NX3008NBKS sot363_6_2x1p25x1p1_p65mm
+5V_SL2_disc_CTRL
C6443 22u 6.3V cap_0603_38mil
C6444 22u 6.3V cap_0603_38mil
C6445 22u 6.3V cap_0603_38mil
+5V_SL2_disc
Q6402A NX3008NBKS sot363_6_2x1p25x1p1_p65mm
GND

+5V_SL1
Imin=1.5A

EffCap(22uf_0603@5V) = 4.7uF X 9 = 42uF
EffCap(10uf_0.90mm@5V) = 2.7uF
EffCap(10uf_0.95mm@5V) = 4.8uF
EffCap(22uf_0805_1.4mm@5V) = 7.5uF X 9 = 68uF

Close Page 70

+3P3VSB
R6423 100K RES_0201_12mil
[31] SL1_5V_OC#
[31,70] SL1_5V_PWR_EN
R6421 1K RES_0201_12mil
U6403 NCP380HMUAJAATBG dfn7_2x2xp55_p65mm
3 FLAG# IN 6
4 EN
5 GND1 OUT 1 +5V_SL1_REG
7 GND2 ILIM 2 5V_SL1_REG_ILIM
GND
Imax(DFN) <= 2.1A
Imax(DFN) <= 2.1A
1.02A <= ILIM(20K) <= 1.38A
0.5 A <= ILIM(43K) <= 0.65A
ILIM(11.8K) <= 2.0A
+5VSB
C6403 1u 6.3V CAP_0201_14mil
C6420 22u 6.3V cap_0603_38mil
C6419 22u 6.3V cap_0603_38mil
C6418 22u 6.3V cap_0603_38mil
GND
SP-tp-c0p381 PMTP6417
SP-tp-c0p381 PMTP6418
DB,SL_PWR
R6424 0.01 res_0402_22mil
+5V_SL1
R6429 11.8K res_0201_12mil
D6404 BZX584C6V2 6.2V 5mA
C6404 10u 6.3V CAP_0402_28mil
C6417 22u 6.3V cap_0603_38mil
C6416 22u 6.3V cap_0603_38mil
C6410 22u 6.3V cap_0603_38mil
R6425 1K RES_0201_12mil
SL1_5V_PWR_EN_R
TP6401 SP_TP_SMDp58mm
+3P3VSB
R6420 499K RES_0201_12mil
Q6401B NX3008NBKS sot363_6_2x1p25x1p1_p65mm
+5V_SL1_disc_CTRL
C6408 22u 6.3V cap_0603_38mil
C6409 22u 6.3V cap_0603_38mil
C6405 22u 6.3V cap_0603_38mil
+5V_SL1_disc
R6422 100K RES_0201_12mil
Q6401A NX3008NBKS sot363_6_2x1p25x1p1_p65mm
GND

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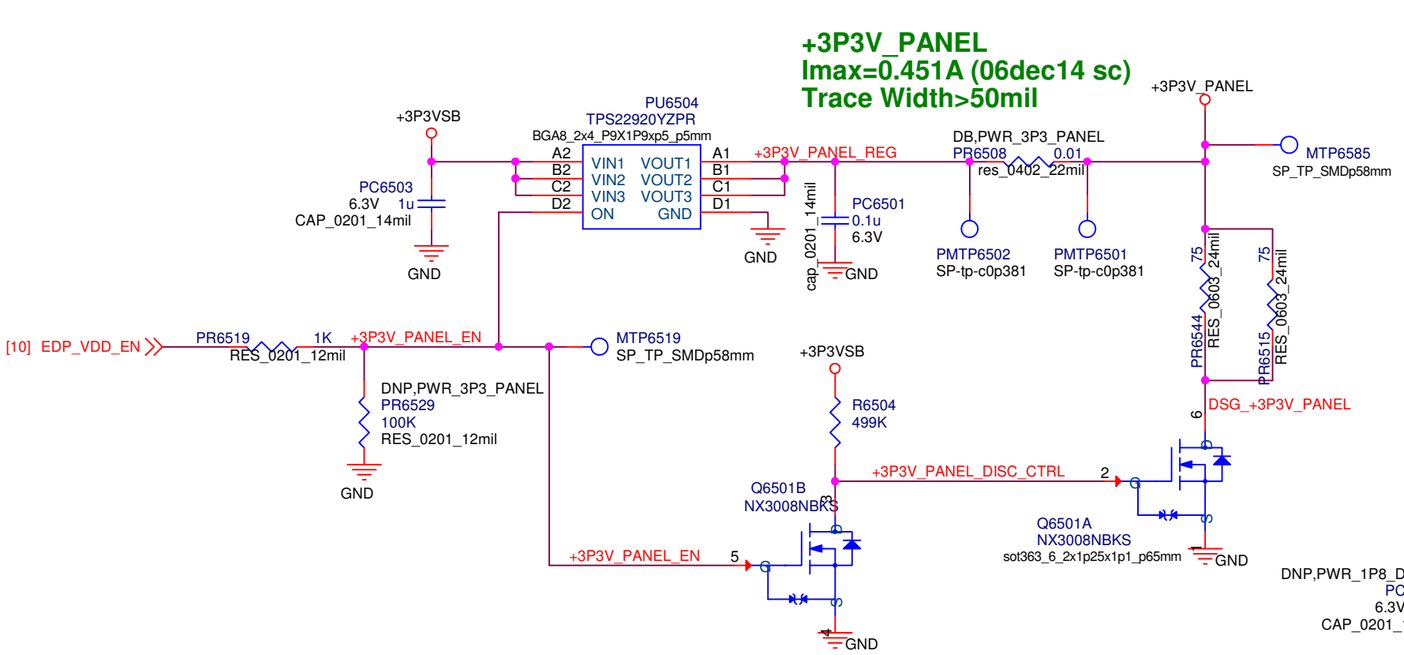
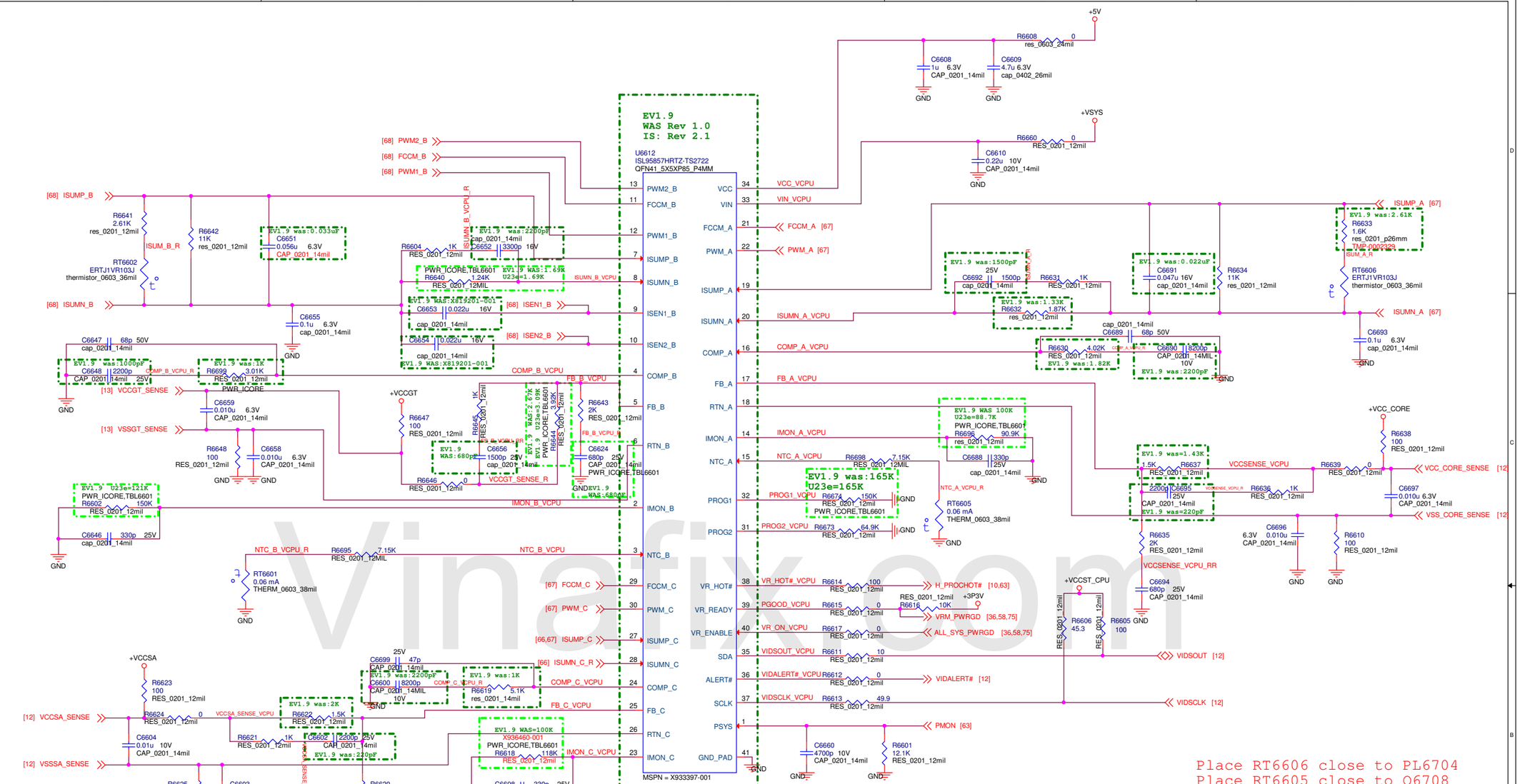
Title:	+5V Load SW	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 64 of 76	



Vinafix.com

Title:	+3P3V Load SW	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 65 of 76	



Place RT6606 close to PL6704
Place RT6605 close to Q6708
Place RT6602 close to L6805
Place RT6601 close to Q6811
Place RT6607 close to L6703
Place RT6904 close to Q6916
Place RT6903 close to PL6905

	SKL-U 2+2 (15W)	SKL-U 2+3e (15W)
Intel SPEC		
ICCMAX/TDC of Vcore	28A/21A	29A/21A
ICCMAX/TDC of VCCGT	31A/18A	57A/32A
ICCMAX/TDC of VCCSA	4.5A/3.7A	5.1A/4.5A
ICCMAX/TDC of VCCGTx	N/A	7A/4A
DC_LL of Vcore	2.35 mohm	2.1 mohm
DC_LL of VCCGT	3.1 mohm	2 mohm
DC_LL of VCCSA	10.3 mohm	10.3 mohm
DC_LL of VCCGTx	N/A	6.9 mohm
Change items		
Vcore	No need to changed	No need to changed
VCCGT	R6674 : 150kohm (ICCMAX) R6640 : 1.24kohm (60A OCP) R6644 : 3.09kohm (LL 3.1mohm)	R6674 : 165kohm (ICCMAX) R6640 : 1.69kohm (80A OCP) R6644 : 2.68kohm(LL 2mohm)
VCCSA	No need to changed	No need to changed
VCCGTx	Disable U6916	Enable U6916

	U22	U23E
R6674	150K	165K
R6696	90.9K	88.7K
R6644	3.92K	3.09K
C6624	680pF	390pF
R6640	1.24K	1.69K
R6602	150K	121K
R6618	118K	100K

Title: VCPU contoller
Microsoft
Engineer: Surface
Size: C
Project Name: U -- EV 1.90
Rev: 1.90.2
Date: Monday, May 11, 2015
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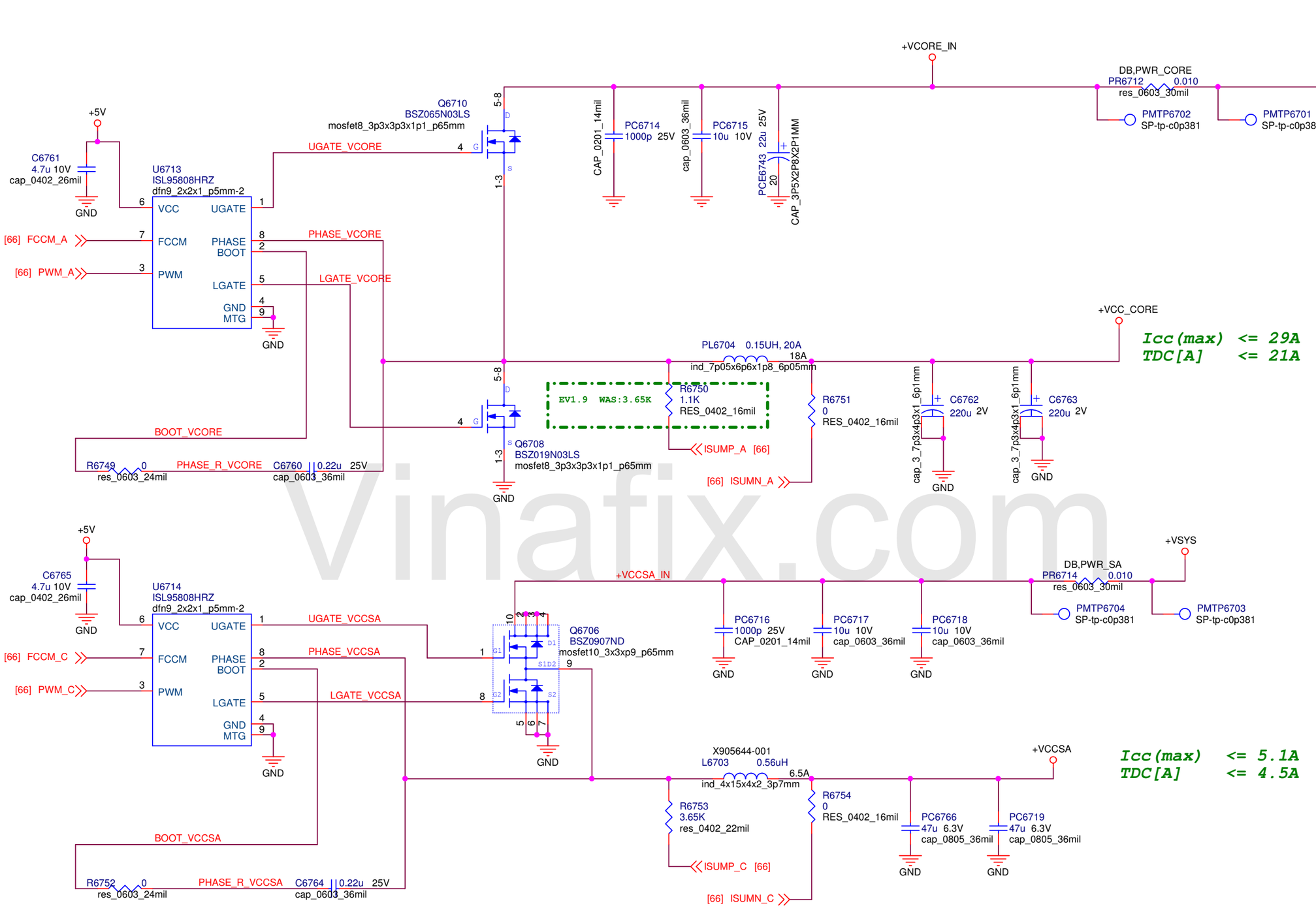
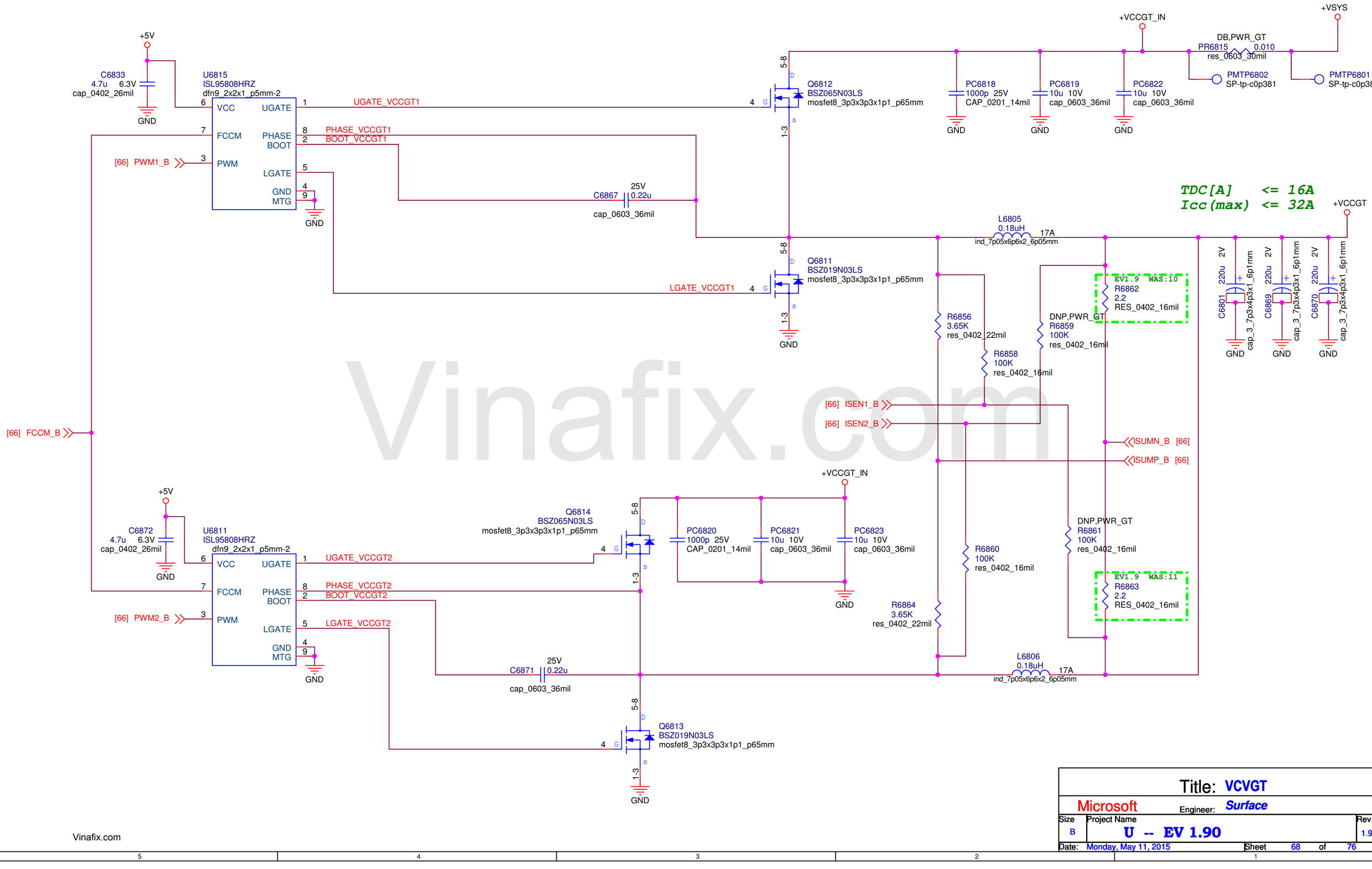
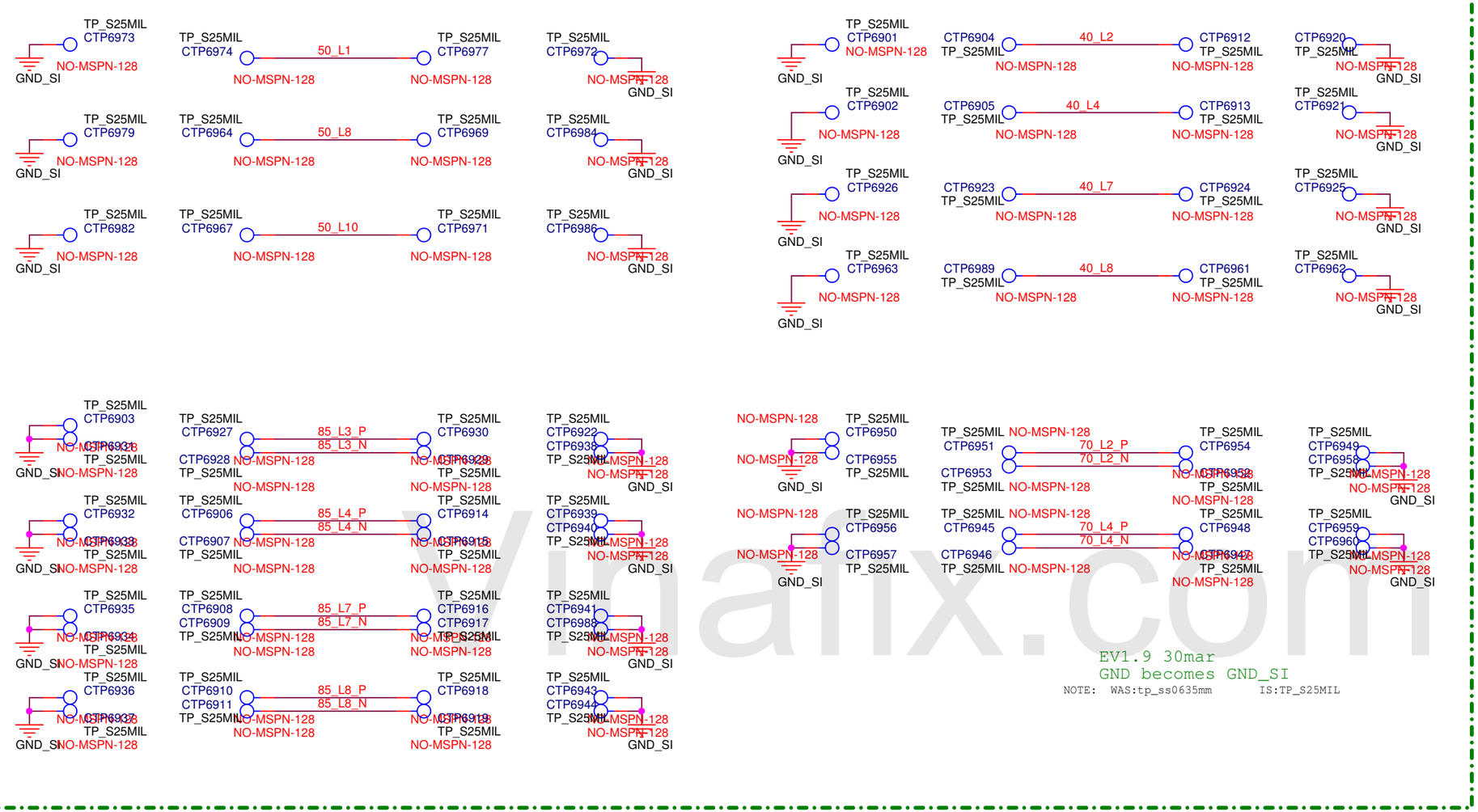


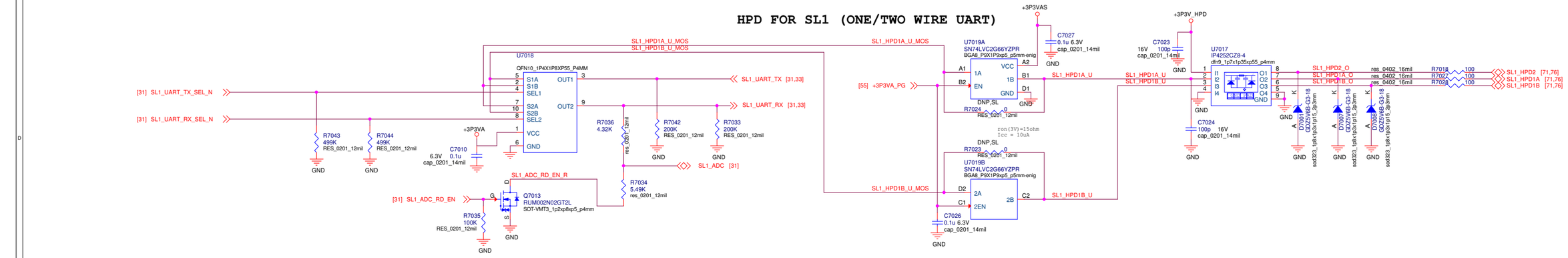
Title: VCORE VCCSA		
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 67 of 76	


+5V
C6833
4.7u 6.3V
cap_0402_26mil
GND
U6815
ISL95808HRZ
dfn9_2x2x1_p5mm-2
VCC
FCCM
PWM
UGATE
PHASE
BOOT
LGATE
GND
MTG
[66] PWM1_B
UGATE_VCCGT1
PHASE_VCCGT1
BOOT_VCCGT1
LGATE_VCCGT1
C6867
25V
0.22u
cap_0603_36mil
Q6812
BSZ065N03LS
mosfet8_3p3x3p3x1p1_p65mm
Q6811
BSZ019N03LS
mosfet8_3p3x3p3x1p1_p65mm
+VCCGT_IN
PC6818
1000p 25V
CAP_0201_14mil
PC6819
10u 10V
cap_0603_36mil
PC6822
10u 10V
cap_0603_36mil
DB,PWR_GT
PR6815
0.010
res_0603_30mil
+VSYS
PMTP6802
SP-tp-c0p381
PMTP6801
SP-tp-c0p381
TDC[A] <= 16A
Icc(max) <= 32A
L6805
0.18uH
17A
ind_7p05x6p6x2_6p05mm
+VCCGT
C6801
C6869
C6870
220u 2V
cap_3_7p3x4p3x1_6p1mm
R6856
3.65K
res_0402_22mil
R6858
100K
res_0402_16mil
DNP,PWR_GT
R6859
100K
res_0402_16mil
EV1.9 WAS:10
R6862
2.2
RES_0402_16mil
[66] ISEN1_B
[66] ISEN2_B
ISUMN_B [66]
ISUMP_B [66]
[66] FCCM_B
+5V
C6872
4.7u 6.3V
cap_0402_26mil
U6811
ISL95808HRZ
dfn9_2x2x1_p5mm-2
[66] PWM2_B
UGATE_VCCGT2
PHASE_VCCGT2
BOOT_VCCGT2
LGATE_VCCGT2
Q6814
BSZ065N03LS
mosfet8_3p3x3p3x1p1_p65mm
Q6813
BSZ019N03LS
mosfet8_3p3x3p3x1p1_p65mm
+VCCGT_IN
PC6820
1000p 25V
CAP_0201_14mil
PC6821
10u 10V
cap_0603_36mil
PC6823
10u 10V
cap_0603_36mil
R6860
100K
res_0402_16mil
R6864
3.65K
res_0402_22mil
DNP,PWR_GT
R6861
100K
res_0402_16mil
EV1.9 WAS:11
R6863
2.2
RES_0402_16mil
C6871
25V
0.22u
cap_0603_36mil
L6806
0.18uH
17A
ind_7p05x6p6x2_6p05mm
Vinafix.com
Title: VCVGT
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 68 of 76

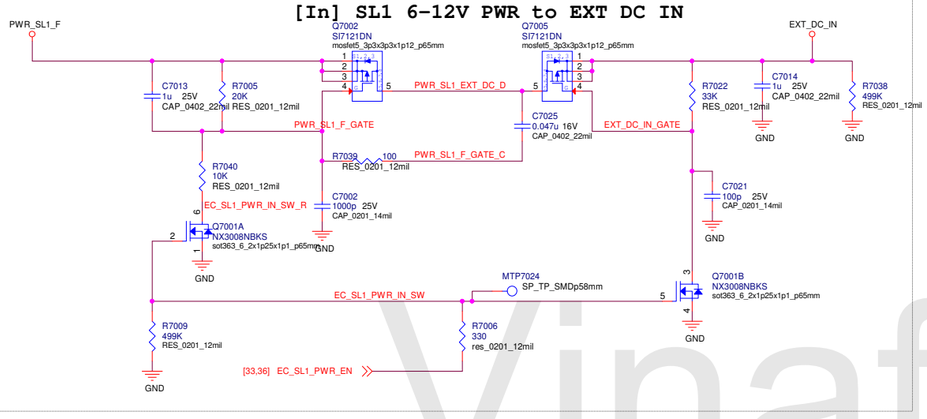


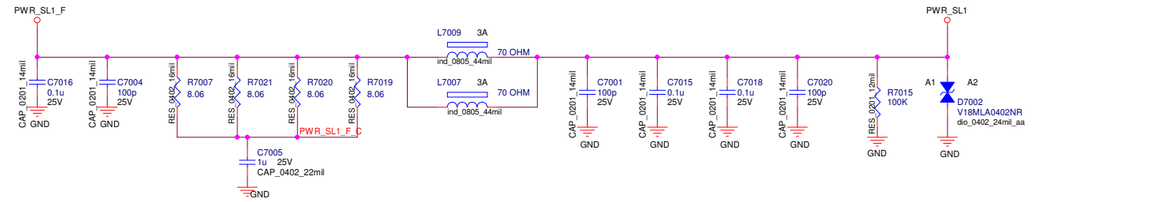
Title:	SI Coupon (was BOOST/GTX REG)		
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 69 of 76		

HPD FOR SL1 (ONE/TWO WIRE UART)

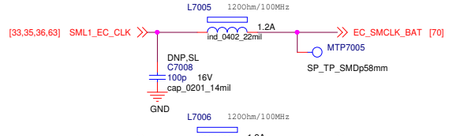


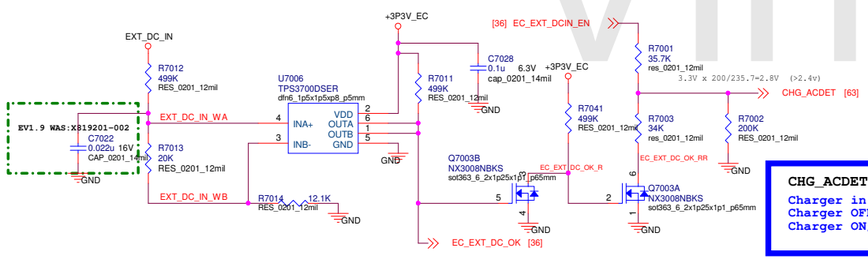
[In] SL1 6-12V PWR to EXT DC IN





Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

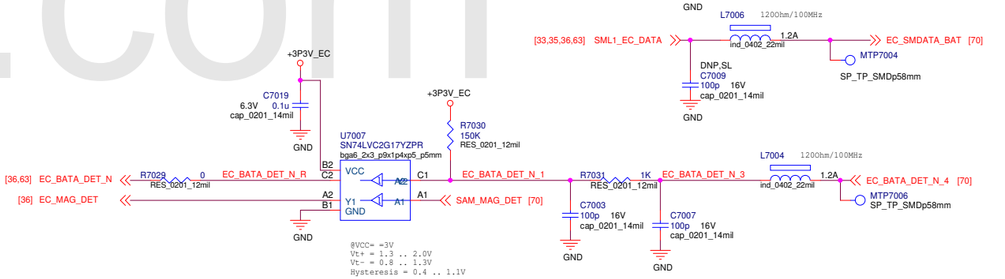


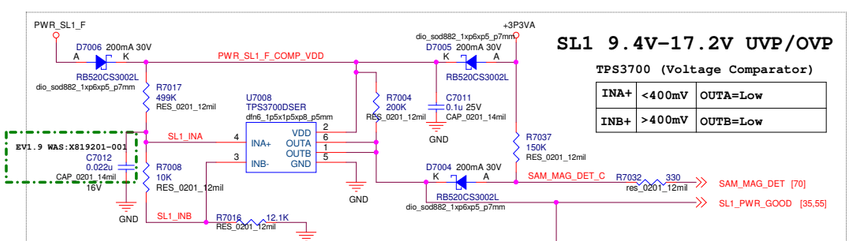


TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

CHG_ACDET	EC_EXT_DCIN_EN	EXT_DC_IN >9V
Charger in RESET	0	X
Charger OFF/ SMBUS EN	1	No
Charger ON/ SMBUS EN	1	YES

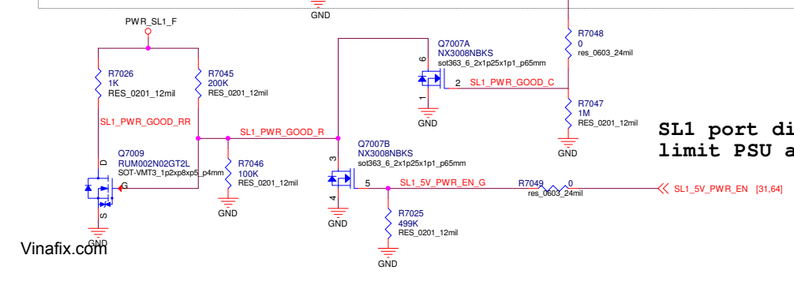




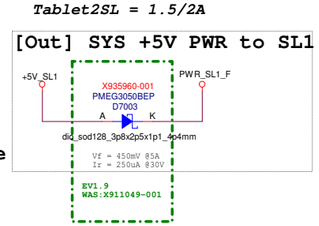
SL1 9.4V-17.2V UVP/OVP

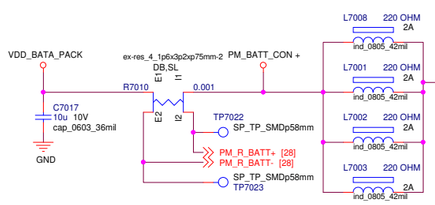
TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

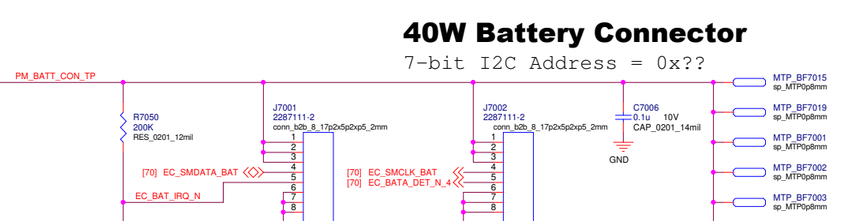


SL1 port discharger limit PSU anti-arc pulse voltage





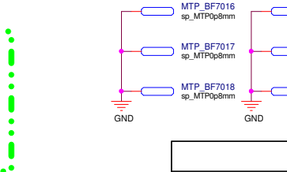
Tablet2SL = 1.5/2A



40W Battery Connector

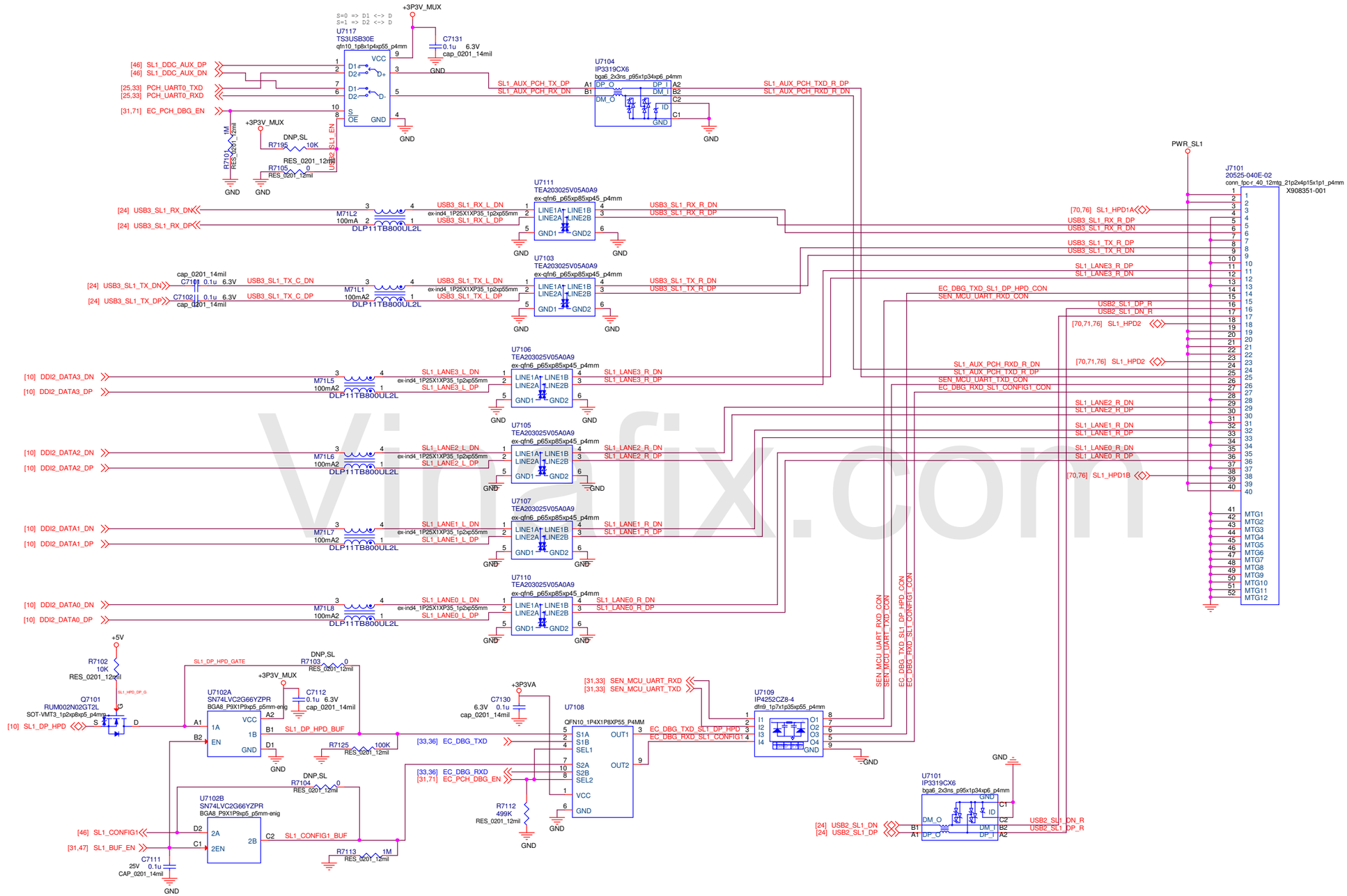
7-bit I2C Address = 0x??

NOTE: 1.7A/pin



5jan14: Place TP's 0.2 inch apart,
Place on component side, near battery.
Must be accessible when battery is installed

Title:	SL1 PWR/ BATT CONN
Microsoft	Engineer: Surface
Size: A2	Project Name: U -- EV 1.90
Rev:	1.90.2
Date:	Monday, May 11, 2015
Sheet	70 of 76



Title: SL1 SIGNALS

Microsoft Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 71 of 76

+3P3VAS
R7201
499K
RES_0201_12mil
+3P3V_HDP_EN
[31] SL1_3P3V_DIS
Q7201
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
R7206
499K
RES_0201_12mil
GND
GND
U7201
RT9728AHZQW
dfn7_2x2xp8_p65mm-2
+3P3V_HDP_EN
EN/EN#
FAULT#
VIN
ILIM
VOUT
GND1
GND2
+3P3V_HPD
Imax=75mA
+3P3V_HPD
MTP7283
SP_TP_SMDp58mm
+3P3VAS
DB,PWR_3P3V_HPD
R7202 0.01
res_0402_22mil
C7209
10u 6.3V
CAP_0402_28mil
R7203 0
RES_0201_12mil
+3P3V_HPD_VIN
+3P3V_HPD_ILIMIT
DNP,PWR_3P3V_HPD
R7204
33K
RES_0201_12mil
C7202
10u 6.3V
CAP_0402_28mil
C7203
10u 6.3V
CAP_0402_28mil
isolated ground on layer 2 to tie Cin GND, Cout GND, and controller PGND together. Then tie this isolated ground plane to main GND under the exposed pads.

+VCC_EDP_BKLT_IN_REG [28]
SP-tp-c0p381
PMTP7221
SP-tp-c0p381
PMTP7222
+VSYS
Q7203
IRLML6402
SOT23_2p9X1P3X1P12_P95MM
DB,PWR_BKLT
R7209 0.01
res_0402_22mil
R7213
100K
RES_0201_12mil
C7224
1000p 25V
CAP_0201_14mil
DNP,PWR_BKLT
C7225
0.1u 10V
CAP_0201_14mil
BKLT_EDP_IN_DRI
R7212
200K
RES_0201_12mil
R7210
4.99K
RES_0201_12mil
R7211
4.99K
RES_0201_12mil
jks 15dec14:
EffCap (10u@8.7V) = 1.4uF
EffCap (22u@8.7V) = 3.6uF
Novatek: Cin = 4.7uF
+VCC_EDP_BKLT_IN
C7210
22u 10V
cap_0603_40mil
C7201
10u 10V
cap_0603_36mil
+VCC_EDP_BKLT_IN
Imax=??A
TDC=??A
Novatek 15dec14: Ipeak(Vin=6V) = 1.144A
X913828-001
PMEG6030EVP
D7201
L7204 10uH 2.5A
ind_5p4x5p2x1p8mm
X911507-001
Rdc = 154mOhm
BKLT_LX
dio_sod128_3p8x2p5x1p1_4p4mm
+VCC_EDP_BKLT_OUT_R
R7333 0
RES_0402_16mil
+VCC_EDP_BKLT_OUT
MTP7201
SP_TP_SMDp58mm
jks 15dec14:
EffCap (10u@28V) = 1.5uF
EffCap (4.7u@28V) = 0.8uF
Novatek: Cout = 4.7uF
R7230
681K
res_0201_12mil
R7231
20K
RES_0201_12mil
C7206 10u 50V cap_1206_72mil
C7207 10u 50V cap_1206_72mil
DNP,PWR_BKLT
C7208 10u 50V cap_1206_72mil
DNP,PWR_BKLT
EV1.9
was:INSTALL
+VCC_EDP_BKLT_IN_DISC
Q7202B
SSM6N15AFU
SOT363_6_2x1p25X1_P65MM
R7207 10
res_0603_22mil
+VCC_BKLT
C7204 1u 10V
CAP_0402_22mil
EV1.9
WAS 0603
EV1.9
WAS NNT50273QG/A
U7202
MP3388SGR
qfn25_4x4xp9_p5mm
VIN
EN
OSC
PWMI
ISET
PWMO
COMP
PGND2
PGND1
AGND1
AGND2
VCC
SW2
SW1
OVP
LED8
LED7
LED6
LED5
LED4
LED3
LED2
LED1
FPWM
VFAULT
C7255
1u 10V
CAP_0402_22mil
BKLT_OVS
BKLT_SC1
BKLT_NG2
PWR_BKLT
C7254 150p 50V
CAP_0402_22mil
EV1.9 install
DNP,PWR_BKLT
R7239
1K
RES_0201_12mil
BKLT_EDP_IN_DRI_R
[10] L_BKLTEN
R7208 1K
RES_0201_12mil
BKLT_EN
MTP7224
MTP7225
R7228 10K
RES_0201_12mil
BKLKT_OSC
BKLT_PWM_R
[57] L_BKLT_CTRL_OUT
R7226 1K
RES_0201_12mil
R7227 X936061-001 90.9K
res_0201_12mil
BKLT_ISET
R7232 0.068u
cap_0201_14mil
BKLT_MIX
C7211 0.47u
cap_0201_14mil
BKLT_COMP_R
R7229 X933171-001 270
res_0201_12mil
BKLT_COMP
+3P3V_PANEL
R7215 22K
RES_0201_12mil
R7214
100K
RES_0201_12mil
DNP,PWR_BKLT
C7253
0.1u 6.3V
cap_0201_14mil
Q7202A
SSM6N15AFU
SOT363_6_2x1p25X1_P65MM
R7218 0 BKLT_FB8 [57,72]
R7219 0 BKLT_FB7 [57,72]
R7220 0 BKLT_FB6 [57,72]
R7221 0 BKLT_FB5 [57,72]
R7222 0 BKLT_FB4 [57,72]
R7223 0 BKLT_FB3 [57,72]
R7224 0 BKLT_FB2 [57,72]
R7225 0 BKLT_FB1 [57,72]
MTP7202 SP_TP_SMDp58mm BKLT_FB1 [57,72]
MTP7203 SP_TP_SMDp58mm BKLT_FB2 [57,72]
MTP7206 SP_TP_SMDp58mm BKLT_FB3 [57,72]
MTP7210 SP_TP_SMDp58mm BKLT_FB4 [57,72]
MTP7204 SP_TP_SMDp58mm BKLT_FB5 [57,72]
MTP7205 SP_TP_SMDp58mm BKLT_FB6 [57,72]
MTP7207 SP_TP_SMDp58mm BKLT_FB7 [57,72]
MTP7208 SP_TP_SMDp58mm BKLT_FB8 [57,72]
GND

Title: +3P3V_HPD/LCD backlight
Microsoft
Engineer: Surface
Size: B
Project Name: U -- EV 1.90
Rev: 1.90.2
Date: Monday, May 11, 2015
Sheet 72 of 76

BLADE Connector

+5V_KB_CONN
Imax = 0.5A

SP_TP_SMDp58mm MTP7314
SP_TP_SMDp58mm MTP7315
SP_TP_SMDp58mm MTP7316
SP_TP_SMDp58mm MTP7317

[74] BLADE_TX_USB_D+
[74] BLADE_RX_USB_D-
[74] +5V_SHA_CONN_UART_RX_CONN
[74] BLADE_AUTH_DATA_UART_TX_CONN

J7302
2287111-2
conn_b2b_8_17p2x5p2xp5_2mm
X904496-001
pins 1 2 3 4 5 6 7 8
GND

MTP_BF7305 sp_MTP0p8mm
MTP_BF7306 sp_MTP0p8mm
MTP_BF7313 sp_MTP0p8mm
MTP_BF7314 sp_MTP0p8mm
GND

MTP_BF7309 sp_MTP0p8mm
MTP_BF7310 sp_MTP0p8mm
MTP_BF7311 sp_MTP0p8mm
MTP_BF7312 sp_MTP0p8mm

FANG_PWR
D7301 A1 A2 V18MLA0402NR dio_0402_24mil_aa
R7301 100K RES_0201_12mil
C7301 0.1u 25V CAP_0402_22mil
GND

L7301 220 OHM 2A ind_0805_42mil
FANG_PWR_F

+5V_KB_CONN
L7304 120Ohm/100MHz ind_0402_22mil 1.2A
+5V_KB
C7302 0.1u 6.3V cap_0201_14mil
D7302 A1 A2 V18MLA0402NR dio_0402_24mil_aa
GND

SP_TP_SMDp58mm MTP7319
SP_TP_SMDp58mm MTP7318
GND

J7303
2287111-2
conn_b2b_8_17p2x5p2xp5_2mm
X904496-001
pins 1 2 3 4 5 6 7 8
GND

eFang power = 3.5A max
using +1 rule

[In] BLADE 6-12V PWR to EXT DC IN

Imax=4.5A

EXT_DC_IN
Q7303 SI7121DN mosfet5_3p3x3p3x1p12_p65mm
R7302 33K RES_0201_12mil
EXT_DC_IN_FET_GATE
DNP,BLADE C7310 1000p 25V CAP_0201_14mil
GND

Q7302A NX3008NBKS sot363_6_2x1p25x1p1_p65mm
GND

Q7301 SI7121DN mosfet5_3p3x3p3x1p12_p65mm
FANG_DRAIN_FET_PWR
DNP,BLADE C7303 25V 0.047u CAP_0402_22mil
DNP,BLADE R7318 100 RES_0201_12mil

FANG_PWR_F
EV1.9 WAS 0603
C7304 1u 25V CAP_0402_22mil
FANG_PWR_FET_GATE
R7304 20K RES_0201_12mil
R7310 10K RES_0201_12mil
DNP,BLADE C7309 25V 1000p CAP_0201_14mil
GND

EC_BLADE_PWR_IN_SW
Q7302B NX3008NBKS sot363_6_2x1p25x1p1_p65mm
R7308 499K RES_0201_12mil
MTP7301 SP_TP_SMDp58mm
R7303 330 RES_0402_16mil
[33,36] EC_BLADE_PWR_EN
GND

[31] BLADE_AUTH_PWR_EN
GND
R7311 1M RES_0201_12mil

+5VA_SHA
R7307 100K RES_0201_12mil
SHA_OC#
SHA_VIN
SHA_ILIMIT

Rds(on)=120mOhm (typ)
Iq=170uA

U7301
RT9728AHZQW
dfn7_2x2xp8_p65mm-2
EN/EN# FAULT# VIN ILIM VOUT GND1 GND2

+5V_SHA_CONN
+5V_SHA_CONN
Imax=75mA
C7305 0.1u 6.3V cap_0201_14mil
R7305 2.2K RES_0201_12mil
C7307 1u 6.3V CAP_0201_14mil
C7308 22p 25V CAP_0201_14mil
GND

+5VA_SHA
DB,BLADE R7314 0.01 res_0402_22mil
PMTP7321 SP-tp-c0p381
PMTP7322 SP-tp-c0p381
BLADE R7313 0 RES_0402_16mil
C7306 10u 6.3V cap_0603_38mil
GND
EV1.9
CHG MSPN

DNP,BLADE R7319 33K RES_0201_12mil
GND

Imax = 1.4A
50mA <= ILIM(connected to VIN) <=100mA

+VSYS
L7313 30OHMS @100MHZ 1.7A IND_0402_24mil
L7312 30OHMS @100MHZ 1.7A IND_0402_24mil
FANG_PWR_IN
C7312 2.2u CAP_0603_38mil 25V
C7313 0.1u CAP_0201_14mil 25V
GND

V(operating) = 4.5 to 13.8 Max

U7302
TPS2592ZADRCR
son11_3x3x1_p5mm
VIN3 VIN2 VIN1 OUT1 OUT2 OUT3 BFET EN/UVLO dV/dT ILIM GND_PAD

current = 3A
FANG_PWR_OUT
C7316 0.1u CAP_0201_14mil 25V
C7317 2.2u CAP_0603_38mil 25V
GND

X935960-001
PMEG3050BEP
D7303 A K
dio_sod128_3p8x2p5x1p1_4p4mm
Vf = 450mV @5A
Ir = 250uA @30V
EV1.9
WAS:X911049-001

FANG_PWR_F
C7315 2.2u CAP_0603_38mil 25V
GND

LTE eFANG PWR = 2.10A(min)
2.47A(nom)
2.84A(max)

[36] EC_BLADE_5VLDSW_EN
R7309 0 RES_0201_12mil
R7315 100K RES_0201_12mil
C7314 1000p CAP_0201_14mil 25V 10%
C7311 1000p CAP_0201_14mil 25V 10%
GND

FANG_REG_ILIM
R7316 59K RES_0201_12mil
GND
MTP7320 SP_TP_SMDp58mm

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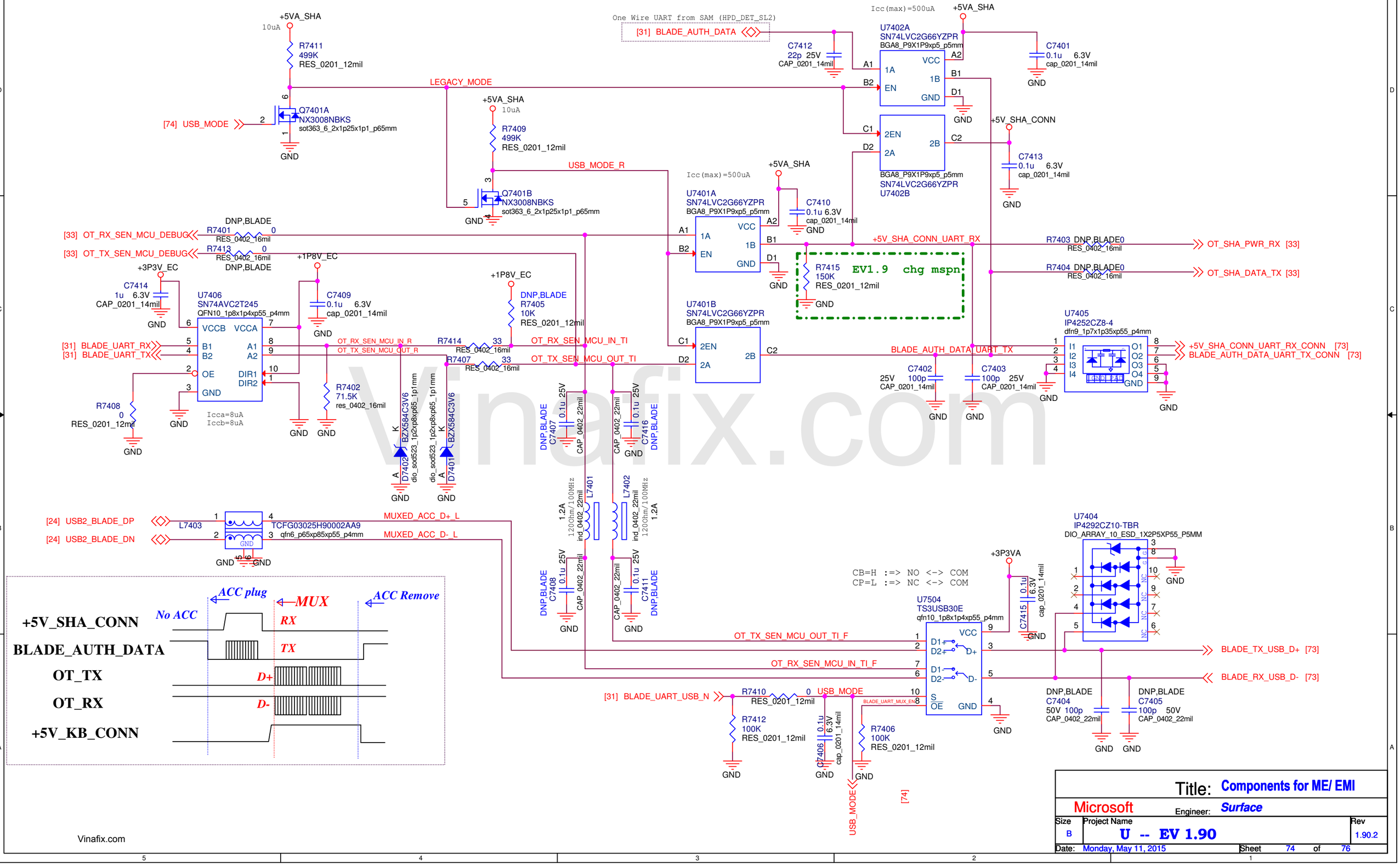
Title:	BLADE PWR	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 73 of 76	


+5VA_SHA
10uA
R7411
499K
RES_0201_12mil
LEGACY_MODE
[74] USB_MODE
Q7401A
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
GND
+5VA_SHA
10uA
R7409
499K
RES_0201_12mil
USB_MODE_R
Q7401B
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
GND
One Wire UART from SAM (HPD_DET_SL2)
[31] BLADE_AUTH_DATA
C7412
22p 25V
CAP_0201_14mil
Icc(max)=500uA
+5VA_SHA
U7402A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
VCC
1A
1B
EN
GND
A1
B2
A2
B1
D1
C7401
0.1u 6.3V
cap_0201_14mil
GND
C1
D2
2EN
2A
2B
C2
U7402B
+5V_SHA_CONN
C7413
0.1u 6.3V
cap_0201_14mil
GND
Icc(max)=500uA
+5VA_SHA
U7401A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
C7410
0.1u 6.3V
cap_0201_14mil
GND
U7401B
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
+5V_SHA_CONN_UART_RX
R7415
150K
RES_0201_12mil
EV1.9 chg mspn
GND
DNP,BLADE
[33] OT_RX_SEN_MCU_DEBUG
R7401
RES_0402_16mil
[33] OT_TX_SEN_MCU_DEBUG
R7413
RES_0402_16mil
+3P3V_EC
C7414
1u 6.3V
CAP_0201_14mil
U7406
SN74AVC2T245
QFN10_1p8x1p4xp55_p4mm
VCCB VCCA
B1 A1
B2 A2
OE DIR1
DIR2
GND
Icca=8uA
Iccb=8uA
+1P8V_EC
C7409
0.1u 6.3V
cap_0201_14mil
R7402
71.5K
res_0402_16mil
R7408
0
RES_0201_12mil
[31] BLADE_UART_RX
[31] BLADE_UART_TX
OT_RX_SEN_MCU_IN_R
OT_TX_SEN_MCU_OUT_R
+1P8V_EC
DNP,BLADE
R7405
10K
RES_0201_12mil
R7414
33
RES_0402_16mil
R7407
33
RES_0402_16mil
OT_RX_SEN_MCU_IN_TI
OT_TX_SEN_MCU_OUT_TI
BZX584C3V6
dio_sod523_1p2xp8xp65_1p1mm
D7402
D7401
DNP,BLADE
C7407
0.1u 25V
CAP_0402_22mil
C7416
DNP,BLADE
C7408
0.1u 25V
CAP_0402_22mil
C7411
DNP,BLADE
L7403
TCFG03025H90002AA9
qfn6_p65xp85xp55_p4mm
[24] USB2_BLADE_DP
[24] USB2_BLADE_DN
MUXED_ACC_D+_L
MUXED_ACC_D-_L
L7401
L7402
1.2A
120Ohm/100MHz
ind_0402_22mil
U7405
IP4252CZ8-4
dfn9_1p7x1p35xp55_p4mm
I1 I2 I3 I4
O1 O2 O3 O4
GND
+5V_SHA_CONN_UART_RX_CONN [73]
BLADE_AUTH_DATA_UART_TX_CONN [73]
BLADE_AUTH_DATA_UART_TX
C7402
25V 100p
CAP_0201_14mil
C7403
100p 25V
CAP_0201_14mil
R7403 DNP,BLADE0
RES_0402_16mil
OT_SHA_PWR_RX [33]
R7404 DNP,BLADE0
RES_0402_16mil
OT_SHA_DATA_TX [33]
U7504
TS3USB30E
qfn10_1p8x1p4xp55_p4mm
CB=H :=> NO <-> COM
CP=L :=> NC <-> COM
+3P3VA
C7415
0.1u 6.3V
cap_0201_14mil
OT_TX_SEN_MCU_OUT_TI_F
OT_RX_SEN_MCU_IN_TI_F
D1+ D2+ D+
D1- D2- D-
S OE
U7404
IP4292CZ10-TBR
DIO_ARRAY_10_ESD_1X2P5XP55_P5MM
BLADE_TX_USB_D+ [73]
BLADE_RX_USB_D- [73]
DNP,BLADE
C7404
50V 100p
CAP_0402_22mil
DNP,BLADE
C7405
100p 50V
CAP_0402_22mil
[31] BLADE_UART_USB_N
R7410
0 USB_MODE
RES_0201_12mil
R7412
100K
RES_0201_12mil
C7406
0.1u 6.3V
cap_0201_14mil
R7406
100K
RES_0201_12mil
BLADE_UART_MUX_EN
USB_MODE
[74]
ACC plug
MUX
ACC Remove
No ACC
RX
TX
D+
D-
+5V_SHA_CONN
BLADE_AUTH_DATA
OT_TX
OT_RX
+5V_KB_CONN
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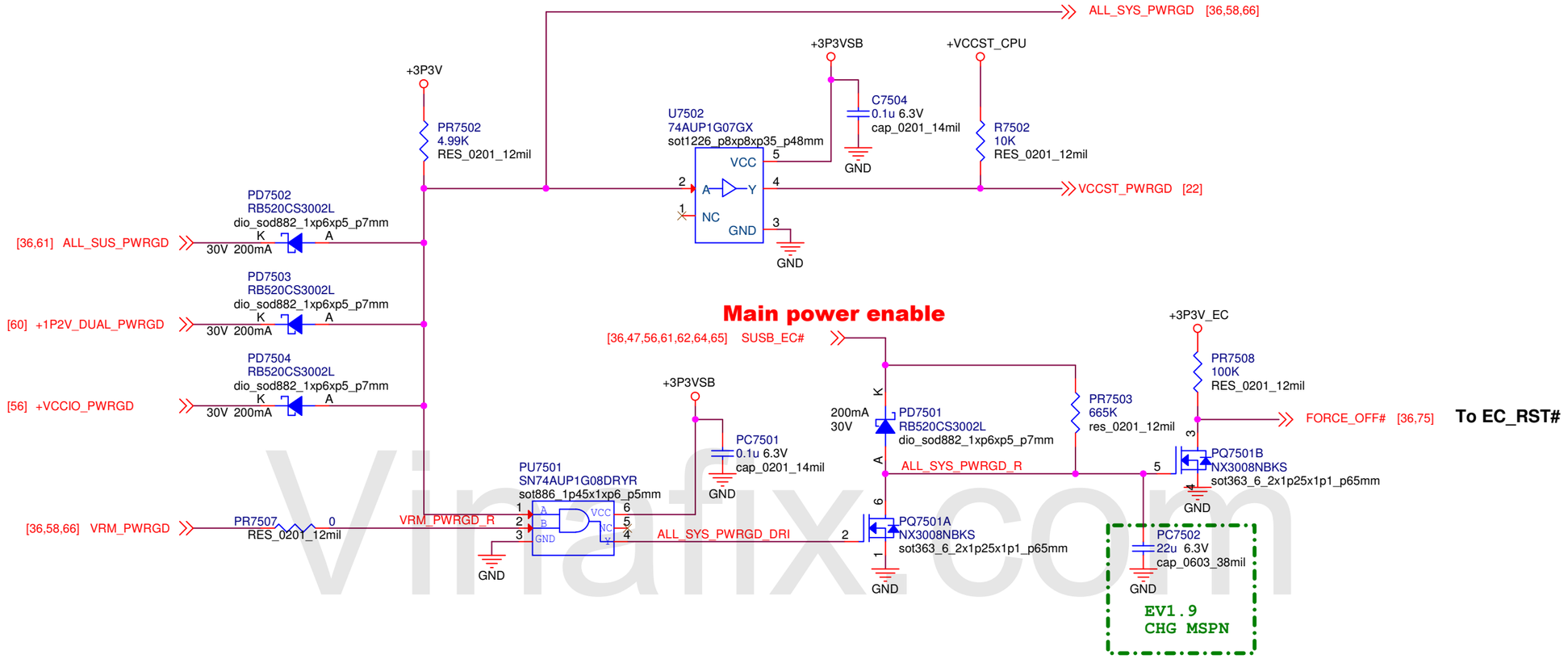
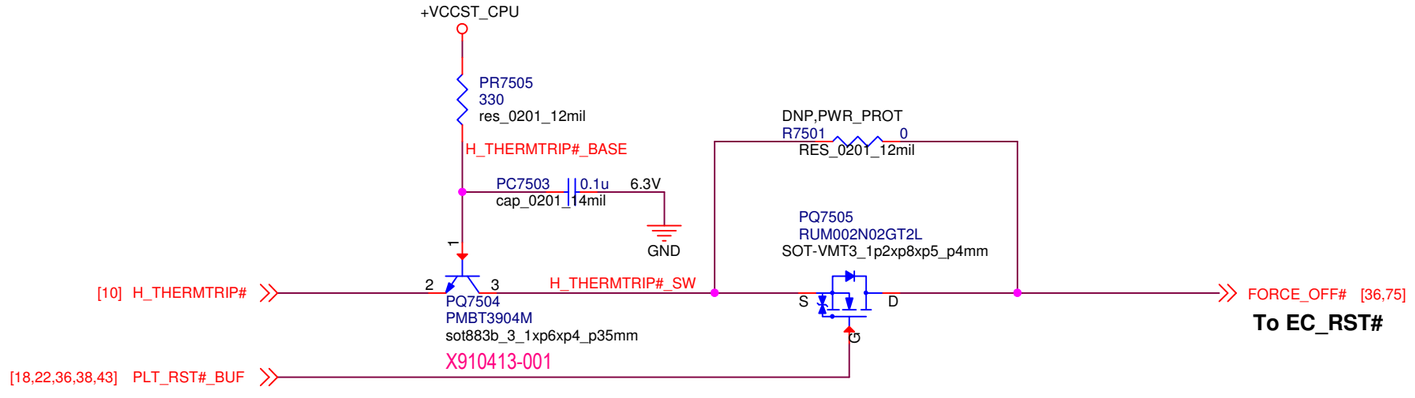
Title: Components for ME/ EMI
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 74 of 76





Title:	Power Protect	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 75 of 76	

SFT1 SHIELD 1
MSPN = X933943-001
SHIELD, FRAME, T1, V1
PCB Footprint = shield-X933943-001

SFT2 SHIELD 1
MSPN = X933944-001
SHIELD, FRAME, T2, V1
PCB Footprint = shield-X933944-001

SFT3 SHIELD 1
MSPN = X933945-001
SHIELD, FRAME, T3, V1
PCB Footprint = shield-X933945-001

SFT4 SHIELD 1
MSPN = X933946-001
SHIELD, FRAME, T4, V1
PCB Footprint = shield-X933946-001

SFT5 SHIELD 1
MSPN = X933947-001
SHIELD, FRAME, T5, V1
PCB Footprint = shield-X933947-001

SFT6 SHIELD 1
MSPN = X933948-001
SHIELD, FRAME, T6, V1
PCB Footprint = shield-X933948-001

SFT7 SHIELD 1
MSPN = X933949-001
SHIELD, FRAME, T7, V1
PCB Footprint = shield-X933949-001

GND

H7601
Value = X934367-001
washer-X934367-001
GND

H7602
Value = X934367-001
washer-X934367-001
GND

EV1.9 Add

SFT8 SHIELD 1
MSPN = X933950-001
SHIELD, FRAME, T8, V1
PCB Footprint = shield-X933950-001

SFT9 SHIELD 1
MSPN = X933951-001
SHIELD, FRAME, T9, V1
PCB Footprint = shield-X933951-001

SFT10 SHIELD 1
MSPN = X933952-001
SHIELD, FRAME, T10, V1
PCB Footprint = shield-X933952-001

SFT11 SHIELD 1
MSPN = X933953-001
SHIELD, FRAME, T11, V1
PCB Footprint = shield-X933953-001

SFT12 SHIELD 1
MSPN = X933954-001
SHIELD, FRAME, T12, V1
PCB Footprint = shield-X933954-001

GND

J7601
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

J7602
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

J7603
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

J7604
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

EV1.9 Add

SFB1 DNP,MECH_SHIELD SHIELD 1
MSPN = X933968-001
SHIELD, FRAME, B1, V1
PCB Footprint = shield-X933968-001

SFB2 MECH_SHIELD SHIELD 1
MSPN = X933969-001
SHIELD, FRAME, B2, V1
PCB Footprint = shield-X933969-001

SFB3 DNP,MECH_SHIELD SHIELD 1
MSPN = X933970-001
SHIELD, FRAME, B3, V1
PCB Footprint = shield-X933970-001

SFB4 MECH_SHIELD SHIELD 1
MSPN = X933971-001
SHIELD, FRAME, B4, V1
PCB Footprint = shield-X933971-001

SFB5 DNP,MECH_SHIELD SHIELD 1
MSPN = X933972-001
SHIELD, FRAME, B5, V1
PCB Footprint = shield-X933972-001

SFB6 MECH_SHIELD SHIELD 1
MSPN = X933973-001
SHIELD, FRAME, B6, V1
PCB Footprint = shield-X933973-001

SFB7 DNP,MECH_SHIELD SHIELD 1
MSPN = X933974-001
SHIELD, FRAME, B7, V1
PCB Footprint = shield-X933974-001

GND

SFB8 DNP,MECH_SHIELD SHIELD 1
MSPN = X933975-001
SHIELD, FRAME, B8, V1
PCB Footprint = shield-X933975-001

SFB9 MECH_SHIELD SHIELD 1
MSPN = X933976-001
SHIELD, FRAME, B9, V1
PCB Footprint = shield-X933976-001

SFB10 MECH_SHIELD SHIELD 1
MSPN = X933976-001
SHIELD, FRAME, B9, V1
PCB Footprint = shield-X933976-001

GND

[36,55] VCCDSW_EN >> MTP7669 SP_TP_SMDp58mm

[70,71] SL1_HPD2 <> MTP76101 SP_TP_SMDp58mm

[70,71] SL1_HPD1B <> MTP7682 SP_TP_SMDp58mm

[70,71] SL1_HPD1A <> MTP7684 SP_TP_SMDp58mm

MP7605
Value = X935458-001
MSPN = X935458-001
PCB Footprint = sp-pem_nut-x935458-001-1
GND

EV1.9 was:X912411-001
gold plating option provided
for both top and bottom layers

EV1.9
remove fence
x930139-001

MP7601
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

MP7602
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

EV1.9 was X911169-001

MP7603
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

MP7604
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

PWR_SL1
MTTP_BF7670 sp_MTP0p8mm
MTTP_BF7653 sp_MTP0p8mm
MTTP_BF7654 sp_MTP0p8mm
MTTP_BF7655 sp_MTP0p8mm
MTTP_BF76105 sp_MTP0p8mm
MTTP_BF76103 sp_MTP0p8mm

PWR_SL1
MTP_BF7670 sp_MTP0p8mm
MTP_BF7653 sp_MTP0p8mm
MTP_BF7654 sp_MTP0p8mm
MTP_BF7655 sp_MTP0p8mm
MTP_BF76105 sp_MTP0p8mm
MTP_BF76103 sp_MTP0p8mm

MTP_BF7656 sp_MTP0p8mm GND
MTP_BF7671 sp_MTP0p8mm GND
MTP_BF7672 sp_MTP0p8mm GND
MTP_BF7673 sp_MTP0p8mm GND
MTP_BF76104 sp_MTP0p8mm GND
MTP_BF76102 sp_MTP0p8mm GND

MTTP_BF7656 sp_MTP0p8mm GND
MTTP_BF7671 sp_MTP0p8mm GND
MTTP_BF7672 sp_MTP0p8mm GND
MTTP_BF7673 sp_MTP0p8mm GND
MTTP_BF76104 sp_MTP0p8mm GND
MTTP_BF76102 sp_MTP0p8mm GND

+0P85VSB MTP7686 SP_TP_SMDp58mm
+VCCGT MTP7652 SP_TP_SMDp58mm
+VCCSA MTP7657 SP_TP_SMDp58mm
+VCCIO MTP7662 SP_TP_SMDp58mm
+VCCST_CPU MTP7661 SP_TP_SMDp58mm
+VCCSTG MTP7659 SP_TP_SMDp58mm
+VCCEDRAM MTP7658 SP_TP_SMDp58mm
+VCCEOPIO MTP7660 SP_TP_SMDp58mm
+1P2V_DUAL MTP7611 SP_TP_SMDp58mm
+V_VDDQ_VTT MTP7612 SP_TP_SMDp58mm
+VCC_CORE MTP7613 SP_TP_SMDp58mm
+VDDQ_VREF TP7614 SP_TP_SMDp58mm

PTH18 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH1 c1p35x0p75d mtg_pin_c1p35x0p75d
PTH2 c1p35x0p75d mtg_pin_c1p35x0p75d
PTH3 c1p35x0p75d mtg_pin_c1p35x0p75d
GND

EV1.9 remove PTH4-PTH9

PTH19 MSPN = NO-MSPN-119 MTG_pin_slot-3p00x3p50_2p50X3p00d
GND

EV1.9 remove PTH20 slot-3p00x3p50_2p50X3p0

EV1.9 remove PTH10 MH31x2.5d

PTH11 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH12 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH13 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH14 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH15 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH16 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH17 MH3.1x2.5d mtg_hole_3p10x2p50d
GND

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Title:	Test Point		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 76 of 76		