BRENDAN LONG

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https://github.com/bccbrendan

TECHNICAL STRENGTHS

Skills	Process evolution through better CI/CD, mentoring, training, on-boarding documentation
Languages	C++, Python, Rust, C, C#
Technology	boost, asio, gsl, gtest, CMake, I3C, UART, SPI, JTAG, XML, JSON
Tools	Git, Conan, Coverity, valgrind, CI/CD (Jenkins, TeamCity, GitHub Actions, GitLab)

EXPERIENCE

Intel 2023 - Present
Staff Software Engineer *Austin, TX*

- Regularly mentor and train 3-4 engineers on multiple teams through 1:1s and pair programming.
- Curate team task and issues backlog, matching task to team member's individual expertise
- Set up and managed automatic static code analysis for security, drove a reduction of 90% of issues
- DRA for resolving debug tool and silicon integration problem in 3 products, and identifying test strategy to prevent it in future
- 2023 Project awards for contributing to successful silicon power-on, for enabling debug tools in record time, and for executing silicon validation test plan 8 weeks ahead of schedule.

Intel May 2019 - 2023
Senior Software Developer *Austin, TX*

- Led team transition to Git as software repository tool, automated migration process, administered permissions, and led trainings
- Gathered requirements and led development of debug tools adapting to new chip architectures and debug protocols - two Project awards in 2022
- As product owner for pre-silicon debug tools, gathered requirements, planned features, and balanced work priorities in a group of 4 developers to deliver tools across the entire product roadmap. Received 2021 DRA for integrating debug tools with new I3C protocol.
- Mentored 3-4 engineers through weekly 1:1 tech talks, led several multi-team sessions on git and silicon debug technologies. Received 2021 SRA for training new remote team members.
- Reduced debug tool costs by adapting tool suite software and hardware to run on Raspberry Pi - received 2020 Project Award.
- Developed and verified debug tools and supported record time successful power-on of discrete graphics product. Received 2020 DRA.
- Delivered debug tools for next-gen server cpu on-time and with exceptional stability for power-on. Received Q1'2019 DRA.

Intel June 2012 - April 2019
Software Developer *Austin, TX*

- Designed and developed software libraries bridging silicon debug software to pre-silicon emulation models. Used to verify new products in every market segment. Received 3 Division Recognition Awards and one Special Recognition Award.
- Created in-house software replacement for 3rd party hardware tools in 2018, saving an estimated total $5.75M; received one DRA and one SRA.
- Developed several key features of the software connecting debug tools to Intel's Direct Connect Interrface. Received a Q1'2016 DRA.

· Drove company-wide adoption of 3rd party debug tools by developing compatibility software for existing use cases. Developed and provided training for new tools. Received Q2'13 Transformation Award, Q3'13 DRA, Q4'14 DRA, and Q4'14 "Above and Beyond" SRA

Intel January 2010 - June 2012
Validation Engineer Intern *Austin, TX*

· Developed embedded HTTP server to provide remote debug access to silicon validation platforms. Received Q2/13 Excellence award for silicon power-on support.
· Developed Linux kernel module to provide PCI access to FPGA platform for hybrid simulation model.

Schlumberger Summer 2009, Summer 2010
Software Engineering Intern *Houstin, TX*

· Enhanced cable tension monitoring/prediction system for oil well devices. Implemented features requested by oilfield engineers and reduced risk of equipment loss.
· Created prototype document classification and search system to enable efficient search of unstructured data.

EDUCATION

University of Texas, Austin
M.S. in Software Engineering
B.S. in Electrical and Computer Engineering