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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
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-- Create Date: 09/17/2021 10:19:29 PM
-- Design Name:
-- Module Name: fullsubtractor - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fullsubtractor is
    port( A : in STD_LOGIC;
          B : in STD_LOGIC;
          Bin : in STD_LOGIC;
          D : out STD_LOGIC;
          Bout : out STD_LOGIC);
end fullsubtractor;

architecture Behavioral of fullsubtractor is

begin

d <= (A xor B) xor Bin;
bout <= ((not A) and (B or Bin)) or (B and Bin);

end Behavioral;
```