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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
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-- Create Date: 09/17/2021 10:28:58 PM
-- Design Name:
-- Module Name: test_sub - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity test_sub is
--  Port ( );
end test_sub;

architecture Behavioral of test_sub is

    component fullsubtractor is
        Port ( A : in STD_LOGIC;
               B : in STD_LOGIC;
               Bin : in STD_LOGIC;
               D : out STD_LOGIC;
               Bout : out STD_LOGIC);
    end component;

    signal A, B, Bin, D, Bout  :  std_logic;
begin

    tb : fullsubtractor port map ( A => A,
                                   B => B,
                                   Bin => Bin,
                                   D => D,
                                   Bout => Bout);

    process
    begin
        A <= '0';
```

```
        B <= '0';
        Bin <= '0';
        wait for 100ns;

        A <= '0';
        B <= '0';
        Bin <= '1';
        wait for 100ns;

        A <= '0';
        B <= '1';
        Bin <= '0';
        wait for 100ns;

        A <= '0';
        B <= '1';
        Bin <= '1';
        wait for 100ns;

        A <= '1';
        B <= '0';
        Bin <= '0';
        wait for 100ns;

        A <= '1';
        B <= '0';
        Bin <= '1';
        wait for 100ns;

        A <= '1';
        B <= '1';
        Bin <= '0';
        wait for 100ns;

        A <= '1';
        B <= '1';
        Bin <= '1';
        wait for 100ns;

        wait;
    end process;

end Behavioral;
```