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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 10/06/2021 09:48:51 PM
-- Design Name:
-- Module Name: test4bitsubtractor - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity test4bitsubtractor is
--  Port ( );
end test4bitsubtractor;

architecture Behavioral of test4bitsubtractor is
    component Sub4bit is
        Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
               B : in STD_LOGIC_VECTOR (3 downto 0);
               D : out STD_LOGIC_VECTOR (3 downto 0);
               Bout : out STD_LOGIC);
    end component;

    signal A, B, D : std_logic_vector (3 downto 0);
    signal Bout : std_logic;
begin

    tb : Sub4bit port map(A => A,
                          B => B,
                          D => D,
                          Bout => Bout);

    process
    begin
        A <= "0000";
        B <= "0000";
        wait for 100ns;
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        A <= "0010";
        B <= "0001";
        wait for 100ns;

        A <= "0001";
        B <= "0001";
        wait for 100ns;

        A <= "1111";
        B <= "0001";
        wait for 100ns;

        wait;
     end process;
end Behavioral;
```