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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 10/10/2021 06:45:17 PM
-- Design Name:
-- Module Name: Mux2to1WS - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux2to1WS is
    port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           S0 : in STD_LOGIC;
           Z : out STD_LOGIC);
end Mux2to1WS;

architecture Behavioral of Mux2to1WS is
    signal s : std_logic;
begin

    s <= S0;
    with s select
    Z <= A when '0',
         B when '1',
        '0' when others;

end Behavioral;
```