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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
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-- Create Date: 10/06/2021 08:33:25 PM
-- Design Name:
-- Module Name: test4bitadder - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity test4bitadder is
--  Port ( );
end test4bitadder;

architecture Behavioral of test4bitadder is
    component Adder4bit is
        Port ( num1 : in STD_LOGIC_VECTOR (3 downto 0);
               num2 : in STD_LOGIC_VECTOR (3 downto 0);
               Sum : out STD_LOGIC_VECTOR (3 downto 0);
               Cout : out STD_LOGIC);
    end component;

    signal num1, num2, sum : std_logic_vector (3 downto 0);
    signal cout : std_logic;
begin

    tb : adder4bit port map(num1 => num1,
                            num2 => num2,
                            sum => sum,
                            cout => cout);

    process
    begin
        num1 <= "0000";
        num2 <= "0000";
        wait for 100ns;
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        num1 <= "0010";
        num2 <= "0001";
        wait for 100ns;

        num1 <= "0001";
        num2 <= "0001";
        wait for 100ns;

        num1 <= "1111";
        num2 <= "0001";
        wait for 100ns;

        wait;
     end process;
end Behavioral;
```