```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 10/10/2021 06:56:49 PM
-- Design Name:
-- Module Name: Mux2To1WS_Tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux2To1WS_Tb is
--  Port ( );
end Mux2To1WS_Tb;

architecture Behavioral of Mux2To1WS_Tb is
      component Mux2To1WS is
        port ( A : in STD_LOGIC;
               B : in STD_LOGIC;
               S0 : in STD_LOGIC;
               Z : out STD_LOGIC);
        end component;

    signal A, B, S0 : std_logic;
    signal Z : std_logic;
begin

    tb : Mux2To1WS port map(A => A,
                      B => B,
                      S0 => S0,
                      Z => Z);

    process
    begin
    A <= '0';
    B <= '0';
    S0 <= '0';
```

```
    wait for 100ns;

    A <= '1';
    B <= '0';
    S0 <= '0';
    wait for 100ns;

    A <= '0';
    B <= '1';
    S0 <= '0';
    wait for 100ns;

    A <= '1';
    B <= '1';
    S0 <= '0';
    wait for 100ns;

    A <= '0';
    B <= '0';
    S0 <= '1';
    wait for 100ns;

    A <= '1';
    B <= '0';
    S0 <= '1';
    wait for 100ns;

    A <= '0';
    B <= '1';
    S0 <= '1';
    wait for 100ns;

    A <= '1';
    B <= '1';
    S0 <= '1';
    wait for 100ns;

    wait;
    end process;
end Behavioral;
```