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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
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-- Create Date: 10/06/2021 07:58:39 PM
-- Design Name:
-- Module Name: Adder4bit - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Adder4bit is
    Port ( num1 : in STD_LOGIC_VECTOR (3 downto 0);
           num2 : in STD_LOGIC_VECTOR (3 downto 0);
           Sum : out STD_LOGIC_VECTOR (3 downto 0);
           Cout : out STD_LOGIC);
end Adder4bit;

architecture Behavioral of Adder4bit is
    component fulladder is
        Port ( A : in STD_LOGIC;
               B : in STD_LOGIC;
               Cin : in STD_LOGIC;
               Sum : out STD_LOGIC;
               Cout : out STD_LOGIC);
    end component;

    signal tempCin : std_logic_vector(4 downto 0);
begin
    tempCin(0) <= '0';

    b0 : fulladder port map(A => num1(0),
                            B => num2(0),
                            Cin => tempCin(0),
                            Sum => Sum(0),
                            Cout => tempCin(1));
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    b1 : fulladder port map(A => num1(1),
                            B => num2 (1),
                            Cin => tempCin(1),
                            Sum => Sum(1),
                            Cout => tempCin(2));

    b2 : fulladder port map(A => num1(2),
                            B => num2(2),
                            Cin => tempCin(2),
                            Sum => Sum(2),
                            Cout => tempCin(3));

    b3 : fulladder port map(A => num1(3),
                            B => num2(3),
                            Cin => tempCin(3),
                            Sum => Sum(3),
                            Cout => tempCin(4));

    Cout <= tempCin(4);

end Behavioral;
```