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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 10/10/2021 08:25:22 PM
-- Design Name:
-- Module Name: FinaldesignTB - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FinaldesignTB is
--  Port ( );
end FinaldesignTB;

architecture Behavioral of FinaldesignTB is
    component Mux2To1 is
        port ( A : in STD_LOGIC_VECTOR (3 downto 0);
               B : in STD_LOGIC_VECTOR (3 downto 0);
               S0 : in STD_LOGIC_VECTOR (7 downto 0);
               Z : out STD_LOGIC);
    end component;

    signal A, B : std_logic_vector (3 downto 0);
    signal S0 : std_logic_vector (7 downto 0);
    signal Z : std_logic;

begin

    tb : Mux2To1 port map(A => A,
                          B => B,
                          S0 => S0,
                          Z => Z);

    process
    begin
        A(0) <= '0';
```

```
        B(0) <= '0';
        S0(0) <= '0';
        wait for 100ns;

        A(0) <= '1';
        B(0) <= '0';
        S0(0) <= '0';
        wait for 100ns;

        A(0) <= '0';
        B(0) <= '1';
        S0(0) <= '0';
        wait for 100ns;

        A(0) <= '1';
        B(0) <= '1';
        S0(0) <= '0';
        wait for 100ns;

--        A <= '0';
--        B <= '0';
--        S0 <= '1';
--        wait for 100ns;

--        A <= '1';
--        B <= '0';
--        S0 <= '1';
--        wait for 100ns;

--        A <= '0';
--        B <= '1';
--        S0 <= '1';
--        wait for 100ns;

--        A <= '1';
--        B <= '1';
--        S0 <= '1';
--        wait for 100ns;

        wait;
      end process;
end Behavioral;
```