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-- Company:
-- Engineer:
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-- Create Date: 10/06/2021 09:00:15 PM
-- Design Name:
-- Module Name: Sub4bit - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Sub4bit is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           B : in STD_LOGIC_VECTOR (3 downto 0);
           Overflow : out STD_LOGIC;
           D : out STD_LOGIC_VECTOR (3 downto 0);
           Bout : out STD_LOGIC);
end Sub4bit;

architecture Behavioral of Sub4bit is
    component fulladder is
        port ( A, B, Cin : in STD_LOGIC;
               Sum, Cout : out STD_LOGIC);
    end component;

    signal A1, A2, A3, A4 : std_logic;
    signal temp : STD_LOGIC_VECTOR (3 downto 0);

begin

    temp(0) <= '1' xor B(0);
    temp(1) <= '1' xor B(1);
    temp(2) <= '1' xor B(2);
    temp(3) <= '1' xor B(3);

    d0 : fulladder port map (A(0), temp(0), '1', D(0), A1);
    d1 : fulladder port map (A(1), temp(1), A1, D(1), A2);
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    d2 : fulladder port map (A(2), temp(2), A2, D(2), A3);
    d3 : fulladder port map (A(3), temp(3), A3, D(3), A4);

    Overflow <= A3 XOR A4;
    Bout <= A4;

end Behavioral;
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