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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
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-- Create Date: 10/10/2021 07:44:57 PM
-- Design Name:
-- Module Name: Finaldesign - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Finaldesign is
    port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           B : in STD_LOGIC_VECTOR (3 downto 0);
           S : in STD_LOGIC_VECTOR (7 downto 0));
end Finaldesign;

architecture Behavioral of Finaldesign is
    component Mux2To1 is
        port ( A : in STD_LOGIC;
               B : in STD_LOGIC;
               S0 : in STD_LOGIC;
               Z : out STD_LOGIC);
    end component;

    component adder4bit is
        Port ( num1 : in STD_LOGIC_VECTOR (3 downto 0);
               num2 : in STD_LOGIC_VECTOR (3 downto 0);
               Sum : out STD_LOGIC_VECTOR (3 downto 0);
               Cout : out STD_LOGIC);
        end component;

    signal X : std_logic_vector (7 downto 0);
    signal Y : std_logic_vector (7 downto 0);

begin
    X(0) <= '0';
```

```
    X0 : Mux2To1 port map(A => A(0),
                          B => B(0),
                          S0 => S(0),
                          Z => X(0));


    X1 : Mux2To1 port map(A => A(0),
                          B => B(0),
                          S0 => S(1),
                          Z => X(1));

    X2 : Mux2To1 port map(A => A(1),
                          B => B(1),
                          S0 => S(2),
                          Z => X(2));

    X3 : Mux2To1 port map(A => A(1),
                          B => B(1),
                          S0 => S(3),
                          Z => X(3));

    X4 : Mux2To1 port map(A => A(2),
                          B => B(2),
                          S0 => S(4),
                          Z => X(4));

    X5 : Mux2To1 port map(A => A(2),
                          B => B(2),
                          S0 => S(5),
                          Z => X(5));

    X6 : Mux2To1 port map(A => A(3),
                          B => B(3),
                          S0 => S(6),
                          Z => X(6));

    X7 : Mux2To1 port map(A => A(3),
                          B => B(3),
                          S0 => S(7),
                          Z => X(7));


end Behavioral;
```