```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 11/09/2021 09:02:42 PM
-- Design Name:
-- Module Name: fsm_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fsm_tb is
--  Port ( );
end fsm_tb;

architecture Behavioral of fsm_tb is
    component fsm is
    port (clk : in STD_LOGIC;
          reset : in STD_LOGIC;
          x : in STD_LOGIC;
          z : out STD_LOGIC
          );
    end component;

    signal clk, reset, x, z : std_logic;
begin

    A1 : fsm port map (
            clk => clk,
            reset => reset,
            x => x,
            z => z
            );
    process
    begin
        clk <= '0';
        wait for 20ns;
```

```
        clk <= '1';
        wait for 20ns;
    end process;

    process
    begin
        reset <= '1';
        x <= '0';
        wait for 15ns;
        reset <= '0';
        x <= '0';
        wait for 20ns;
        x <= '0';
        wait for 20ns;
        x <= '1';
        wait for 20ns;
        x <= '0';
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        x <= '1';
        wait for 20ns;
        x <= '1';
        wait for 20ns;
        x <= '0';
        wait for 20ns;
        x <= '1';
        wait;
    end process;

end Behavioral;
```