Ben Chavet

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Final Project Schematic Check off

We began construction of several portions of our final design. We have the majority of the design fully designed. However, due to epic battles with Electric, we were unable to successfully simulate the design. Many problems have appeared as a result of timing issues, which are difficult to account for in the design process.

We designed three vital parts of the CAM: match (detector), found logic, slice, and assembled a series of three slices into a CAM. At the current time, the CAM uses two bits of address and mask, and stores three bits of data. It will be extremely easy to duplicate the logical hardware into larger address and data fields.

Independently, the majority of components have been tested and simulate successfully, including the match detection logic, the found logic, and much of the storage logic in the slice.

Our current main issue is working with a D Latch that initializes itself to high. The particular latch signifies that a memory address is occupied. Our design demands that the latch's initial output must be low, so that data can be written to the CAM by recognizing that an empty memory space exists.