Condition

Equal to zero (4 bit)

inv

or

or   or

Less than zero (4 bit)

out

MSB

Greater than zero (4 bit)

out

inv

MSB

Instruction:

0 0 0 0 0 0 0 0 0 0 0 0

Ci *   Op bits   Target   Lt   eq   gt

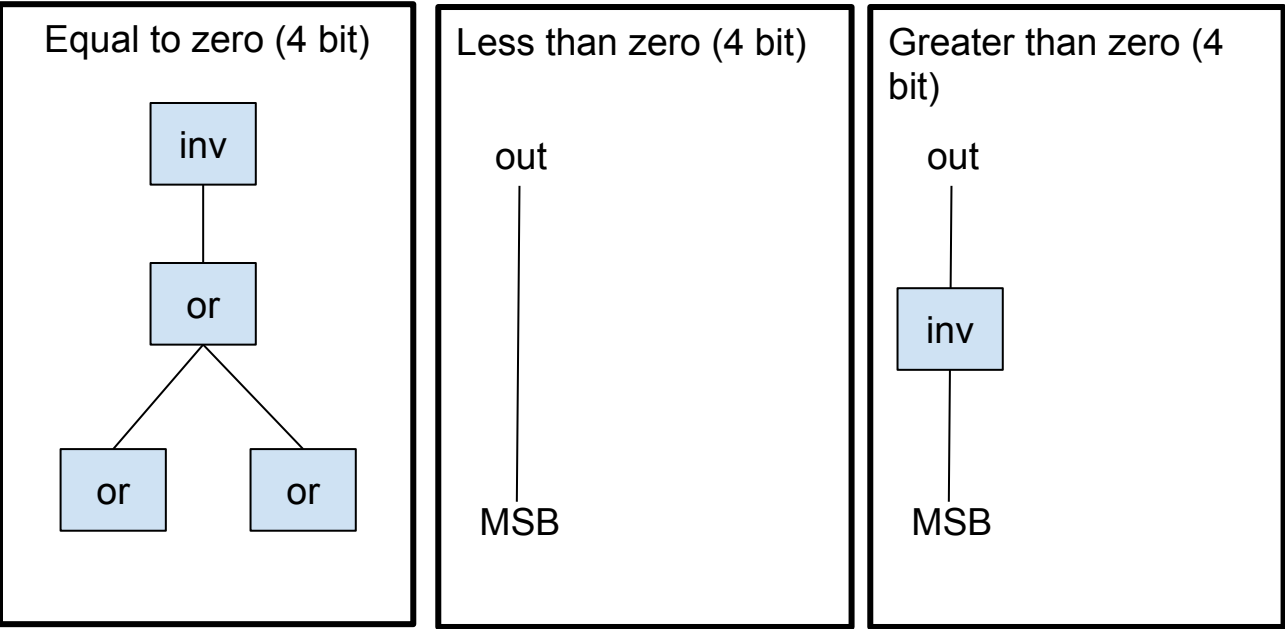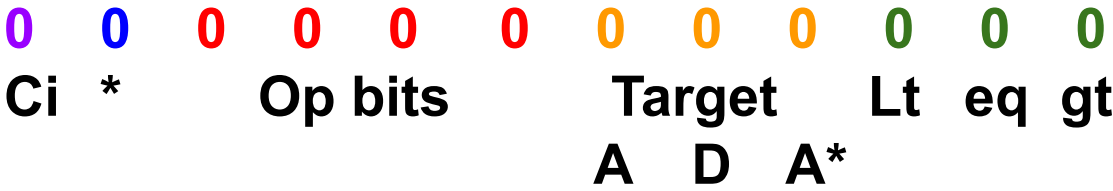A   D   A*

Operations:

Bits 0 and 1 of the op bits refer to the actual operation being performed.

00 - NOT(D)
01 - AND(D,A)
10 - ADD(D+A)
11 - OR(D,A)

Bits 3 and 4 refer to SW and ZX
SW -> (D->A, A->D), ie: NOT(D) -> NOT(A)
ZX -> (D->0, A->A), ie: ADD(D+A) -> ADD (0+A)

Ci determines whether or not the instruction will call the ALU.

ALU Instruction

R

J

Dest

ALU   Y   **Condition**   **2 Bit select**   **2 Bit select**

Operation Bits (6-9)

Lt Eq Gt (Bits 0-2)

A - 3,2   **A* - 3,2**   **A - 1,0**   **A* - 1,0**

A D A* (Bits 3-5)

* (Bit 10)