## PCB FABRICATION NOTES

CONSTRUCTION FAB SPECIFICATION LEAD-FREE RoHS MATERIAL FINAL PCB THICKNESS LAYER COUNT LAYER STACK-UP **IMPEDANCE CONTROL** 

IPC-6012 CLASS □1 □2 ■3 □ MIL-SPEC P-55110 ☐ YES TO EU DIRECTIVE ■ NOT REQD REFER TO STACKUP FOR DETAIL □ 0.8mm □ 1.0mm □ 1.2mm □ 1.6mm □ 2.4mm ■ 0.6mm □1 □2 ■4 □6 □8 □10 □12 □OTHER\_\_

SEE DETAIL DRAWING ☐ YES ■ NO ■ YES □ NO IF YES, See Stackup Detail SPECIAL CORES NO METAL BURRS AND SHARP EDGES BOARD EDGE

**BOW & TWIST** 1% MAX ON SMD PCBS ☐ NC-ROUTE ☐ V-SCORE ■ BOTH AS INDICATED PROFILING

### **CONDUCTIVE MATERIAL**

CU THICKNESS INTERNAL ☐ 17um ☐ 35um ☐ 70um ☐ \_\_\_\_um FINISHED FINAL CU THICKNESS EXT ☐ 17um ☐ 35um ☐ 70um ☐ 105um FINISHED ☐ HASL ☐ ENIG ☐ FLASH GOLD ☐ I-Sn (Imm-Tin) ■ DIG PLATING FINISH PLATING PARAMETERS Au 0.0254um to 0.0762um Ni 4.0-6.0um SELECTIVE AU PLATING ■ NO □ YES ON EDGE FINGERS ☐ AS INDICATED

**INTERCONNECTS** 

DRILL PROCESS ■ THT ■ BACK DRILL VIAS BLIND VIAS HOLE WALL PLATING AS SPECIFIED IN IPC-6012 CLASS FINAL HOLE SIZE AS PER TABLE, AFTER TH PLATING (TOL -0.0mm +0.1mm) □ 0.10 □ 0.15 ■ 0.2 □ 0.25 □ LARGER MIN HOLE SIZE (mm) □1 □2 ■3 □4 □5 □6 □7 □8 □9 □10 QTY SIGNAL LAYERS QTY COPPER PLANES  $\blacksquare 0 \square 1 \square 2 \square 3 \square 4 \square 5 \square 6$ MIN TRACE WIDTH (mm)  $\square$  0.10  $\square$  0.15  $\blacksquare$  0.2  $\square$  0.3 LARGER MIN TRACE SPACING (mm)  $\square$  0.10  $\square$  0.15  $\square$  0.2 □ 0.3 LARGER

COSMETICS

☐ TOP ■ BOT ☐ BOTH SIDES ☐ NO MASK SOLDERMASK SIDES SOLDER MASK OVER BARE COPPER (SMOBC) SOLDER MASK TYPE SOLDER MASK COLOUR ☐ GRN ■ WHITE ☐ YEL ☐ RED ☐ BLACK **SOLDERMASK WEBBING** GANG RELIEF NOT ALLOWED, UNLESS BELOW CAPABILITY SILKSCREEN COLOUR ■ BLACK □ YEL □ WHITE SILKSCREEN PRINT NO LEGEND TO BE APPLIED OVER SOLDER PADS SILKSCREEN QTY ☐ TOP ■ BOT ☐ BOTH SIDES SILKSCREEN LINE WIDTH ■ 0.1mm □ 0.15mm □ 2mm SILKSCREEN OVER PADS NOT PERMITTED, PLEASE REMOVE IF PRESENT

#### MANUFACTURING DEVIATIONS

PAD REMOVAL **TEARDROPPING** 

ALLOWED ON UNUSED PADS ON INNER LAYERS PREFERRED

THIEVING ALLOWED ON PANEL STRIPS **VIA SIZE REDUCTION** NOT ALLOWED

#### ADDITIONAL REQUIREMENTS

☐ NONE ☐ FIXTURE ■ FLYING PROBE ELECTRICAL TEST MANUFACTURER LOGO ☐ YES ■ NO

BATCH No ON S/SCREEN ☐ YES ■ NO

■ E-TEST □ UL □ IPC-6011/12 □ MIL-SPEC P-55110 CERTIFICATE REQ'D

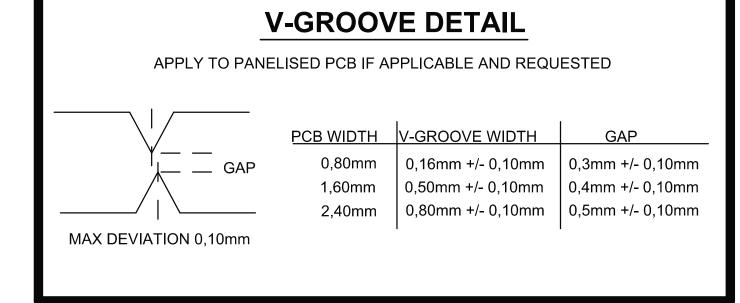
## MANUFACTURING DATA

FILENAME.EXT: EEE5004Z Antenna **GERBER DATA** TOP COPPER ☐ YES ■ NO NO COPPER ■ YES □ NO . GP2 GND COPPER ■ YES □ NO **BOTTOM COPPER** ■ YES □ NO TOP SOLDER MASK **BOTTOM SOLDER MASK** ■ YES □ NO . GBS ☐ YES ■ NO TOP OVERLAY . GTO ■ YES □ NO **BOTTOM OVERLAY** . GBO TOP SELECTIVE GOLD ☐ YES ■ NO BOTTOM SELECTIVE GOLD ☐ YES ■ NO ☐ YES ■ NO TOP PEELABLE BLUE BOTTOM PEELABLE BLUE ☐ YES ■ NO MANUFACTURING DRAWING ■ YES □ NO YES . GM1 PCB OUTLINE YES NO . GG1 DRILL GUIDE ■ YES □ NO **DRILL DRAWING** . GD1 YES NO EEE59845211940Httenhensa.TXT DRILL SET #1 (ROUND) DRILL SET #2 (SLOTS) ☐ YES ■ NO EEE5984bZthAorteenThXT

MANUFACTURING ZIP FILENAME: EEE50041211 AG12111 AG1211 AG12111 AG1211 AG121 AG1211 AG121 AG1211 AG1211 AG1211 AG1211 AG1211 AG121 AG1211 AG1211 AG1211 AG1211 AG1211 AG121

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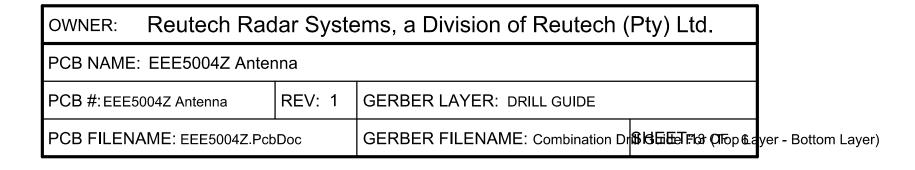
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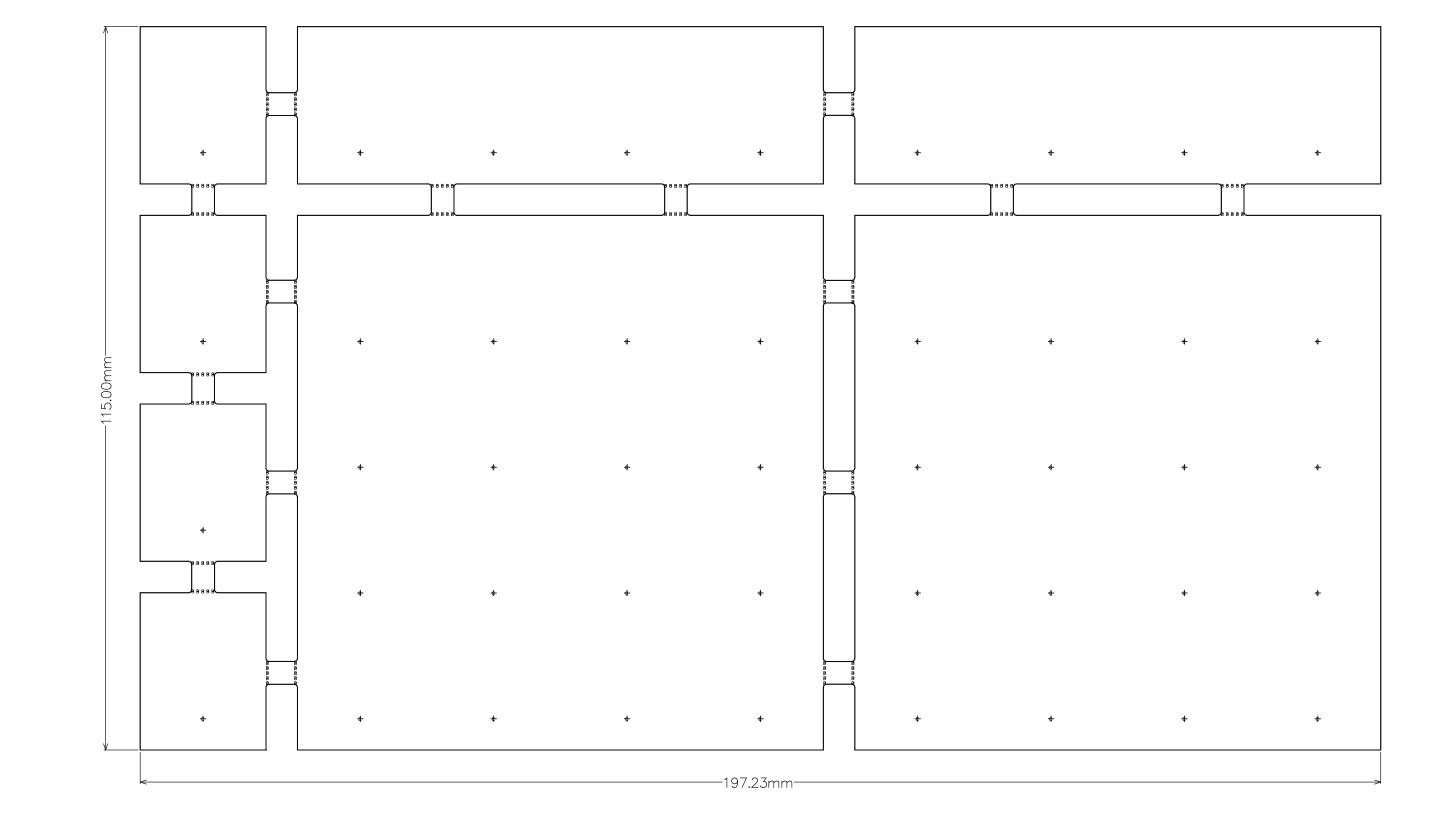


ALL DIMENSIONS IN mm

0 5 10 15 20

Scale in Millimeters





# THROUGH HOLES

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair
A	1386	0.200mm	PTH	Round	Layer 3 - Bottom Layer
В	150	0.400mm	NPTH	Round	Top Layer – Bottom Layer
С	44	0.900mm	PTH	Round	Top Layer – Bottom Layer
	1580 Total				

### **SPECIAL INSTRUCTIONS**

**BUILD STATISTICS GENERAL** COMPONENTS 22 **PRIMITIVES** FILLS TRACKS STRINGS ARCS PRINT SCALE

> PRINT DATE 13/02/2025 PRINT TIME 12:52:51

Layer	Name	Material	Thickness
	Top Overlay		
	Top Surface Finish	DIG (Direct Immersion Gold)	0.005mm
1	Top Layer	18u + Plating	0.035mm
	Dielectric 1	R04003C	0.203mm
2	Layer 2	No Copper Required	0.001mm
	Dielectric 2	R04450F	0.102mm
3	Layer 3	<b>3</b> 5u	0.035mm
	Dielectric 3	R04003C	0.203mm
4	Bottom Layer	18u + Plating	0.035mm
	Bottom Surface Finish	DIG (Direct Immersion Gold)	0.005mm
	Bottom Overlay		
Total	board thickness:		0.624mm

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KEL	JTECH						
l R	ADAR SYSTEMS	B Loots	B Loots		1	04/02/2025	N/A
	ADAK SISILMS	CAD	DESIGNER	APPROVED	REVISION	DATE	ECP No
Altium	TITLE: EEE5004Z	Z Antenna					A2
24.9.1.31	DRAWING NUMBER: EEE5004Z Antenna_D						
ASSEMBLY NUMBER: EEE5004Z Antenna FILE NAME: EEE5004Z.PcbDoc							1 OF 6

# PCB FABRICATION NOTES

CONSTRUCTION FAB SPECIFICATION LEAD-FREE RoHS **MATERIAL** FINAL PCB THICKNESS LAYER COUNT LAYER STACK-UP IMPEDANCE CONTROL SPECIAL CORES BOARD EDGE

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SEE DETAIL DRAWING ☐ YES ■ NO ■ YES □ NO IF YES, See Stackup Detail NO METAL BURRS AND SHARP EDGES

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COSMETICS

SOLDERMASK SIDES ☐ TOP ■ BOT ☐ BOTH SIDES ☐ NO MASK SOLDER MASK TYPE SOLDER MASK OVER BARE COPPER (SMOBC) SOLDER MASK COLOUR ☐ GRN ■ WHITE ☐ YEL ☐ RED ☐ BLACK **SOLDERMASK WEBBING** GANG RELIEF NOT ALLOWED, UNLESS BELOW CAPABILITY ■ BLACK ☐ YEL ☐ WHITE SILKSCREEN COLOUR SILKSCREEN PRINT NO LEGEND TO BE APPLIED OVER SOLDER PADS ☐ TOP ■ BOT ☐ BOTH SIDES SILKSCREEN QTY SILKSCREEN LINE WIDTH ■ 0.1mm □ 0.15mm □ 2mm SILKSCREEN OVER PADS NOT PERMITTED, PLEASE REMOVE IF PRESENT

MANUFACTURING DEVIATIONS

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**TEARDROPPING** PREFERRED THIEVING

ALLOWED ON PANEL STRIPS NOT ALLOWED

ADDITIONAL REQUIREMENTS

VIA SIZE REDUCTION

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■ E-TEST □ UL □ IPC-6011/12 □ MIL-SPEC P-55110 CERTIFICATE REQ'D

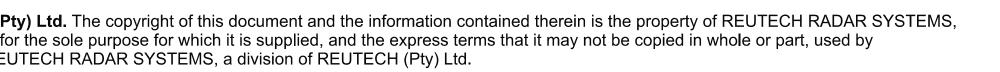
MANUFACTURING DATA

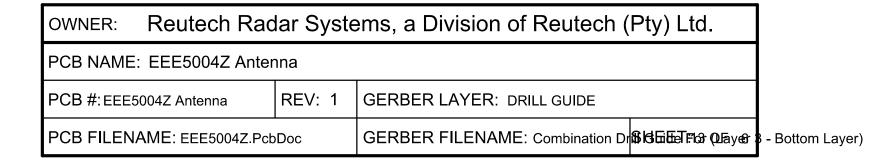
**GERBER DATA** FILENAME.EXT: EEE5004Z Antenna ■ YES □ NO □ YES ■ NO TOP COPPER NO COPPER ■ YES □ NO . GP2 **GND COPPER** ■ YES □ NO **BOTTOM COPPER** ■ YES □ NO TOP SOLDER MASK ■ YES □ NO **BOTTOM SOLDER MASK** ☐ YES ■ NO . GTO TOP OVERLAY ■ YES □ NO BOTTOM OVERLAY TOP SELECTIVE GOLD ☐ YES ■ NO ☐ YES ■ NO **BOTTOM SELECTIVE GOLD** ☐ YES ■ NO TOP PEELABLE BLUE BOTTOM PEELABLE BLUE ☐ YES ■ NO MANUFACTURING DRAWING ■ YES □ NO ■ YES □ NO
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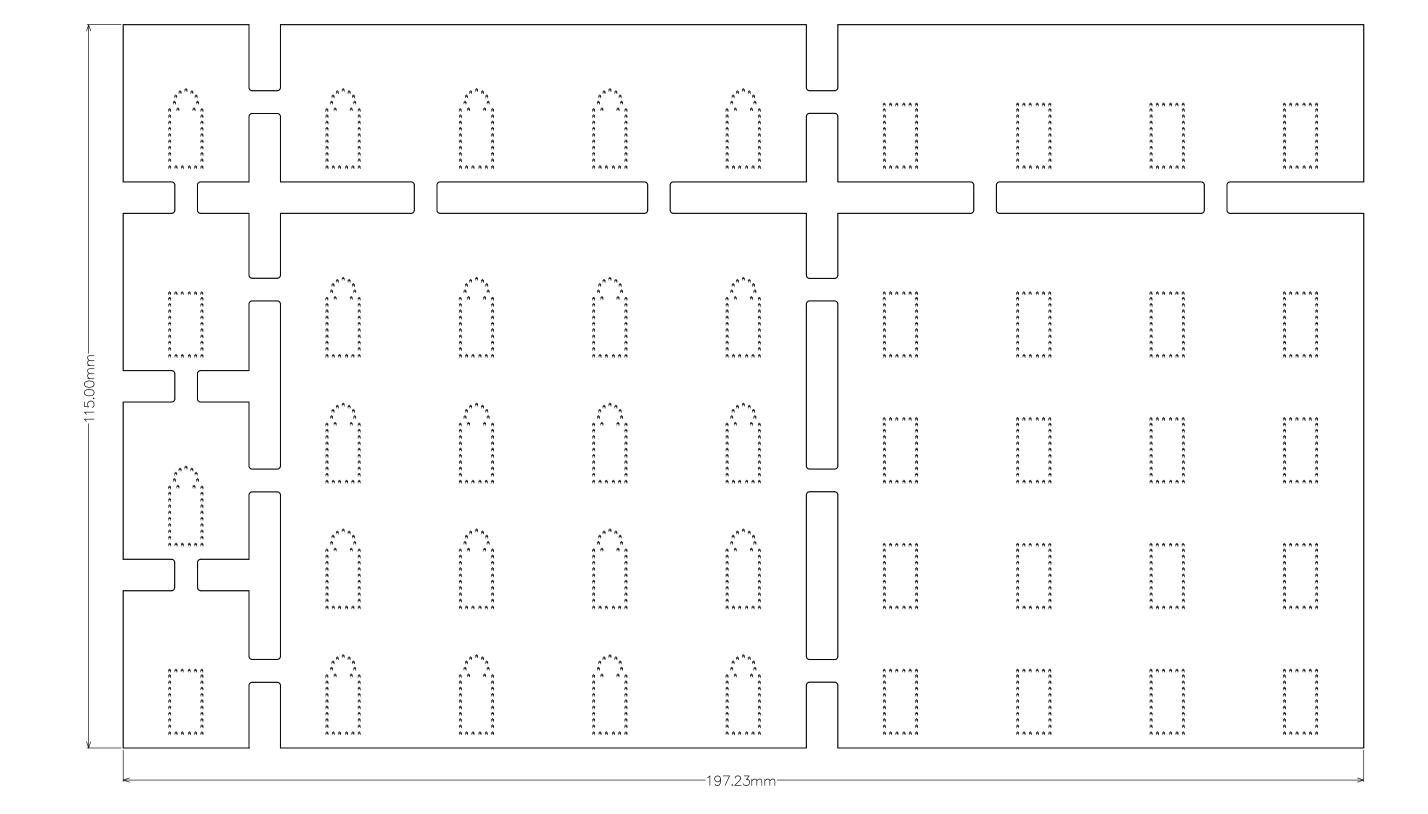
MANUFACTURING ZIP FILENAME: EEE50041211 AG12111 AG1211 AG12111 AG1211 AG121 AG1211 AG121 AG1211 AG1211 AG1211 AG1211 AG1211 AG121 AG1211 AG1211 AG1211 AG1211 AG1211 AG121

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# BLIND VIAS BOTTOM

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair
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PRINT DATE 13/02/2025 PRINT TIME 12:52:52

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	Dielectric 2	R04450F	0.102mm	
3	Layer 3	35u	0.035mm	
	Dielectric 3	R04003C	0.203mm	
4	Bottom Layer	18u + Plating	0.035mm	
	Bottom Surface Finish	DIG (Direct Immersion Gold)	0.005mm	
	Bottom Overlay			
Total	board thickness:		0.624mm	

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REUTECH								
RADAR SYSTEMS		B Loots	B Loots		1	04/02/2025	N/A	
		CAD	DESIGNER	APPROVED	REVISION	DATE	ECP No	
Altium	TITLE: EEE5004Z Antenna							
24.9.1.31	DRAWING NUMBER: EEE5004Z Antenna_D							
	ASSEMBLY NUMBER: EEE5004Z Antenna FILE NAME: EEE5004Z.PcbDoc						1 OF 6	

ALL DIMENSIONS IN mm

Scale in Millimeters

0,3mm +/- 0,10mm

0,4mm +/- 0,10mm

0,5mm +/- 0,10mm

V-GROOVE DETAIL

APPLY TO PANELISED PCB IF APPLICABLE AND REQUESTED

0,80mm

1,60mm

2,40mm

MAX DEVIATION 0,10mm

PCB WIDTH V-GROOVE WIDTH

0,16mm +/- 0,10mm

0,50mm +/- 0,10mm

0,80mm +/- 0,10mm