COEN 122L - Spring 2019
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Assignment 4 - Pipeline Buffers

Description

Pipeline buffers receive data from one stage of the pipeline as input and pass the same data to the next stage. Splitting the datapath like this allows multiple stages to execute at once and lets us coordinate them based on the clock. Thus, we can start processing an instruction while others are still in the datapath, making the entire system faster and more efficient.

Goal

You will be constructing three pipeline buffers that connect its distinct stages. The buffers are represented in Figure 1 by the three vertical bar modules. In addition to the inputs/outputs shown, all three must take a clock as input in order to synchronize with the other CPU components for the final project and to ensure that the data is passed all at once.

- IF/ID Buffer: connects instruction fetch and instruction decode stages
- ID/EX Buffer: connects instruction decode and execution stages
- EX/WB Buffer: connections execution and write-back/memory stages

As in the previous lab, only a single test-bench is required.

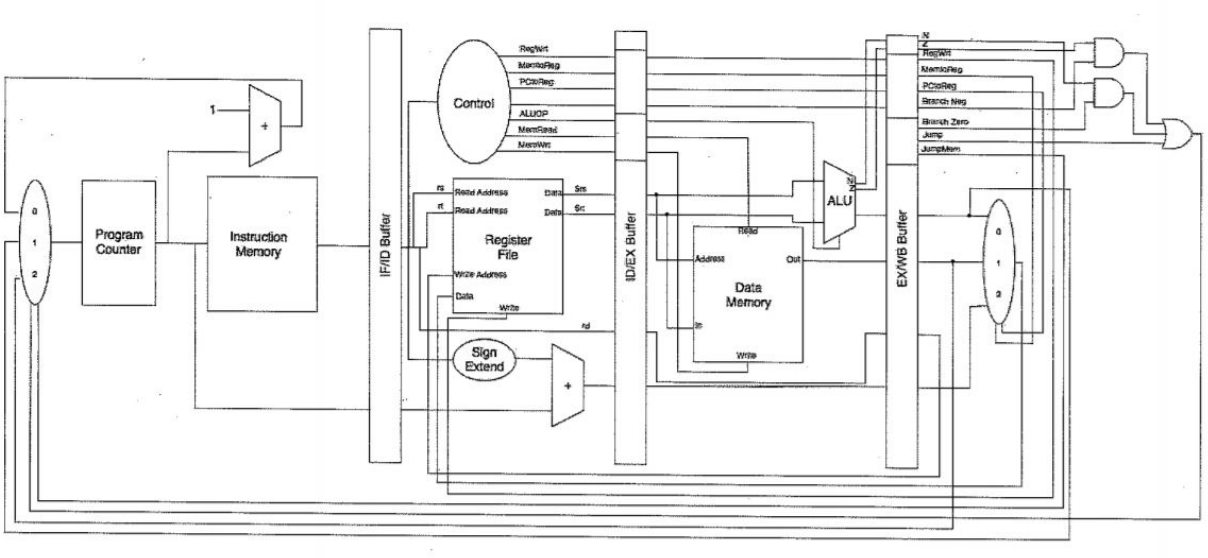

Figure 1: datapath for the project's processor

Deliverable

To receive credit for the lab, you must demo your lab to me and also submit a .zip file on Camino containing: commented source code, commented test-bench code, and a screenshot of your waveform. Please paste your code into .txt files and submit your .zip titled *firstname_lastname.zip*.

Grading is as follows:

- Demo 60%
- Submission 40%
- Due one week after lab, -10% late one week, no credit after two weeks