COEN 122L - Spring 2019
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Assignment 2 - Arithmetic Logic Unit

Description

An Arithmetic Logic Unit, or ALU, is responsible for completing simple mathematical operations for the CPU. In this case, it takes two 32-bit inputs to be operated on and a 4-bit opcode that signals which operation will be completed. It then returns one 32-bit output as the result of said operation, in addition to the ZERO and NEGATIVE control flag values. Our ALU, shown in Figure 1, will be able to perform add, increment, negate (2's complement), subtract, and pass operations.

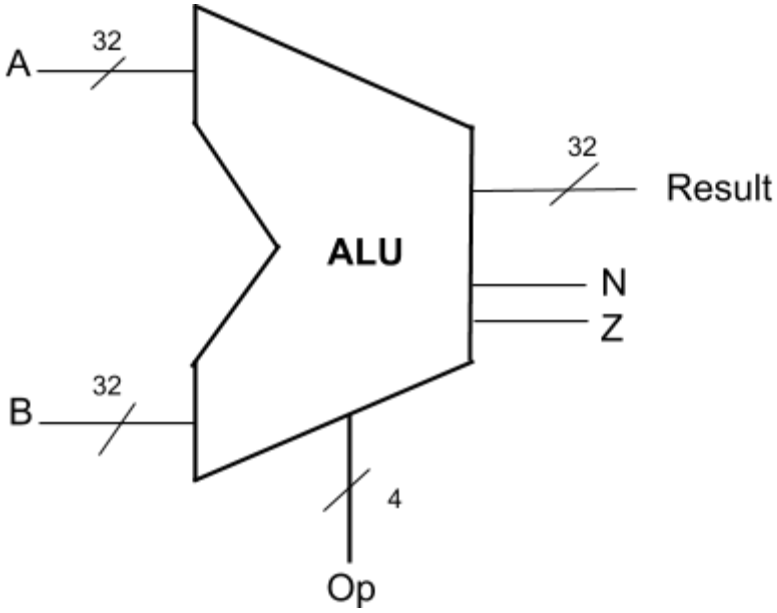

Figure 1: arithmetic logic unit

Goal

The goal of this lab is to continue learning Verilog and apply it to a more complicated CPU component to create an ALU. Inputs are: the two 32-bit values and the 4-bit opcode (even though 3-bit would be adequate). Outputs are: one 32-bit value and two 1-bit flags. The ALU must be able to compute the five specified operations, as elaborated on in Figure 2.

Operation	Opcode	Logic
ADD	0000	A + B
INCREMENT	0001	A + 1

NEGATE	0010	0 + ~A
SUBTRACT	0011	A + ~B
PASS A	0100	A + 0

Figure 2: Table of ALU operations

Here are some tips for working on the lab:

- In Verilog, you negate with the ~ operator
- NEGATE should return 2's complement, so just using ~ to flip bits will not be enough
- To SUBTRACT remember to add the 2's complement of B, following the same steps from NEGATE
- Set your flags
- Try a wide variety of values to make sure it all works

Deliverable

To receive credit for the lab, you must demo your lab to me and also submit a .zip file on Camino containing: commented source code, commented test-bench code, and a screenshot of your waveform. Please paste your code into .txt files and submit your .zip titled *firstname_lastname.zip*.

Grading is as follows:

- Demo 60%
- Submission 40%
- Due two weeks after lab, -10% late one week, no credit after two weeks