COEN 122L - Spring 2019
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Assignment 1 - 4:1 Multiplexer

Description

Multiplexers receive a number of standard inputs and return one of them based on the value of the select input. In our case, we will be building a multiplexer with four one-bit inputs and a two-bit select to have a value corresponding to each one-bit input. As an example, in Figure 1 A, B, C, and D are our inputs, S is our select, and O is our output, so if S=01 then O=B.

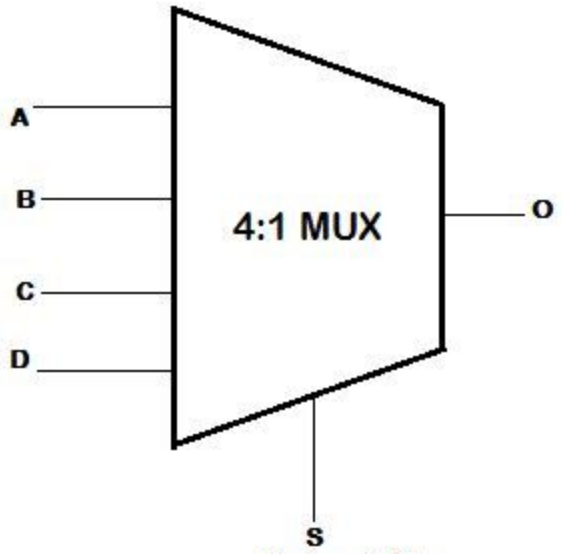

Figure 1: a 4:1 multiplexer

Goal

The goal of this lab is to familiarize ourselves with Verilog and use it to create a 4:1 multiplexer. As stated, you will have four inputs, one select, and one output. There are no guidelines for code complexity, especially not for the first lab. We will go over the basics of Verilog during the first lab session.

Deliverable

To receive credit for the lab, you must demo your lab and also submit a .zip file on Camino containing: commented source code, commented test-bench code, and a screenshot of your waveform. Please paste your code into .txt files and submit your .zip titled *firstname_lastname.zip*.

Grading is as follows:

- Demo 60%
- Submission 40%
- Due one week after lab, -10% late one week, no credit after two weeks