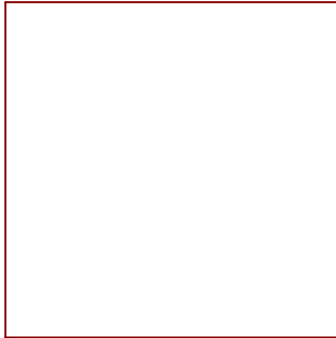
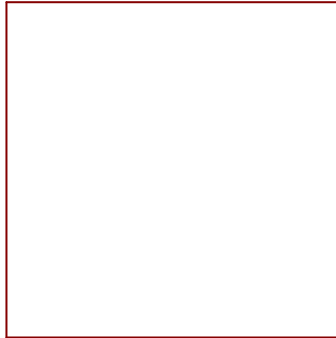


uC\_Header



File: uC\_Header.kicad\_sch

Untrimmed\_LDOs



File: LDOs.kicad\_sch

Trimmed\_LDOs



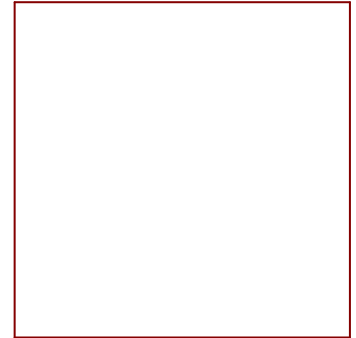
File: LDO\_Powers.kicad\_sch

Analog\_Voltages



File: Analog.kicad\_sch

Chip\_Interface



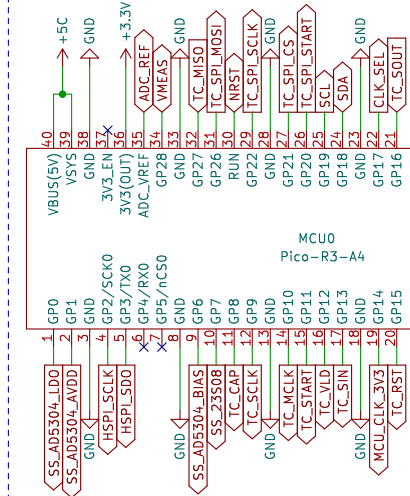
File: Chip.kicad\_sch

Clocking



File: clocking.kicad\_sch

## Raspberry Pi Pico Header (<https://www.raspberrypi.com/products/raspberry-pi-pico/>)



Female pin header sockets are about 8.5mm tall; we can fit SMT underneath Pico.

+5C is 5V from USB from microcontroller.

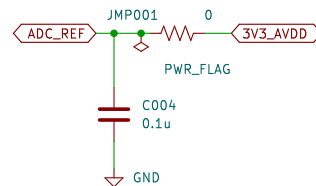
I put it through TPS2110 then we use it as usual.

+3.3V is 3.3V from Microcontroller Board Buck/Boost

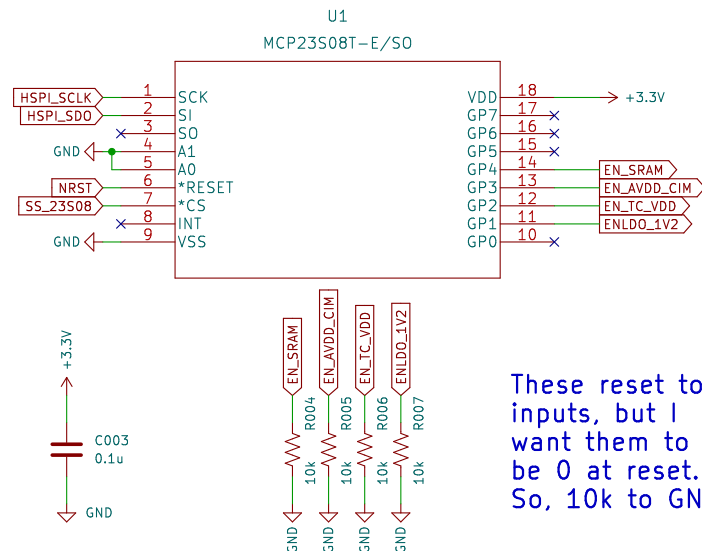
GP28 is our ADC pin

SDI/NSS are not used. We can do the SS using software. HW SS is weird.

### Optional AVDD for ADC

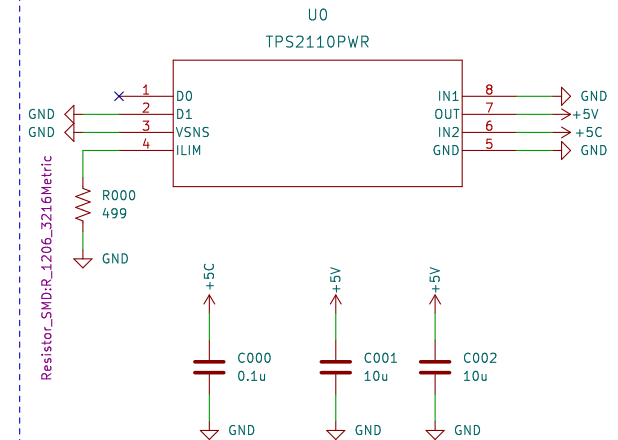


## Bus Expander



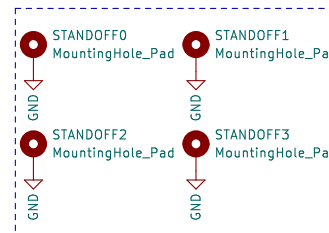
These reset to be inputs, but I want them to be 0 at reset. So, 10k to GND.

## Power Section



+5V is our main 5V rail on PCB. Consider adding banana plugs?

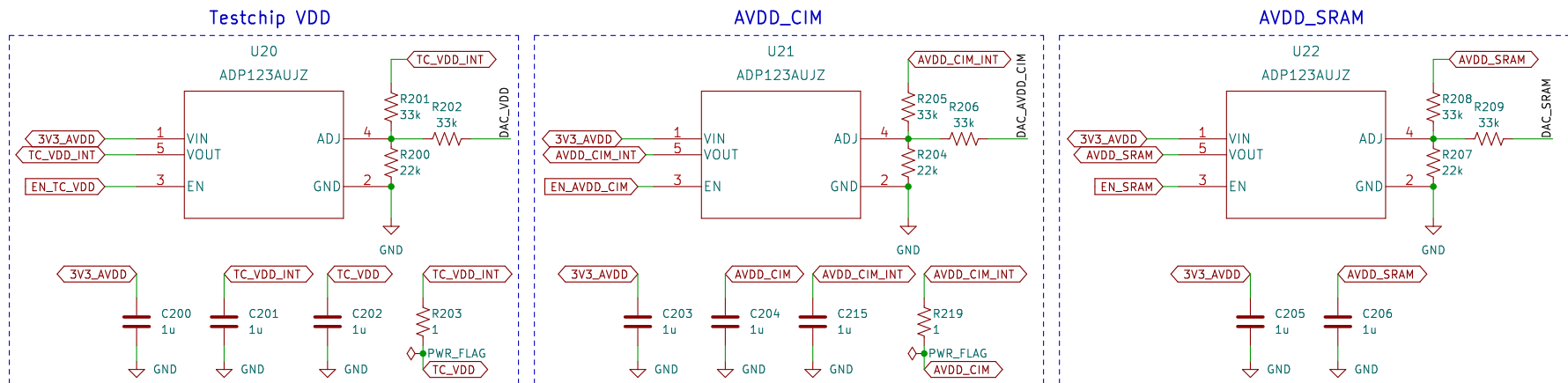
## Corner Standoffs



I just use TPS2110 to limit inrush here. TPS2110 also gives us a 500mA current limit to protect our USB host computer. TPS2110 could give us automatic switching between USB 5V and external 5V if we want.

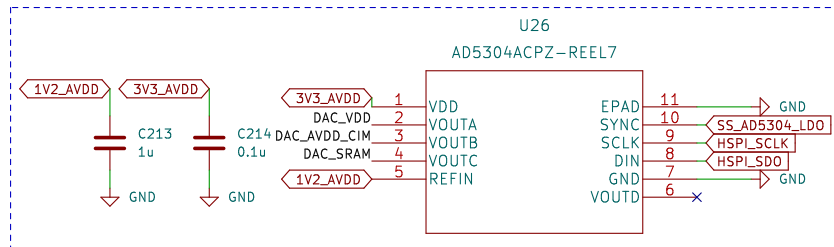
Trimmed Power Supplies: AVDD\_SRAM1~4, AVDD\_CIM, VDD. 300mA total allowed.

Range: 0.544V ~ 1.25V (Approx.)

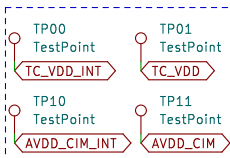


This trimmed LDO circuit (e.g. R202) is classic way to trim/margin an LDO with digital from uC + DAC chip.  
[https://e2e.ti.com/blogs\\_/archives/b/precisionhub/posts/give-your-voltage-regulator-the-margin-it-deserves](https://e2e.ti.com/blogs_/archives/b/precisionhub/posts/give-your-voltage-regulator-the-margin-it-deserves)

VDD LDO Trimming DAC. 1 chip trims all the VDDs on this sheet.

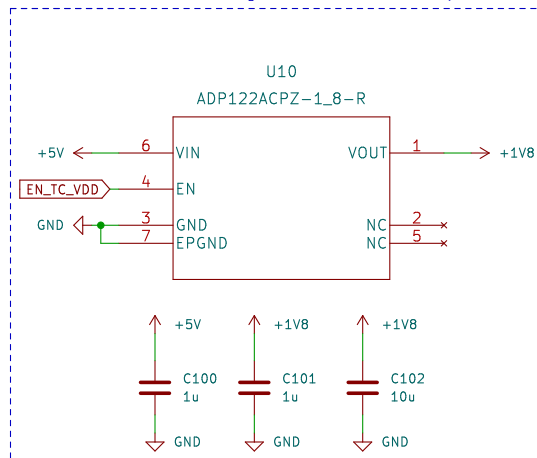


Current Measurement  
TPs



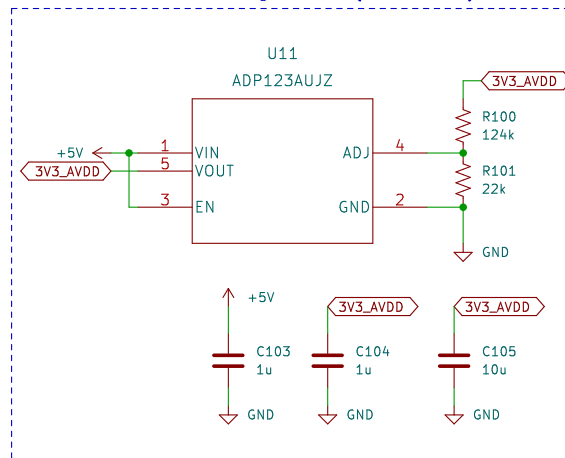
$$IDAC\_MAX = 4 \cdot (1V2 - 0.5) / 33k \sim 85\mu A, \text{ fine.}$$

### 1.8V Fixed Regulator for Chip IO



Note we have to use the ACPZ LF style package b/c AUJZ leaded package is not in stock for 1V8.

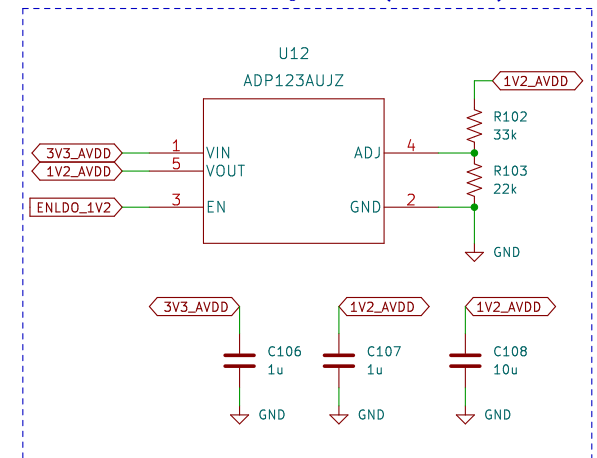
### 3.3V Analog Rail (for PCB)



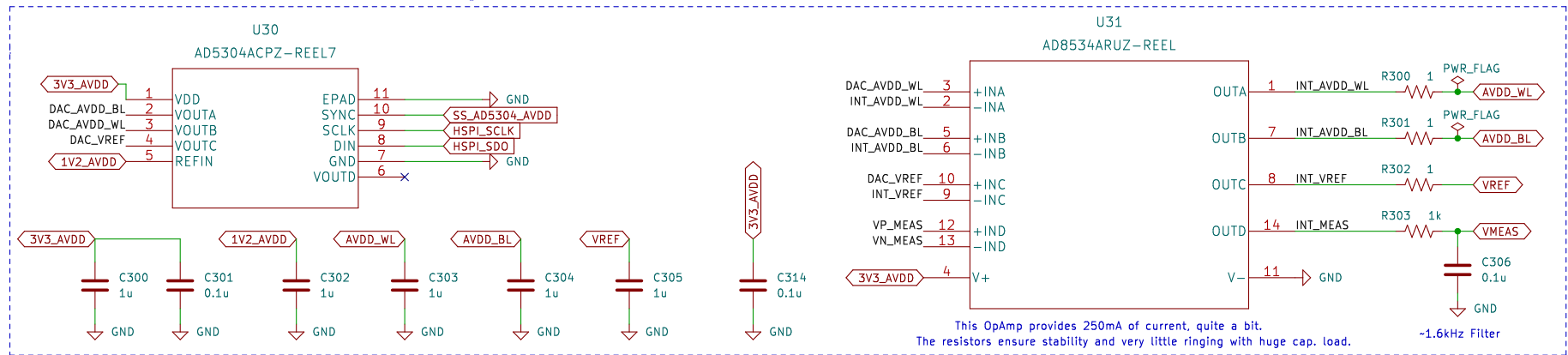
For these we can use the AUJZ leaded package, and there's 130k in stock on digikey for these. Since I route most stuff thru this ~3.3V regulator, we are limited to a total of ~300mA total among all the analog voltages and VDDs. I think it should be fine.

I added 10uF capacitors to all these just to be safe. 1uF prob fine.

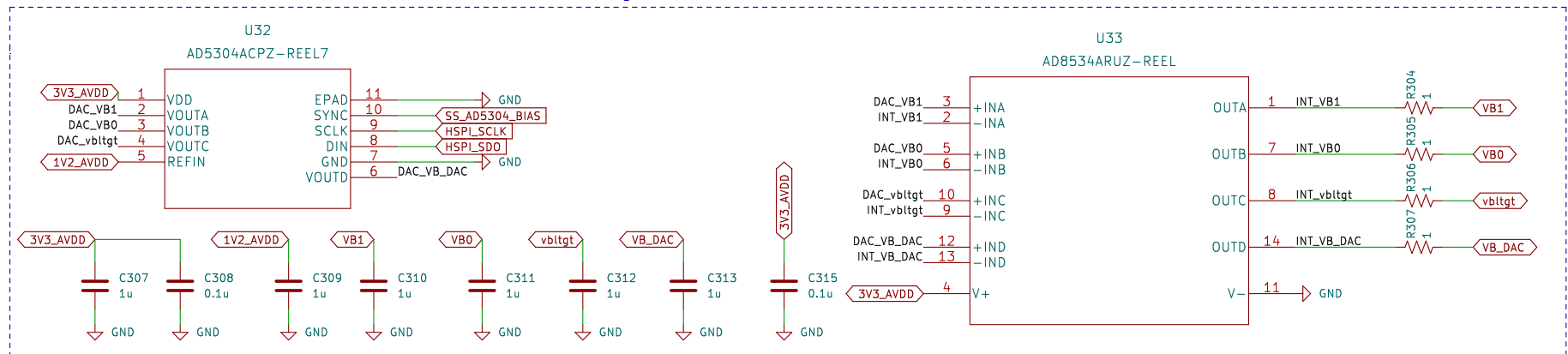
### 1.2V Analog Rail (for PCB)



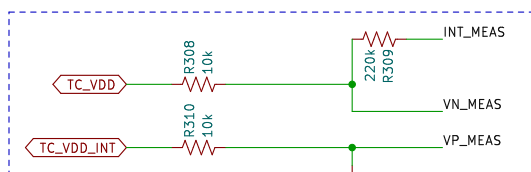
## Buffered Voltage Generation for VREF and Full-Scale AVDDs to TC



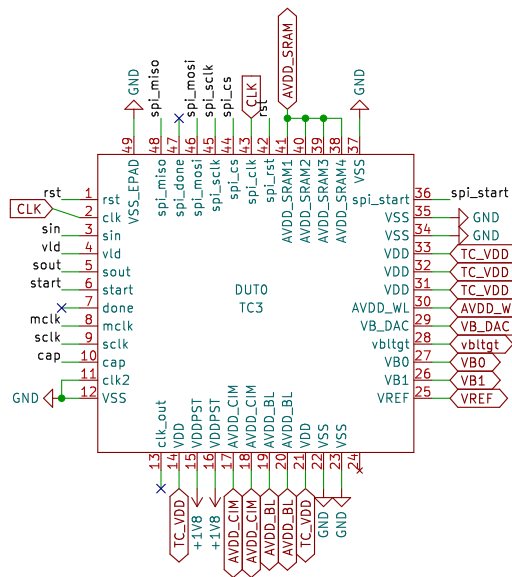
## Buffered Voltage Generation for TC Bias Points



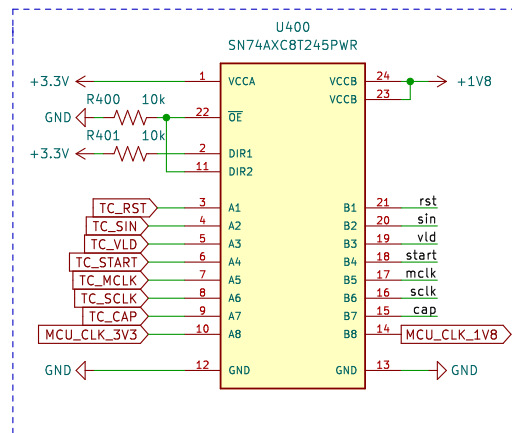
## Current Measurement Diff. Amp – Gain of 22



Had an unused OpAmp channel, so we can use it as  
a diff-amp to give precise current sensing on  
the VDD rail.

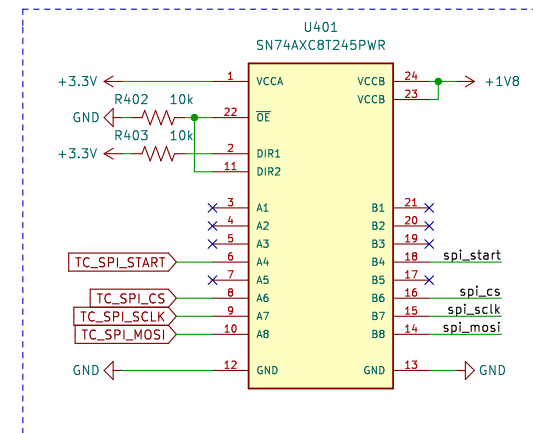


### A-to-B Direction



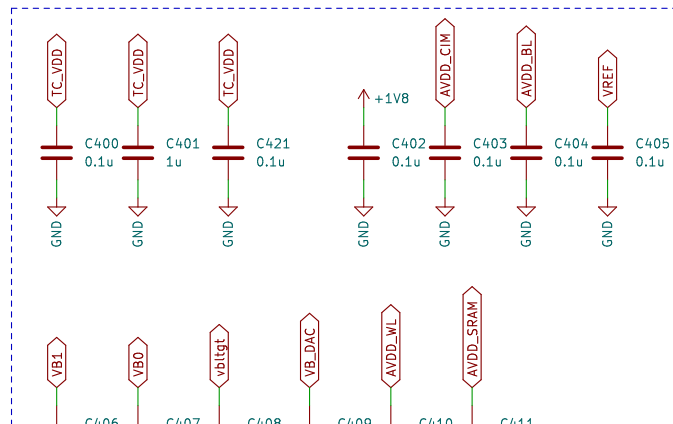
DIR2 = 0 and DIR1 = VDD should give A-to-B  
 DIR2 = DIR1 = 0 should give B-to-A

### A-to-B Direction

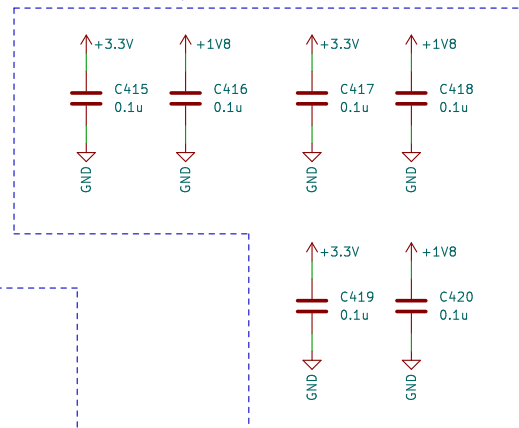


### TC Decap:

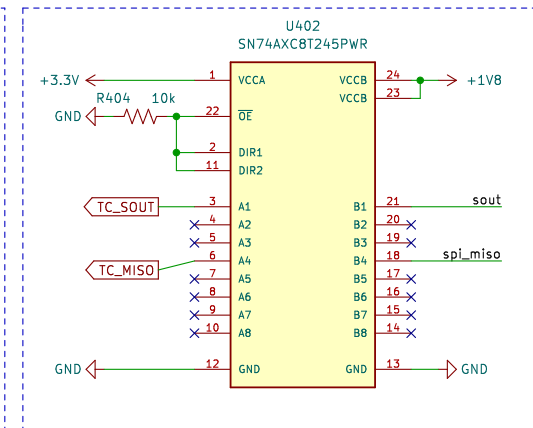
- 0.1uF Everywhere
  - 1uF on VDD
- On the actual PCB, we could put 1uF instead.



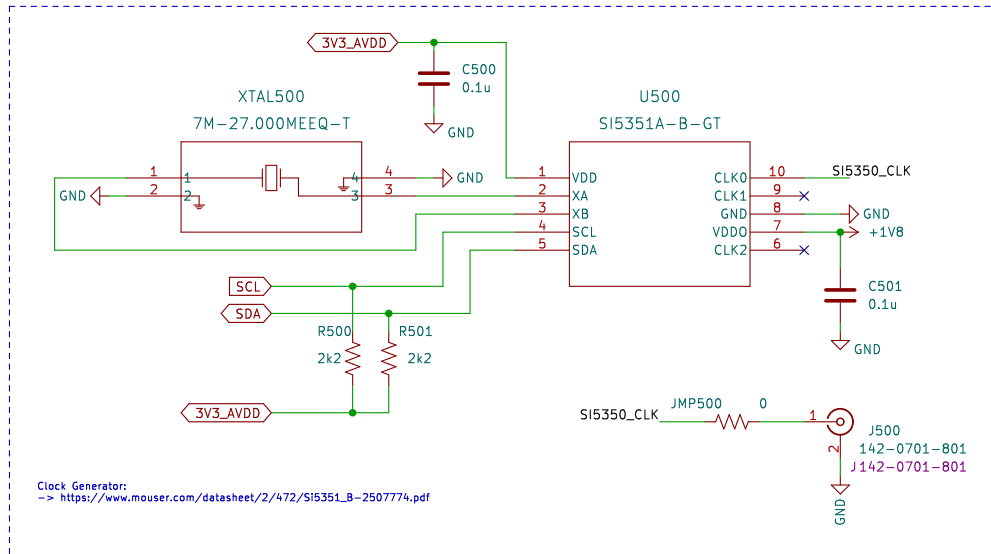
### LS Decap: 0.1uF Each on Both



### B-to-A Direction



## Clock Generator IC (I2C) w/ External Probe/Input



## Switch between Clock Gen./External & MCU

