A Quick User Guide on

Stanford University
Resistive-Switching Random Access Memory (RRAM)
Verilog-A Model

v. 1.0.0

Patent Pending.

Zizhen Jiang, Shimeng Yu, Ximeng Guan, and Prof. H-S Philip Wong
Dept. of Electrical Engineering, Stanford University

May 6, 2014

Resistive-Switching Random Access Memory Verilog-A implementation based on "Verilog-A Compact Model for Oxide-based Resistive Random Access Memory" by Jane Zizhen Jiang, Shimeng Yu, Yi Wu, Jesse H. Engel, Ximeng Guan, Prof. H.-S Philip Wong

Early description of the model can be found at:
X. Guan, S. Yu, H.-S. P. Wong, “A SPICE Compact Model of Metal Oxide Resistive Switching Memory with Variations,” *IEEE Electron Device Letters*, vol. 33, No.10, pp. 1405 – 1407, October 2012. DOI: 10.1109/LED.2012.2210856

and

S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, and H.-S. P. Wong, “A Neuromorphic Visual System Using RRAM Synaptic Devices with Sub-pJ Energy and Tolerance to Variability: Experimental Characterization and Large-Scale Model,” *IEEE International Electron Devices Meeting (IEDM)*, paper 10.4, pp, 239 – 242, December 9 – 12, San Francisco, 2012

1. Model Files

Table 1. Summary of Model Files and Modules

Module	File Name	Description
RRAM	RRAM.va	RRAM, top level model
-	constants.vams	Global and default parameter values
-	disciplines.vams	Standard Verilog-A Disciplines Definition

Additional Files

File Name	Description
User Guide	
Stanford RRAM Model Quick User Guide.doc	This User Guide in Word format.
Stanford RRAM Model Quick User Guide.pdf	This User Guide in PDF format.
References/Publications	
RRAM_CompactModel_VerilogA.pdf	Upcoming
RRAM_CompactModel_I.pdf	Describes the core of the model.
RRAM_CompactModel_II.pdf	Describes the SPICE implementation of the model.
Sample Decks	
DCSweep.sp	DC sweep HSPICE deck using this model
pulseSweep.sp	Pulse sweep HSPICE deck using this model

This documentation pertains to the model modules and files in the Resistive-Switching Random Access Memory (RRAM) Verilog-A Model package. A brief summary and description of the model files included in the package are shown in Table 1.

The package should include all and only these files, plus this User Guide document. A summary of the model scope is in *2. Scope of the Model*; details regarding model usage and instantiation can be found in *3. Model Usage*; lastly, *4. Global Parameters* describes the various global parameters that can be adjusted.

2. Scope of the Model

Table 2 below summarizes the scope of the model.

Table 2. Summary of the Scope of the RRAM Model

Device Types	Metal Oxide Bipolar RRAM
Device Dimensions:	
Oxide Thickness (Minimum)	~2 nm
Oxide Thickness (Maximum)	~100 nm
Cell Size (Minimum)	10 x 10 nm^2
Cell Size (Maximum)	100 x 100 um^2
Number of RRAMs / device (Minimum)	1
Number of RRAMs / device (Maximum)	Unlimited
Physics Aspects & Practical Non-idealities:	
Filament Growth	Simplified into one dominant filament growth.
Electronic Conduction	Generalized tunneling mechanism.
Temperature and Heat Conduction	Joule heating
Dynamic Variations	Standard Model: No variations; Dynamic Model: Variation included

This model was designed for bipolar metal oxide RRAM devices as defined in [1]. In principle, this model has no limitations on the size of the RRAM cell.

Conductive filament growth, which is attributed to the movement of oxygen ions and the vacancy generation and recombination events, is simplified to changes of the length (g) of a single dominant filament. Multiple conduction mechanisms are generalized to be a current that has an exponential dependence on the tunneling distance (the gap between the top electrode and the tip of the conductive filament) and the electric field strength. Joule heating effects is included in the simulation using an equivalent thermal resistance. Lastly, dynamic variations of the filament length, which are due to random migration of oxygen ions, are included through a random variable, δg, which describes the random variation of the gap distance [1][2][3][4].

3. Model Usage

The model is implemented in Verilog-A, and can be instantiated in HSPICE (with the appropriate Verilog-A support). This section illustrates how to instantiate the model in HSPICE.

3.1 Model Variants – Standard Model vs Dynamic Model

Two model variants are available:

1) Standard RRAM Model
2) Dynamic RRAM Model

The Standard Model is recommended for describing the ensemble-average DC switching behavior. The Dynamic Model is recommended for applications that involve dynamic current fluctuations and variations of RRAM cell characteristics.

3.2 Convergence and Settings

For improved accuracy, include the following lines of code at the beginning of the SPICE deck:

```
*************************************************
.OPTION POST
.OPTION RUNLVL = 6
*************************************************
```

3.3 Model Instantiation

To instantiate the devices in the model, the library must be included at the beginning of the SPICE deck. For an RRAM cell with or without variation (Standard RRAM Model), include:

```
.hdl rram_v_1_0_0.va
```

If more than one type of devices are used, then all the corresponding model files must be included. The other model files and modules included in the package are automatically referenced by the top level model files; thus, these auxiliary model modules should never be instantiated directly in the SPICE deck.

The VHDL Verilog-A compiler should automatically compile the Verilog-A model when the SPICE deck is compiled. The Verilog-A compilation should only occur the first time the model is used and can take a few minutes. Afterwards, the model does not need to be recompiled for different simulation runs or different SPICE decks. The model should run fast. For a single DC switching transient simulation over a 10 ms time period, the wall-clock time is less than 0.23 s using a computer with a Dual Core AMD Opteron(tm) Processor 280. Please refer to the template, *DCSweep.sp*, for a single DC switching simulation run.

The only file that should ever be modified is the parameters.vams file, which holds the global device parameters. Each time this file is changed, Verilog-A will recompile before the simulation. All other files should not be modified.

To instantiate an RRAM device, use the appropriate syntax below. The usage of this model is similar to that of the Si CMOS transistor model.

```
* Standard RRAM Model
-Hspice 2013.03 SP2
RRAM   TE  BE  rram_v_1_0_0     <    switch = 0                 gap_ini = initial_gap
    g0 = IV_fitting_parameter_1    v0 = IV_fitting_parameter_2    Vel0 = IV_fitting_parameter_3
    I0 = IV_fitting_parameter_4    beta = IV_ _fitting_parameter_5 gamma0 = IV_fitting_parameter_6 >

*Dynamic RRAM Model
-Hspice 2013.03
RRAM   TE  BE  rram_v_1_0_0     <    switch = 1            gap_ini = initial_gap
    tstep = iteration_time_step      g0=IV_fitting_parameter_1     v0=IV_fitting_parameter_2
    Vel0=IV_fitting_parameter_3  I0=IV_fitting_parameter_4      beta=IV_fitting_parameter_5
    gamma0 = IV_fitting_parameter_6         deltaGap0 = variation_fitting_parameter_1
    T_smith = variation_fitting_parameter_2 >
```

The port definitions, *TE and BE,* for the RRAM are for the top electrode and the bottom electrode, respectively. The ports *TE* and *BE* are not interchangeable in this model due to nature of the asymmetry of the RRAM programming mechanism and the details of the model implementation.

The device parameters indicated in the < … > are optional and can be set differently for each device instance. If the device parameters are omitted, default or global values set in the parameter definition file are used. The syntax for setting a parameter is:
parameter_name = value or parameter

The assigned values shown in the code above are the default values (or global parameter value) for the parameters. See Table 3 for the definitions and default values of the device parameters (Figure 1 illustrates the basic physical model for the set and reset programming of the RRAM [1]).

Table 3. Device Parameter Definitions and Default Values

Device Parameter	Description	Default Value	Suggested Range[1]	Unit	Unit in Hspice
model_switch	A switch to select Standard Model (0) or Dynamic Model (1)	0	{0, 1}	NA	NA
T_ini	Initial temperature in the device, room temperature	298	[4, 500]	K	K
F_min	Minimum field requirement to enhance gap formation	1.4e9	(0, 3e9]	V/m	V/m
tox	Oxide thickness	12	[0, 100]	nm	m
gap_ini	Initial gap distance	1.8	[gap_min, gap_max]	nm	m
gap_min	Minimum gap distance	0.2	[0,100]	nm	m
gap_max	Maximum gap distance	1.8	[0,100]	nm	m
Rth	Thermal resistance	2.1e3	(0,1e8]	K/W	K/W
T_crit	Threshold temperature for significant random variations	450	[400,450]	K	K
g0	Average Switching Fitting parameter.	0.25	(0, 2)	nm	m
V0	Average Switching Fitting parameter.	0.25	(0, 10]	V	V
Vel0	Average Switching Fitting parameter.	10	(0,20)	nm/ns	nm/ns
I0	Average Switching Fitting parameter.	1	[1pA, 1mA]	mA	A
beta	Average Switching Fitting parameter.	0.8	(0, gamma0]	1	1
gamma0	Average Switching Fitting parameter.	16	[5,50]	1	1
deltaGap0	Variations Fitting Parameter	0.02	(0,0.1)	m	m
T_smth	Variations Smoothing Parameter	500	[400,600]	K	K

[1] The entire range and all possible combinations of the parameters have not been tested. The range listed are are reasonable values based on experimental observations and physical insights.

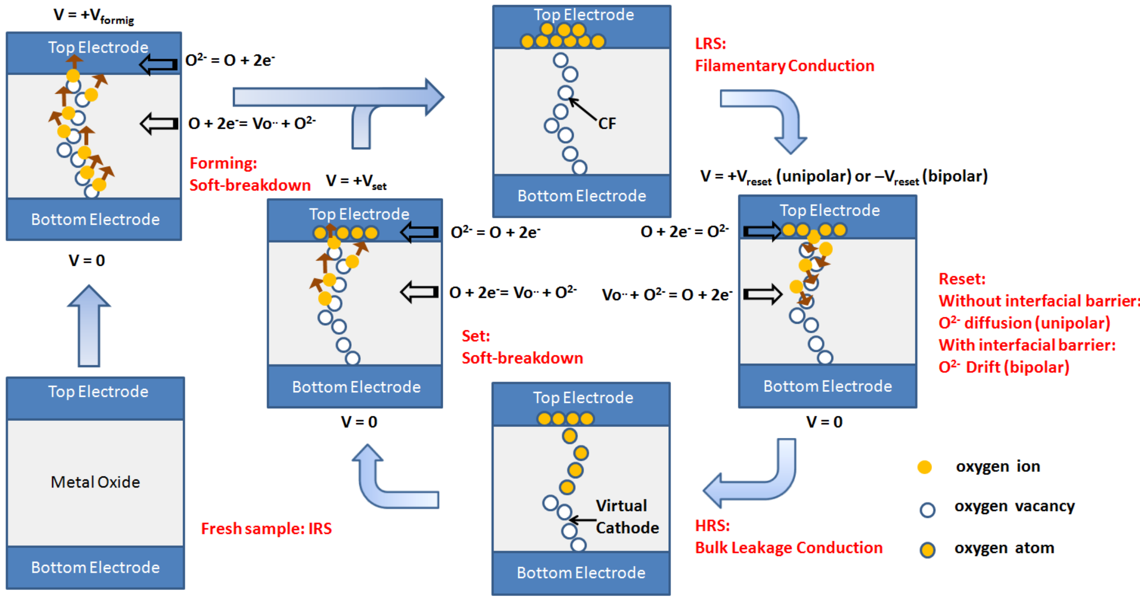

Figure 1. Illustration of Modeled RRAM Device Operations

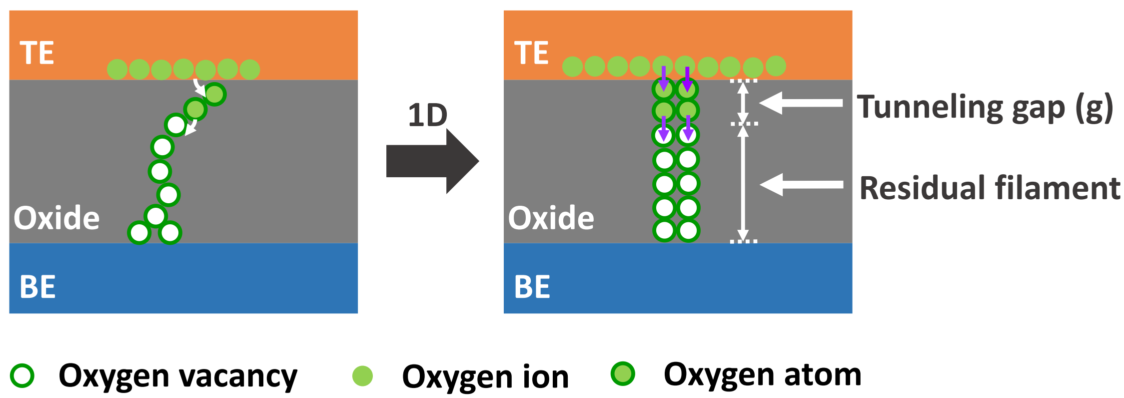

Figure 2. Illustration of Modeled RRAM's one dimension tunneling gap, described as "gap" in the codes (2)

In addition to the device parameters which can be individually set for each device instance, there are some global parameters in the "parameters.vams" file which can be modified to change the default values for device parameters or values used in model calculations[2]. The definition and values of those global parameters are summarized in Table 4.

Table 4. Global Parameter Definitions and Values[2]

Global Parameters	Description	Default Value	Unit	Unit in Hspice
Ea	Activation energy for vacancy generation	0.6	eV	eV
a0	Atom spacing	0.25	nm	m

Other variables used in the Hspice codes are illustrated in the Table 5.

Table 5. Program Variables and Typical Range

Device Parameter	Description	Unit in Hspice
T_cur	Real time temperature in the device	K
Vtb	Potential from TE to BE	V
Itb	Current flow into TE	A
gap_ddt	Time derivative of gap	m
gap	Real time gap status	m
gamma	Real time local enhancement factor	1

[2] Several other global parameters are also defined in the PARAMETERS.vams model file but should not be changed, such as fundamental constants and model critical values.

4. Template Result

A set of model-fitted experimental data will be available in the upcoming version 1.0.1 in September, 2014.

a. DC Switching

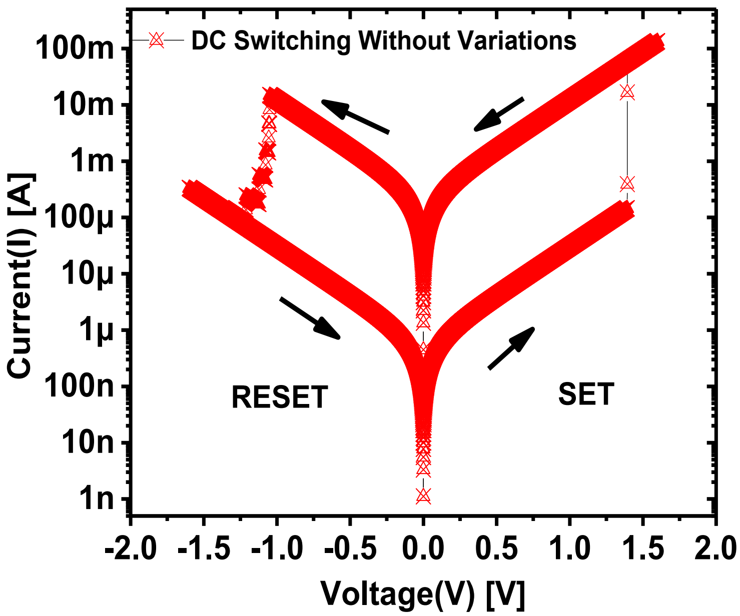

Figure 3. Typical DC Switching Without Variations

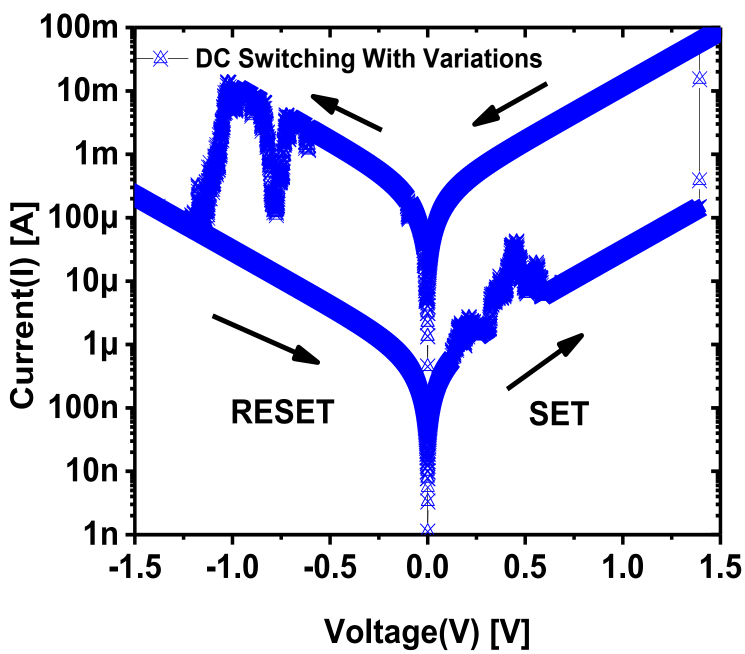

Figure 4. Typical DC Switching With Variations

b. Pulse Switching

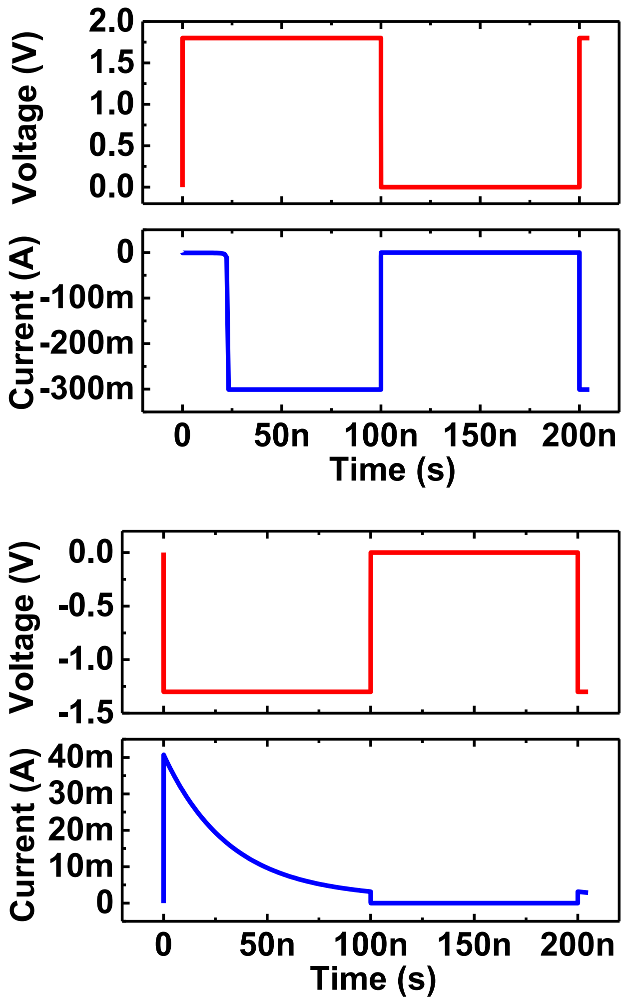

Figure 5. Typical Pulse Operation without Variations (SET and RESET)

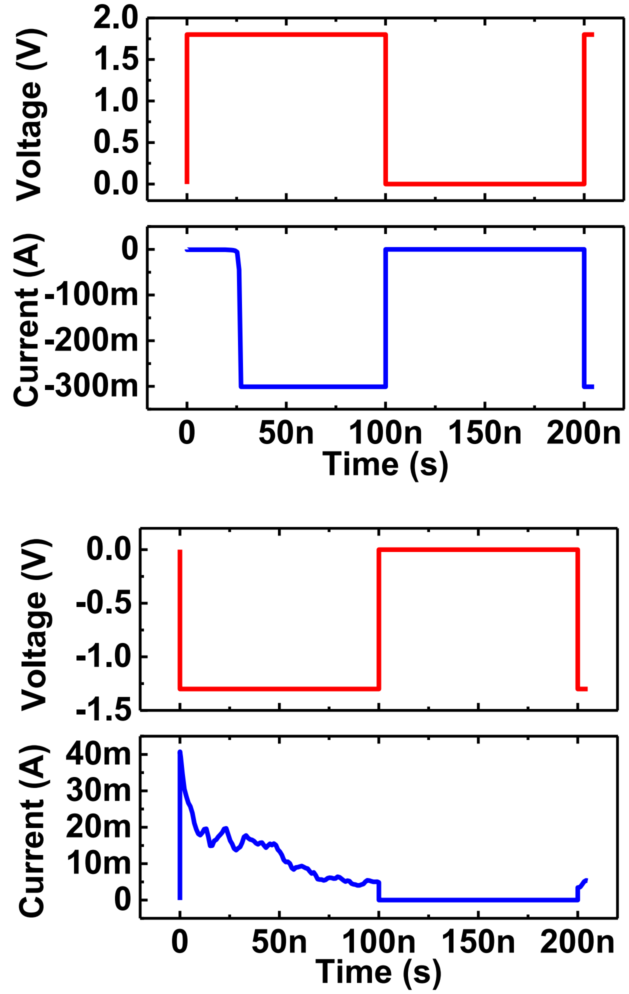

Figure 6. Typical Pulse Operation with Variations (SET and RESET)

5. References

1. H. -S P. Wong; Heng-Yuan Lee; Shimeng Yu; Yu-Sheng Chen; Yi Wu; Pang-Shiu Chen; Byoungil Lee; Chen, F.T.; Ming-Jinn Tsai, "Metal–Oxide RRAM," Proceedings of the IEEE , vol.100, no.6, pp.1951,1970, June 2012, doi: 10.1109/JPROC.2012.2190369

2. Jane Zizhen Jiang; Shimeng Yu; Yi Wu; Jesse H. Engel; Ximeng Guan; H. –S P. Wong, "Verilog-A Compact Model for Oxide-based Resistive Random Access Memory," SISPAD 2014, submitted

3. Shimeng Yu; Bin Gao; Zheng Fang; Hongyu Yu; Jinfeng Kang; , H.-S. P. Wong, "A neuromorphic visual system using RRAM synaptic devices with Sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling," Electron Devices Meeting (IEDM), 2012 IEEE International , vol., no., pp.10.4.1,10.4.4, 10-13 Dec. 2012, doi: 10.1109/IEDM.2012.6479018

4. Ximeng Guan; Shimeng Yu; H.-S. P ,Wong, "A SPICE Compact Model of Metal Oxide Resistive Switching Memory With Variations," Electron Device Letters, IEEE , vol.33, no.10, pp.1405,1407, Oct. 2012, doi: 10.1109/LED.2012.2210856

7. Contacts and Website

Please direct all inquiries and comments to:

Stanford RRAM Model Email Address
Email: stanford.nano.rrammodel@gmail.com

H.-S. Philip Wong, Professor of Electrical Engineering
Email: hspwong@stanford.edu

or

Zizhen(Jane) Jiang, Ph.D Candidate in Electrical Engineering
Email: jiangzz@stanford.edu

For the latest model file updates and the most current Terms of Use ("Software Download License") as well as other documents, please visit:
http://nano.stanford.edu/models.php .

Please report any bugs to us. Suggestions and comments are also welcome.