Sample Inputs and Outputs

a. Run Hspice for DC switching under the Linux Environment.

Input:

~>hspice DCSweep.sp

Output:

```
Using: /usr/bin/time -p /cad/synopsys/hspice/H-2013.03-SP2/hspice/amd64/hspice  DCSweep.sp
 ****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
  Copyright (C) 2013 Synopsys, Inc. All Rights Reserved.
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  This program is protected by law and is subject to the
  terms and conditions of the license agreement from Synopsys.
  Use of this program is your acceptance to be bound by the
  license agreement. HSPICE is the trademark of Synopsys, Inc.
  Input File: DCSweep.sp
  Command line options: DCSweep.sp
 lic:
 lic: FLEXlm: v10.9.8
 lic: USER:   jiangzz             HOSTNAME: nanosol.Stanford.EDU
 lic: HOSTID: 001517bf57aa        PID:      3081
 lic: Using FLEXlm license file:
 lic: 27000@cadlic0.stanford.edu
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 16-oct-2014/2013.12
 lic: 1(in_use)/200(total) FLOATING license(s) on SERVER 27000@cadlic0.stanford.edu
 lic:
 Init: read install configuration file: /cad/synopsys/hspice/H-2013.03-SP2/hspice/meta.cfg


*pvaI* current limit stacksize=10485760, set new limit stacksize=62914560
 ----------------------------------------------------
|                                                    |
|        Synopsys Unified Verilog-A (pVA v3.0)       |
|                                                    |
```

| Machine Name: nanosol.Stanford.EDU |
| Copyright (c) 2013 Synopsys Inc., All Rights Reserved. |
| |
 ----

libepva built by pvamgr synmake_pva_build on Sat Jul 20 15:34:12 PDT 2013

HSP_HOME: /cad/synopsys/hspice/H-2013.03-SP2/hspice

HSP_ARCH: amd64

HSP_GCC : /cad/synopsys/hspice/H-2013.03-SP2/hspice/GNU/amd64/gcc-4.5.2-static/bin/gcc -m64

HSP_GCC_VER: 4.5.2

Working-Dir: /home/jiangzz/RRAM/Compact_model/upload/2014_05_06

Args: -p hsp -t spi -f DCSweep.pvadir/pvaHDL.lis -o DCSweep.pvadir

optimize mode

Args: pva -p hsp -t spi -f DCSweep.pvadir/pvaHDL.lis -o DCSweep.pvadir

Begin of pVA compiling on Tue May 6 11:28:18 2014

Parsing './rram_v_1_0_0.va'

Parsing include file '/cad/synopsys/hspice/H-2013.03-SP2/hspice/include/constants.vams'

Parsing include file '/cad/synopsys/hspice/H-2013.03-SP2/hspice/include/disciplines.vams'

End of pVA compiling on Tue May 6 11:28:18 2014

End of build pVA DB on Tue May 6 11:28:18 2014

pvaI Module (rram_v_1_0_0): 2 unexpanded port, 1 init, 16 behav, 1 contrib, 32/14 expr(s)

pvaI Has DIS (AE RD BS ST), 0 afCount, 0 MT

pvaI 0 const-G and 0 const-C, No switchBranch, 0 bypassOpt

pvaI generated 0 flow node(s) during compilation.

End of pVA genC on Tue May 6 11:28:19 2014

**pvaI* #### Total 245 line-size(s), 32/14 expr(s), 1 contr(s), 1 init(s), 16 behav(s), 2 port(s)*

Generating DCSweep.pvadir/pvaRTL_amd64.so

End of submitting pVA DCSweep.pvadir/pvaRTL.mak on Tue May 6 11:28:19 2014

End of pVA elaboration on Tue May 6 11:28:19 2014

```
 Loading pVA library DCSweep.pvadir/pvaRTL_amd64.so...
1****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
 ******
 dc operation

  ******  circuit name directory
 circuit number to circuit name directory
   number circuitname                     definition         multiplier
        0 main circuit
        1 x1.                             rram_v_1_0_0(va)   1.00
  **info** (DCSweep.sp:15) DC voltage reset to initial transient source value              in source
0:vin                new dc=  0.0000D+00
*pvaI* Creating VA module (rram_v_1_0_0) for instance X1 with gmd reduction


 ******************************************************************************
 ******  option summary
 ******
 runlvl  = 4         bypass  = 2
  Opening plot unit= 15
 file=DCSweep.pa0
```

*1****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
******
dc operation

****** operating point information tnom= 25.000 temp= 25.000 *****
***** operating point status is voltage simulation time is 0.
node =voltage

+0:in = 0.

***** job concluded
*1****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
******
dc operation

****** job statistics summary tnom= 25.000 temp= 25.000 *****

****** Machine Information ******
CPU:
model name : Dual Core AMD Opteron(tm) Processor 280
cpu MHz : 1005.158

OS:
Linux version 2.6.9-34.ELsmp (buildcentos@nasha.karan.org) (gcc version 3.4.5 20051201 (Red Hat 3.4.5-2)) #1 SMP Thu Mar 9 06:23:23 GMT 2006

****** HSPICE Threads Information ******

Command Line Threads Count : 1

Available CPU Count : 4
Actual Threads Count : 1

****** Circuit Statistics ******
 # nodes = 2 # elements = 2
 # resistors = 0 # capacitors = 0 # inductors = 0
 # mutual_inds = 0 # vccs = 0 # vcvs = 0
 # cccs = 0 # ccvs = 0 # volt_srcs = 1
 # curr_srcs = 0 # diodes = 0 # bjts = 0
 # jfets = 0 # mosfets = 0 # U elements = 0
 # T elements = 0 # W elements = 0 # B elements = 0
 # S elements = 0 # P elements = 0 # va device = 1
 # vector_srcs = 0 # N elements = 0

****** Runtime Statistics (seconds) ******

analysis	time	# points	tot. iter	conv.iter
op point	0.00	1	3	
transient	0.50	8100	16212	8106 rev= 0
readin	1.16			
errchk	0.00			
setup	0.00			
output	0.00			

peak memory used 161.08 megabytes
total cpu time 1.68 seconds
total elapsed time 1.90 seconds
job started at 11:28:18 05/06/2014
job ended at 11:28:20 05/06/2014

*>info: ***** hspice job concluded*

lic: Release hspice token(s)

lic: total license checkout elapse time: 0.22(s)

pVA concluded on Tue May 6 11:28:20 2014

real 1.94

user 1.42

sys 0.21

b. Run Hspice for pulse switching under the Linux Environment.

Input:

~>hspice pulseSweep.sp

Output:

```
Using: /usr/bin/time -p /cad/synopsys/hspice/H-2013.03-SP2/hspice/amd64/hspice pulseSweep.sp
 ****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
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  Use of this program is your acceptance to be bound by the
  license agreement. HSPICE is the trademark of Synopsys, Inc.
  Input File: pulseSweep.sp
  Command line options: pulseSweep.sp
 lic:
 lic: FLEXlm: v10.9.8
 lic: USER:   jiangzz             HOSTNAME: nanosol.Stanford.EDU
 lic: HOSTID: 001517bf57aa        PID:      20569
 lic: Using FLEXlm license file:
 lic: 27000@cadlic0.stanford.edu
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 16-oct-2014/2013.12
 lic: 3(in_use)/200(total) FLOATING license(s) on SERVER 27000@cadlic0.stanford.edu
 lic:
 Init: read install configuration file: /cad/synopsys/hspice/H-2013.03-SP2/hspice/meta.cfg


*pvaI* current limit stacksize=10485760, set new limit stacksize=62914560
 ------------------------------------------------------
|                                                      |
|         Synopsys Unified Verilog-A (pVA v3.0)        |
|                                                      |
|          Machine Name: nanosol.Stanford.EDU          |
| Copyright (c) 2013 Synopsys Inc., All Rights Reserved. |
|                                                      |
 ------------------------------------------------------

libepva built by pvamgr synmake_pva_build  on Sat Jul 20 15:34:12 PDT 2013
HSP_HOME:   /cad/synopsys/hspice/H-2013.03-SP2/hspice
HSP_ARCH:   amd64
HSP_GCC :   /cad/synopsys/hspice/H-2013.03-SP2/hspice/GNU/amd64/gcc-4.5.2-static/bin/gcc -
m64
HSP_GCC_VER:   4.5.2
Working-Dir: /home/jiangzz/RRAM/Compact_model/upload/2014_05_06
Args:        -p hsp -t spi -f pulseSweep.pvadir/pvaHDL.lis -o pulseSweep.pvadir
```

optimize mode
Args: pva -p hsp -t spi -f pulseSweep.pvadir/pvaHDL.lis -o pulseSweep.pvadir

Begin of pVA compiling on Mon Aug 18 23:27:08 2014

Parsing './rram_v_1_0_0.va'
Parsing include file '/cad/synopsys/hspice/H-2013.03-SP2/hspice/include/constants.vams'
Parsing include file '/cad/synopsys/hspice/H-2013.03-SP2/hspice/include/disciplines.vams'

End of pVA compiling on Mon Aug 18 23:27:08 2014

End of build pVA DB on Mon Aug 18 23:27:08 2014

pulseSweep.pvadir/pvaRTL_amd64.so is reused

End of pVA elaboration on Mon Aug 18 23:27:08 2014

Loading pVA library pulseSweep.pvadir/pvaRTL_amd64.so...
*1****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
******
pulse operation

***** circuit name directory*
circuit number to circuit name directory
number circuitname definition multiplier
0 main circuit
1 x1. rram_v_1_0_0(va) 1.00
***info** (pulseSweep.sp:14) DC voltage reset to initial transient source value in source 0:vin new dc= 0.0000D+00*
**pvaI* Creating VA module (rram_v_1_0_0) for instance X1 with gmd reduction*

****
***** option summary*
******
runlvl = 4 bypass = 2
Opening plot unit= 15
file=pulseSweep.pa0

*1****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
******
pulse operation

```
 ******  operating point information tnom=  25.000 temp=  25.000 *****
***** operating point status is voltage   simulation time is     0.
  node    =voltage

+0:in      =   0.


        ***** job concluded
1****** HSPICE -- H-2013.03-SP2 64-BIT (Aug 26 2013) RHEL64 ******
******
pulse operation

 ******  job statistics summary tnom=  25.000 temp=  25.000 *****


 ******  Machine Information  ******
CPU:
model name       : Dual Core AMD Opteron(tm) Processor 280
cpu MHz   : 1809.285

OS:
Linux version 2.6.9-34.ELsmp (buildcentos@nasha.karan.org) (gcc version 3.4.5 20051201 (Red
Hat 3.4.5-2)) #1 SMP Thu Mar 9 06:23:23 GMT 2006


 ******  HSPICE Threads Information  ******

 Command Line Threads Count :     1
 Available CPU Count        :     4
 Actual Threads Count       :     1


 ******  Circuit Statistics  ******
 # nodes      =       2 # elements   =       2
 # resistors   =      0 # capacitors =       0 # inductors   =       0
 # mutual_inds =       0 # vccs       =       0 # vcvs        =       0
 # cccs        =       0 # ccvs       =       0 # volt_srcs   =       1
 # curr_srcs   =       0 # diodes     =       0 # bjts        =       0
 # jfets       =       0 # mosfets    =       0 # U elements  =       0
 # T elements  =       0 # W elements =       0 # B elements  =       0
 # S elements  =       0 # P elements =       0 # va device   =       1
 # vector_srcs =       0 # N elements =       0


 ******  Runtime Statistics (seconds)  ******
```

```
analysis          time    # points    tot. iter  conv.iter
op point          0.00          1           3
transient         0.03      206001         463         227 rev=          0
readin            0.54
errchk            0.01
setup             0.00
output            0.00


        peak memory used        161.08 megabytes
        total cpu time            0.59 seconds
        total elapsed time        0.81 seconds
        job started at     23:27:07 08/18/2014
        job ended   at     23:27:08 08/18/2014


>info:          ***** hspice job concluded
 lic: Release hspice token(s)
 lic: total license checkout elapse time:        0.22(s)


pVA concluded on Mon Aug 18 23:27:08 2014

real 0.87
user 0.05
sys 0.03
```

c. Check the waveforms.

A set of model-fitted experimental data will be available in the upcoming version 1.0.1 in September, 2014.

c.1) DC Switching

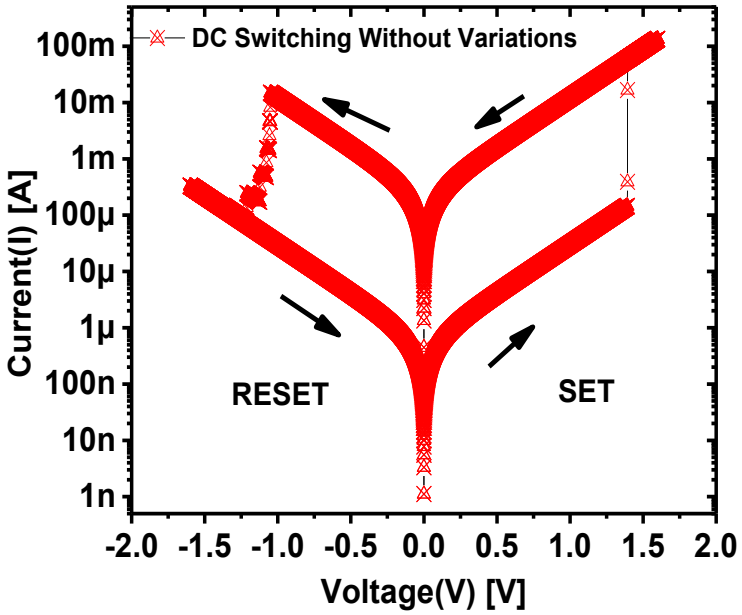

Figure 1. Typical DC Switching Without Variations

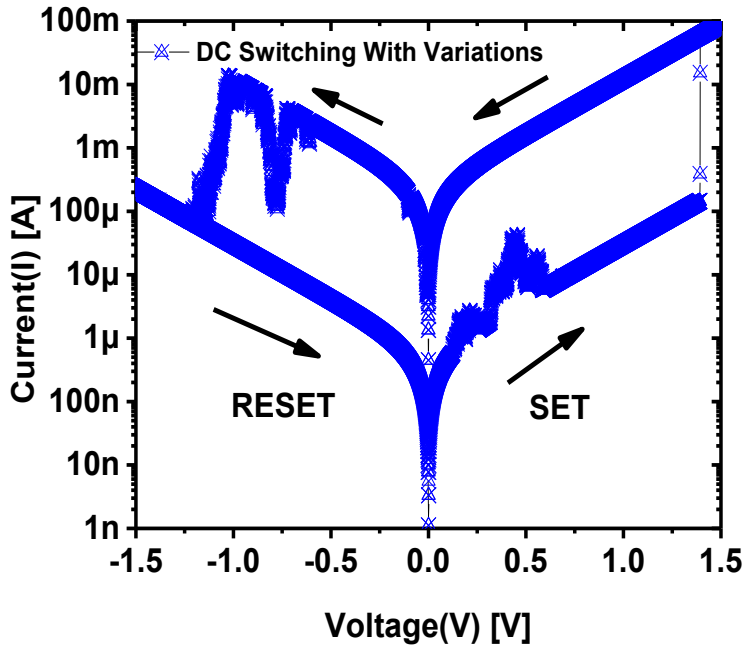

Figure 2. Typical DC Switching With Variations

c.2) Pulse Switching

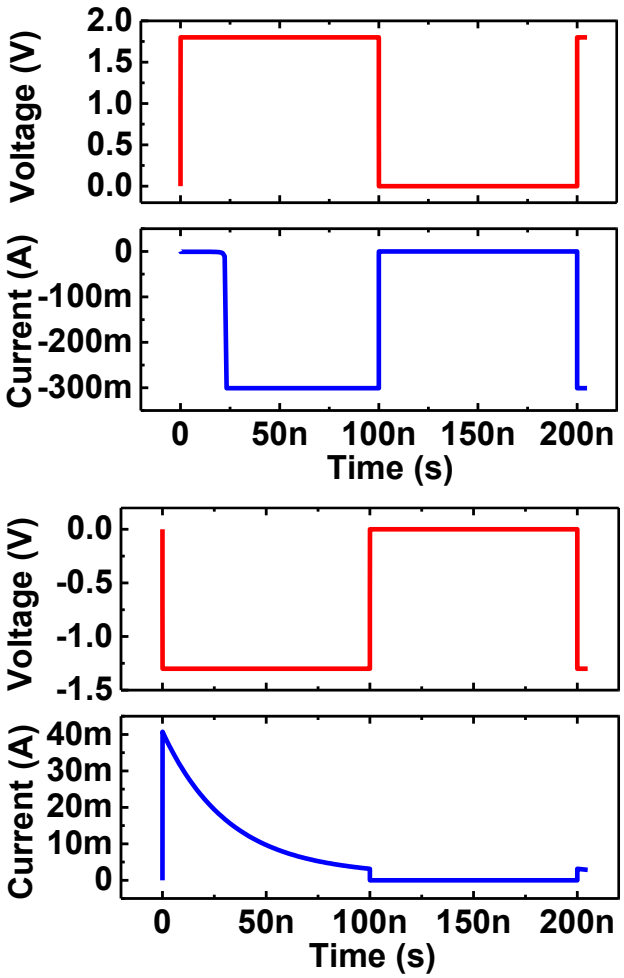

Figure 3. Typical Pulse Operation without Variations (SET and RESET)

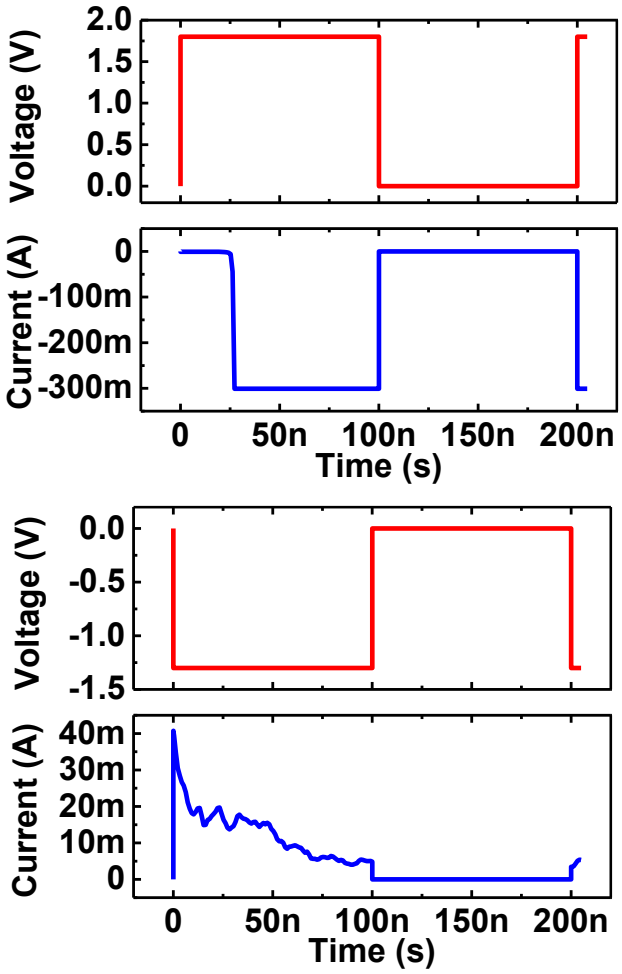

Figure 4. Typical Pulse Operation with Variations (SET and RESET)

Input:

~>cscope

Table 1. DCSweep.sp without variations switching output checklist

Voltage(V) [V]	*Current(I) [A]*
-0.50025	*0.00163*
-1.00025	*0.01227*
-1.50025	*2.24888E-4*

Table 2. pulseSweep.sp without variations switching output checklist

Time(t) [ns]	*Current(I) [A]*
13.2	*-0.000784389*
18.2	*-0.00131103*
23.2	*-0.300922*