A Compact Model for Metal–Oxide Resistive Random Access Memory With Experiment Verification

Zizhen Jiang, *Student Member, IEEE*, Yi Wu, Shimeng Yu, *Member, IEEE*, Lin Yang, Kay Song, Zia Karim, *Member, IEEE*, and H.-S. Philip Wong, *Fellow, IEEE*

***Abstract*— A dynamic Verilog-A resistive random access memory (RRAM) compact model, including cycle-to-cycle variation, is developed for circuit/system explorations. The model not only captures dc and ac behavior, but also includes intrinsic random fluctuations and variations. A methodology to systematically calibrate the model parameters with experiments is presented and illustrated with a broad set of experimental data, including multilayer RRAM. The physical meanings of the various model parameters are discussed. An example of applying the RRAM cell model to a ternary content-addressable-memory (TCAM) macro is provided. Tradeoffs on the design of RRAM devices for the TCAM macro are discussed in the context of the energy consumption and worst case latency of the memory array.**

***Index Terms*— Compact model, experimental verification, OXRAM, ReRAM, resistive random access memory (RRAM), variations, Verilog-A.**

I. Introduction

METAL–OXIDE resistive random access memory (RRAM) is a competitive emerging memory candidate, as it offers the potential for high storage density (∼4 F^2), fast speed (∼5 ns), and low energy consumption (<pJ) [1]–[4]. Extensive research has been conducted to improve the device performance and understand the resistive switching mechanisms [5], leading to interest in exploring possible applications. The array sizes demonstrated have been increasing [5], reaching 32 Gb in 2013 [6]. At the same time, several 3-D RRAM concepts have been reported [7]–[9], providing possible solutions to complement ultrahigh density 3-D NAND [10]. Beyond the traditional data storage, various RRAM applications have been reported, such as using RRAM devices in neuromorphic systems, ternary content-addressable-memory (TCAM), and nonvolatile SRAM [11]–[16]. To satisfy the increasing need for the explorations of circuit- and system-level RRAM applications, several circuit-compatible analytical models have been developed. Yu *et al.* [12] and Guan *et al.* [17] employed a 1-D filament simplification, where the tunneling gap growth reflects the resistance change during programming. Bocquet *et al.* [18] and Noh *et al.* [19] used the filament diameter to capture different resistance states. Huang *et al.* [20] and Li *et al.* [21] took 2-D filament growth into account during the SET process. To deal with the inherent variability in RRAM devices, we have developed and made available in the public domain [22], an RRAM model that is implemented in Verilog-A and can be executed in the circuit simulator SPICE.

Based on our previous 1-D filament simplification (Fig. 1) [23], the RRAM Verilog-A compact model is enhanced and systematically verified in this paper through calibration with hardware. The equivalent field enhancement equation is modified to more accurately reflect the abrupt/gradual RESET process of various RRAM devices. For the first time, a general parameter extraction procedure is developed for an RRAM compact model. This model properly reflects the effects of the TiO_X buffer layer thickness for a bilayer RRAM and Al-doped HfO_X-based RRAM, thus illustrating the general applicability of the model for a variety of RRAM materials and device designs.

This paper is organized as follows. Section II presents the underlying physics of the model, including the filament evolution, electrical transport, heat conduction, and the intrinsic fluctuations. Examples of simulations for dc/ac programming modes are provided. Section III illustrates how the parameters

Manuscript received February 3, 2016; revised March 16, 2016; accepted March 18, 2016. Date of publication April 7, 2016; date of current version April 20, 2016. This work was supported in part by the NCN-NEEDS Program through the National Science Foundation under Grant 1227020-EEC and Semiconductor Research Corporation (SRC), in part by the Systems on Nanoscale Information Fabrics Center (SONIC), Semiconductor Research Corporation (SRC), one of the six SRC STARnet Centers through the Microelectronics Advanced Research Corporation (MARCO) and the Defense Advanced Research Projects Agency (DARPA), in part by the Intelligence Advanced Research Projects Activity (IARPA), Office of the Director of National Intelligence, within the Trusted Integrated Circuits Program, and in part by the member companies of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI) and the Stanford SystemX Alliance. The review of this paper was arranged by Editor J. Kang.

Z. Jiang and H.-S. P. Wong are with the Department of Electrical Engineering, Stanford SystemX Alliance, Stanford University, Stanford, CA 94305 USA (e-mail: jiangzz@stanford.edu; hspwong@stanford.edu).

Y. Wu was with the Department of Electrical Engineering, Stanford SystemX Alliance, Stanford University, Stanford, CA 94305 USA. She is now with Oracle Corporation, Santa Clara, CA 95054 USA (e-mail: ywu1999@stanford.edu).

S. Yu was with the Department of Electrical Engineering, Stanford SystemX Alliance, Stanford University, Stanford, CA 94305 USA. He is now with Arizona State University, Tempe, AZ 85281 USA (e-mail: shimeng.yu@asu.edu).

L. Yang, K. Song, and Z. Karim are with AIXTRON, Inc., Sunnyvale, CA 94089 USA (e-mail: l.yang@aixtron.com; k.song@aixtron.com; z.karim@aixtron.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2016.2545412

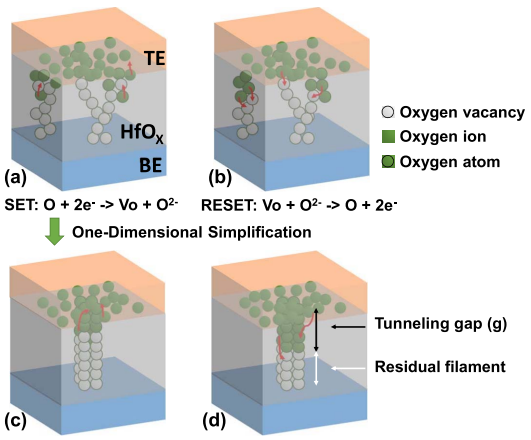


Fig. 1. (a) and (c) Schematic of the SET and RESET switching processes and conductive filament configuration. (b) and (d) Simplified model of the conductive filament at the SET and RESET states. LRS has shorter (b) tunneling gap distance while HRS has (d) longer tunneling gap distance.

in the equations of the model correlate with the observed experimental I–V behavior. A general parameter extraction procedure for the compact model is described. Section IV provides the experimental verification for both dc and ac programming modes, including: 1) the switching voltages and resistance distributions, the influence of the SET compliance current, and multilevel (ML) RESET under dc programming and 2) single-pulse programming and stochastic switching under ac mode. Section V demonstrates an example of applying the model to optimize the design of an RRAM-based TCAM.

II. Physics and Implementation

A. Physical Model

Our model captures the bipolar switching processes after the forming process, during which soft dielectric breakdown occurs. Several physical models have been reported for the SET and RESET processes of RRAM [24], [25]. To capture the essence of the observed I–V characteristics in a simple way, we use the following physical interpretation (Fig. 1) [23]. During the SET process, oxygen ions drift due to the high electric field to the anode interface, where they are stored in the interfacial oxygen reservoir. This leaves a conductive oxygen vacancy path through the oxide and, thus, programs the cell to the low-resistance state (LRS). The reverse electric field in the RESET process drives the oxygen ions back to the bulk to recombine with the oxygen vacancies, ultimately returning the memory cell to the high-resistance state (HRS).

We simplified the oxygen ion movement and the vacancy generation/recombination events into a single dominant filament growth/rupture process. The gap distance (g) between the tip of the filament and the opposite electrode is chosen as the control variable that determines the status (resistance) of the cell. The evolution rate of g due to filament growth/rupture is, according to the Arrhenius law [26], associated with the probability for oxygen ions to overcome the migration barriers, E_A (1). A temporal noise signal is added to the average gap distance change (2) to describe the fluctuations in the current during RRAM switching processes in typical dc and ac measurements [25]. The added variation $\delta_g(T)$ is a function (3) of the kinetic energy of the ions and, thus, the temperature

$$\frac{d\langle g\rangle}{dt} = -v_0 \times \exp\left(-\frac{E_A}{kT}\right) \times \sinh\left(\gamma \times \frac{a_0}{t_{\mathrm{OX}}} \times \frac{qV}{kT}\right) \tag{1}$$

$$g|_{t+\Delta t} = \int \left(\frac{d\langle g\rangle}{dt} + \delta_g \times \chi(t)\right) dt \tag{2}$$

$$\delta_g(T) = \frac{\delta_g^0}{\left\{1 + \exp\left[\frac{(T_{\mathrm{CRIT}} - T)}{T_{\mathrm{SMTH}}}\right]\right\}} \tag{3}$$

where g is the gap distance, $\langle g\rangle$ reflects the average gap distance, $\delta_g(T)$ captures the dynamic random variations, v_0 is the velocity dependent on the attempt-to-escape frequency, E_A is the effective activation energy (migration barrier) for vacancy generation (oxygen migration), t_{OX} is the thickness of the switching material, a_0 is the hopping site distance, δ_g^0 is a fitting parameter for variations, V is the applied voltage across the cell, T_{CRIT} is a threshold temperature above which a significant random variation of the gap size occurs, T_{SMTH} is a smoothing parameter, and $\chi(t)$ is a zero-mean Gaussian noise sequence randomly generated at each time step with a root mean square of unity [17]. A Gaussian function is chosen to fit variations to reflect the Gaussian-like Cumulative distribution function dependence of resistance distribution [17], [27]. γ is the field local enhancement factor that accounts for the polarizability [28] of the material

$$\gamma = \gamma_0 - \beta \cdot g^{\alpha} \tag{4}$$

where γ_0, β, and α are fitting parameters. β and α reflect the gradual nature of the RESET process. A parameter α is introduced to describe the curvature during the RESET process; this parameter will be explained in Section III.

The change of local temperature (5) must be considered, as the average growth rate $d\langle g\rangle/dt$ and the filament variation amplitude $\delta_g(T)$ strongly depend on it

$$T = T_0 + V \times I \times R_{\mathrm{TH}} \tag{5}$$

where I is the current through the memory cell and R_{TH} is the equivalent resistance. This temperature equation is simplified to avoid the use of multiple differential equations, which can cause convergence issues in the Verilog-A implementation.

Multiple conduction mechanisms may coexist in RRAM switching, including trap-assisted tunneling, Poole–Frenkel tunneling, Fowler–Nordheim tunneling, or direct tunneling. Most tunneling mechanisms share a similar exponential dependence on the tunneling gap distance and the electric field strength. Therefore, the current flowing through the cell is generalized as

$$I = I_0 \times \exp\left(-\frac{g}{g_0}\right) \times \sinh\left(\frac{V}{V_0}\right) \tag{6}$$

where the prefactor I_0, the gap coefficient g_0, and the voltage coefficient V_0 are the parameters that are obtained from the experimental results (see Section III).

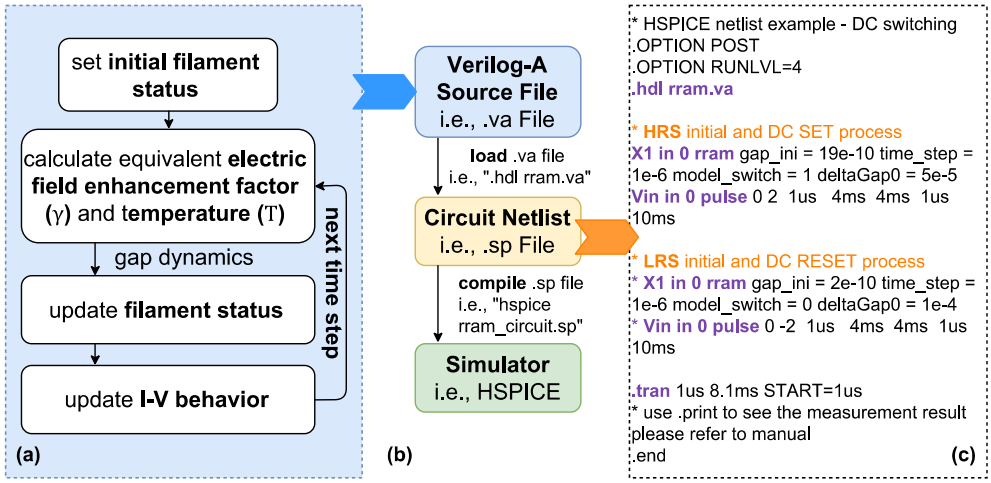


Fig. 2. (a) Flowchart of Verilog-A model implementation. (b) Program flow of compiling Verilog-A in HSPICE. (c) Example of a dc switching netlist.

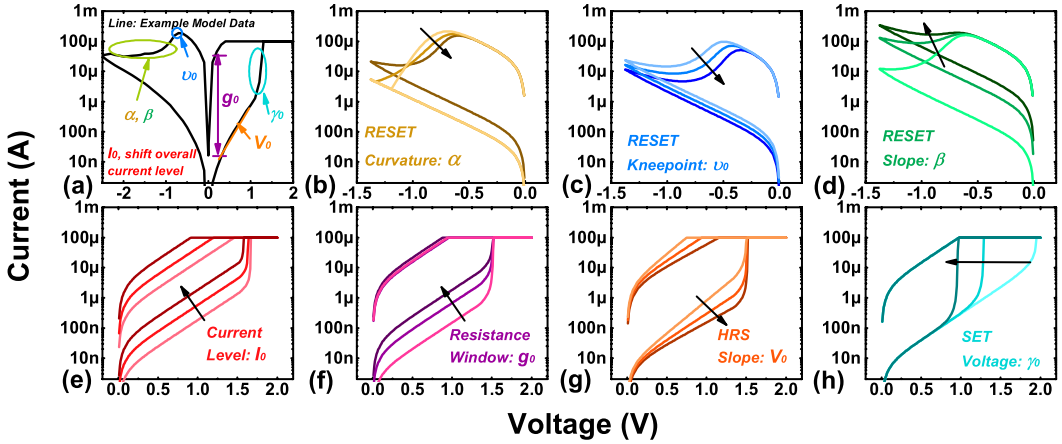


Fig. 3. Principal trends of model parameters. (a) Summary on the impacts of the parameters. (b) α, curvature of the RESET curve. (c) υ_0, RESET knee-point voltage. (d) β, slope of the RESET curve. (e) I_0, current level. (f) g_0, resistance window. (g) V_0, resistance curve. (h) γ_0, SET voltage. The direction of each arrow indicates increasing value of each parameter.

B. Model Implementation

A flowchart illustrating the implementation of this Verilog-A model is shown in Fig. 2(a). The model can be easily integrated with the standard high-precision circuit simulator SPICE [29], the program flow of which is shown in Fig. 2(b), where the modeled RRAM cell is defined as a two-terminal resistive element. A netlist example for the dc programming mode, which is implemented using transient simulation that sweeps the bias range, is shown in Fig. 2(c).

III. Parameter Extraction

Having a clearly defined procedure to extract model parameter is of paramount importance for a compact model. We first investigate how the model is influenced by the model parameters. The effect of each parameter is examined with other parameters fixed. Parameters are divided into four groups.

The first group consists of parameters (E_A, a_0, t_{OX}, T_0, and R_{TH}) defined by the device structure, material properties, and test environment. E_A, activation energy, can be estimated from temperature-accelerated stress measurement [26], first principles modeling, or other independent measurements; a_0, atomic spacing of the switching oxide, is a property of the lattice structure of the material; t_{OX}, the thickness of the oxide, is determined by the device structure; T_0 is the environment temperature; R_{TH}, the equivalent thermal resistance, can be estimated using (5) by considering the properties of the oxide that the filament can usually be heated up to 350–500 K [30], [31] at LRS during the RESET process.

The other three groups are parameters that describe the filament evolution: I_0, g_0, V_0, υ_0, γ_0, β, α, δ_g^0, T_{CRIT}, and T_{SMTH}. In particular, I_0, g_0, V_0, υ_0, γ_0, β, and α are parameters that describe the median of switching behaviors. δ_g^0, T_{CRIT}, and T_{SMTH} are parameters that describe the intrinsic (cycle-to-cycle and temporal) fluctuations during switching. The impact of each parameter on the dc switching curve is shown in Fig. 3.

I_0, g_0, and V_0 dominate the nonlinear resistance I–V curves. I_0 mainly shifts the curve to different current levels. g_0 represents the resistance window. V_0 depicts the nonlinearity of the resistance curve.

υ_0, γ_0, β, and α describe the process of the gap growth. υ_0 and γ_0 determine the voltage, where the gap starts to grow (i.e., the resistance starts to change). υ_0 mainly changes the

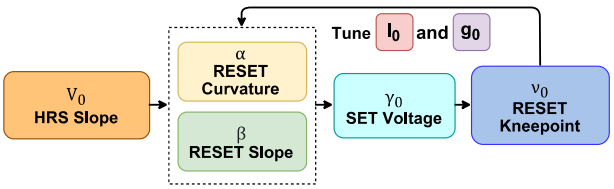


Fig. 4. General procedure extracting parameters that describes the median characteristics.

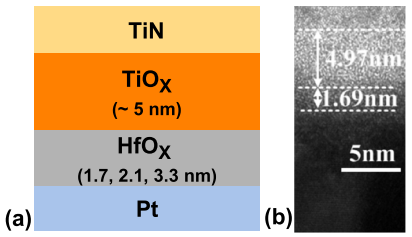


Fig. 5. (a) Structure of the fabricated TiN/TiO_X (~5 nm)/HfO_X (1.7, 2.1, and 3.3 nm) (~5 nm)/Pt devices. (b) HRTEM images of the TiO_X/HfO_X (5/1.7 nm) bilayer devices.

RESET knee-point voltage, while γ_0 sets the SET voltage. β captures the slope of the RESET slope. α changes the curvature of that slope.

The last group of parameters is δ_g^0, T_{CRIT}, and T_{SMTH}, which are used to capture the switching variations. The experimental calibration in this paper focuses on the deterministic switching behavior. Calibrating the model with the stochastic switching experimental data [32], [33] requires a physical model that can effectively represent the probability distribution of the stochastic behavior—a topic that still lacks a clear understanding. It will be an important direction for future work.

A general parameter extraction procedure is shown in Fig. 4. The parameter extraction procedure is based on the assumptions that the following holds.

1) The median current level of LRS and HRS for both SET and RESET processes are almost the same. In addition, the LRS and HRS gap statuses (g_{LRS} and g_{HRS}) for both the SET and RESET processes are the same. Before SET, the gap status begins with g_{HRS}, and after SET, it changes to g_{LRS}. Before RESET, gap status begins with g_{LRS}, and after RESET, it changes back to g_{HRS}.
2) The programmable gap range is estimated to be ~0–3 nm. It is recommended to use the median curve of the experimental data, which represents the deterministic switching behavior of the RRAM devices [23].

After the first group of parameters (E_A, a_0, t_{OX}, T_0, and R_{TH}) is chosen based on the device structure and test environment, we begin with the parameters that describe the median switching behavior.

1) Adjust V_0 to determine the nonlinearity of HRS slope. I_0 and g_0 are also suggested being adjusted to match the basic LRS and HRS current levels. For instance, with a set of parameters, we need to make sure that the experimental I–V curve falls in the assumed gap range. We can use one side of the curve to determine parameters V_0, I_0, and g_0.
2) Adjust β and α to change the slope and curvature of the RESET curve.
3) Adjust γ_0 to change the SET voltage.
4) Adjust v_0 to capture the RESET knee point.
5) Tune I_0 and g_0 if necessary.

Iteration from 2)–5) is necessary for the parameter set to converge to the same set of parameters for both SET and RESET processes. Sometimes it may not be possible to arrive at exactly the same set of parameters for both SET and RESET processes after dozens of iterations, either due to the physics of switching for SET and RESET processes or the local minimum for the fitting procedure caused by the initial set of parameters chosen. To deal with this situation, taking different values of γ_0 and β for SET and RESET in the equivalent field enhancement function (4) can be a solution.

Once these parameters are determined, the parameters that describe the cycle-to-cycle variation are subsequently obtained by calibrating the model to measured resistance distribution.

IV. Experimental Verification

A. TiN/TiO_X/HfO_X/Pt Bi-Layer Devices

Multiple TiN/TiO_X/HfO_X/Pt planar RRAM devices (HfO_X: 1.7, 2.1, and 3.3 nm/TiO_X: ~5 nm) were fabricated to verify the model (Fig. 5). First, 50-nm Pt was deposited by electron-beam evaporation on a silicon substrate to serve as the bottom electrode (BE). Then, HfO_X was deposited at 300 °C with atomic layer deposition (ALD) performed in an AIXTRON minibatch ALD system QXP-8300 equipped with TriJet vaporizers for precursor delivery. Without breaking vacuum, TiO_X was subsequently deposited with ALD at 300 °C. The thickness of ALD films was measured by TEM, which correlated well with ellipsometric measurements. The top electrode (TE) photoresist patterns (0.5 μm × 0.5 μm) were subsequently defined by photolithography. After depositing 50-nm TiN by reactive sputtering, the TE was patterned by liftoff. Electrical measurements were performed with an Agilent 4156C semiconductor parameter analyzer. The BE (Pt) was connected to ground, and the signals were applied to the TE (TiN) in all the measurements.

1) Thickness of HfO_X in Bilayer Devices: The resistive switching layer is the HfO_X layer. As a comparison, single-layer TiO_X (Pt/TiO_X (~5 nm)/TiN) devices were also fabricated. Those devices are initially leaky even before forming. The TiO_X layer works as a resistance in series with the filament resistance in the HfO_X layer, which attenuates the equivalent field in the oxide under the same bias condition, and this attenuation of the equivalent field is accounted for by properly choosing the field local enhancement factor (γ). The switching gap ranges for the three sets of bilayer devices are similar (~0.15–1.5 nm). A thicker HfO_X film can also provide an additional buffer layer, resulting in additional series resistance besides the resistance of TiO_X layer. However, the thicker HfO_X layer also shares more of the total applied voltage, reducing the voltage dropped on the gap, which results in comparably smaller programmable gap range for thicker HfO_X (HfO_X thickness and estimated range of gap length are 1.7/0.16–1.21 nm, 2.1/0.2–1.15 nm, and 3.3/0.34–1.09 nm)

TABLE I
MODEL PARAMETERS FOR TiO_X/HfO_X BILAYER AND Al-DOPED HfO_X RRAM DEVICES

Device Parameters	Unit	TiO_X/HfO_X Bilayer Devices		Al-doped HfO_X devices	
		SET	*RESET*	*SET*	*RESET*
g_0	n m	0.15		(d) 0.15, (e) 0.2, (f) 0.28	
V_0	V	0.35		0.4	
I_0	m A	0.2		(d) 8, (e) 1, (f) 0.35	
v_0	m/s	5×10^6		5×10^8	
γ_0	1	(a) 16.8 (b) 17.8 (c) 20.8	(a) 20.1 (b) 21.3 (c) 24.9	(d) 11.7 (e) 17.2 (f) 20.0	(d) 33.9 (e) 17.2 (f) 20.0
β	1	(a) 1.1 (b) 1.2 (c) 4.8	(a) 12.6 (b) 14.5 (c) 19.0	(d) 0.26 (e) 0.00 (f) 0.00	(d) 18.2 (e) 2.49 (f) 1.46
α	1	1		(d) 1.5, (e-f) 2.5	

** (a-f) indicates various device stacks: (a-c) bilayer TiO_X/HfO_X devices; (d-f) Al-doped HfO_X devices. HfO_X thicknesses: (a) 1.7 nm, (b) 2.1 nm, and (c) 3.3 nm. Al-doping percentage: (d) 0%, (e) 18%, and (f) 45%. Please refer to our model release website [22] for a thorough manual of the model with a more detailed summary of the definitions of the parameters.*

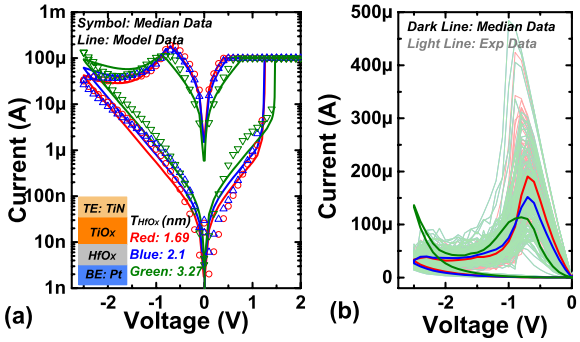


Fig. 6. (a) Experimental and simulated dc switching characteristics of bilayer devices with various HfO_X thicknesses (red: 1.7 nm, blue: 2.1 nm, and green: 3.3 nm). (b) Current overshoot of those three bilayer devices.

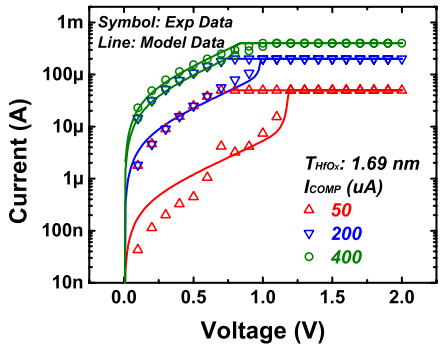


Fig. 7. DC characteristics for different compliance currents of the 1.7-nm HfO_X devices.

under the same dc switching setup (SET compliance current $I_{\mathrm{COMP}} = 100\ \mu$A, and RESET voltage $V_{\mathrm{RESET}} = -2.5$ V). It is also noted in Fig. 6 (inset) that the thicker HfO_X bilayer devices have smaller current overshoot, which is a result of the *in situ* series resistance that reduces the current overshoot during RESET.

For those bilayer devices, the activation energy (E_A) is 1.24 eV, which is estimated by the previous experiments reported [34], [35]; the atomic spacing of the switching oxide (a_0) is ~0.25 nm; the oxide thicknesses (t_{OX}) is set to be the total deposition thicknesses of the bilayer oxides (HfO_X: 1.7, 2.1, and 3.3 nm) from High-resolution transmission electron microscopy (HRTEM) images (6.7, 7.1, and 8.3 nm respectively); the environment temperature (T_0) is 300 K; equivalent thermal resistance (R_{TH}) is estimated to be ~500 K, considering the heated temperature as ~400 K in the cell during programming using (5). Other parameters (I_0, g_0, V_0, v_0, γ_0, β, and α) are then obtained following the previously described procedure. Fig. 6 shows the measured and simulated dc characteristics of the three bilayer devices. The values of the model parameters are summarized in Table I.

2) Compliance Current: As an example, the influence of the SET compliance current (using HfO_X: 1.7-nm devices) on the dc switching characteristics is shown in Fig. 7. A larger compliance current results in a smaller gap distance at LRS (g_{LRS}) after the SET process. The compliance current is currently represented by the minimum gap distance (g_{LRS}) in the model.

3) RESET Voltage: A larger RESET voltage will lead to larger gap distances after RESET (g_{HRS}) under the same set of device parameters, thus setting the RESET voltage achieves ML RESET programming. Fig. 8 compares the measured and simulated dc characteristics for various RESET voltages.

B. Al-Doped HfO_X Devices

Al-doped HfO_X RRAM 1T1R cells were also used to further demonstrate our model's applicability to a broad range of devices. These devices were integrated with select transistors in a 1T1R device structure. A reference cell stack made of TiN/Hf (10 nm)/Hf:AlO_2 (5 nm)/TiN was used. Based on this reference stack, two variations were made by doping them with different levels of Al_2O_3 (18% and 45%) by ALD [34]. The stack with 0% AlO_X doping had cells with a single layer of HfO_X. The dimensions of the RRAM cells was ~40 nm × 40 nm. The electrical measurements were performed with an Agilent B1500 semiconductor parameter analyzer. The source and base electrodes were connected to

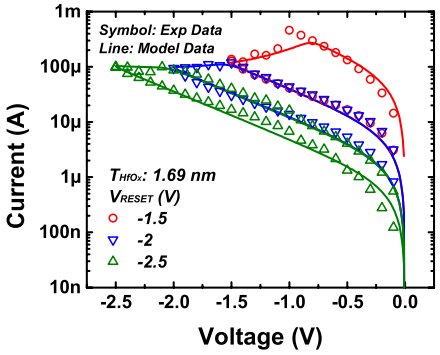


Fig. 8. DC characteristics for different RESET voltages of the 1.7-nm HfO_X devices.

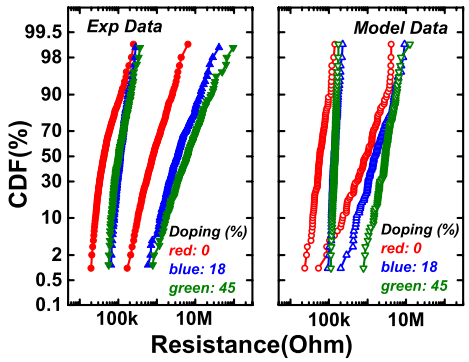


Fig. 10. Experimental and simulated data of the resistance distribution of RRAM with various AlO_X doping.

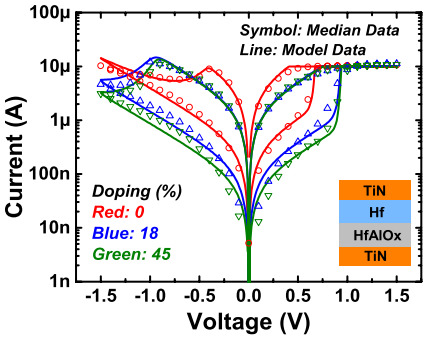


Fig. 9. Experimental and simulated dc switching characteristics of RRAM with various AlO_X doping.

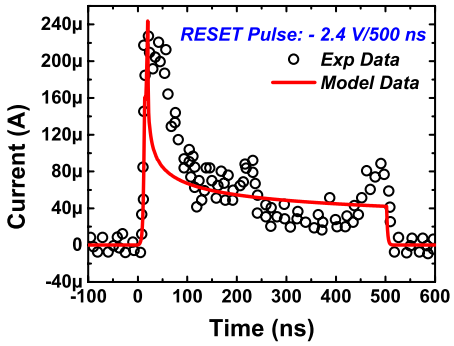


Fig. 11. Experimental and simulated data of pulse transient current in the RESET process.

ground. The drain was connected to the BE of the RRAM. A constant voltage was applied to the gate electrode of the transistor, limiting the compliance current through the RRAM cell, and a programming voltage is applied to the TE of the RRAM.

1) Doping: Similar to the parameter extraction process of the bilayer devices, we use the median switching characteristics to determine the first group of parameters (E_A, a_0, t_{OX}, T_0, and R_{TH}). The gap range is ~1–2.5 nm, since the measurement is performed under low current scale ($I_{COMP} = 10\ \mu A$). According to [28] and [34], AlO_X has larger E_A and a_0 than HfOX. Thus, we assume E_A and a_0 increase linearly with the increasing percentage of AlO_X doping (0%: 1.24 eV, 18%: 1.36 eV, and 45%: 1.54 eV). The change of the crystal structure of the oxide film with AlO_X doping modifies the conducting behavior exhibited in the HRS slope, which is reflected by V_0. The oxygen ion migration process is also different with the change of the crystal structure, which is captured by the parameters γ_0, α, and β. The parameter values of these devices are summarized in Table I. The measured data and the simulation results are shown in Fig. 9.

2) Resistance Distribution: The resistance distribution is modeled through the use of (3). Al doping reduces the variations of LRS and opens up the resistance window. The increased energy barrier of oxygen ion migration with increasing Al doping [28], [34], which slows down the random ion movement during SET, limits the variations of LRS (Fig. 10).

C. AC and Stochastic Switching

To demonstrate the ac and stochastic switching capability of the model, we used the data reported in [25] and [36] for experimental calibration.

1) AC Programming: The experimental pulse transient current was reported in [25]. We perform simulation using the compact model under the same pulse programming condition (pulse amplitude: 2.4 V, pulsewidth: 500 ns, rise time: 10 ns, and fall time: 10 ns). The current behavior is reproduced by the simulation without turning ON the variations in the simulation, as shown in Fig. 11.

2) Stochastic Switching: Yu *et al.* [36] reported the RRAM stochastic switching behavior under weak programming conditions when the SET voltage is slightly below the median SET voltage. The measurement was performed under continuous SET/RESET cycling with different SET pulse amplitudes but the same 10-ns pulsewidth (+1.3 V/10 ns, +1.6 V/10 ns, and +1.9 V/10 ns). This inherently stochastic switching is caused by the randomness of the oxygen vacancy's generation and migration, which is captured in the variation (3). At some point, the variable that describes the gap of the filament may fluctuate largely enough, then the successful switching is activated with enough electric field on the smaller gap of the filament under the same bias condition. Increasing the SET pulse amplitude increased the SET success probability. Fig. 12 shows the simulated stochastic switching behaviors and compared them with measured data.

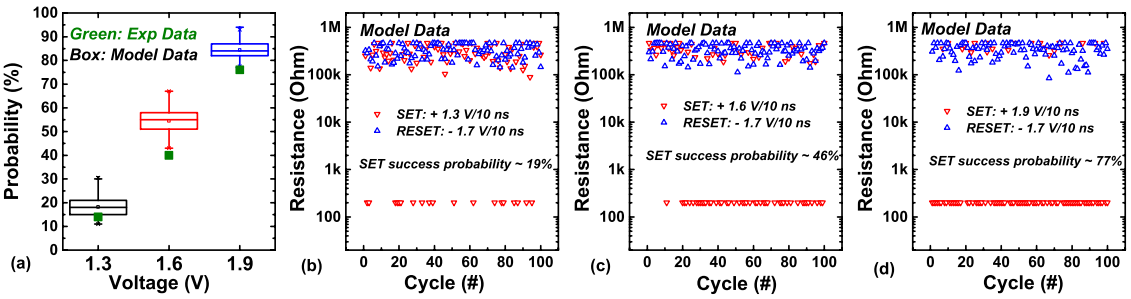


Fig. 12. (a) Comparison of the experimental and simulated result (100 rounds of continuous cycling were performed in the simulation). (b)–(d) Simulated SET/RESET continuous cycling with different SET pulse amplitudes/pulsewidths (+1.3 V/10 ns, +1.6 V/10 ns, and +1.9 V/10 ns).

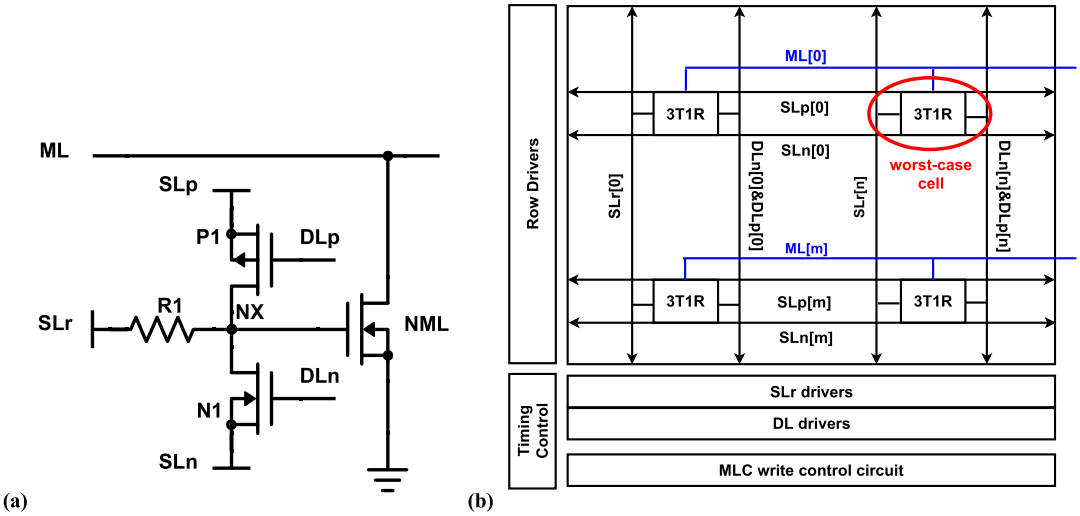


Fig. 13. (a) Schematic of 3T1R TCAM cell. (b) TCAM macrostructure.

V. Application Example

As an illustration of using this compact model for the system design, we consider the design of a reported 8-Mb TCAM macro [15] that uses three transistors and one RRAM (3T1R). The schematic of the 3T1R TCAM cell is shown in Fig. 13(a), comprising a ML cell RRAM device (R1), nMOS transistor (N1), pMOS transistor (P1), and nMOS ML-driver (NML). The gate and the source of N1 are connected to DLn and SLn, respectively. The gate and the source of P1 are connected to DLp and SLp, respectively. R1 is placed between the drain terminal (NX) of P1/N1 and the column-based resistor-source-line (SLr). Applying different bias conditions on DLn, DLp, SLr, SLn, and SLp, we can program the RRAM to 0, 1, or X (intermediate resistance state (MRS) in [15]) or search the data. For example, in write-1 (W1) operations, R1 is SET to LRS in which DLn = $V_{\text{G-SET-L}}$, SLr = V_{SET}, and SLn = 0 V, with sufficient write current (I_{SET}) flowing through N1. In search-1 (S1) operations, P1 and R1 form a voltage divider in which SLr = DLp = DLn = 0 V. If $R1 = 0$ (HRS), the voltage at node NX (V_{NX}) exceeds the threshold voltage of NML ($V_{\text{TH-NML}}$), enabling NML to generate a large $\text{I}_{\text{ML-MIS}}$ to pull down ML voltage V_{ML} and perform the mismatch operation. If $R1 = 1/X$ (LRS/MRS), then V_{NX} is below $V_{\text{TH-NML}}$. Thus, NML is in the cutoff region with ultrasmall $\text{I}_{\text{ML-M}}$ ($\sim$0, $\ll I_{\text{ML-MIS}}$), enabling it to perform the match operation. Fig. 13(b) shows the array structure in the TCAM macro, where worst case cell is circled. In the simulation, the programming energy of a single TCAM cell and the search time of the worst case cell with wiring resistance and capacitance are considered. The programming energy and the time delay resulted from drivers and timing controls are not included.

We use the model to optimize for lowering the programming energy and shortening the search delay. The characteristics of RRAM devices are influenced by the intrinsic fluctuation of the RRAM devices and the variations of the device structure due to variations of the fabrication process. These variations can impact the programming energy and the search delay (i.e., the latency). Without loss of generality, we consider the W1 programming energy and the S1 search time. RRAM is assumed at HRS in the search time simulation. The wiring parasitic latency and the development time [15] are considered as the search time. We simulate RRAM with various model parameters (I_0 and V_0) to gain insights on how these RRAM characteristics may impact the programming energy and the search delay (Fig. 14). The programming energy and the search delay can be estimated by integrating the model in the SPICE simulation. Increasing the RRAM programming current level I_0 and decreasing the value of the nonlinearity parameter of the resistance curve V_0 can decrease the search delay, but the programming energy will be increased at the same time. Tradeoffs of the characteristics of RRAM devices can be explored to optimize the search delay and the programming energy for the target application specifications.

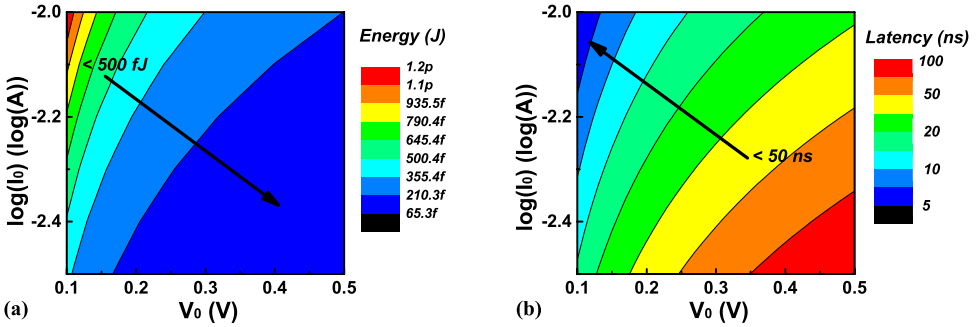


Fig. 14. Ranges of (a) programming energy and (b) search delay with different characteristics of RRAM devices. The parameters (I_0 and V_0) of the model are varied.

VI. Conclusion

This paper presents a parameter extraction method and experimental validation for a Verilog-A RRAM compact model that considers the statistical variability of filament evolution. In addition to the dc switching characteristics, this model also captures the ac programming transient current behavior and SET stochastic switching under weak programming conditions. The salient physics of RRAM with various materials and device structures, such as TiO_X/HfO_X bilayer RRAM and HfO_X RRAM with Al-doping, are captured in the model and reflected in the simulation results. The agreement between the simulated and measured data suggests that this physics-based compact model can be used for circuit simulations to guide the analysis and optimization of various circuit and system designs involving RRAM.

Acknowledgment

The authors would like to thank AIXTRON for collaboration in device fabrication of the bilayer resistive random access memory, and IMEC for supplying the device for the Al-doped HfO_X RRAM. This work has benefited from discussions with P.-Y. Chen from Arizona State University, C.-W. Hsu from National Chiao Tung University, and J. Engel, H. Li, X. Zheng, C.-W. Hsu, and C.-S. Lee from Stanford University (J. Engel is currently affiliated with Baidu Inc.).

References

[1] K. Tsunoda *et al.*, "Low power and high speed switching of Ti-doped NiO ReRAM under the unipolar voltage source of less than 3 V," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2007, pp. 767–770.

[2] H. Y. Lee *et al.*, "Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO_2 based RRAM," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2008, pp. 1–4.

[3] B. Govoreanu *et al.*, "10×10 nm^2 Hf/HfO_x crossbar resistive RAM with excellent performance, reliability and low-energy operation," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 31.6.1–31.6.4.

[4] X. P. Wang *et al.*, "Highly compact 1T-1R architecture ($4F^2$ footprint) involving fully CMOS compatible vertical GAA nano-pillar transistors and oxide-based RRAM cells exhibiting excellent NVM properties and ultra-low power operation," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 20.6.1–20.6.4.

[5] H.-S. P. Wong *et al. Stanford Memory Trends*, accessed on Oct. 2015. [Online]. Available: https://nano.stanford.edu/stanford-memory-trends

[6] T.-Y. Liu *et al.*, "A 130.7 mm^2 2-layer 32 Gb ReRAM memory device in 24 nm technology," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2013, pp. 210–211.

[7] I. G. Baek *et al.*, "Realization of vertical resistive memory (VRRAM) using cost effective 3D process," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 31.8.1–31.8.4.

[8] W. C. Chien *et al.*, "Multi-layer sidewall WO_x resistive memory suitable for 3D ReRAM," in *Proc. Symp. VLSI Technol. (VLSIT)*, 2012, pp. 153–154.

[9] H.-Y. Chen, S. Yu, B. Gao, P. Huang, J. Kang, and H.-S. P. Wong, "HfO_x based vertical resistive random access memory for cost-effective 3D cross-point architecture without cell selector," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 20.7.1–20.7.4.

[10] H.-J. Kim *et al.*, "1 GB/s 2Tb NAND flash multi-chip package with frequency-boosting interface chip," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.

[11] S. Park *et al.*, "RRAM-based synapse for neuromorphic system with pattern recognition function," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 10.2.1–10.2.4.

[12] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, and H.-S. P. Wong, "A neuromorphic visual system using RRAM synaptic devices with sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 10.4.1–10.4.4.

[13] S. Park *et al.*, "Neuromorphic speech systems using advanced ReRAM-based synapse," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 25.6.1–25.6.4.

[14] L.-Y. Huang *et al.*, "ReRAM-based 4T2R nonvolatile TCAM with 7× NVM-stress reduction, and 4× improvement in speed-wordlength-capacity for normally-off instant-on filter-based search engines used in big-data processing," in *Proc. Symp. VLSI Circuit (VLSIC)*, 2014, pp. 1–2.

[15] M.-F. Chang *et al.*, "A 3T1R nonvolatile TCAM using MLC ReRAM with sub-1 ns search time," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.

[16] A. Lee *et al.*, "RRAM-based 7T1R nonvolatile SRAM with 2× reduction in store energy and 94× reduction in restore energy for frequent-off instant-on applications," in *Proc. Symp. VLSI Circuit (VLSIC)*, 2015, pp. C76–C77.

[17] X. Guan, S. Yu, and H.-S. P. Wong, "A SPICE compact model of metal oxide resistive switching memory with variations," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1405–1407, Oct. 2012.

[18] M. Bocquet *et al.*, "Robust compact model for bipolar oxide-based resistive switching memories," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 674–681, Mar. 2014.

[19] J. Noh *et al.*, "Development of a semiempirical compact model for DC/AC cell operation of HfO_x-based ReRAMs," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 1133–1135, Sep. 2013.

[20] P. Huang *et al.*, "A physics-based compact model of metal-oxide-based RRAM DC and AC operations," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4090–4097, Dec. 2013.

[21] H. Li, P. Huang, B. Gao, B. Chen, X. Liu, and J. Kang, "A SPICE model of resistive random access memory for large-scale memory array simulation," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 211–213, Feb. 2014.

[22] Z. Jiang, *et al.*, "Stanford University Resistive-Switching Random Access Memory (RRAM) Verilog-A Model," accessed on Oct. 2014. [Online]. Available: https://nanohub.org/publications/19, doi: 10.4231/D37H1DN48.

[23] Z. Jiang, S. Yu, Y. Wu, J. H. Engel, X. Guan, and H.-S. P. Wong, "Verilog-A compact model for oxide-based resistive random access memory," in *Proc. Int. Conf. Simulation Semiconductor Process. Devices (SISPAD)*, 2014, pp. 41–44.
[24] X. Guan, S. Yu, and H.-S. P. Wong, "On the switching parameter variation of metal-oxide RRAM—Part I: Physical modeling and simulation methodology," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1172–1182, Apr. 2012.
[25] S. Yu, X. Guan, and H.-S. P. Wong, "On the switching parameter variation of metal oxide RRAM—Part II: Model corroboration and device design strategy," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1183–1188, Apr. 2012.
[26] S. Yu and H.-S. P. Wong, "A phenomenological model of oxygen ion transport for metal oxide resistive switching memory," in *Proc. IEEE Int. Memory Workshop (IMW)*, May 2010, pp. 1–4.
[27] D. Veksler *et al.*, "Methodology for the statistical evaluation of the effect of random telegraph noise (RTN) on RRAM characteristics," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 9.6.1–9.6.4.
[28] J. McPherson, J.-Y. Kim, A. Shanware, and H. Mogul, "Thermochemical description of dielectric breakdown in high dielectric constant materials," *Appl. Phys. Lett.*, vol. 82, no. 13, p. 2121, 2003.
[29] Synopsys, Inc., "HSPICE," accessed on Jan. 2016. [Online]. Available: https://www.synopsys.com/tools/Verification/AMSVerification/CircuitSimulation/HSPICE/Pages/default.aspx
[30] S. Yu, X. Guan, and H. S. P. Wong, "Understanding metal oxide RRAM current overshoot and reliability using kinetic Monte Carlo simulation," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2012, pp. 26.1.1–26.1.4.
[31] E. Yalon, A. A. Sharma, M. Skowronski, J. A. Bain, D. Ritter, and I. V. Karpov, "Thermometry of filamentary RRAM devices," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2972–2977, Sep. 2015.
[32] S. Long *et al.*, "A model for the set statistics of RRAM inspired in the percolation model of oxide breakdown," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 999–1001, Aug. 2013.
[33] A. Chen *et al.*, "Utilizing the variability of resistive random access memory to implement reconfigurable physical unclonable functions," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 133–140, Feb. 2015.
[34] N. Raghavan *et al.*, "Stochastic variability of vacancy filament configuration in ultra-thin dielectric RRAM and its impact on OFF-state reliability," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2013, pp. 21.1.1–21.1.4.
[35] P. Gonon *et al.*, "Resistance switching in HfO_2 metal-insulator-metal devices," *Appl. Phys. Lett.*, vol. 107, no. 7, p. 074507, 2010.
[36] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, and H.-S. P. Wong, "Stochastic learning in oxide binary synaptic device for neuromorphic computing," *Frontiers Neurosci.*, vol. 7, Oct. 2013, Art. no. 186.

Zizhen Jiang (S'13) received the B.S. (Hons.) degree from Peking University, Beijing, China, in 2012, and the M.S. degree from Stanford University, Stanford, CA, USA, in 2014, where she is currently pursuing the Ph.D. degree with the Department of Electrical Engineering.

Yi Wu received the B.S. degree from Peking University, Beijing, China, in 2008, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Stanford University, Stanford, CA, USA, in 2010 and 2013, respectively.

She is currently a Hardware Engineer with Oracle Corporation, Santa Clara, CA, USA.

Shimeng Yu (S'10–M'14) received the B.S. degree from Peking University, Beijing, China, in 2009, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Stanford University, Stanford, CA, USA, in 2011 and 2013, respectively.

He is currently an Assistant Professor of Electrical Engineering with Arizona State University, Tempe, AZ, USA.

Lin Yang received the B.E. degree from the South China University of Technology, Guangzhou, China, and the master's and Ph.D. degrees in materials science from RWTH Aachen University, Aachen, Germany.

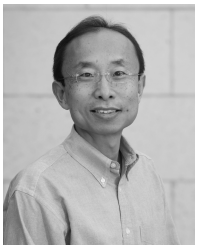
He is currently a Process Engineer with AIXTRON, Inc., Sunnyvale, CA, USA.

Kay Song received the B.S. degree in chemistry from Nanjing University, Nanjing, China, the M.S. degree in chemistry from the University of Iowa, Iowa City, IA, USA, and the Ph.D. degree in solid-state chemistry from the University of California at Davis, Davis, CA, USA.

She is currently a Senior Manager of Business Development and Technology with AIXTRON, Inc., Sunnyvale, CA, USA.

Zia Karim (M'89) received the B.S. and M.S. degrees in electrical and electronic engineering from the Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, and the Ph.D. degree in electronics engineering from Dublin City University, Dublin, Ireland.

He is currently the Vice President of Business Development and Global Customer Support with AIXTRON, Inc., Sunnyvale, CA, USA.



H.-S. Philip Wong (F'01) received the B.Sc. (Hons.) degree from the University of Hong Kong, Hong Kong, in 1982, the M.S. degree from the State University of New York at Stony Brook, Stony Brook, NY, USA, in 1983, and the Ph.D. degree from Lehigh University, Bethlehem, PA, USA, in 1988.

He is currently the Willard R. and Inez Kerr Bell Professor with Stanford University, Stanford, CA, USA.