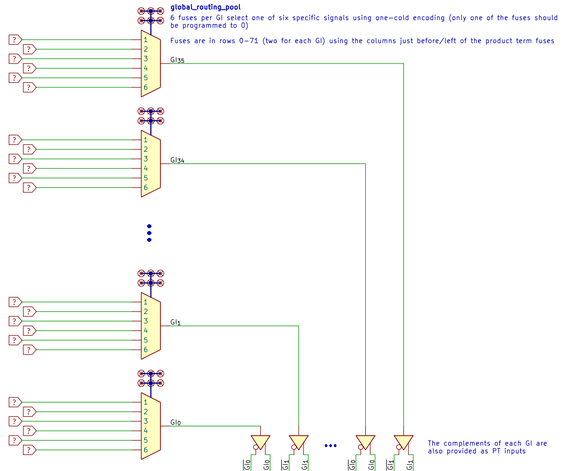
Generic Input (GI) Routing

36 GIs per GLB

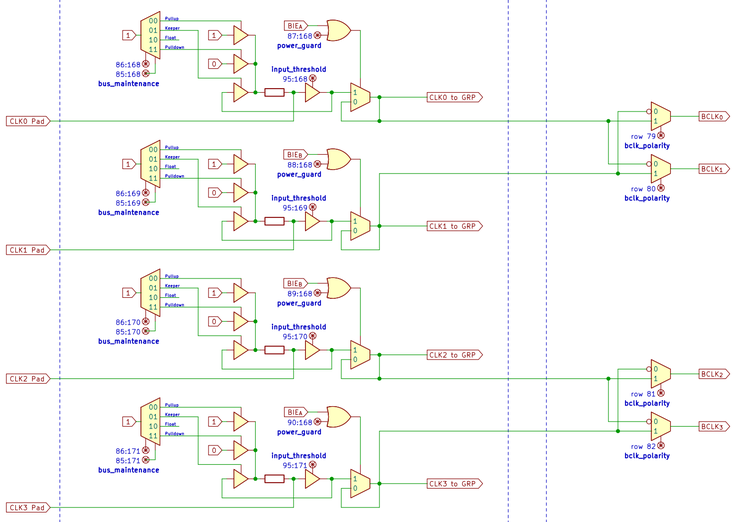
Each GI has a different hardcoded set of possible signals, but they are the same for every GLB. i.e. GI0 in GLBa has the same options as GI0 in GLBb

The set of all routable signals is called the "Global Routing Pool" (GRP)



Clock Input Cells

Shared between all GLBs

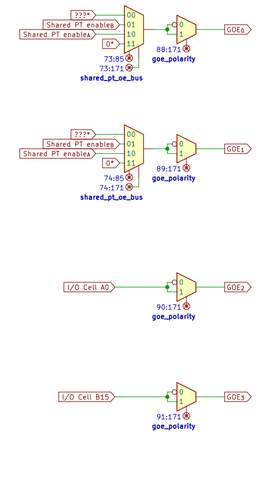


GLB Clocks

Column 89 for GLB A
Column 3 for GLB B

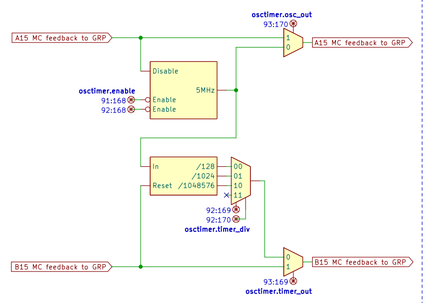
Global OEs

Shared between all GLBs



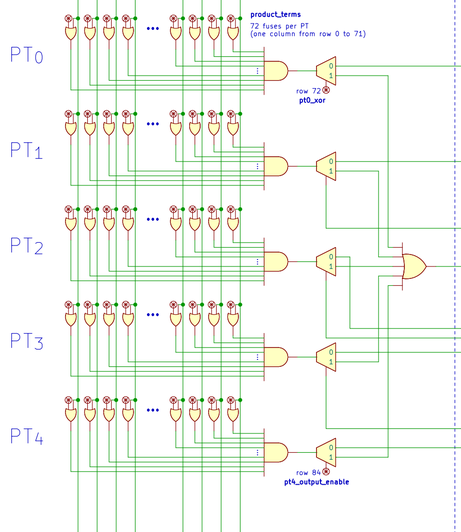
Oscillator/Timer

Shared between all GLBs

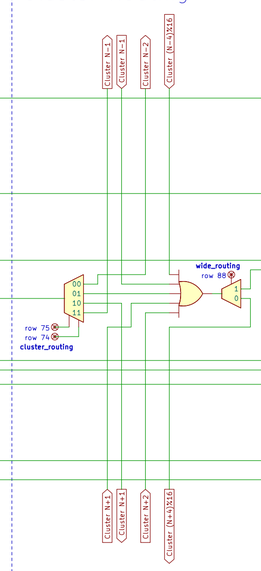


"Macrocell Slice" (1/16)

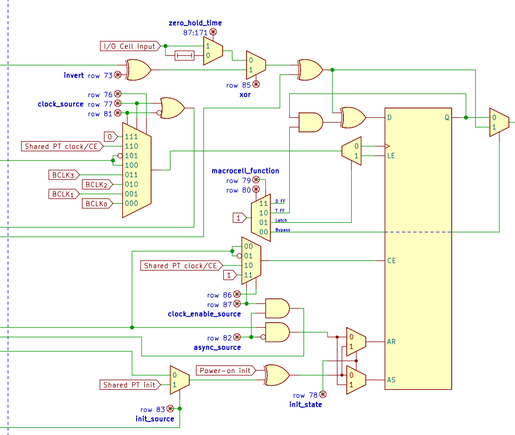
Product Term (PT) Cluster



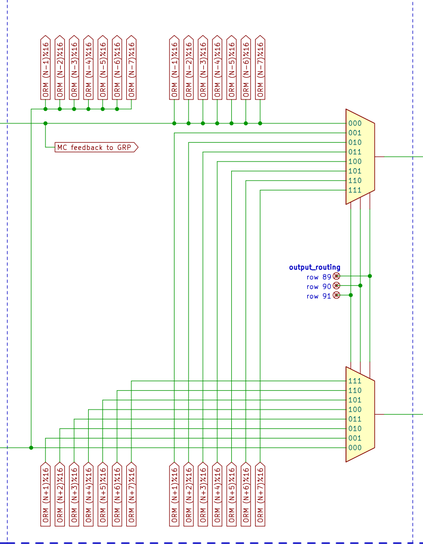
Cluster Routing



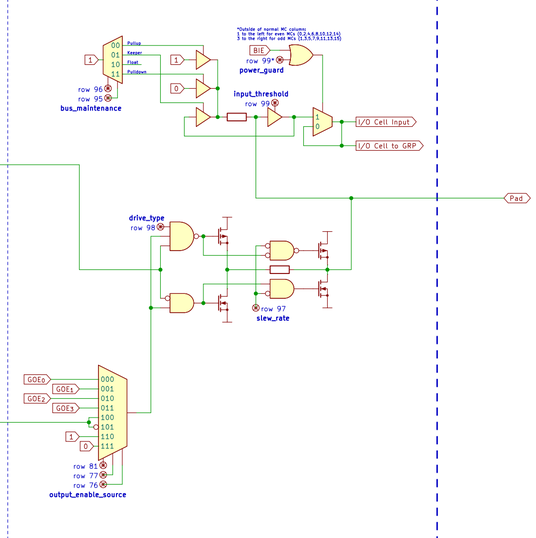
Macrocell (MC)



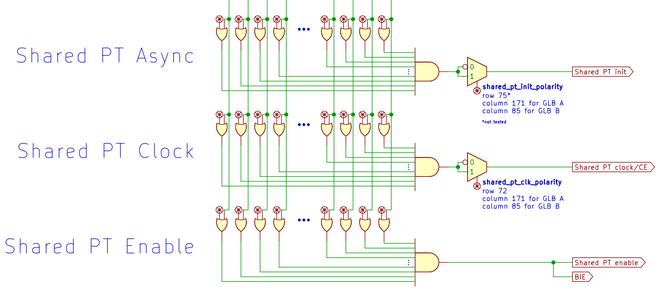
Output Routing Muxes (ORM)



I/O Cell



Shared PT Async



Generic Logic Block (GLB)

Device contains 2 GLBs, A and B

LC4032ZE