LC4032ZE

Generic Logic Block (GLB)

Device contains 2 GLBs, A and B

"Macrocell Slice" (1/16)

Generic Input (GI) Routing

36 GIs per GLB

Each GI has a different hardcoded set of possible signals, but they are the same for every GLB. i.e. GI0 in GLBA has the same options as GI0 in GLBB

The set of all routable signals is called the "Global Routing Pool" (GRP)

6 fuses per GI select one of six specific signals using one-cold encoding (only one of the fuses should be programmed to 0)

Fuses are in rows 0–71 (two for each GI) using the columns just before/left of the product term fuses

GI35

GI34

GI1

GI0

The complements of each GI are also provided as PT inputs

Clock Input Cells

Shared between all GLBs

CLK0 Pad

CLK1 Pad

CLK2 Pad

CLK3 Pad

CLK0 to GRP

CLK1 to GRP

CLK2 to GRP

CLK3 to GRP

GLB Clocks

Column 89 for GLB A
Column 3 for GLB B

BCLK0

BCLK1

BCLK2

BCLK3

Global OEs

Shared between all GLBs

GOE0

GOE1

GOE2

GOE3

Product Term (PT) Cluster

PT0

PT1

PT2

PT3

PT4

72 fuses per PT (one column from row 0 to 71)

Cluster Routing

Macrocell (MC)

I/O Cell Input

Shared PT clock/CE

Shared PT async

Power-on init

Output Routing Muxes (ORM)

MC feedback to GRP

I/O Cell

Pad

Shared PT Async

Shared PT async

Shared PT Clock

Shared PT clock/CE

Shared PT Enable

BIE