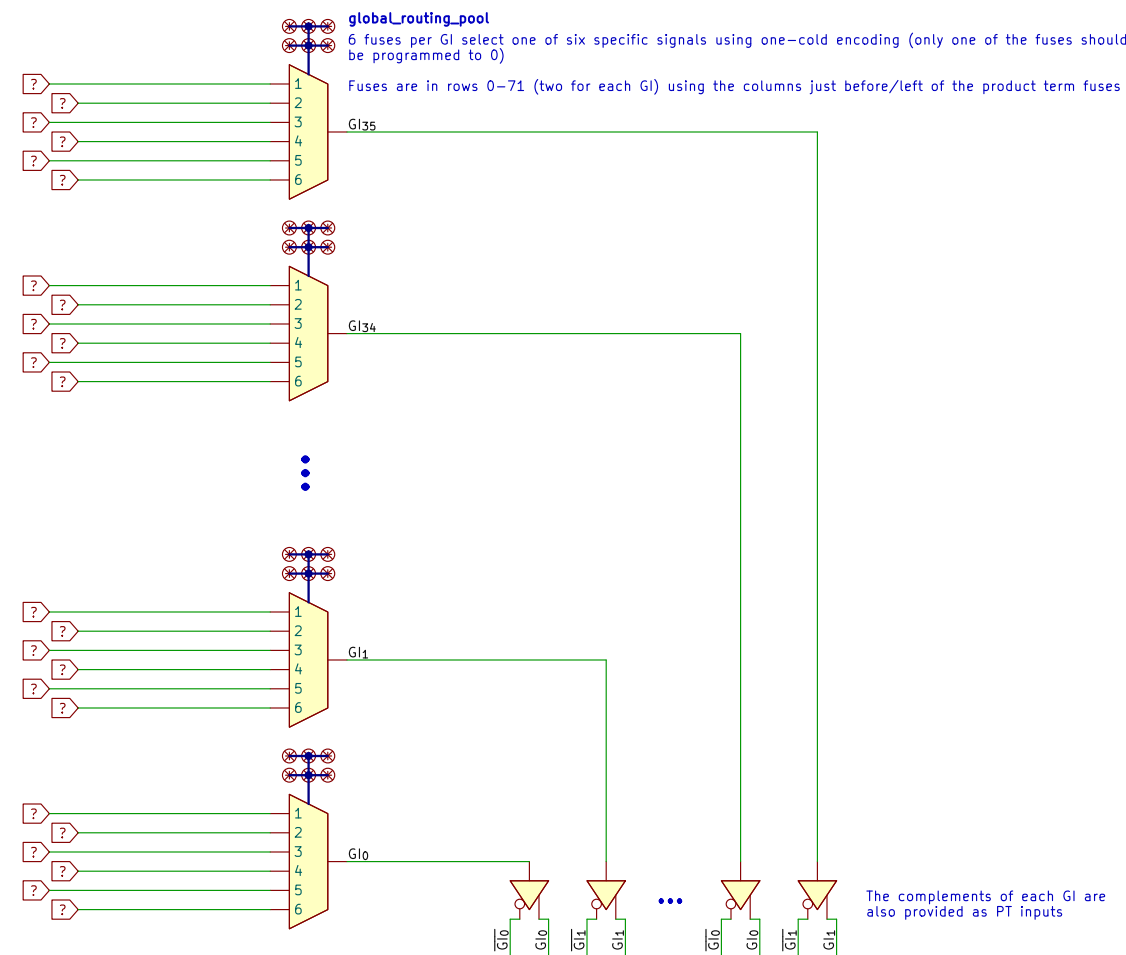


Generic Input (GI) Routing

36 GIs per GLB

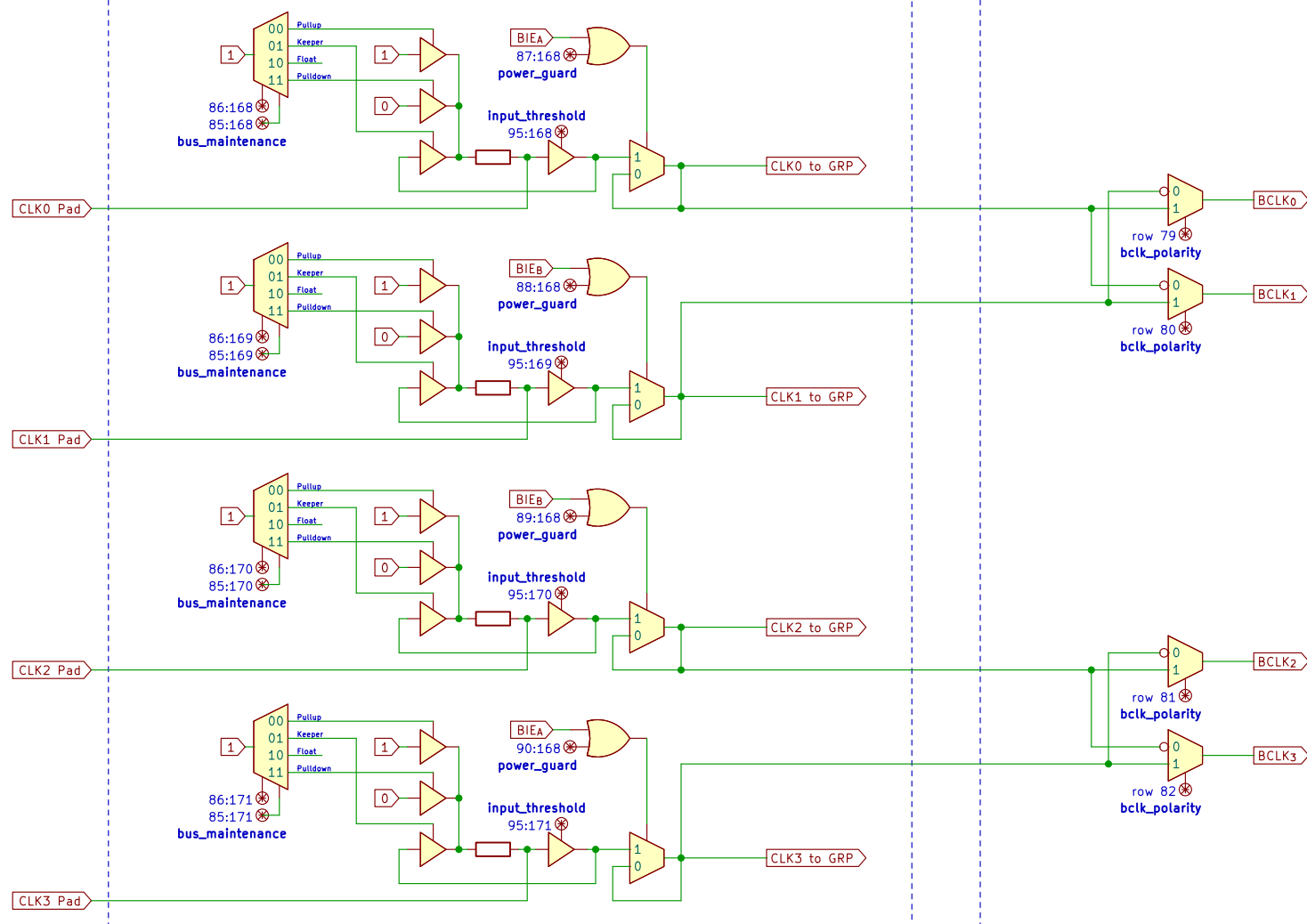
Each GI has a different hardcoded set of possible signals, but they are the same for every GLB. I.e. Gio in GLB A has the same options as Gio in GLB B.

The set of all routable signals is called the "Global Routing Pool" (GRP)



Clock Input Cells

Shared between all GLBs



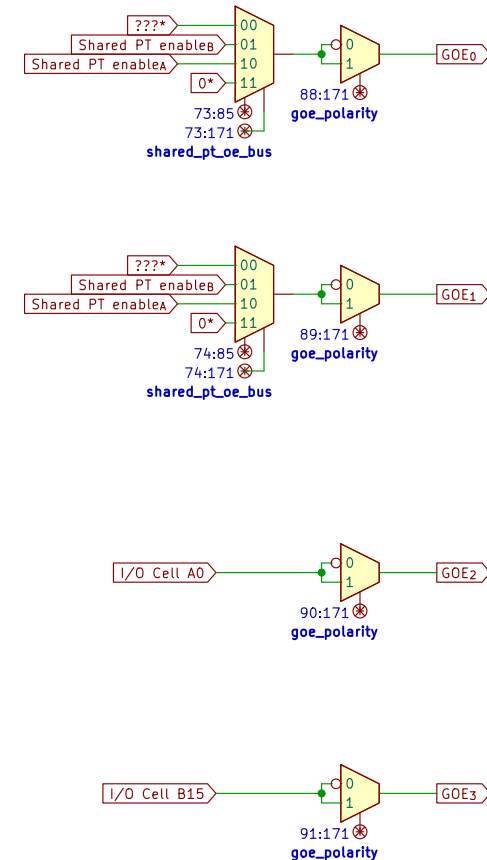
GLB Clocks

Column 89 for GLB A
Column 3 for GLB B



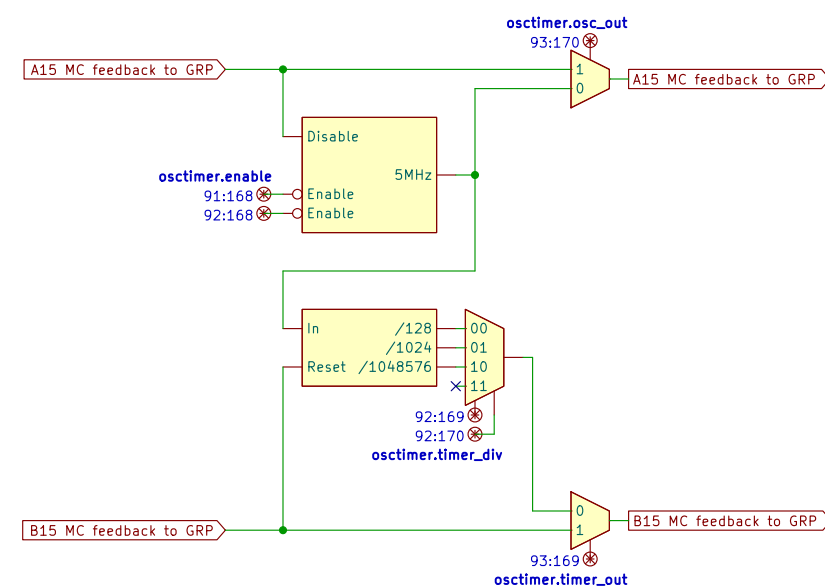
Global OEs

Shared between all GLBs



Oscillator/Timer

Shared between all GLBs



Product Term (PT) Cluster

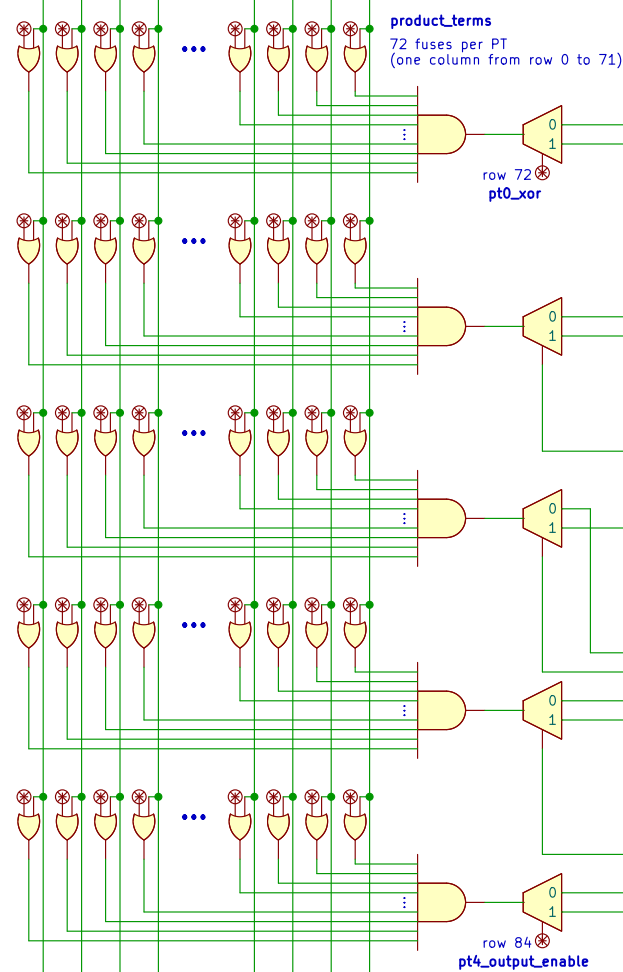
PT0

PT1

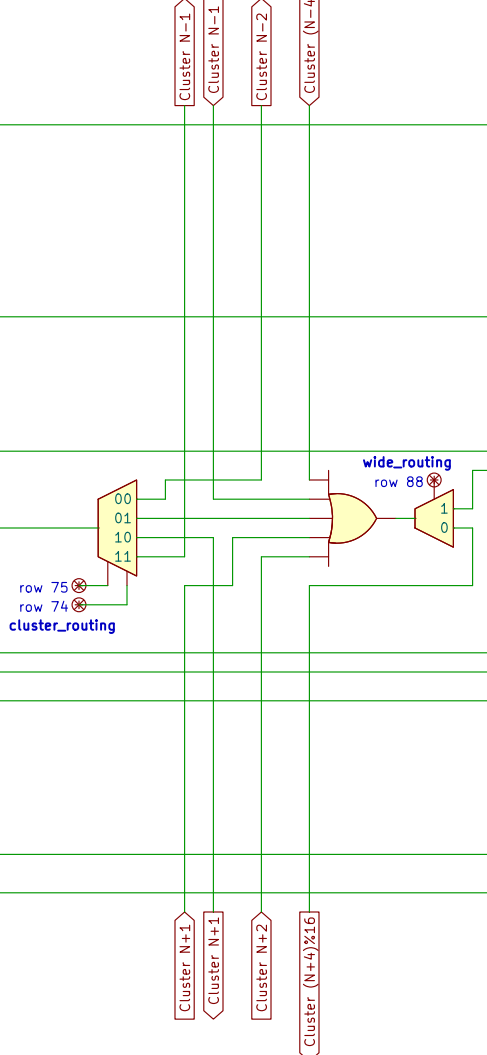
PT2

PT3

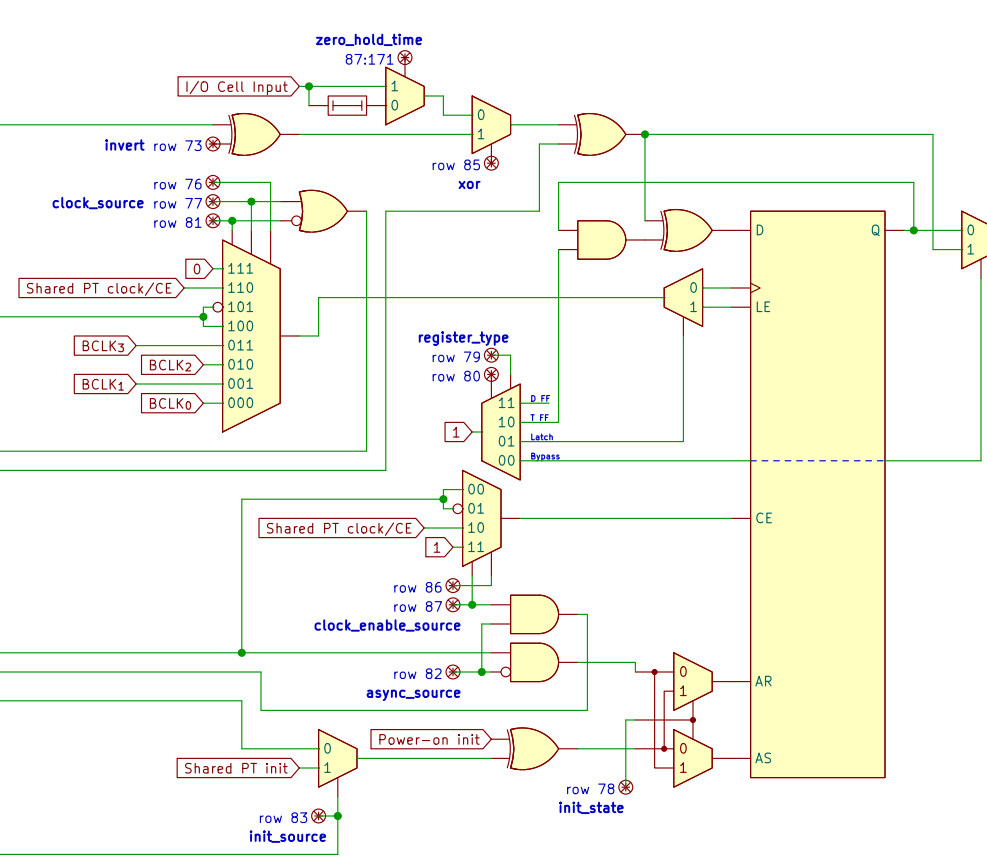
PT4



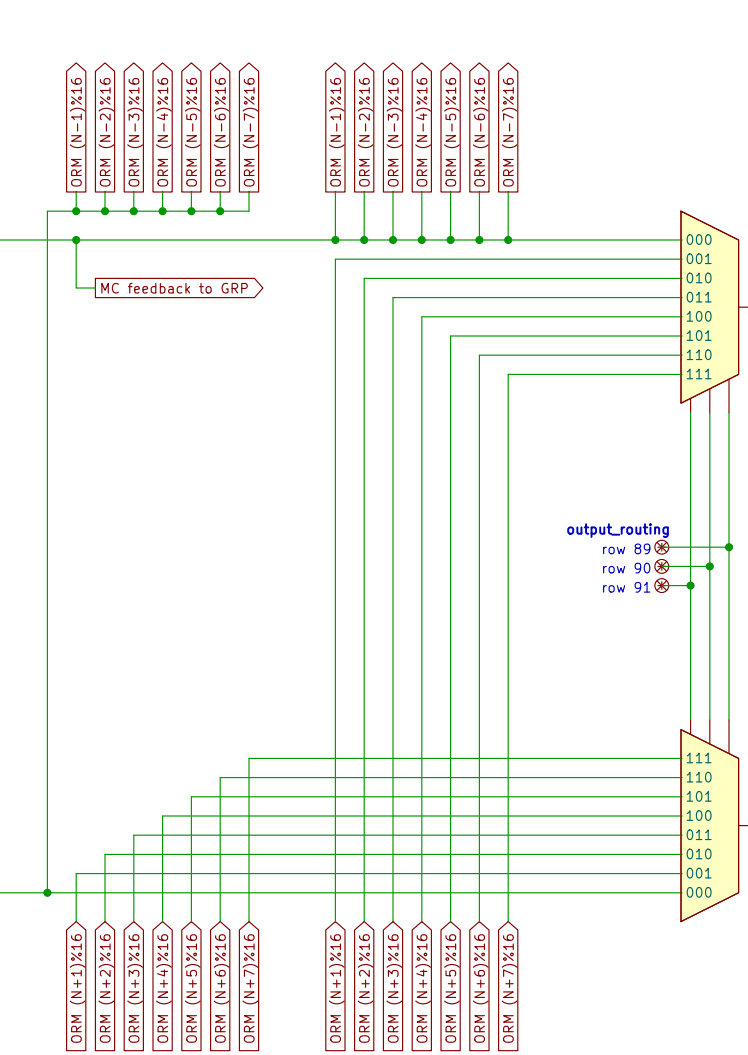
Cluster Routing



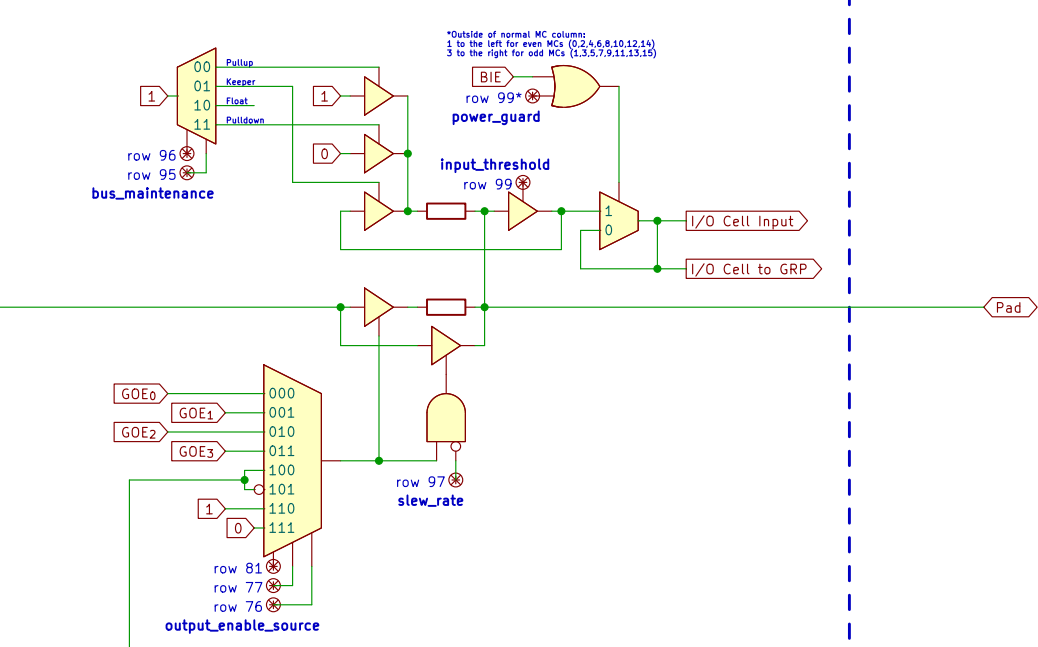
Macrocell (MC)



Output Routing Muxes (ORM)



I/O Cell

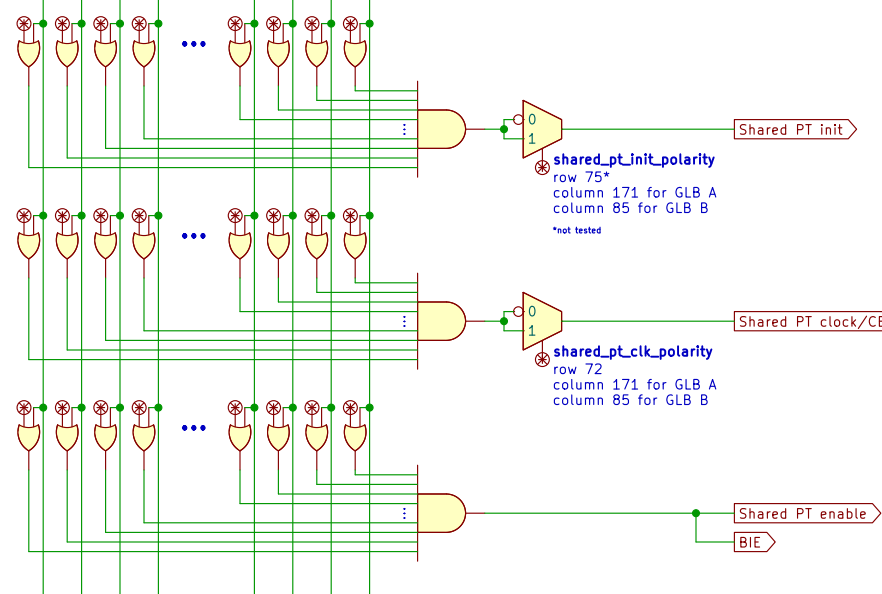


"Macrocell Slice" (1/16)

Shared PT Async

Shared PT Clock

Shared PT Enable



Generic Logic Block (GLB)

Device contains 2 GLBs, A and B

LC4032ZE