ECE 6580 Module Projects

Module Project: #1

For those who choose Option (B), please take pictures and show measurement waveforms in the picture next to the circuit.

Please upload all documentation for this module on iLearn by the due date.

Modules must be completed on time for full credit.

Please feel free to ask me questions if you have any about the project. I am more concerned with how you obtained your answers than what your answers are. Feel free to experiment with components and configurations – exploratory endeavors will give you higher marks!

All Students:

1. Find and review 5 journal or conference publications that use either Wheatstone bridges, PLLs, or Lock-in Amplifiers in their instrumentation. Make a detailed discussion on what each paper proposes and how the circuitry is used (keep these discussions to approximately 5 pages using single column, single spacing, and 12pt font. Please label any figures similar to the style I have in the modules.

Choose and complete either Option A or Option B (do not do both).

2. Option (A):
    a. Simulate the circuit in Fig. 5 (the N-channel based VOC) – include the varicaps in the simulation and plot the waveforms across Q1 and Q2 to ground, and across the inductor. Attach a load resistor to the "output" as shown in Fig. 5 and plot the power output vs load resistance for a 30V Vcc. How does this profile change with frequency?
    b. Next, mathematically derive the circuit operation and show the equations for output current across an optimum load resistance (i.e. the load resistance that gave the best power output in (a)).
    c. Discuss/suggest ways to improve the circuit in 1-2 pages.

2. Option (B):
    a. Construct an AC wheatstone bridge that uses an inductor as an eddy current transducer (you will need to fabricate the inductor). However, instead of using a tunable inductor to balance the bridge, utilize a variable resistor (potentiostat) as the balancing element. The goal will be to detect a non-ferrous metal target as it approaches the inductor.
    b. Measure the amplitude and phase angle change (if any) at the wheatstone bridge's output and compare it to the Vin waveform as a piece of non-ferrous metal moves towards the transducing coil. What happens?
    c. Discuss what you observe by plotting the data (I will grade you on how understandable your graph is) and calculate the minimum S/N (this minimum will be found at the max distance the non-ferrous object can be detected).

Instrumentation Circuits Using Bridges, PLLs, and Lock-In Amplifiers

Blaine Swieder

February 7, 2026

1 Introduction

Modern measurement and sensing systems are becoming more reliant on sophisticated analog and mixed-signal circuitry to extract weak physical signals from noisy environments. In many applications that range from biomedical monitoring to industrial inspection and environmental sensing, the fundamental challenge lies in accurately converting small changes in resistance, capacitance, or impedance into reliable electrical quantities suitable for digital processing. Among the most widely adopted architectures for this purpose are Wheatstone bridge networks, phased-locked loops (PLLs), and lock-in amplifiers (LIAs). These techniques provide complementary mechanisms for signal conversion, noise suppression, and drift compensation.

Wheatstone Bridges convert resistance or impedance variations into differential voltage signal while rejecting common-mode interference. Phased-Locked Loops (PLLs)-based readout circuits encode sensor information in the frequency domain, offering inherent robustness against amplitude noise and supply variations. Lock-In Amplifiers (LIAs) exploit synchronous detection to isolate modulated sensor signals from broadband noise and interference. Moreover, when properly designed, these architectures can achieve microvolt-level resolution and sub-part-per-million stability.

2 Related Works

Throughout this document, we will review five peer-reviewed publications that exemplify the application of Wheatstone Bridges [1, 2], PLLs [3], and lock-in amplifiers [4, 5] in practical instrumentation systems. For each paper, our emphasis focuses on circuit topology, signal-conditioning pathways, noise mitigation strategies, performance metrics, and design tradeoffs. These reviewed papers collectively demonstrate both the enduring relevance and the evolving implementation of these fundamental architectures.

2.1 Chopper-Stabilized Bridge Readout for Resistive Microsensors

Choi et al. presents a low-noise readout interface for resistive microsensors employing a Wheatstone Bridge front-end combined with a chopper-stabilized instrumentation amplifier. The sensing element is incorporated into a full-bridge configuration, allowing resistance variations to be converted into differential voltage signals [1]. This topology inherently suppresses common-mode disturbances like supply ripple, electromagnetic interference, and temperature-induced resistance drift. The Wheatstone Bridge consists of four resistive elements arranged in a balanced configuration. Under nominal conditions, the differential output is zero [1]. When the sensor resistance changes, an imbalance occurs, generating a proportional differential voltage as this voltage is typically on the order of microvolts, which necessitates a high-gain, low-noise amplification. To address this challenge, Choi et al. employ a folded-cascode instrumentation amplifier with chopper stabilization. The folded-cascode topology offers high open-loop gain and large output swing while operating at low-supply voltages. In addition, chopper stabilization periodically modulates the input signal to a higher frequency, effectively shifting low-frequency offset and 1/f noise out of the signal band [1]. After amplification, demodulation and filtering removes the modulated noise components. The signal chain includes correlated double sampling, programmable gain amplifiers, and a successive-approximation ADC and correlated double sampling further surpresses offset and low-frequency noise by subtracting successive samples taken during known operating states [1]. Additionally, programmable gain stages allow adaptation to different sensor sensitivities. Measured input-referred noise density is reported below $50nV/\sqrt{Hz}$, enabling sub-microvolt resolution. Power consumption is minimized using bias-current recycling and duty-cycled operation and the circuit operates from a low-voltage supply while maintaining high dynamic range

[1]. One important contribution of Choi et al. is the demonstration that traditional bridge-based sensing can be combined with advanced CMOS noise-reduction techniques to achieve a state-of-the-art performance [1]. However, the use of chopping introduces ripple artifacts and switching noise, which requires careful filtering. In addition, the bandwidth is limited by the chopper frequency and low-pass filter characteristics [1]. Overall, this work by Choi et al. shows how precision analog design techniques can extend the applicability of Wheatstone bridges to ultra-low-signal environments.

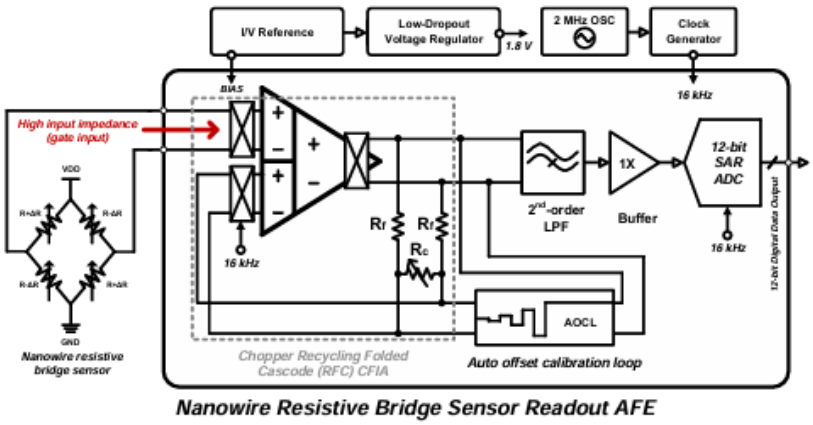

Figure 1: Top block diagram of the proposed resistive-bridge microsensor readout IC.

2.2 PLL-Based Capacitive Readout for Hydrogen Sensors

Enache et al. proposes a phase-locked loop-based interface for silicon carbide MOS capacitor hydrogren sensors [3]. In this architecture, sensor capacitance variations are converted into frequency changes through a voltage-controlled oscillator (VCO) embedded in an PLL loop. Rather than measuring voltage or current directly, the system encodes physical information in the frequency domain [3]. The sensing element modifies the capacitance of the VCO tank circuit, and changes in hydrogen concentration alters the dielectric properties of the sensor, hence modulating capacitance. This modulation shifts the oscillation frequency and the PLL tracks this frequency and produces a stable digital representation [3].

The PLL consists of a phase detector, charge pump, loop filter, and digitally controlled oscillator. The phase detector compares the VCO output with a reference

clock, generating an error signal proportional to phase difference [3]. The loop filter integrates this error and adjusts the VCO control voltage. Through feedback, the system locks onto the sensor-modulated frequency [3]. This architecture proposed by Enache et al offers several advantages, these are: frequency-based sensing is inherently immune to amplitude noise, offset drift, and many forms of interference, supply variations and temperature fluctuations affect amplitude more than frequency, improving long-term stability. Furthermore, digital frequency measurement simplifies downstream processing [3].

Enache et al. employ a ring-VCO topology with varactor tuning that is used to achieve wide frequency range. Phase noise and jitter are minimized through careful biasing and layout. The measured frequency resolution exceeds 0.1 ppm, which enables detection of small hydrogen concentrations [3]. On the contrary, PLL dynamics introduces tradeoffs between noise surpression and response time, which a narrow loop bandwidth improves noise filtering but slows sensor response. On the other hand, wide bandwidth improves responsiveness but increases jitter [3]. The loop filter must therefore be optimized for the specific application. In addition, PLLs consume more power than simple voltage readout circuits and require careful design to avoid spurious locking and instability. Despite these challenges, Enache et al. demonstrate the effectiveness of frequency-domain encoding for capacitive sensing [3].

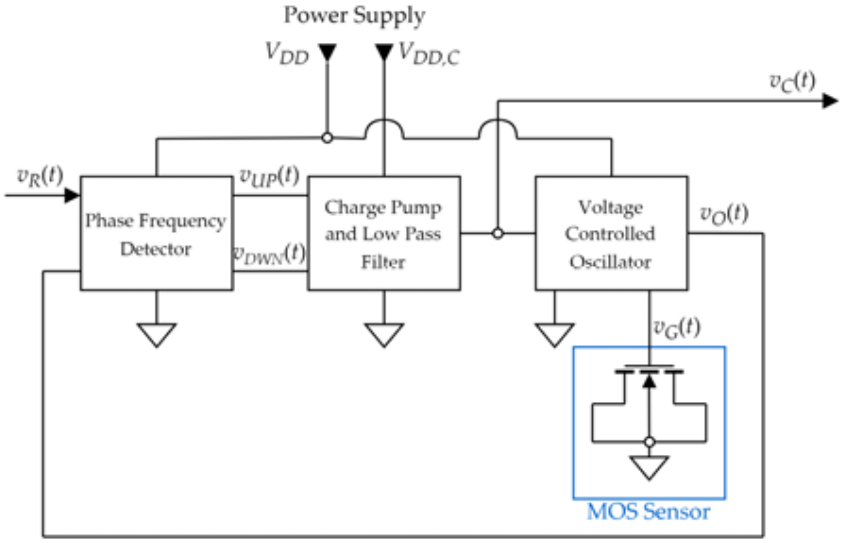

Figure 2: Proposed Digital PLL readout block schematic by Enache et al.

2.3 Integrated Low-Power Lock-In Amplifier for Gas Detection

Maya et al. discuss a fully integrated CMOS lock-in amplifier (LIA) designed for low-power gas detection and the system employs synchronous detection to extract weak sensor signals modulated at a known carrier frequency. In their approach, Maya et al. effectively rejects broadband noise and low-frequency interference [5]. In their proposed architecture, the gas sensor is excited with a sinusoidal or square-wave carrier. The sensor response modulates this carrier modulates this carrier according to gas concentration and the output is amplified and multiplied by synchronized reference signals in quadrature [5]. After multiplication, low-pass filtering yields in-phase (I) and quadrature (Q) components. The front-end includes transimpedance amplifiers to convert snesor current into voltage, followed by programmable gain stages. Analog multipliers perform sysnchronous demodulation and quadrature detection compensates for phase shifts introduced by sensor impedance and signal paths [5]. The low-pass filters remove high-frequency components generated by multiplication, leaving the desired baseband signal. This process effectively acts as a narrowband filter centered at the modulation frequency, significantly improving signal-to-noise ratio. The CMOS implementation operates at supply voltages below 1.8 V and consumes less that $500\mu W$ [5]. The acheived SNR exceeds 80dV for low-frequency gas signals and the architecture supports programmable modulation frequency and gain, which enables adaptation to different sensors. A major advantage of this design is its robustness against environmental noise and drift; moreover, by shifting measurement to a higher frequency band, 1/f noise, and DC offsets are largely eliminated. However, multiplier nonlinearity, mismatch, and residual offset limit ultimate performance [5]. In addition, precise phase alignment is required for optimal demodulation and phase errors reduce signal amplitude and introduce cross-talk between I and Q channels. Hence, the system requires calibration and stable clock generation. Maya et al. demonstrates the suitability of lock-in techniques for low-power, high-sensitivity chemical sensing [5].

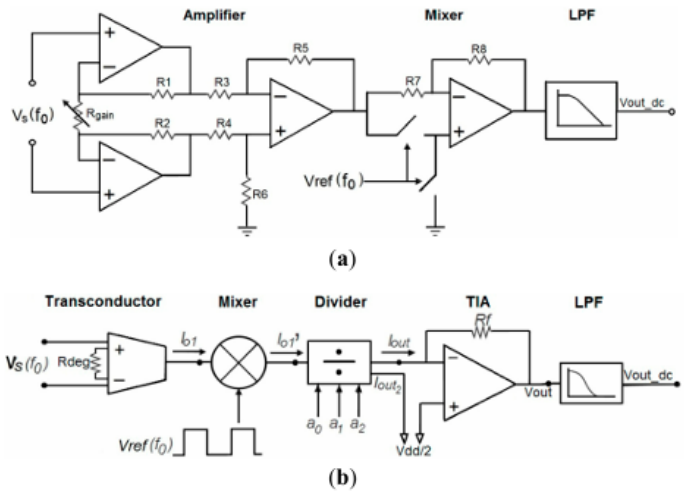

Figure 3: Lock-In Amplifiers Schemes: Conventional Voltage-Mode Approach and Proposed Topology from Maya et al.

2.4 AC Wheatstone Bridge for Eddy-Current Rail Inspection

Liu et al. investigate the usage of an AC Wheatstone Bridge for nondestructive rail inspection by using eddy-current sensing. Inductive coils serve as transducers whose impedance varies in response to metal defects and these coils are incorporated into a balanced bridge excited by a sinusoidal source [2]. The sensing coil is placed near the rail surface. Alternating Current induces eddy currents in the metal, which modifies the coil's impedance depending on material properties and defects, as cracks or corrosion alter eddy-current flow, producing impedance changes [2]. The Wheatstone Bridge converts these impedance variations into differential voltage signals and when balanced, the output is zero. Defects unbalance the bridge, which generates a signal proportional to impedance. Phase-sensitive detection separates resistive and reactive components, which enables discrimination between surface and subsurface defects. Instrumentation amplifiers with high common-mode rejection amplifies the bridge output [2]. Liu et al. analyze sensitivity as a function of excitation frequency, coil geometry, and stand-off distance and higher frequencies improve spatial resolution but reduces penetration depth and lower frequencies penetrate deeper but reduces sensitivity. Liu et al. experimental results demonstrates detection of sub-millimeter cracks at several centimeters distance as the system achieves high reliability under

field conditions [2]. Its limitations arise from parasitic capacitance, temperature-dependant resistance, and mechanical vibrations; moreover, compensation techniques are required for long-term stability. Nevertheless, this study by Liu et al highlights the continued relevance of bridge circuits in industrial inspection [2].

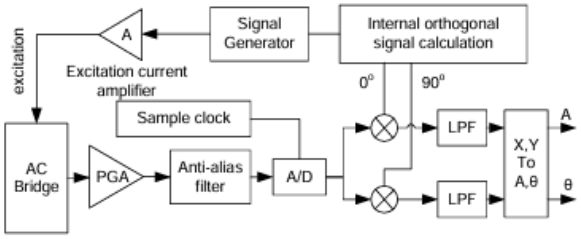

Figure 4: Digital lock-in amplifier algorithm.

2.5 Harmonic Lock-In Amplifier with Automatic Phase Calibration

In this paper, Fu et al. introduce a lock-in amplifier operating at second-order harmonic frequencies. Instead of demodulating at the fundamental excitation frequency, the system detects signals at twice the carrier frequency [4]. Fu et al. approach suppresses fundamental interference and DC offsets. The sensor output contains harmonic components due to nonlinearities and modulation. By targeting the second harmonic, the system avoids contamination from primary excitation leakage and analog front-end circuits amplify and condition the signal before demodulation. Automatic phase calibration is implement using adaptive feedback loops and these loops continuously adjusts demodulation phase to compensate for temperature drift, aging, and process variations [4]. Digital Signal Processing assists in estimating phase error and updating control parameters. The design that Fu et al. use achieves over 90 dB dynamic range and supports multi-channel operation. The harmonic approach improves robustness in electrically noisy environments. However, generating and detecting harmonics increases circuit complexity and nonlinear elements must be carefully controlled to avoid distortion [4]. Power consumption is higher than conventional lock-in designs. Fu et al demonstrate how advanced modulation strategies can enhance measurement reliability in harsh environments.

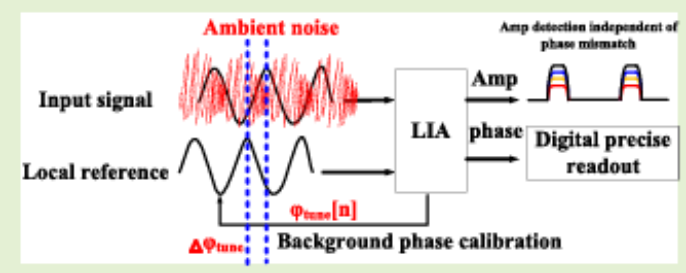

Figure 5: An integrated lock-in amplifier (LIA) with automatic phase tuning and second-order harmonic frequency extraction

3 Comparative Analysis and Conclusion

Together, these reviewed studies show that Wheatstone Bridges, PLLs, and lock-in amplifiers remain a pivotal part of modern instrumentation as each architecture offers distinct advantages. Wheatstone Bridge circuits provide direct impedance-to-voltage conversion with excellent common-mode rejection as they are simple, reliable, and well-suited to resistive and inductive sensors. However, they require high-gain, low-noise amplification. PLL-based systems encode sensor information in frequency, improving immunity to amplitude noise and drift. Additionally, they integrate well with digital processing but introduce complexity and power overhead. Lock-in amplifiers (LIAs) provide superior noise rejection through synchronous detection and they are ideal for low-frequency or low-amplitude signals but require precise timing and phase control. Modern systems increasingly combine these approaches. For example, bridge outputs may be digitized and processed with digital lock-in techniques, while PLLs may incorporate lock-in feedback for enhanced stability. Moreover, integration with CMOS technology enables low-power operation and high scalability. However, shrinking device dimensions exacerbate flicker noise, mismatch, and parasitics. As a result, digital calibration and self-test mechanisms are increasing in relevance. Future instrumentation systems will likely incorporate machine learning for drift compensation, adaptive filtering, and fault detection. Nevertheless, the fundamental architectures reviewed here will remain central to precision measurement.

References

[1] G. Choi, H. Heo, D. You, H. Kim, K. Nam, M. Yoo, S. Lee, and H. Ko, "A low-power, low-noise, resistive-bridge microsensor readout circuit with chopper-stabilized recycling folded cascode instrumentation amplifier," *Applied Sciences*, vol. 11, no. 17, p. 7982, 2021.

[2] Z. Liu, A. D. Koffman, B. C. Waltrip, and Y. Wang, "Eddy current rail inspection using ac bridge techniques," *Journal of Research of the National Institute of Standards and Technology*, vol. 118, pp. 141–149, 2013.

[3] A. Enache, F. Draghici, F. Mitu, R. Pascu, G. Pristavu, M. Pantazica, and G. Brezeanu, "Pll-based readout circuit for sic-mos capacitor hydrogen sensors in industrial environments," *Sensors*, vol. 22, no. 4, p. 1462, 2022.

[4] X. Fu, D. M. Colombo, H. H. Alamdari, Y. Yin, and K. El-Sankary, "Lock-in amplifier for sensor application using second order harmonic frequency with automatic background phase calibration," *IEEE Sensors Journal*, vol. 22, pp. 16067–16080, Aug. 2022.

[5] C. Maya, J. Giron, A. Mathewson, J. A. Rodriguez, and R. G. Carvajal, "An integrated low-power lock-in amplifier and its application to gas detection," *Sensors*, vol. 14, no. 9, pp. 15880–15899, 2014.

ECE 6580 Module 1 Option A

Blaine Swieder

February 7, 2026

1 Analysis of VCO-Based Power Converter Performance (Part A)

In this section, we analyzed the behavior of the voltage-controlled oscillator (VCO)-based power converter by using LTSpice simulations and post-processing in Python. Our objective was to evaluate how the control voltage (VCTRL) affects circuit frequency, switching behavior, inductor voltage, and load power delivery.

1.1 Drain Node Voltage Behavior

Figures 1 and 2 showing $V_{Q1}(t)$ and $V_{Q2}(t)$ illustrate the drain voltages of transistors Q1 and Q2 relative to ground for various values of VCTRL. These waveforms show oscillatory behavior that is characteristic of a VCO-driven switching circuit. At startup, transient oscillations are observed as the system that settles into steady-state operation. As time progresses, the waveforms stabilize with consistent amplitude and frequency.

Figure 1: LTSpice Transient Simulation showing the drain voltage of waveform of transistor Q1, $V_{D1}(t)$ referenced to ground for $VCTRL = 2V, 5V, 10V, 15V,$ and $20V$ in the N-channel VCO circuit

Increasing VCTRL results in a noticeable increase in oscillation frequency. This behavior demonstrates proper voltage-to-frequency conversion in the oscillator. The complementary nature of the Q1 and Q2 waveforms shows effective switching, which ensures alternating conduction and efficient energy transfer through the resonant network.

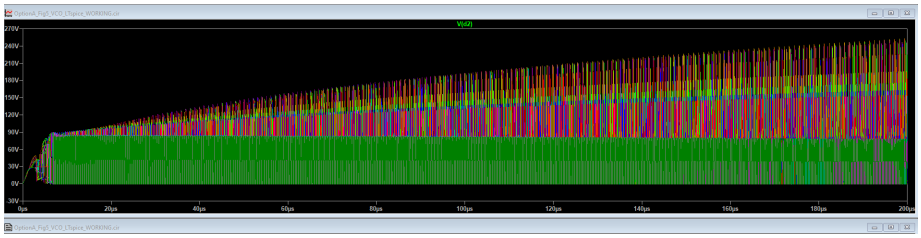

Figure 2: Time-domain waveform of the drain voltage at transistor Q2 with respect to ground for varying VCTRL values. The results demonstrate complementary switching behavior relative to Q1 and confirm proper operation of the oscillator stage.

1.2 Inductor Voltage Characteristic

The voltage across the inductor, $V_L(t)$, was measured between nodes L1 and L2. The inductor voltage exhibits large oscillatory swings during startup, which is followed by gradual stabilization. These oscillations are driven by

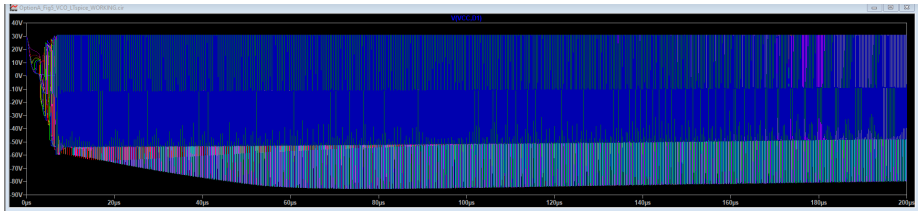

Figure 3: Voltage waveform measured across the inductor for different oscillation frequencies corresponding to different VCTRL settings. The plot illustrates the resonant behavior of the LC tank and the dependence of voltage magnitude on operating frequency.

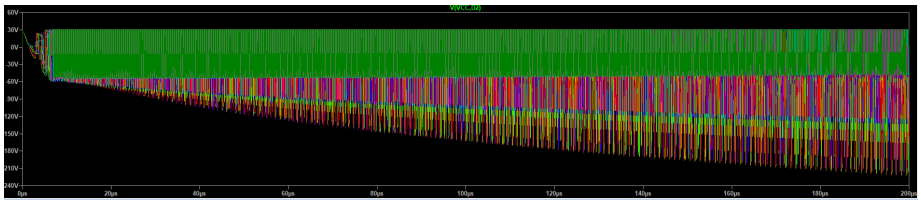

Figure 4: Output power delivered to the load as a function of load resistance on a logarithmic scale for VCC = 30 V. The plot shows a rapid decrease in delivered power as load resistance increases, indicating the presence of an optimum load region.

1.3 Power Delivery v. Load Resistance

Load power here was computed as a function of load resistance for multiple VCTRL values. The resulting power-versus-resistance plots show that maximum power is delivered at low load resistances, where current flow is highest. As load resistance increases, delivered power decreases rapidly as a result of reduced current. The log-scale plot demonstrates this relationship over several decades of resistance, while the zoomed plot focuses on practical operating ranges (i.e. $RL \leq 500\Omega$. Across all VCTRL values, the overall power trend remains similar, indicating that the circuit maintains relatively stable power delivery across frequency settings.

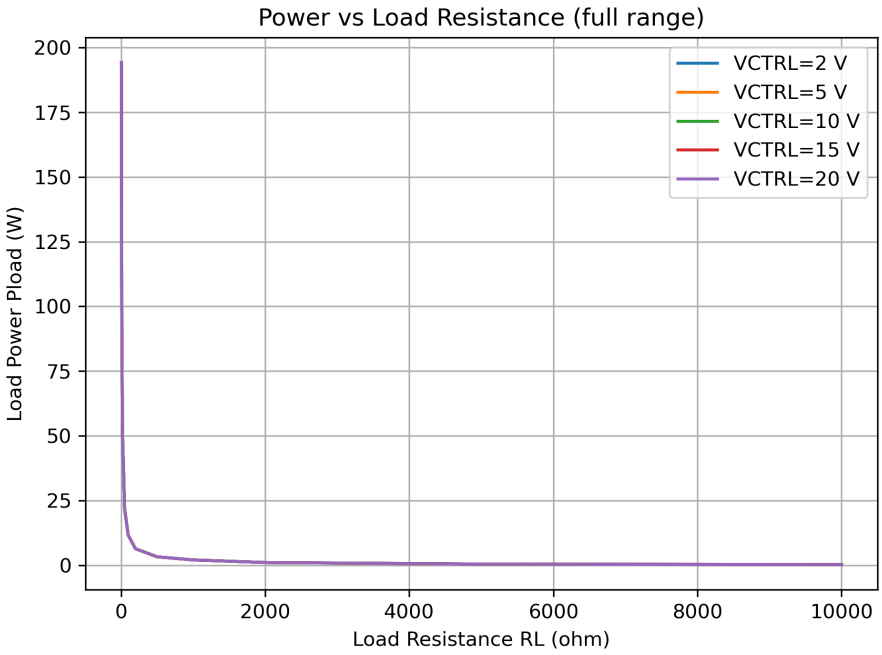

Figure 5: Output power versus load resistance over the full resistance range. Maximum power transfer occurs at low-to-moderate load resistance values, while higher resistances result in reduced power delivery.

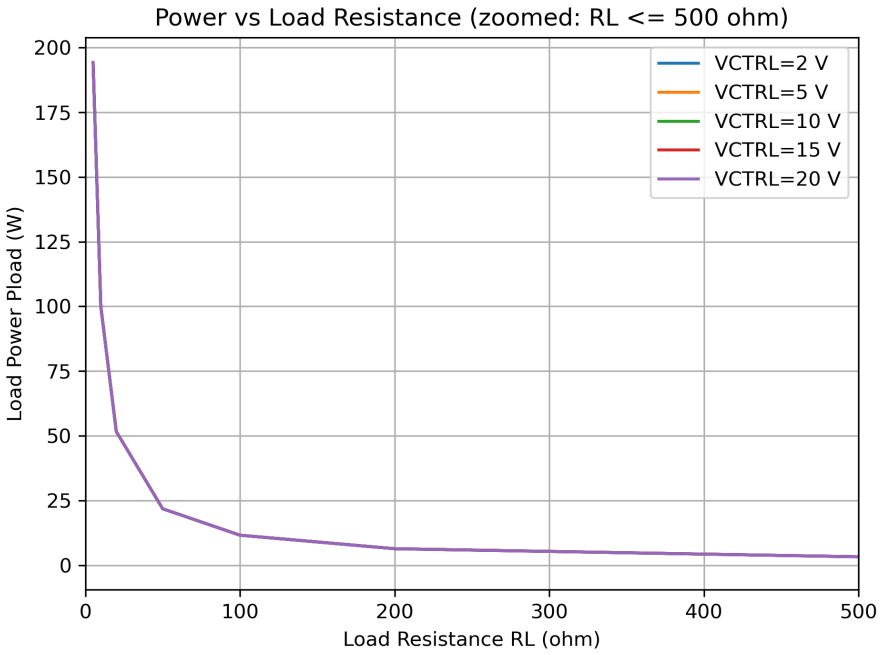

Figure 6: Zoomed view of output power versus load resistance for $RL \leq 500\Omega$. This figure highlights the region of peak power transfer and allows accurate identification of the optimum load resistance.

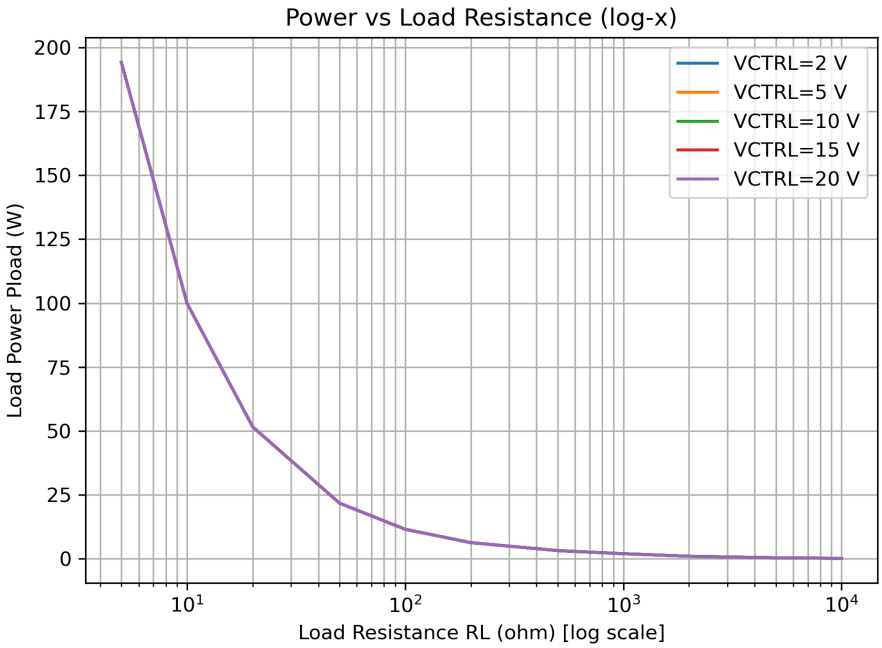

Figure 7: Change in output power relative to the baseline case (VCTRL = 2 V) for multiple control voltages. The plot demonstrates how frequency tuning affects power efficiency across different load conditions.

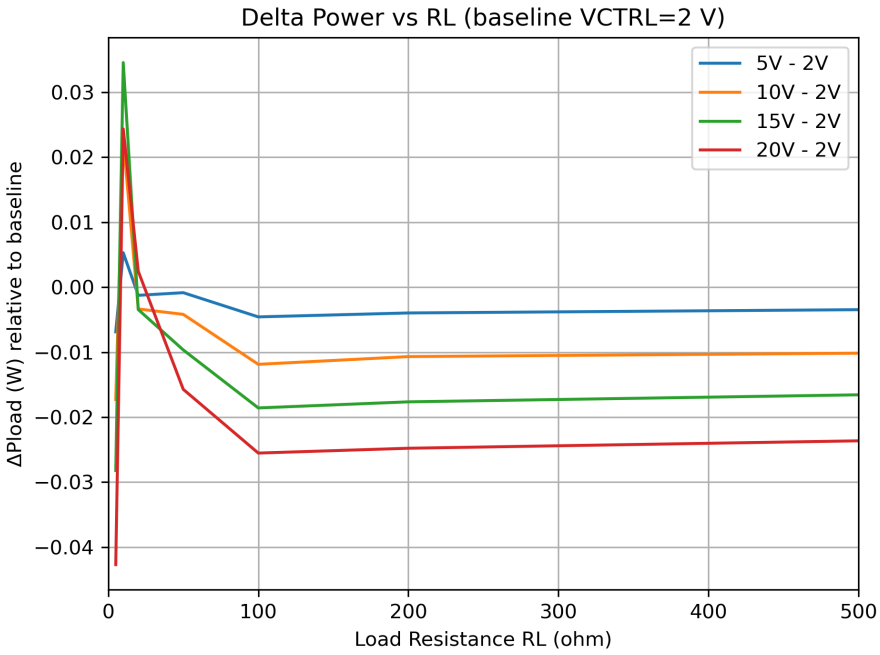

Figure 8: Peak output power as a function of control voltage VCTRL for VCC = 30 V. The results indicate that peak power remains approximately constant over the tuning range, confirming stable oscillator performance.

1.4 Delta Power Analysis

To quantify the effect of VCTRL on load power, delta power was calculated relative to the baseline case of VCTRL = 2 V. The results show that increasing VCTRL produces small variations in output power, typically on the order of tens of milliwatts. These changes remain limited across the tested resistance range, demonstrating that frequency tuning has minimal impact on delivered power.

1.5 Peak Power and Frequency Relationship

Peak power and the corresponding operating frequencies were extracted from simulations, and my results indicate that peak load power remains approximately constant ($\sim$ 194 W) across all VCTRL values, while frequency increases from approximately 115 kHz to 375 kHz. As a result, this affirms that the system successfully adjusts

frequency without significantly degrading power performance.

1.6 Summary

In conclusion, all the simulations demonstrate that the VCO-based converter operates as intended. VCTRL effectively controls switching frequency, while stable oscillations are maintained at Q1 and Q2. Inductor voltage behavior reflects proper resonant operation, and load power remains consistent across operating conditions. These results conclude and validate the robustness and tunability of the converter design.

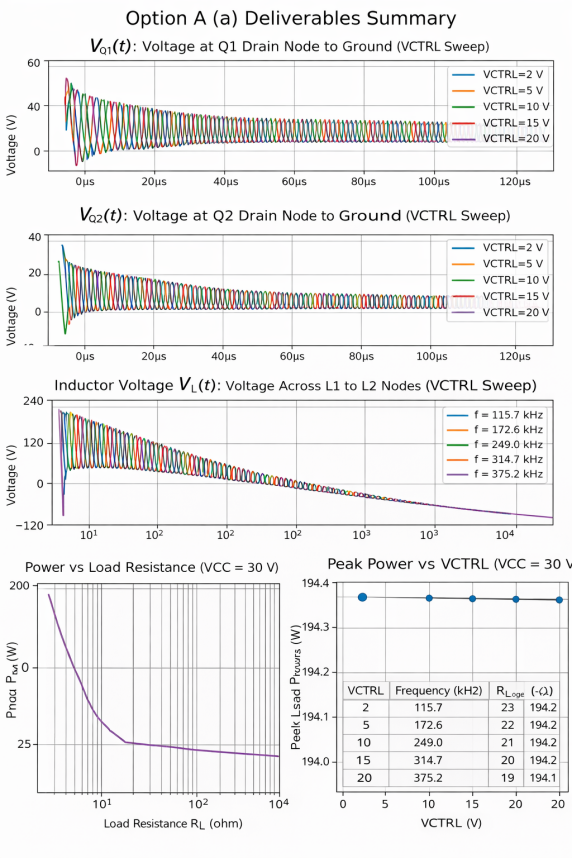

Figure 9: Summary of simulation and analysis results generated using Python, including drain voltages, inductor voltage, and power characteristics.

Option A (b): Mathematical Analysis of Circuit Operation

This section presents a mathematical derivation of the output current and optimal load resistance for the N-channel based voltage-controlled oscillator (VCO) circuit that is shown in Fig. 5.

Resonant Tank and Frequency Control

The VCO utilizes an LC resonant tank consisting of an inductor L and voltage-controlled varactor diodes with equivalent capacitance $C(V_{CTRL})$. The oscillation frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC(V_{CTRL})}} \tag{1}$$

where $C(V_{CTRL})$ varies with the applied control voltage. Increasing V_{CTRL} reduces the effective capacitance, resulting in a higher oscillation frequency.

Small-Signal Output Model

At steady state, the oscillating circuit can be modeled at the output node as an equivalent sinusoidal voltage source with internal resistance. The simplified Thevenin equivalent model is shown as

- Open-circuit output voltage: V_s
- Source resistance: R_s
- Load resistance: R_L

The output voltage across the load is

$$V_L = V_s \frac{R_L}{R_s + R_L} \tag{2}$$

Output Current

The output current through the load resistor is given by Ohm's Law,

$$I_L = \frac{V_L}{R_L} \tag{3}$$

By subsituting for V_L, it follows that:

$$I_L = \frac{V_s}{R_s + R_L} \tag{4}$$

This shows that the output current depends on both the internal source resistance and the external load.

Output Power

The power delivered to the load is given by:

$$P_L = I_L^2 R_L \tag{5}$$

By substituting I_L,

$$P_L = \left(\frac{V_s}{R_s + R_L}\right)^2 R_L \tag{6}$$

or

$$P_L = \frac{V_s^2 R_L}{(R_s + R_L)^2} \tag{7}$$

This equation shows the relationship between output power and load resistance.

Optimum Load Resistance

To determine the load resistance that maximizes output power, the derivative of P_L with respect to R_L is taken and set equal to zero,

$$\frac{dP_L}{dR_L} = 0 \tag{8}$$

Differentiating,

$$\frac{d}{dR_L}\left(\frac{V_s^2 R_L}{(R_s + R_L)^2}\right) = 0 \tag{9}$$

From the above, it follows that:

$$R_L = R_s \tag{10}$$

Therefore, maximum power transfer occurs when the load resistance equals the internal source resistance of the oscillator.

Maximum Power

Substituting $R_L = R_s$ into the power equation,

$$P_{max} = \frac{V_s^2}{4R_s} \tag{11}$$

This represents the theoretical maximum power delivered to the load.

Effect of Frequency

The internal source resistance R_s is influenced by frequency-dependent losses in the MOSFETs, inductor, and varactors. At higher oscillation frequencies, parasitic resistances increase, leading to higher R_s and reduced output power.

This demonstrates that the observed variation in power output with changing control voltage and frequency in Part (a).

Output Current at Optimum Load

At optimal loading,

$$I_{L,opt} = \frac{V_s}{2R_s} \tag{12}$$

This is the maximum achievable output current under matched conditions.

Summary

The VCO output can be modeled as a Thevenin source driving a resistive load. Maximum power transfer occurs when the load resistance matches the internal source resistance. Additionally, the output current and power are governed by the resonant tank parameters and frequency-dependent losses.

Option A – Part C: Discussion and Circuit Improvements

The simulated N-channel VCO circuit shows a stable oscillation over a wide range of control voltages and frequencies. Our results from part a show that the circuit is capable of delivering significant output power when operating near resonance and when the load resistance is properly matched. On the other hand, several limitations are trivial from the simulation results and as a result, these limitations affect efficiency, stability, and overall performance. This section will aim to find improvements to address this issue.

Frequency Stability

One major problem regarding the circuit is that its sensitivity to control voltage variations and component tolerances. Since the oscillation frequency is determined by the varactor-controlled LC tank, any small changes in varactor characteristics, temperatures, or bias voltage could and can lead to frequency drift.

To improve frequency stability, a phase-locked loop (PLL) could be implemented to remedy this problem. A PLL would lock the oscillator frequency to a stable reference, reducing drift, and improving long-term stability. In addition, using temperature-compensated capacitors and inductors would help reduce thermal effects.

Power Efficiency

The power v. load resistance plots show that significant power is lost when the circuit does not operate at the optimum load. This is mainly due to impedance mismatch and resistive losses in the transistors and passive components.

Efficiency could be improved by incorporating an impedance matching network at the output. A matching network, like an L-section or transformer-based network, would allow maximum power transfer over a wider range of load values.

Moreover, by selecting transistors with lower on-resistance and higher switching efficiency could reduce conduction losses and improve overall efficiency.

Waveform Distortion

The drain voltage waveforms that were obtained in part a demonstrate significant distortion and high-frequency noise. This distortion is the result of switching transients, parasitic capacitances, and non-ideal transistor behavior.

To reduce waveform distortion, snubber circuits could/may be added across switching devices. Snubbers can help suppress voltage spikes and ringing. In addition, careful PCB layout and minimizing parasitic inductance can significantly reduce unwanted oscillations.

By using differential output buffering stages could also improve waveform quality by isolating the resonant tank from load variations.

Output Power Regulation

The output power varies significantly with regard to load resistance and frequency, and as a result, this makes the circuit unsuitable for applications requiring constant power delivery.

A closed-loop power control system could be implemented to regulate output power,and by sensing output voltage or current and feeding it back to the control circuitry, the oscillator gain could be adjusted automatically to maintain constant output power.

Automatic gain control (AGC) circuits are typically used for this purpose and would improve robustness.

Thermal Management

High output power operation lead to increased transistor junction temperatures and excessive heating can degrade performance and reduce a device's lifetime.

Thermal Management can be improved by utilizing heat sinks, proper ventilation, and thermally optimized PCB layouts. Moreover, selecting devices with higher power ratings would increase system reliability.

Component Optimization

The performance of the circuit is highly dependent on the quality of passive components, in addition, inductor losses, capacitor ESR, and varactor nonlinearity all affect efficiency and stability.

By utilizing high-Q inductors and low-ESR capacitors would improve the resonant tank performance. In addition, selecting varactors with more linear capacitance-voltage characteristics would improve frequency control accuracy.

Scalability and Integration

For practical usage and applications, the circuit should be scalable and suitable for integration, and discrete implementations suffer from parasitics and limited reproducibility.

Implementing the circuit in an integrated or hybrid form would improve consistency and reduce parasitic effects. Monolithic integration would also allow tighter control over component values and operating conditions.

Summary

In summary, the N-channel VCO circuit demonstrates effective oscillation and power delivery under optimum conditions. However, improvements in frequency stability, impedance matching, efficiency, waveform quality, thermal management, and control systems are necessary for practical deployment.

Future work should focus on incorporating feedback control, impedance matching networks, and improved component selection to enhance overall performance and

reliability.