Table 5. High-density STM32F103xC/D/E pin definitions

Pins						Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
A3	A3	-	-	1	1	PE2	I/O	FT	PE2	TRACECK/ FSMC_A23	-
A2	B3	-	-	2	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
B2	C3	-	-	3	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
B3	D3	-	-	4	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
B4	E3	-	-	5	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
C2	B2	C6	1	6	6	V_{BAT}	S	-	V_{BAT}	-	-
A1	A2	C8	2	7	7	PC13-TAMPER-RTC[5]	I/O	-	PC13[6]	TAMPER-RTC	-
B1	A1	B8	3	8	8	PC14-OSC32_IN[5]	I/O	-	PC14[6]	OSC32_IN	-
C1	B1	B7	4	9	9	PC15-OSC32_OUT[5]	I/O	-	PC15[6]	OSC32_OUT	-
C3	-	-	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	-
C4	-	-	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	-
D4	-	-	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	-
E2	-	-	-	-	13	PF3	I/O	FT	PF3	FSMC_A3	-
E3	-	-	-	-	14	PF4	I/O	FT	PF4	FSMC_A4	-
E4	-	-	-	-	15	PF5	I/O	FT	PF5	FSMC_A5	-
D2	C2	-	-	10	16	V_{SS_5}	S	-	V_{SS_5}	-	-
D3	D2	-	-	11	17	V_{DD_5}	S	-	V_{DD_5}	-	-
F3	-	-	-	-	18	PF6	I/O	-	PF6	ADC3_IN4/FSMC_NIORD	-
F2	-	-	-	-	19	PF7	I/O	-	PF7	ADC3_IN5/FSMC_NREG	-
G3	-	-	-	-	20	PF8	I/O	-	PF8	ADC3_IN6/FSMC_NIOWR	-
G2	-	-	-	-	21	PF9	I/O	-	PF9	ADC3_IN7/FSMC_CD	-
G1	-	-	-	-	22	PF10	I/O	-	PF10	ADC3_IN8/FSMC_INTR	-
D1	C1	D8	5	12	23	OSC_IN	I	-	OSC_IN	-	-
E1	D1	D7	6	13	24	OSC_OUT	O	-	OSC_OUT	-	-
F1	E1	C7	7	14	25	NRST	I/O	-	NRST	-	-
H1	F1	E8	8	15	26	PC0	I/O	-	PC0	ADC123_IN10	-
H2	F2	F8	9	16	27	PC1	I/O	-	PC1	ADC123_IN11	-
H3	E2	D6	10	17	28	PC2	I/O	-	PC2	ADC123_IN12	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
H4	F3	-	11	18	29	PC3[7]	I/O	-	PC3	ADC123_IN13	-
J1	G1	E7	12	19	30	V_{SSA}	S	-	V_{SSA}	-	-
K1	H1	-	-	20	31	V_{REF-}	S	-	V_{REF-}	-	-
L1	J1	F7 (8)	-	21	32	V_{REF+}	S	-	V_{REF+}	-	-
M1	K1	G8	13	22	33	V_{DDA}	S	-	V_{DDA}	-	-
J2	G2	F6	14	23	34	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS[9] ADC123_IN0 TIM2_CH1_ETR TIM5_CH1/TIM8_ETR	-
K2	H2	E6	15	24	35	PA1	I/O	-	PA1	USART2_RTS[9] ADC123_IN1/ TIM5_CH2/TIM2_CH2[9]	-
L2	J2	H8	16	25	36	PA2	I/O	-	PA2	USART2_TX[9]/TIM5_CH3 ADC123_IN2/ TIM2_CH3 [9]	-
M2	K2	G7	17	26	37	PA3	I/O	-	PA3	USART2_RX[9]/TIM5_CH4 ADC123_IN3/TIM2_CH4[9]	-
G4	E4	F5	18	27	38	V_{SS_4}	S	-	V_{SS_4}	-	-
F4	F4	G6	19	28	39	V_{DD_4}	S	-	V_{DD_4}	-	-
J3	G3	H7	20	29	40	PA4	I/O	-	PA4	SPI1_NSS[9]/ USART2_CK[9] DAC_OUT1/ADC12_IN4	-
K3	H3	E5	21	30	41	PA5	I/O	-	PA5	SPI1_SCK[9] DAC_OUT2 ADC12_IN5	-
L3	J3	G5	22	31	42	PA6	I/O	-	PA6	SPI1_MISO[9] TIM8_BKIN/ADC12_IN6 TIM3_CH1[9]	TIM1_BKIN
M3	K3	G4	23	32	43	PA7	I/O	-	PA7	SPI1_MOSI[9]/ TIM8_CH1N/ADC12_IN7 TIM3_CH2[9]	TIM1_CH1N
J4	G4	H6	24	33	44	PC4	I/O	-	PC4	ADC12_IN14	-
K4	H4	H5	25	34	45	PC5	I/O	-	PC5	ADC12_IN15	-
L4	J4	H4	26	35	46	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3 TIM8_CH2N	TIM1_CH2N
M4	K4	F4	27	36	47	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4[9] TIM8_CH3N	TIM1_CH3N

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
J5	G5	H3	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
M5	-	-	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	-
L5	-	-	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	-
H5	-	-	-	-	51	V_{SS_6}	S	-	V_{SS_6}	-	-
G5	-	-	-	-	52	V_{DD_6}	S	-	V_{DD_6}	-	-
K5	-	-	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	-
M6	-	-	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	-
L6	-	-	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	-
K6	-	-	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	-
J6	-	-	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	-
M7	H5	-	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	J5	-	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	K5	-	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	-	-	61	V_{SS_7}	S	-	V_{SS_7}	-	-
G6	-	-	-	-	62	V_{DD_7}	S	-	V_{DD_7}	-	-
J7	G6	-	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	H6	-	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	J6	-	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	K6	-	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	G7	-	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	H7	-	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	J7	G3	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX(9)	TIM2_CH3
M10	K7	F3	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX(9)	TIM2_CH4
H7	E7	H2	31	49	71	V_{SS_1}	S	-	V_{SS_1}	-	-
G7	F7	H1	32	50	72	V_{DD_1}	S	-	V_{DD_1}	-	-
M11	K8	G2	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK(9)/ TIM1_BKIN(9)	-
M12	J8	G1	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK USART3_CTS(9)/ TIM1_CH1N	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
L11	H8	F2	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS[9]/	-
L12	G8	F1	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD TIM1_CH3N[9]/	-
L9	K9	-	-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	J9	-	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	H9	-	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
H9	G9	-	-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	K10	-	-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
K10	J10	-	-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	-	-	83	V_{SS_8}	S	-	V_{SS_8}	-	-
F8	-	-	-	-	84	V_{DD_8}	S	-	V_{DD_8}	-	-
K11	H10	-	-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	G10	-	-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	-	-	-	-	87	PG2	I/O	FT	PG2	FSMC_A12	-
J11	-	-	-	-	88	PG3	I/O	FT	PG3	FSMC_A13	-
J10	-	-	-	-	89	PG4	I/O	FT	PG4	FSMC_A14	-
H12	-	-	-	-	90	PG5	I/O	FT	PG5	FSMC_A15	-
H11	-	-	-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	-
H10	-	-	-	-	92	PG7	I/O	FT	PG7	FSMC_INT3	-
G11	-	-	-	-	93	PG8	I/O	FT	PG8	-	-
G10	-	-	-	-	94	V_{SS_9}	S	-	V_{SS_9}	-	-
F10	-	-	-	-	95	V_{DD_9}	S	-	V_{DD_9}	-	-
G12	F10	E1	37	63	96	PC6	I/O	FT	PC6	I2S2_MCK/ TIM8_CH1/SDIO_D6	TIM3_CH1
F12	E10	E2	38	64	97	PC7	I/O	FT	PC7	I2S3_MCK/ TIM8_CH2/SDIO_D7	TIM3_CH2
F11	F9	E3	39	65	98	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
E11	E9	D1	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
E12	D9	E4	41	67	100	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1[9]/MCO	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
D12	C9	D2	42	68	101	PA9	I/O	FT	PA9	USART1_TX[9]/ TIM1_CH2[9]	-
D11	D10	D3	43	69	102	PA10	I/O	FT	PA10	USART1_RX[9]/ TIM1_CH3[9]	-
C12	C10	C1	44	70	103	PA11	I/O	FT	PA11	USART1_CTS/USBDM CAN_RX[9]/TIM1_CH4[9]	-
B12	B10	C2	45	71	104	PA12	I/O	FT	PA12	USART1_RTS/USBDP/ CAN_TX[9]/TIM1_ETR[9]	-
A12	A10	D4	46	72	105	PA13	I/O	FT	JTMS-SWDIO	-	PA13
C11	F8	-	-	73	106	Not connected					-
G9	E6	B1	47	74	107	V_{SS_2}	S	-	V_{SS_2}	-	-
F9	F6	A1	48	75	108	V_{DD_2}	S	-	V_{DD_2}	-	-
A11	A9	B2	49	76	109	PA14	I/O	FT	JTCK-SWCLK	-	PA14
A10	A8	C3	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS/ I2S3_WS	TIM2_CH1_ETR PA15 / SPI1_NSS
B11	B9	A2	51	78	111	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
B10	B8	B3	52	79	112	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
C10	C8	C4	53	80	113	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
E10	D8	D8	5	81	114	PD0	I/O	FT	OSC_IN[10]	FSMC_D2[11]	CAN_RX
D10	E8	D7	6	82	115	PD1	I/O	FT	OSC_OUT[10]	FSMC_D3[11]	CAN_TX
E9	B7	A3	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	-
D9	C7	-	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
C9	D7	-	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	B6	-	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	-	-	120	V_{SS_10}	S	-	V_{SS_10}	-	-
F7	-	-	-	-	121	V_{DD_10}	S	-	V_{DD_10}	-	-
A8	C6	-	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
A9	D6	-	-	88	123	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK
E8	-	-	-	-	124	PG9	I/O	FT	PG9	FSMC_NE2/FSMC_NCE3	-
D8	-	-	-	-	125	PG10	I/O	FT	PG10	FSMC_NCE4_1/ FSMC_NE3	-

Table 5. High-density STM32F103xC/D/E pin definitions (continued)

Pins						Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LFBGA100	WLCSP64	LQFP64	LQFP100	LQFP144					Default	Remap
C8	-	-	-	-	126	PG11	I/O	FT	PG11	FSMC_NCE4_2	-
B8	-	-	-	-	127	PG12	I/O	FT	PG12	FSMC_NE4	-
D7	-	-	-	-	128	PG13	I/O	FT	PG13	FSMC_A24	-
C7	-	-	-	-	129	PG14	I/O	FT	PG14	FSMC_A25	-
E6	-	-	-	-	130	V_{SS_11}	S	-	V_{SS_11}	-	-
F6	-	-	-	-	131	V_{DD_11}	S	-	V_{DD_11}	-	-
B7	-	-	-	-	132	PG15	I/O	FT	PG15	-	-
A7	A7	A4	55	89	133	PB3	I/O	FT	JTDO	SPI3_SCK / I2S3_CK/	PB3/TRACESWO TIM2_CH2 / SPI1_SCK
A6	A6	B4	56	90	134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO
B6	C5	A5	57	91	135	PB5	I/O	-	PB5	I2C1_SMBA/ SPI3_MOSI I2S3_SD	TIM3_CH2 / SPI1_MOSI
C6	B5	B5	58	92	136	PB6	I/O	FT	PB6	I2C1_SCL[9]/ TIM4_CH1[9]	USART1_TX
D6	A5	C5	59	93	137	PB7	I/O	FT	PB7	I2C1_SDA[9] / FSMC_NADV / TIM4_CH2[9]	USART1_RX
D5	D5	A6	60	94	138	BOOT0	I	-	BOOT0	-	-
C5	B4	D5	61	95	139	PB8	I/O	FT	PB8	TIM4_CH3[9]/SDIO_D4	I2C1_SCL/ CAN_RX
B5	A4	B6	62	96	140	PB9	I/O	FT	PB9	TIM4_CH4[9]/SDIO_D5	I2C1_SDA / CAN_TX
A5	D4	-	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	-
A4	C4	-	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	-
E5	E5	A7	63	99	143	V_{SS_3}	S	-	V_{SS_3}	-	-
F5	F5	A8	64	100	144	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).

5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. In the WCLSP64 package, the PC3 I/O pin is not bonded and it must be configured by software to output mode (Push-pull) and writing 0 to the data register in order to avoid an extra consumption during low-power modes.
8. Unlike in the LQFP64 package, there is no PC3 in the WLCSP package. The V_{REF+} functionality is provided instead.
9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
10. For the WCLSP64/LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100/BGA100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
11. For devices delivered in LQFP64 packages, the FSMC function is not available.