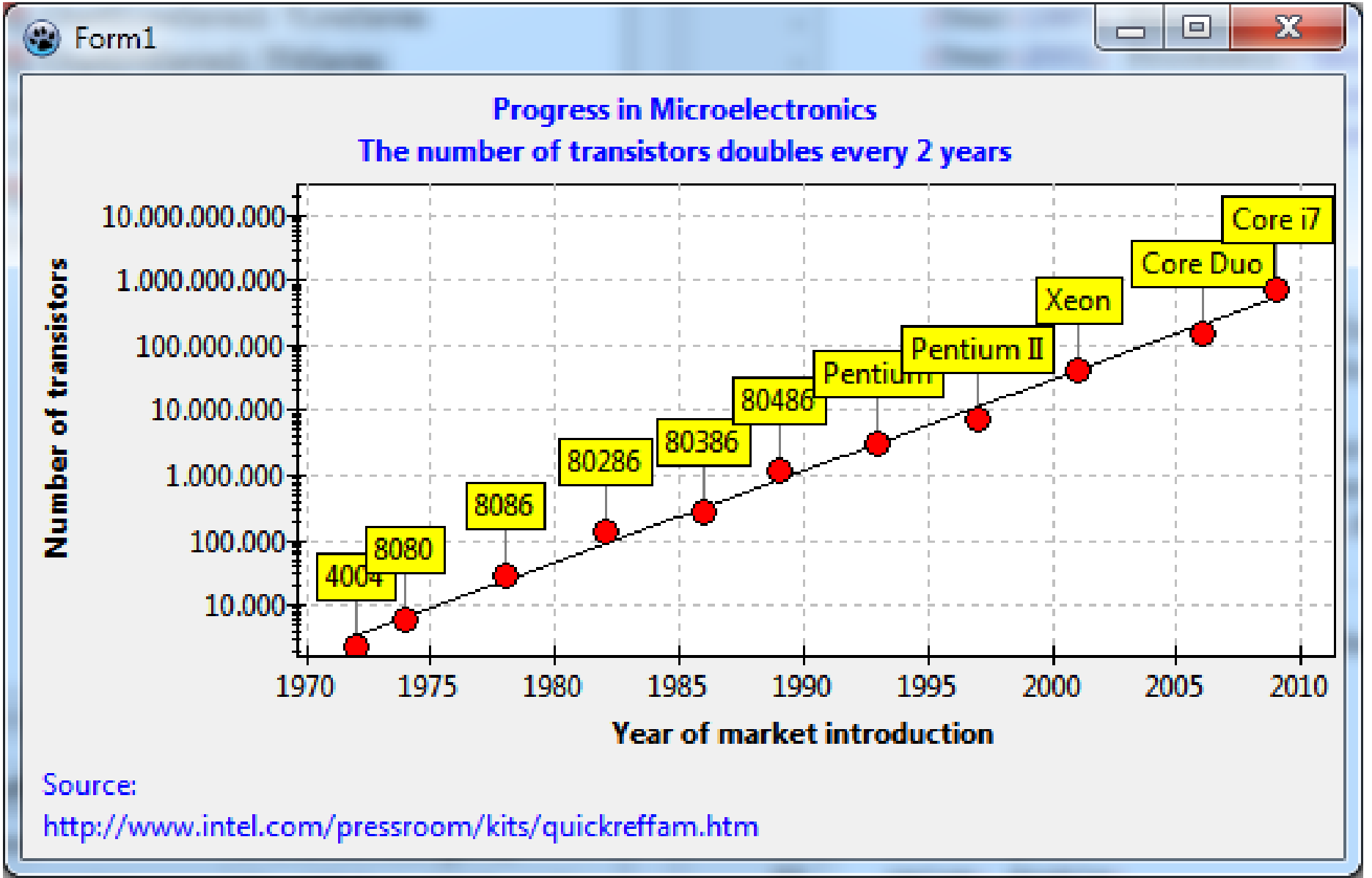
CMOS technology and CMOS Logic gate

Transistors in microprocessors



Clock frequencies of microprocessors

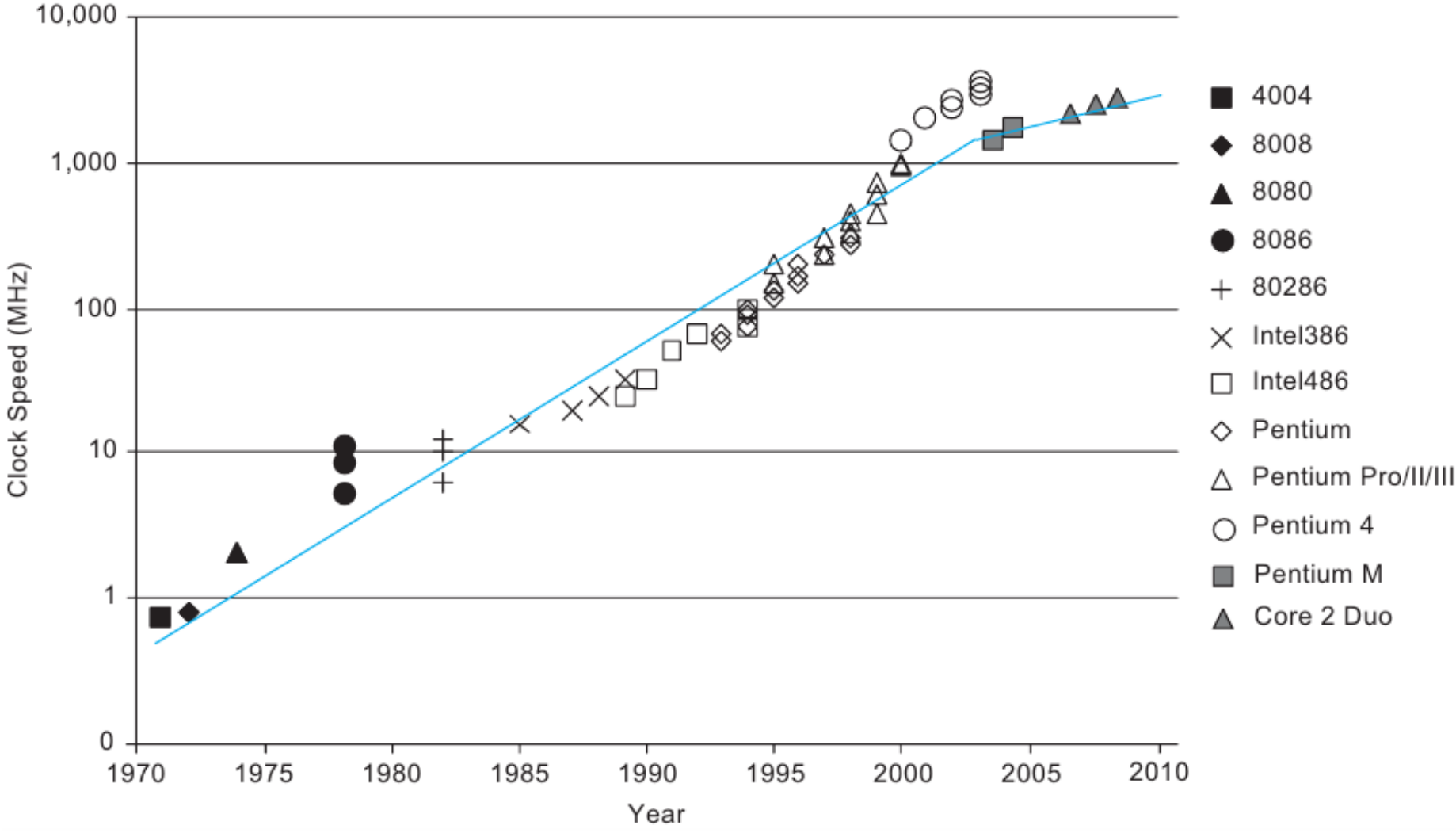


FIGURE 1.5 Clock frequencies of Intel microprocessors

Process generations

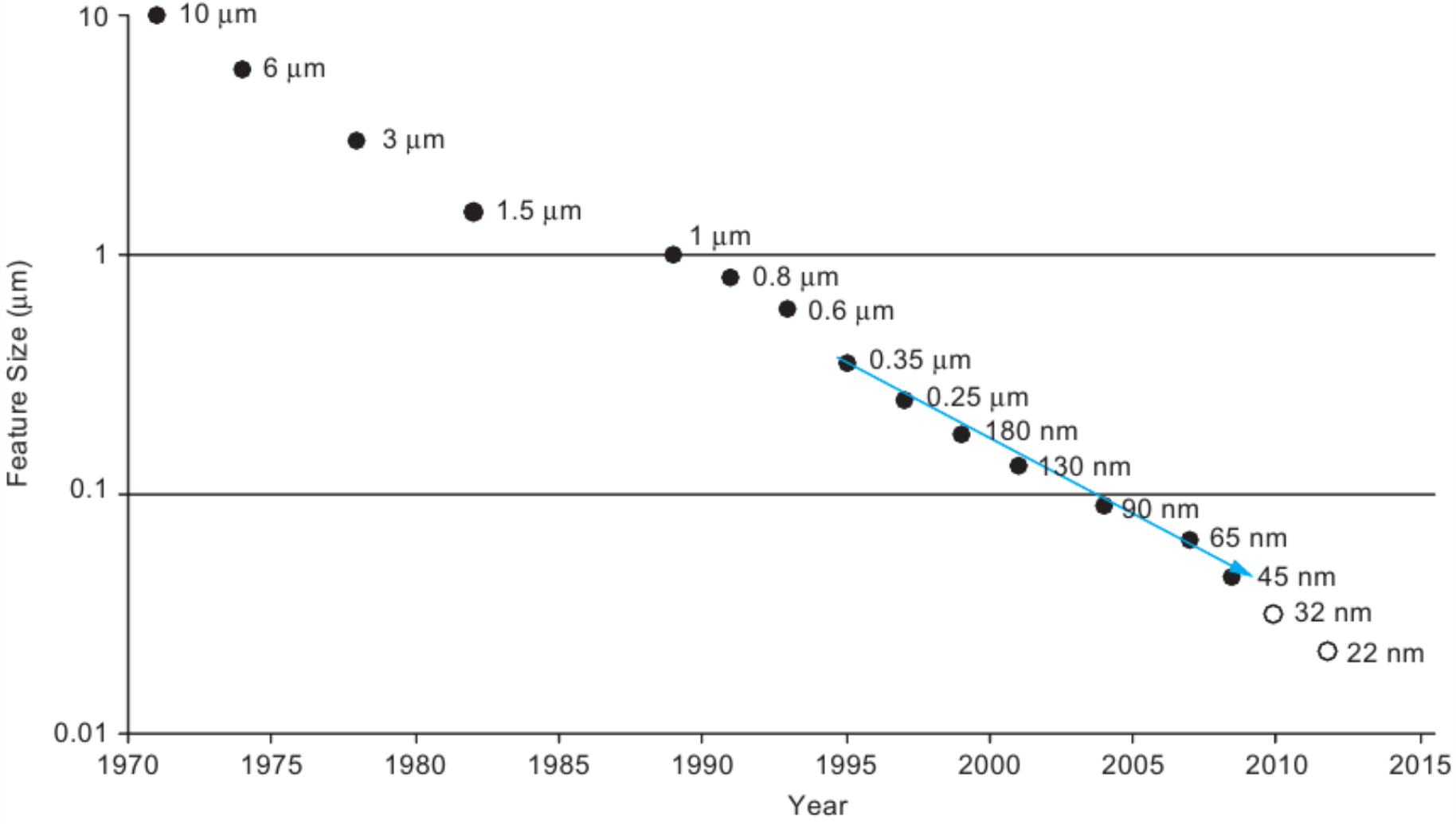
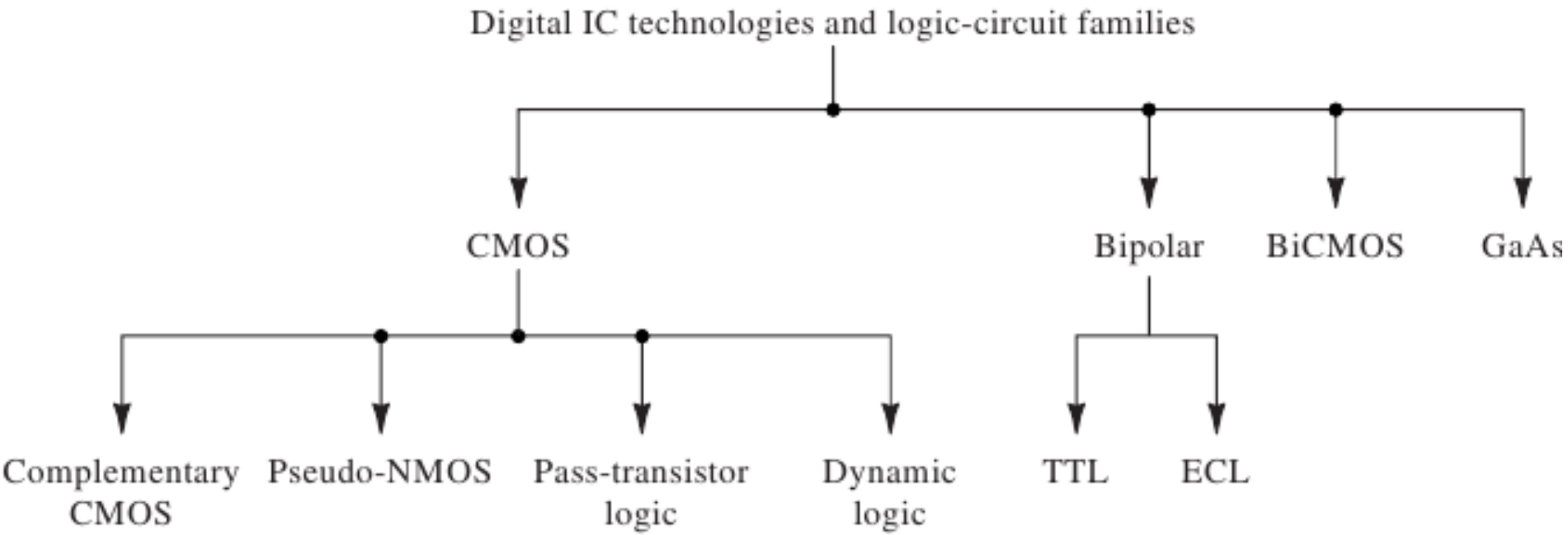


FIGURE 1.6 Process generations. Future predictions from [SIA2007].

Digital IC technologies and logic-circuit families



Digital IC technologies and logic-circuit families

- Bipolar Two logic-circuit families based on the bipolar junction transistor are in some use at present: TTL and ECL (emitter-coupled logic)
- BiCMOS combines the high operating speeds possible with BJTs with the low power dissipation and other excellent characteristics of CMOS. BiCMOS allows for the implementation of both analog and digital circuits on the same chip
- At present, BiCMOS is used to great advantage in special applications, including memory chips

Digital IC technologies and logic-circuit families

- Gallium Arsenide (GaAs) The high carrier mobility in GaAs results in very high speeds of operation
- GaAs remains an “emerging technology,” one that appears to have great potential but has not yet achieved such potential commercially.

CMOS technology

- CMOS technology is, by a very large margin, the most dominant of all the IC technologies available for digital-circuit design.
- Although early microprocessors were made using NMOS logic CMOS has completely replaced NMOS.
- There are a number of reasons for this development, the most important of which is the much lower power dissipation of CMOS circuits.

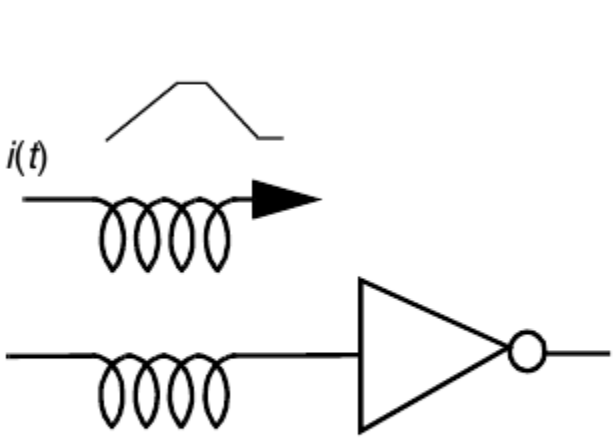
Some of the reasons for CMOS displacing bipolar technology in digital applications are as follows.

1. CMOS logic circuits dissipate much less power than bipolar logic circuits and thus one can pack more CMOS circuits on a chip than is possible with bipolar circuits.
2. The high input impedance of the MOS transistor allows the designer to use charge storage as a means for the temporary storage of information in both logic and memory circuits. This technique cannot be used in bipolar circuits.
3. The feature size (i.e., minimum channel length) of the MOS transistor has decreased dramatically over the years, with some recently reported designs utilizing channel lengths as short as 32 nm. This permits very tight circuit packing and, correspondingly, very high levels of integration. A microprocessor chip reported in 2009 had 2.3 billion transistors.

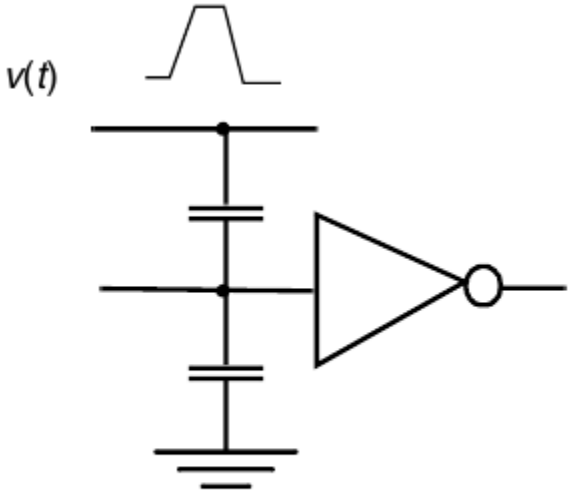
Noise Margin

"The word noise in the context of digital circuits means "unwanted variations of voltages and currents at the logic nodes."

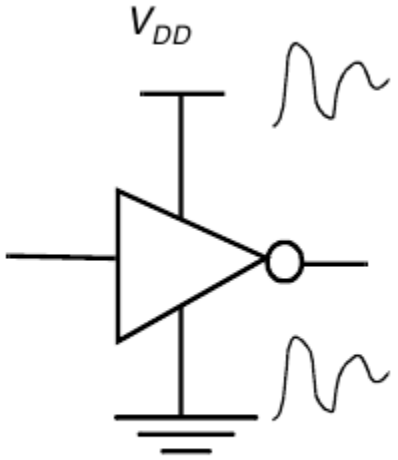
Noise signals can enter a circuit in many ways



(a) Inductive coupling

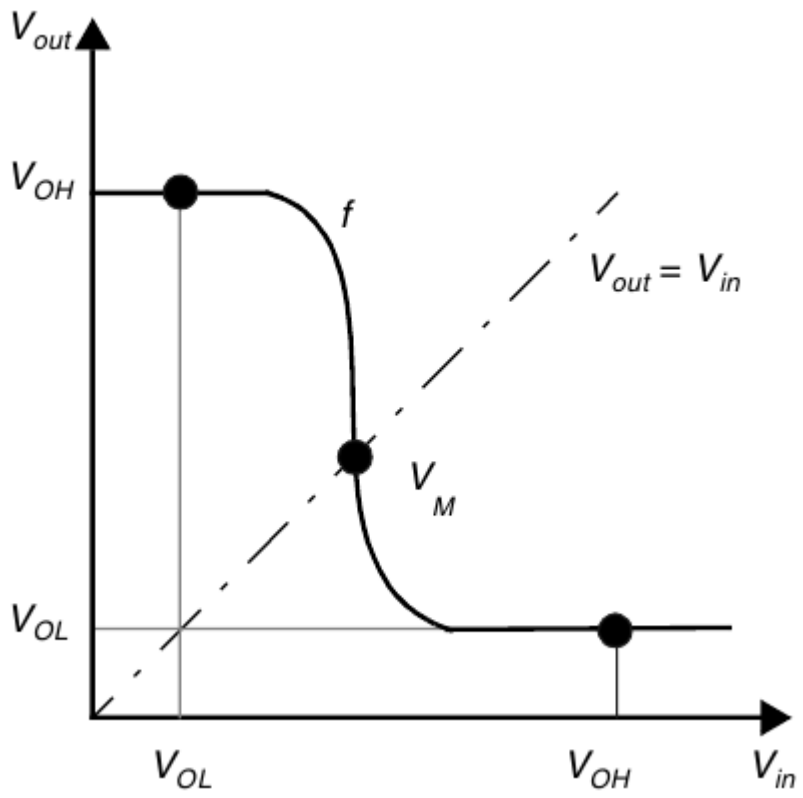


(b) Capacitive coupling



(c) Power and ground noise

The Voltage-Transfer Characteristic (VTC)

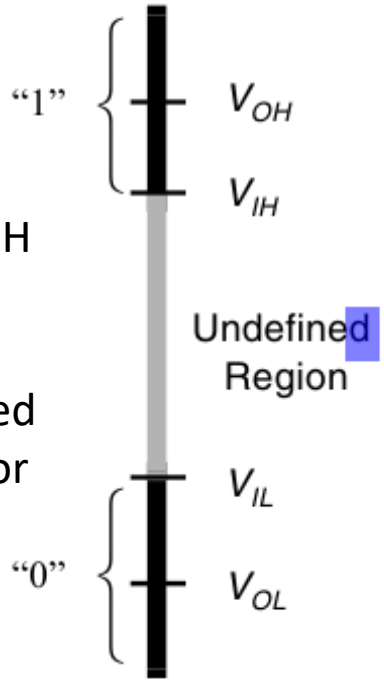


Inverter voltage-transfer characteristic

The electrical function of a gate is best expressed by its voltage-transfer characteristic (VTC) (sometimes called the DC transfer characteristic), which plots the output voltage as a function of the input voltage
Vout = f(Vin).

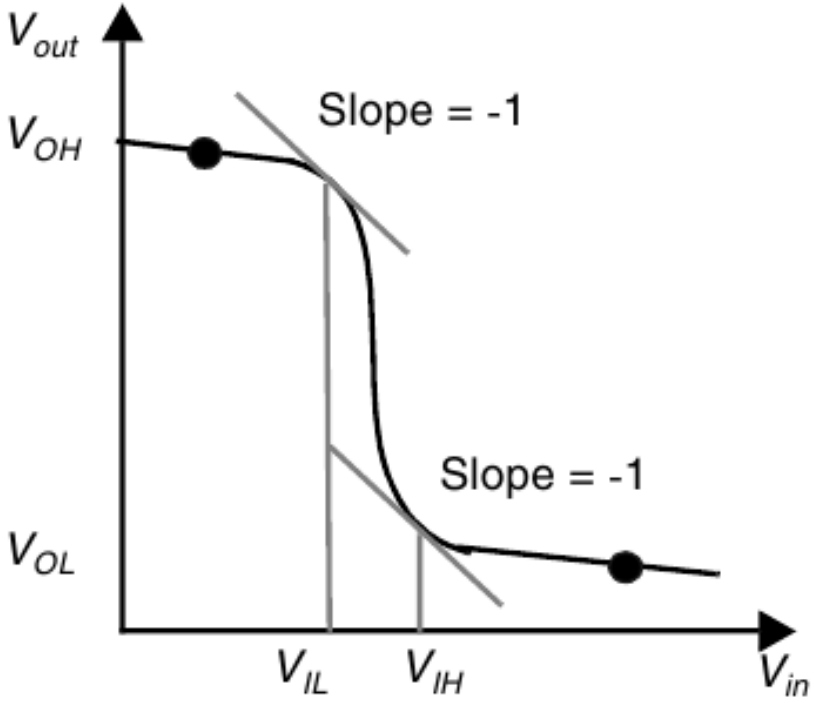
The Voltage-Transfer Characteristic

The region between VIH and VIL is called the undefined region (sometimes also referred to as transition width, or TW)



(a) Relationship between voltage and logic level

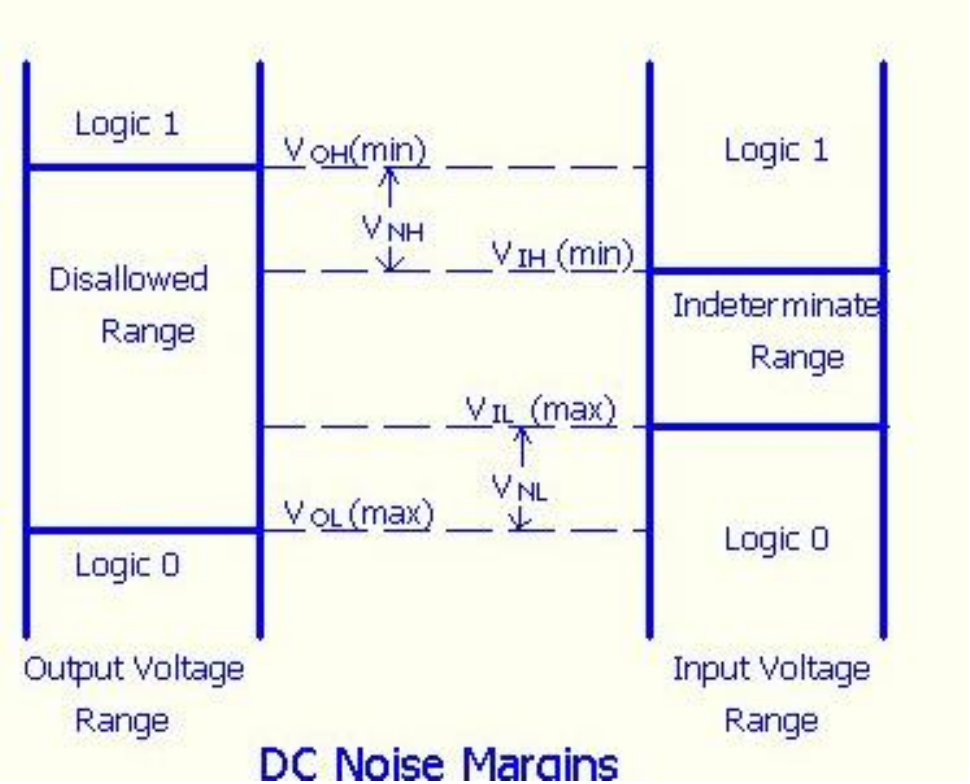
The regions of acceptable high and low voltages are delimited by the VIH and VIL voltage levels, respectively

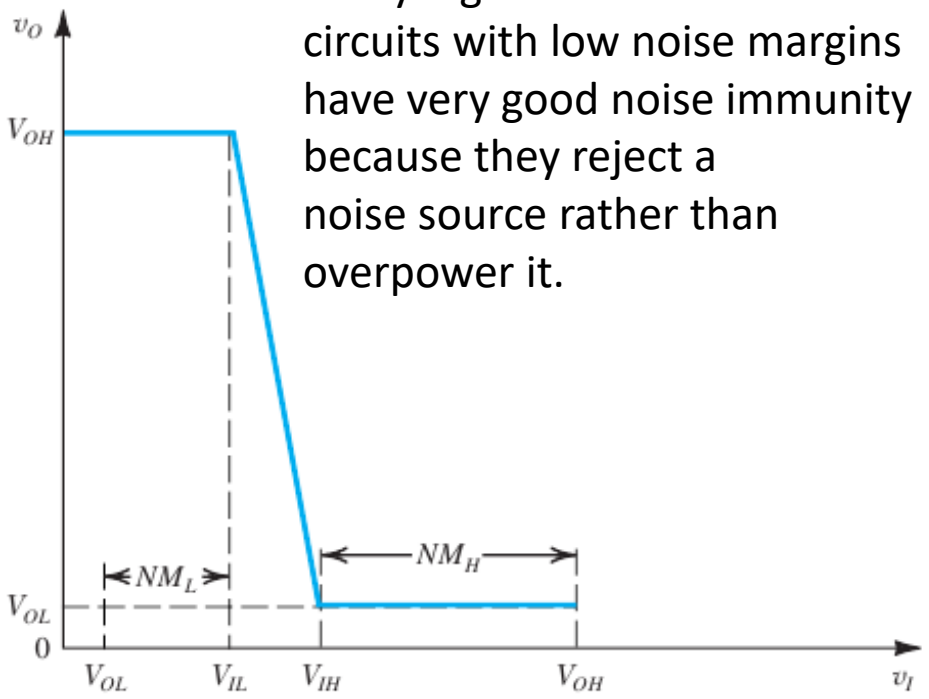


(b) Definition of V_{IH} and V_{IL}

These represent by definition the points where the gain (= dVout / dVin) of the VTC equals −1

Noise Margins





Many digital circuits with low noise margins have very good noise immunity because they reject a noise source rather than overpower it.

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

It is obvious that the margins should be larger than 0 for a digital circuit to be functional and by preference should be as large as possible.

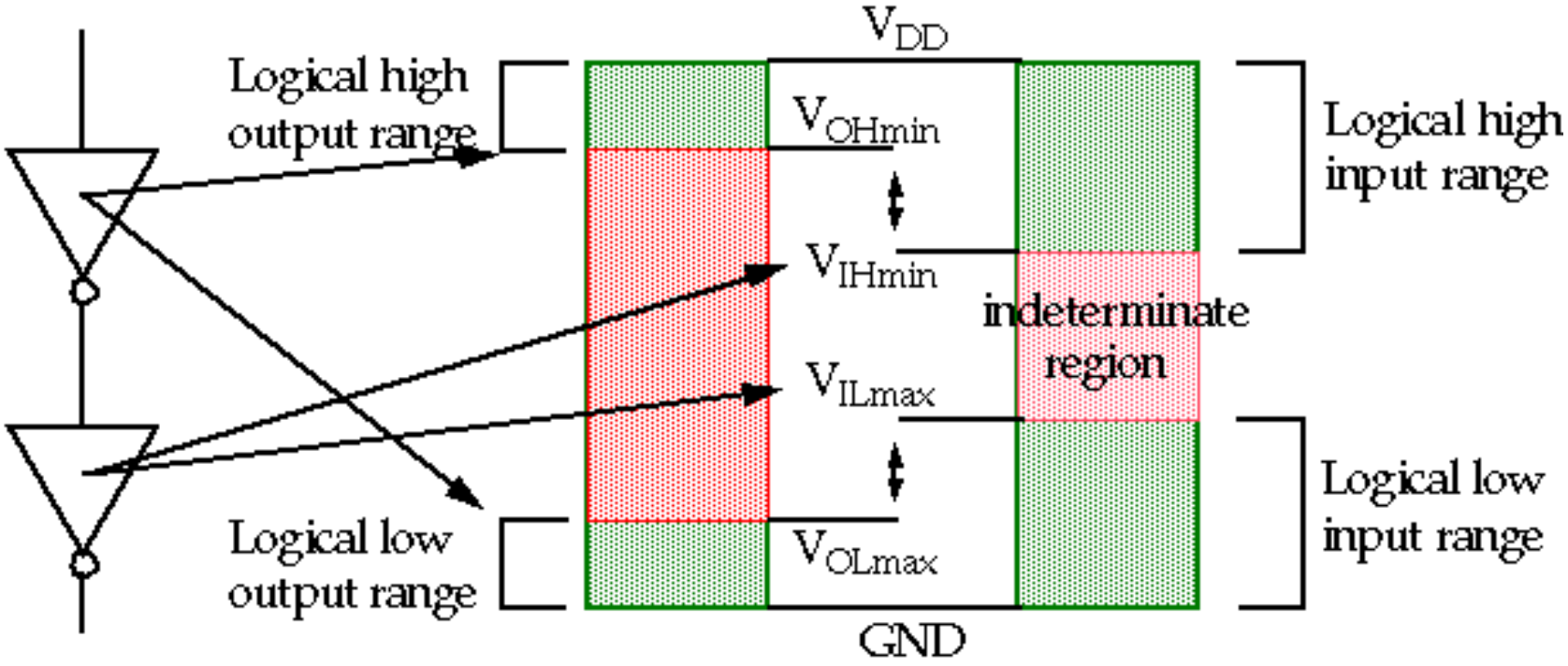
Noise Margin

Noise Margin

- เป็นพารามิเตอร์ที่มีความสัมพันธ์ใกล้เคียงกับคุณลักษณะของแรงดันของอินพุทและเอาท์พุท
- กำหนดขนาดของสัญญาณรบกวนที่สามารถยอมรับได้ที่อินพุท โดยที่ไม่ส่งผลต่อทางด้านเอาท์พุท (นั่นคือวงจรยังสามารถทำงานได้ถูกต้อง)
- ในการกำหนด Noise margin มีสองแบบคือ
  - Noise margin low $NM_L = |V_{IL} - V_{OL}|$
  - Noise margin high $NM_H = |V_{OH} - V_{IH}|$

  โดยที่ V_{IH} = Minimum HIGH input voltage
  V_{IL} = Minimum LOW input voltage
  V_{OH} = Minimum HIGH input voltage
  V_{OL} = Minimum LOW input voltage

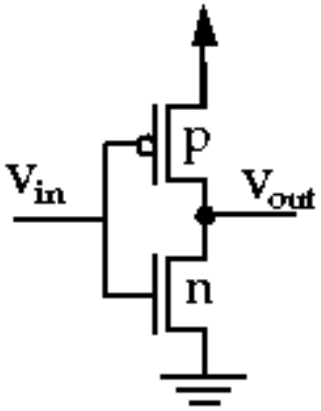
Noise Margin



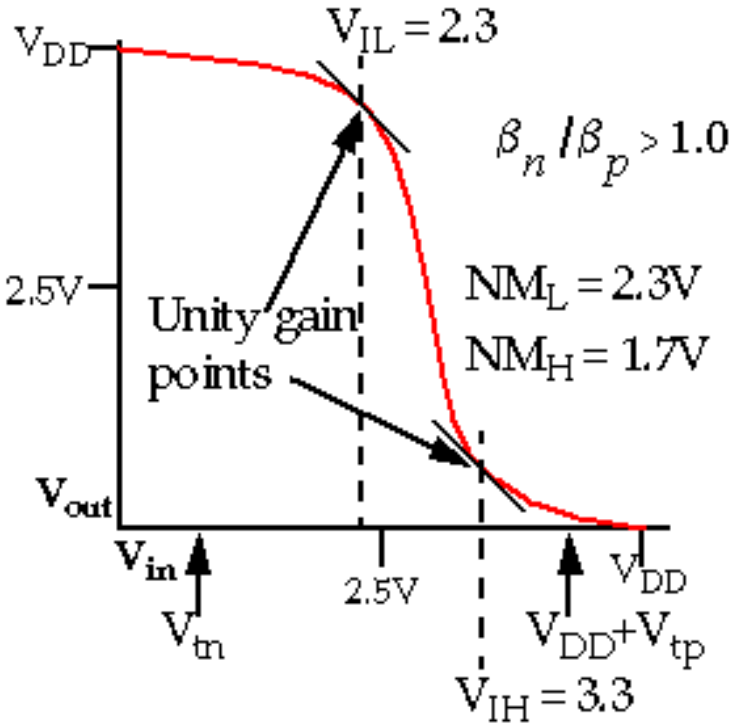
- การนำอุปกรณ์หลาย ๆ ชนิด เช่น CMOS กับ TTL มาต่ออนุกรมกันโดยที่ o/p ของตัวหนึ่งต่อเข้าเป็น i/p ของอีกตัว จำเป็นจะต้องพิจารณา Noise margin ให้เหมาะสมกับการนำมาใช้งานด้วย

Noise Margin

- *Ideal characteristic: $V_{IH} = V_{IL} = (V_{OH} + V_{OL})/2$.*



Assume output of driving gate is stable at supply voltage, e.g.,
$V_{OH} = 5V$
$V_{OL} = 0V$



Noise margins are often compromised to improve speed.

CMOS technology

CMOS technology provides two types of transistors (also called devices): an n-type transistor (nMOS) and a p-type transistor (pMOS)

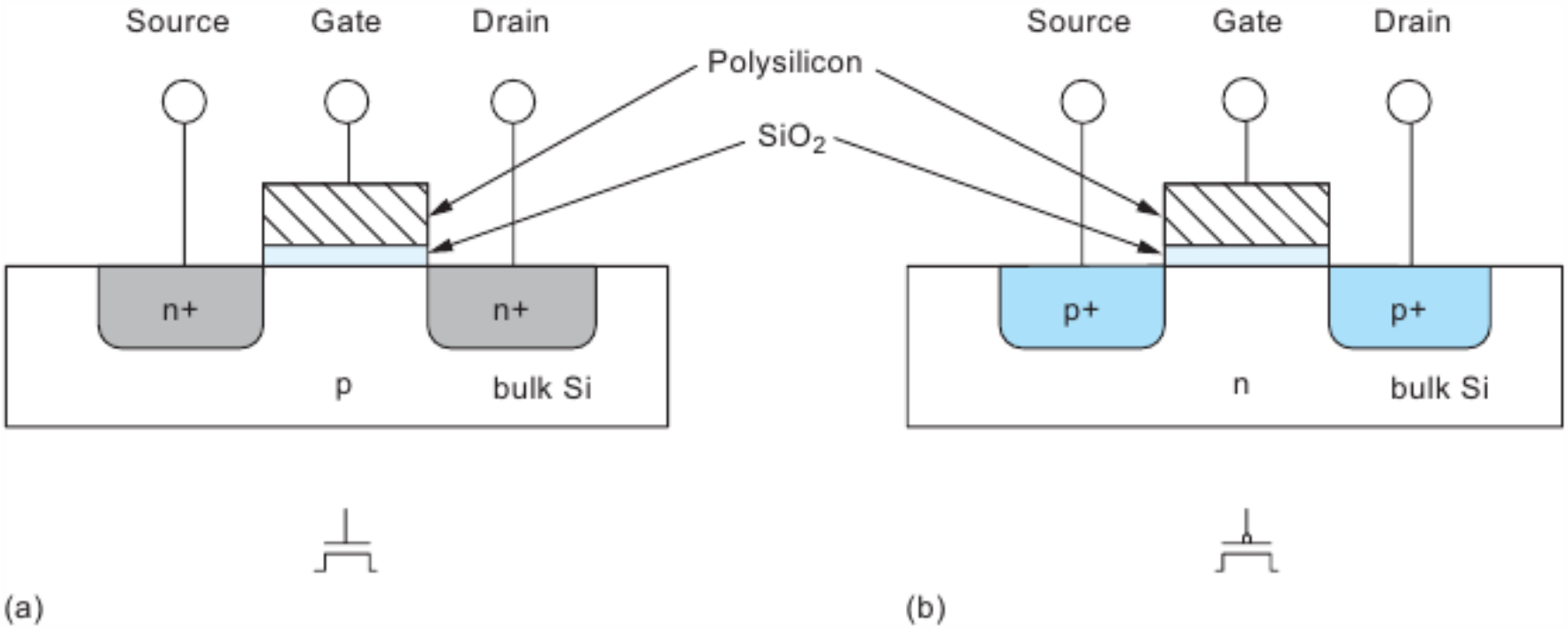


FIGURE 1.9 nMOS transistor (a) and pMOS transistor (b)

Transistor symbols and switch-level models

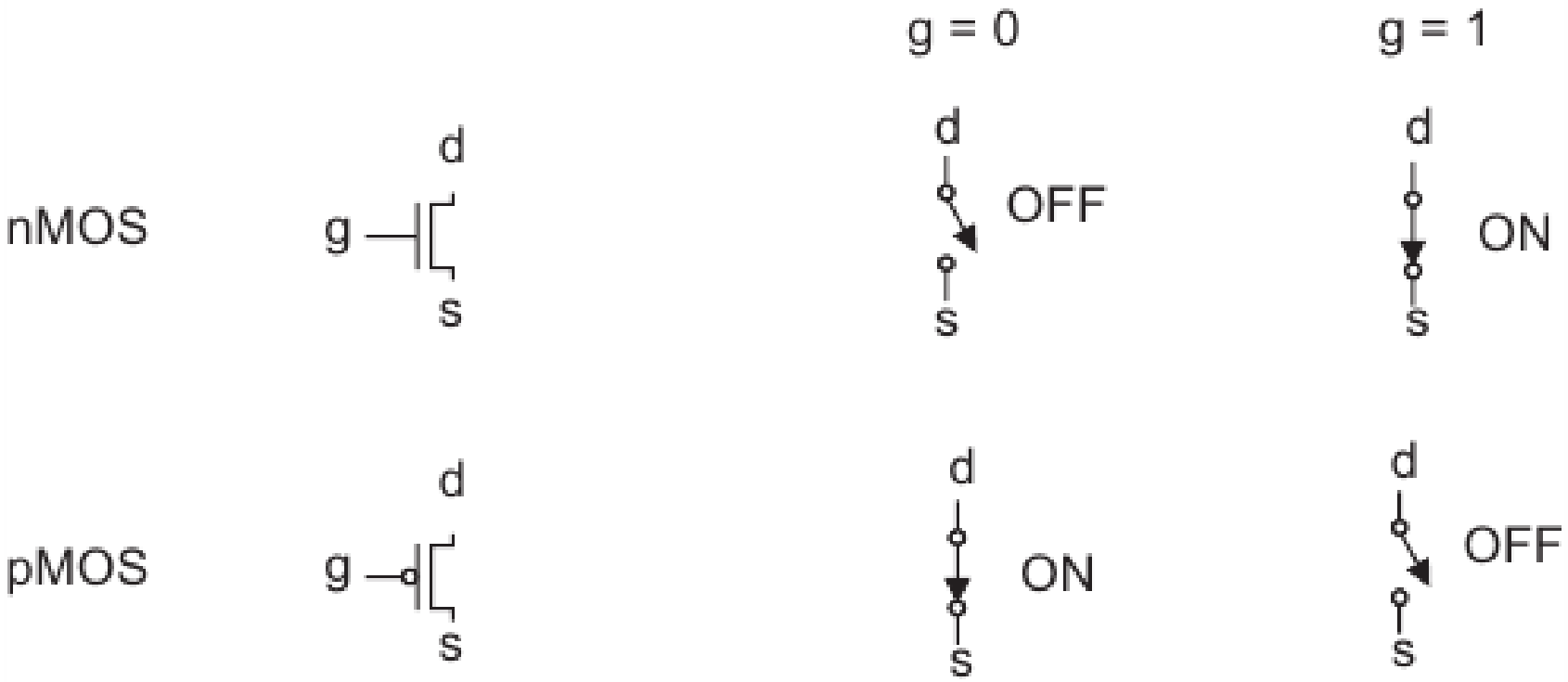


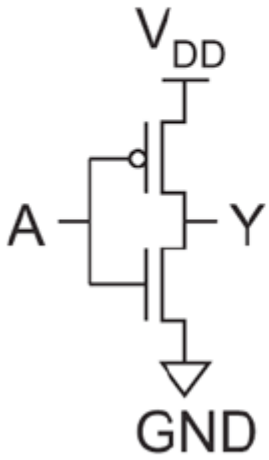
FIGURE 1.10 Transistor symbols and switch-level models

CMOS Logic

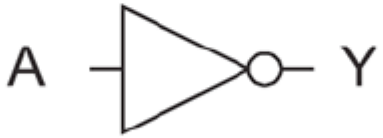
- The Inverter

Table 1.1 Inverter truth table

A	Y
0	1
1	0



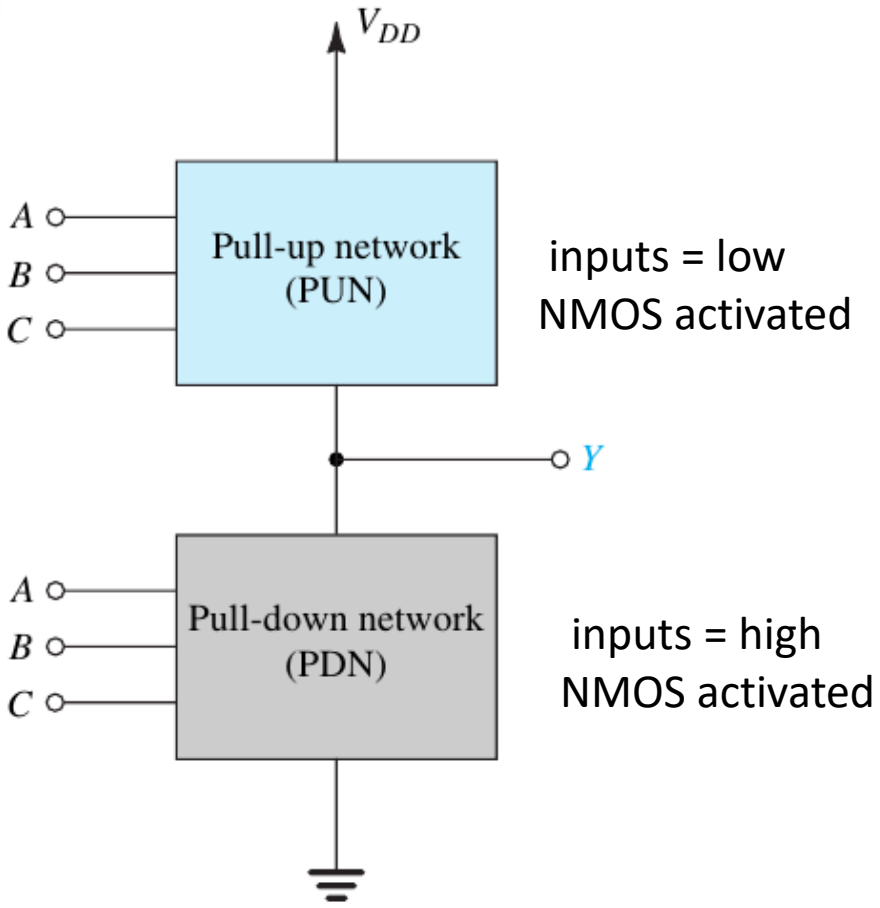
(a)



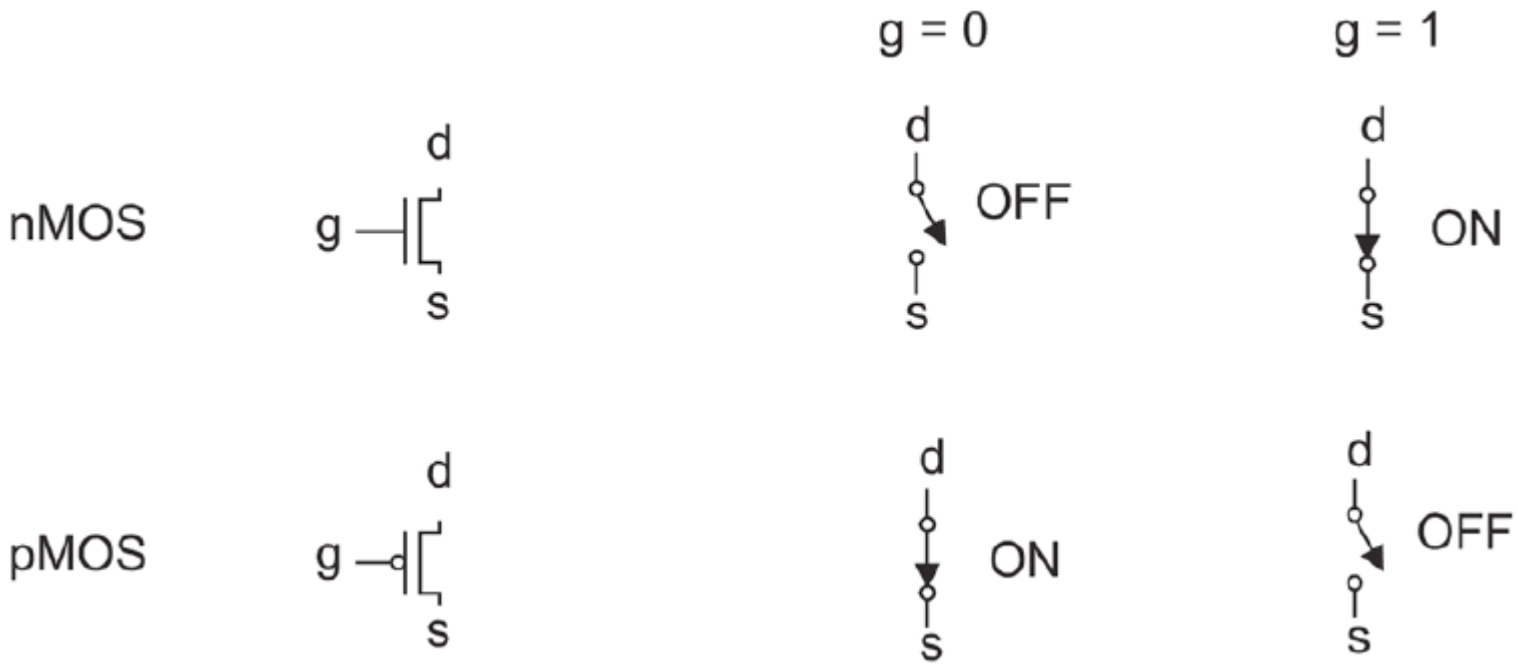
(b)

Basic Structure

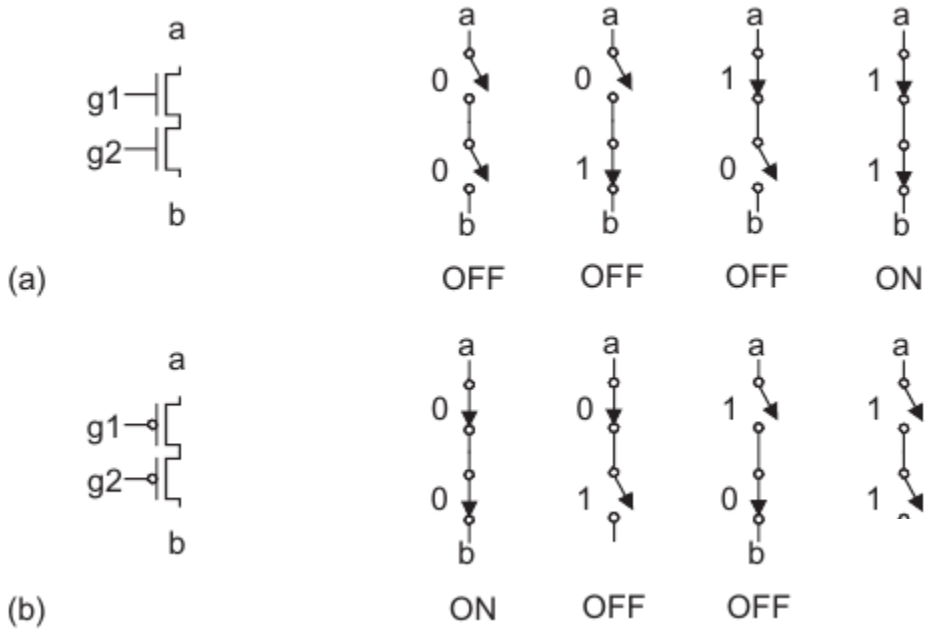
- The CMOS logic gate consists of two networks: the pull-down network (PDN) constructed of NMOS transistors, and the pull up network (PUN) constructed of PMOS transistors
- More elaborate networks are used for more complex gates. Two or more transistors in series are ON only if all of the series transistors are ON. Two or more transistors in parallel are ON if any of the parallel transistors are ON.

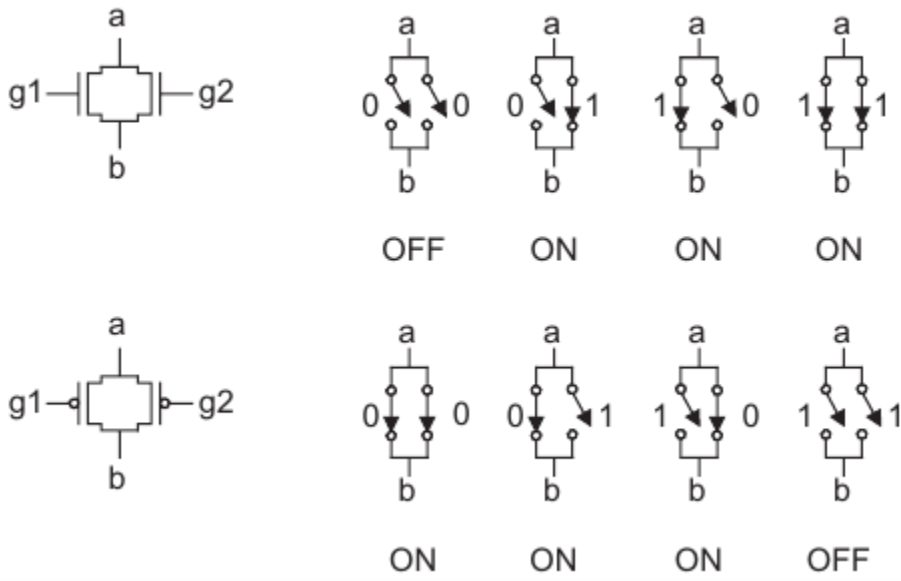


CMOS LOGIC GATE

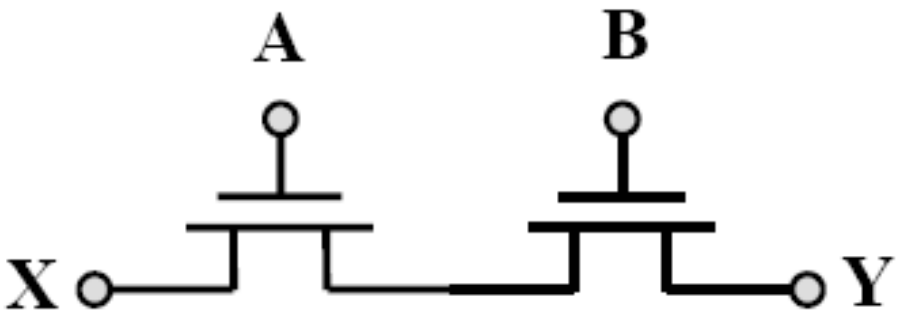


Connection and behavior of series and parallel transistors

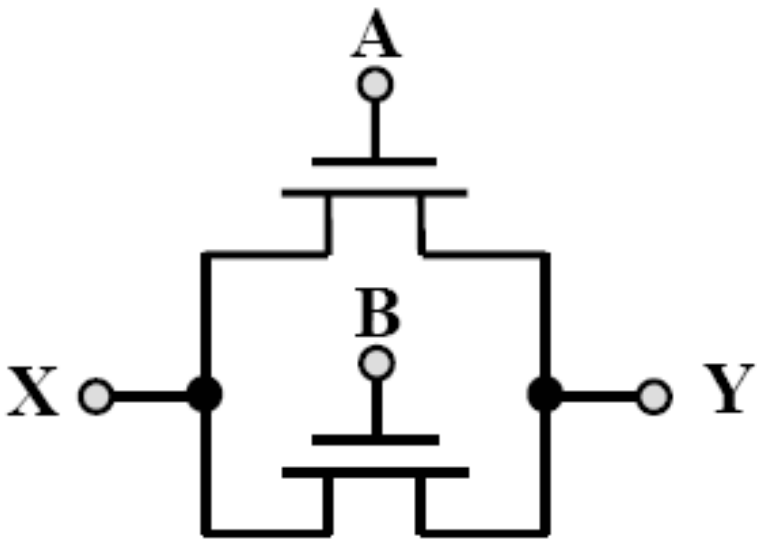




An NMOSFET is a closed switch when the input is high



Y = X if A and B

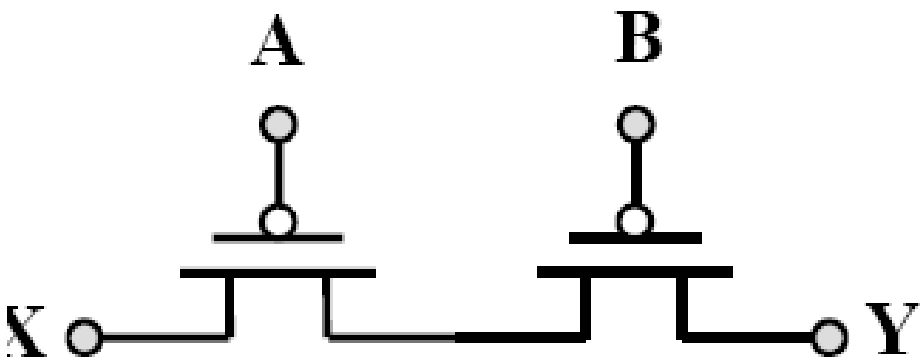


Y = X if A or B

NMOSFETs pass a "strong" **0** but a "weak" **1**

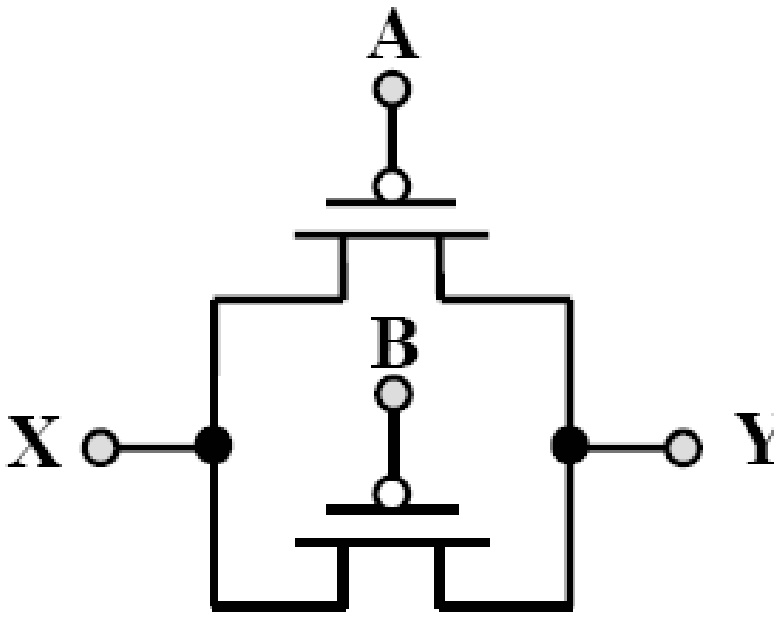
Ref. Prof. King

A PMOSFET is a closed switch when the input is low



$Y = X$ if $\overline{A}$ and $\overline{B}$

$= (\overline{A + B})$



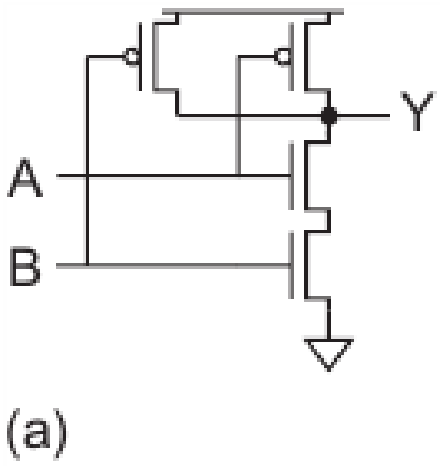
$Y = X$ if $\overline{A}$ or $\overline{B}$

$= (\overline{AB})$

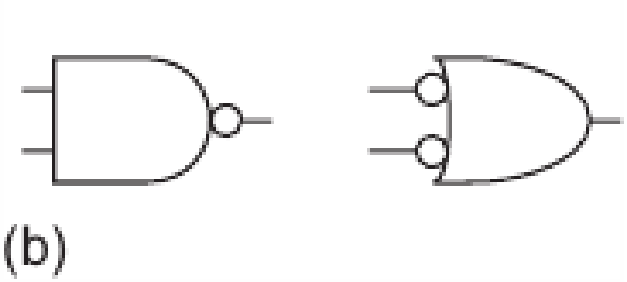
PMOSFETs pass a "strong" **1** but a "weak" **0**

Ref. Prof. King

The NAND Gate



(a)



(b)

FIGURE 1.12 2-input NAND gate schematic (a) and symbol (b) $Y = \overline{A \cdot B}$

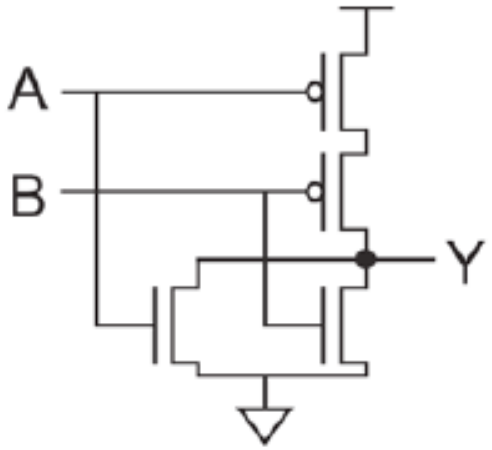
TABLE 1.2 NAND gate truth table

A	B	Pull-Down Network	Pull-Up Network	Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

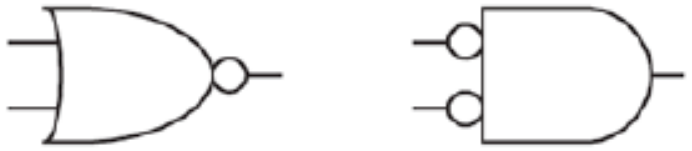
The NOR Gate

Table 1.4 NOR gate truth table

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	0



(a)



(b)

Compound Gates

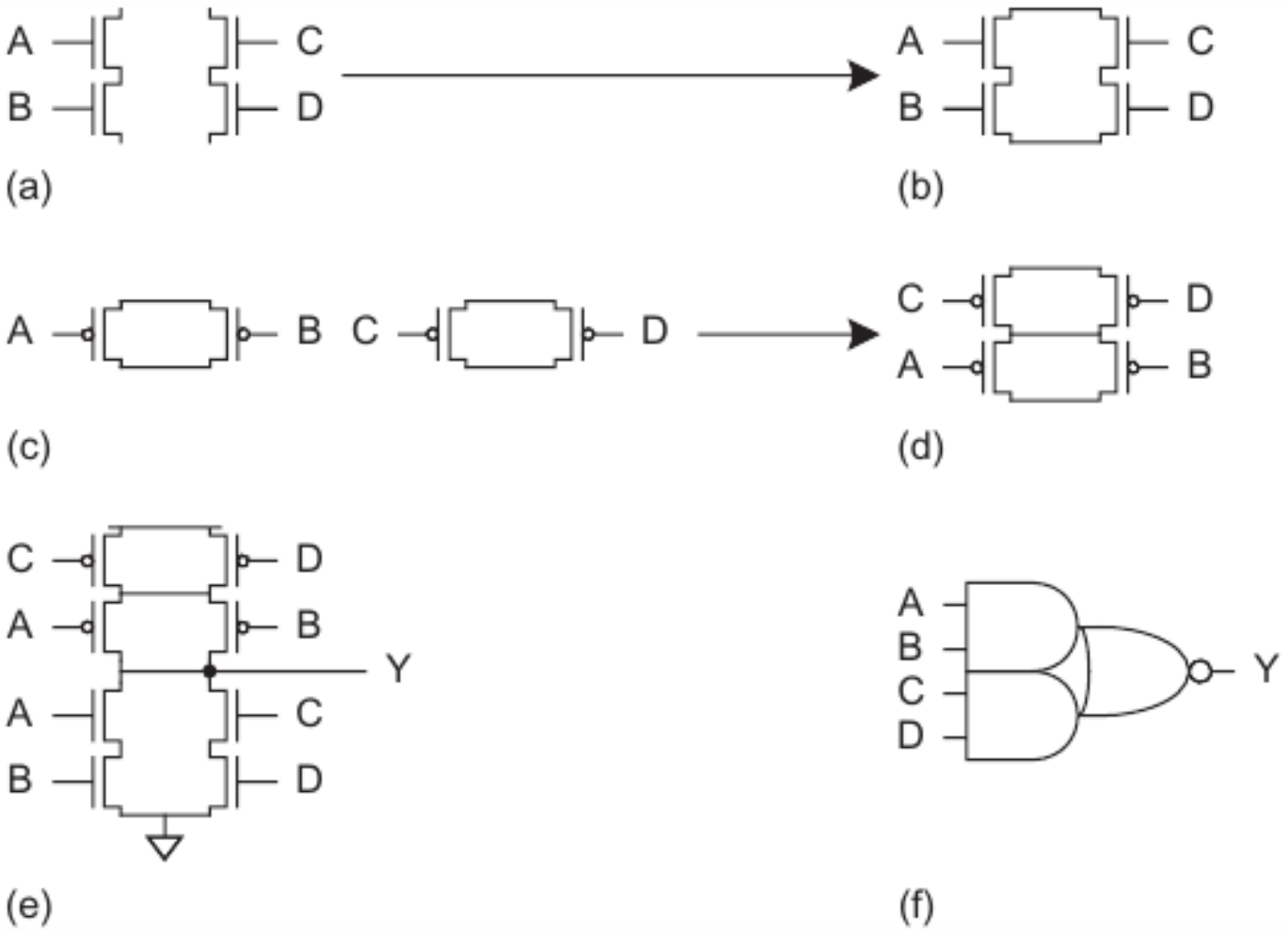


FIGURE 1.18 CMOS compound gate for function $Y = \overline{(A \cdot B) + (C \cdot D)}$

Reference books

- CMOS VLSI Design A Circuits and Systems Perspective Fourth Edition, Neil H. E. Weste ,David Money Harris.
- VLSI Design and Tools : ดร. ธีรยศ เวียงทอง
- Sedra/Smith,*Microelectronic Circuits*, 6^{th} edition
- Digital Integrated Circuits : A Design Perspective 2 Edition : Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic