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01076244 Advanced Digital System Design

Bachelor Program in Computer Engineering (B.Eng.)
Faculty of Engineering
King Mongkut's Institute of Technology Ladkrabang

Clocked Synchronous State-Machine Design

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1. Construct a ________________ corresponding to ________ __________ or ________________, using mnemonic names for the states.
2. (Optional) Minimize the ________________ in the state/output table.
3. Choose a set of ___________________ to the named state.
4. _______________ the state-variable combination into the state/output table to create _____________ _______________ that shows the desired ___________ _________ combination and ___________ for each state/input combination

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5. Choose a ____________________ for the state memory.
6. Construct ____________________ that shows the _____ _________________ required to obtain the desired next state for each/input combination.
7. Derive ________________ from the __________________.
8. Derive ________________ from the transition/output table.
9. ________________________ that shows the state-variable storage elements and realized the required excitation and output equations.

State-Table Design Example

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Design a clocked synchronous state machine with two inputs, A and B, and a single output Z that is 1 if :

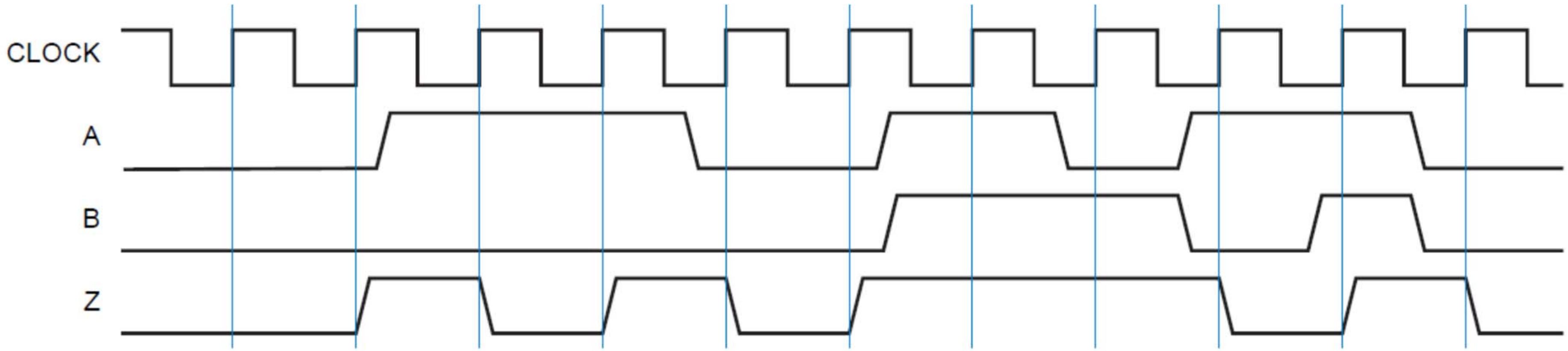
- A had the same value at each of the two previous clock ticks, *or*
- B has been 1 since the last time that the first condition was true.

Otherwise, the output should be 0.

The output Z is 1 if :

- A had the same value at each of the two previous clock ticks, *or*
- B has been 1 since the last time that the first condition was true.

Otherwise, the output should be 0.



Timing diagram for example state machine

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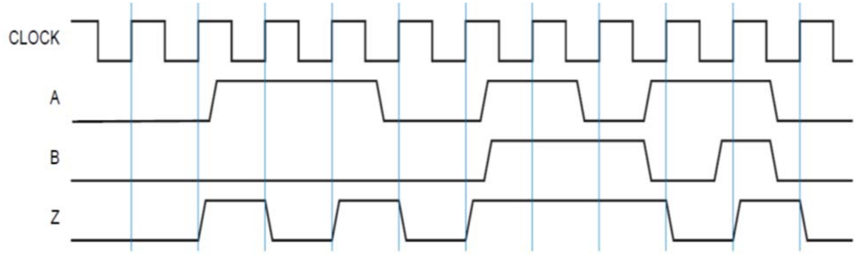

		AB				
Meaning	S	00	01	11	10	Z
Initial state	INIT					0
	. . .					
	. . .					
	. . .					
		S*				

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The output Z is 1 if :

- A had the same value at each of the two previous clock ticks, *or*
- B has been 1 since the last time that the first condition was true.

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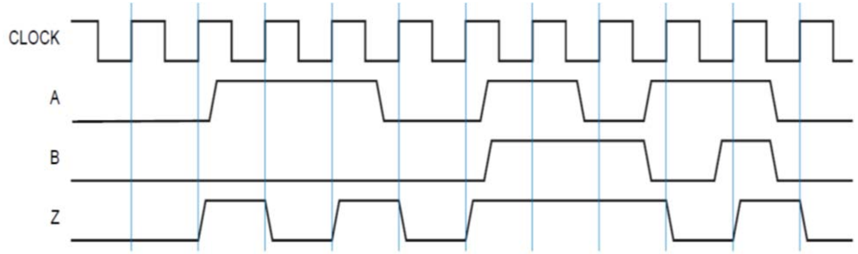

		AB				
Meaning	S	00	01	11	10	Z
Initial state	INIT					0
	. . .					
	. . .					
	. . .					
		S*				

		AB				
Meaning	S	00	01	11	10	Z
Initial state	INIT					0
Got a 0 on A	A0					0
Got a 1 on A	A1					0
		S*				

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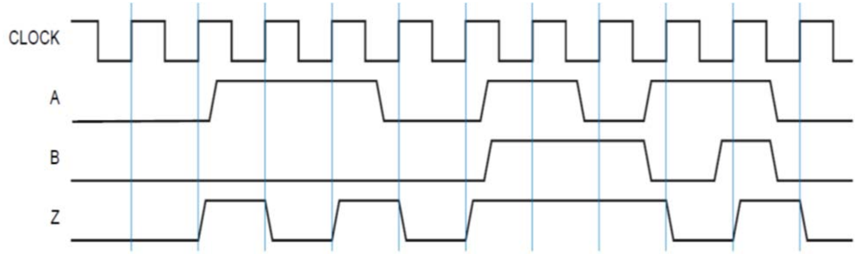
The output Z is 1 if :

- A had the same value at each of the two previous clock ticks, *or*
- B has been 1 since the last time that the first condition was true.

Otherwise, the output should be 0.



		A B				
Meaning	S	00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0					0
Got a 1 on A	A1					0
		S*				

		A B				
Meaning	S	00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0					0
Got a 1 on A	A1					0
Got two equal A inputs	OK					1
		S*				

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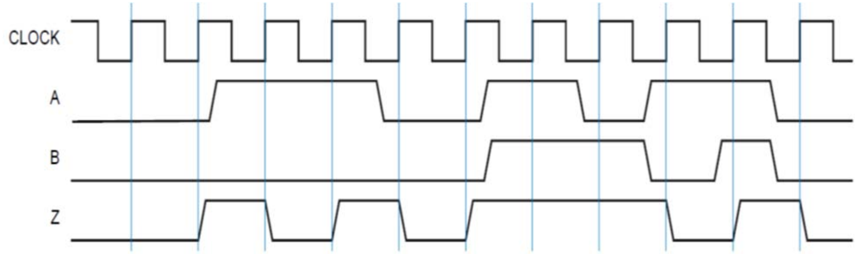
The output Z is 1 if :

- A had the same value at each of the two previous clock ticks, *or*
- B has been 1 since the last time that the first condition was true.

Otherwise, the output should be 0.



		A B				
Meaning	S	00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1					0
Got two equal A inputs	OK					1
		S*				

		A B				
Meaning	S	00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1					0
Got two equal A inputs	OK					1
		S*				

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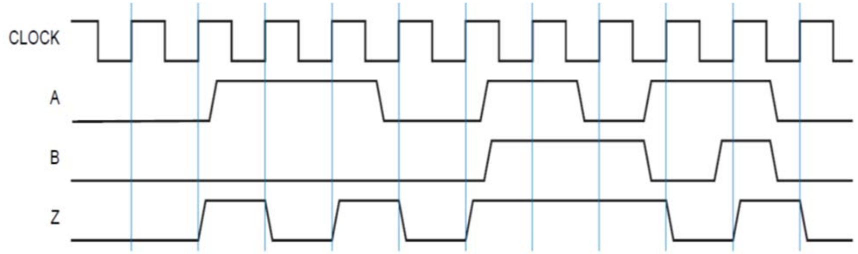

Meaning	S	AB 00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1	A0	A0	OK	OK	0
Got two equal A inputs	OK					1
		S*				

Meaning	S	AB 00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1	A0	A0	OK	OK	0
Got two equal A inputs	OK		OK	OK		1
		S*				

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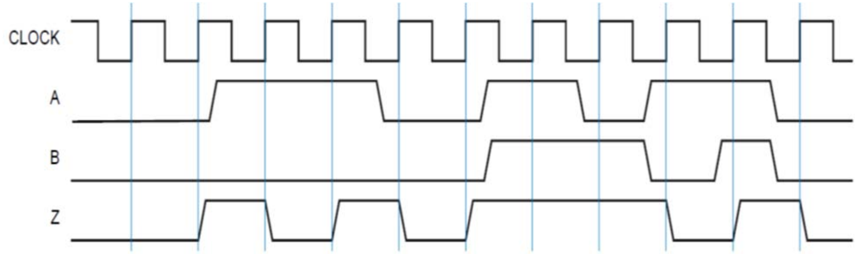
The output Z is 1 if :

- A had the same value at each of the two previous clock ticks, *or*
- B has been 1 since the last time that the first condition was true.

Otherwise, the output should be 0.



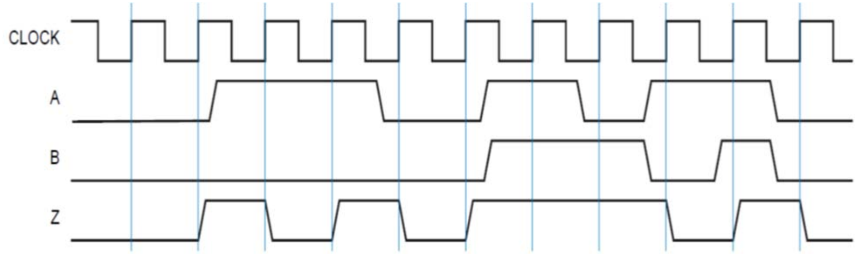
Meaning	S	AB 00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK	OK	A1	A1	0
Got a 1 on A	A1	A0	A0	OK	OK	0
Got two equal A inputs	OK	?	OK	OK	?	1
		S*				

Meaning	S	AB 00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0			A1	A1	0
Got a 1 on A	A1	A0	A0			0
		S*				

The output Z is 1 if :

- A had the same value at each of the two previous clock ticks, *or*
- B has been 1 since the last time that the first condition was true.

Otherwise, the output should be 0.



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Meaning	S	AB 00	AB 01	AB 11	AB 10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0					1
Two equal, A=1 last	OK1					1
		S*				

Meaning	S	AB 00	AB 01	AB 11	AB 10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0					1
Two equal, A=1 last	OK1					1
		S*				

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The output Z is 1 if :

- A had the same value at each of the two previous clock ticks, *or*
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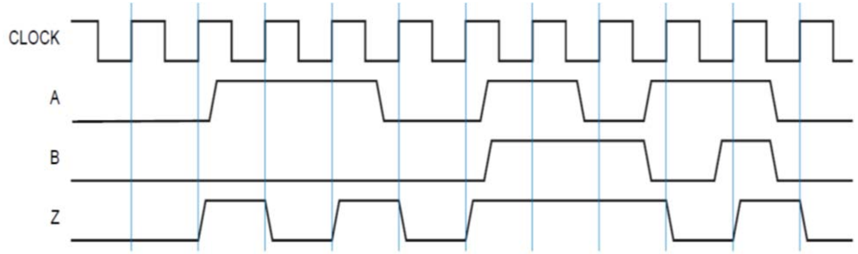

Meaning	S	AB 00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0	OK0	OK0	OK1	A1	1
Two equal, A=1 last	OK1					1
		S*				

Meaning	S	AB 00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0	OK0	OK0	OK1	A1	1
Two equal, A=1 last	OK1					1
		S*				

State Minimization

Meaning	S	00	01	11	10	Z
		A B				
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK0	OK0	A1	A1	0
Got a 1 on A	A1	A0	A0	OK1	OK1	0
Two equal, A=0 last	OK0	OK0	OK0	OK1	A1	1
Two equal, A=1 last	OK1	A0	OK0	OK1	OK1	1
		S*				

Minimal state table

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Meaning	S	00	01	11	10	Z
		A B				
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK00	OK00	A1	A1	0
Got a 1 on A	A1	A0	A0	OK11	OK11	0
Got 00 on A	OK00	OK00	OK00	OKA1	A1	1
Got 11 on A	OK11	A0	OKA0	OK11	OK11	1
OK, got a 0 on A	OKA0	OK00	OK00	OKA1	A1	1
OK, got a 1 on A	OKA1	A0	OKA0	OK11	OK11	1
		S*				

Meaning	S	00	01	11	10	Z
		A B				
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK00	OK00	A1	A1	0
Got a 1 on A	A1	A0	A0	OK11	OK11	0
Got 00 on A	OK00	OK00	OK00	A001	A1	1
Got 11 on A	OK11	A0	A110	OK11	OK11	1
Got 001 on A, B=1	A001	A0	AE10	OK11	OK11	1
Got 110 on A, B=1	A110	OK00	OK00	AE01	A1	1
Got bb...10 on A, B=1	AE10	OK00	OK00	AE01	A1	1
Got bb...01 on A, B=1	AE01	A0	AE10	OK11	OK11	1
		S*				

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Two state S1 and S2 are equivalent if:

1. S1 and S2 must ______________________ at the state-machine output(s).
2. For each input combination, S1 and S2 must have either _____________ _________________ or _______________________.

		AB				
Meaning	S	00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK00	OK00	A1	A1	0
Got a 1 on A	A1	A0	A0	OK11	OK11	0
Got 00 on A	OK00	OK00	OK00	OKA1	A1	1
Got 11 on A	OK11	A0	OKA0	OK11	OK11	1
OK, got a 0 on A	OKA0	OK00	OK00	OKA1	A1	1
OK, got a 1 on A	OKA1	A0	OKA0	OK11	OK11	1
		S*				

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		A B				
Meaning	S	00	01	11	10	Z
Initial state	INIT	A0	A0	A1	A1	0
Got a 0 on A	A0	OK00	OK00	A1	A1	0
Got a 1 on A	A1	A0	A0	OK11	OK11	0
Got 00 on A	OK00	OK00	OK00	A001	A1	1
Got 11 on A	OK11	A0	A110	OK11	OK11	1
Got 001 on A, B=1	A001	A0	AE10	OK11	OK11	1
Got 110 on A, B=1	A110	OK00	OK00	AE01	A1	1
Got bb...10 on A, B=1	AE10	OK00	OK00	AE01	A1	1
Got bb...01 on A, B=1	AE01	A0	AE10	OK11	OK11	1
		S*				

State Assignment

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- A ____________________ is the binary combination assigned to a particular state.
- The ________________________ in a machine with n flip-flops is 2^n, so the number of flip-flops needed to code s states is $\lceil \log_2 s \rceil$, the smallest integer greater than or equal to $log_2 s$.

S	A B 00	01	11	10	Z
INIT	A0	A0	A1	A1	0
A0	OK0	OK0	A1	A1	0
A1	A0	A0	OK1	OK1	0
OK0	OK0	OK0	OK1	A1	1
OK1	A0	OK0	OK1	OK1	1
	S*				

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	Assignment			
State name	Simplest Q1 - Q3	Decomposed Q1 - Q3	One-hot Q1 - Q5	Almost one-hot Q1 - Q4
INIT	000	000	00001	0000
A0	001	100	00010	0001
A1	010	101	00100	0010
OK0	011	110	01000	0100
OK1	100	111	10000	1000

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- The simplest state assignment ______________________ to the simplest excitation equations, output equations, and resulting logic circuit.

- Most digital designers rely on _________________ and ______ ___________________ for making reasonable state assignments.

- Choose __________________________ into which the machine can easily be forced at reset (00 … 00 or 11 … 11 in typical circuits).
- __________________________________ that change on each transition.
- If there are unused states, then ____________________ of the available state-variable combinations to ______________________ __________________; *i.e.*, ____________________ the choice of coded states to the first *s* *n*-bit integers.

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- ________________ the set of state variables into ________________ ________________ where each bit or field has a ________________ __________ with respect to the ______________ or ______________ __________ of the machine.
- Consider using _______________________ number of state variables to make a decomposed assignment possible.
- Etc.

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When the number of states available with n flip-flops, 2^n, is greater than the number of states required, s.

Two possible approaches:

- Minimal risk.
  - Assume that it is possible for the state machine somehow to get into one of the unused ________________ states : hardware failure, an unexpected input, or a design error.
  - Therefore, all of the unused state-variable combination are ________ ________, and ___________________________ are made so that, for any input combination, the unused states go to the ______________ state, the ___________ state, or some other ____________ state.

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- Minimal cost.
  - Assume that the machine ________________ an unused state.
  - Therefore, in the transition and excitation tables, the next-state entries of the unused states can be marked as ________________ In most case, this simplifies the excitation logic.
  - However, the machine's behavior if it ever does enter an unused state may be pretty weird.

Synthesis Using D Flip-Flops

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	A B				
S	00	01	11	10	Z
INIT	A0	A0	A1	A1	0
A0	OK0	OK0	A1	A1	0
A1	A0	A0	OK1	OK1	0
OK0	OK0	OK0	OK1	A1	1
OK1	A0	OK0	OK1	OK1	1
	S*				

State / output table

	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	111	101	1
111	100	110	111	111	1
	Q1* Q2* Q3*				

Transition / output table
(possibly minimized)

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	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	111	101	1
111	100	110	111	111	1
	Q1* Q2* Q3*				

Transition / output table
(possibly minimized)

	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	111	101	1
111	100	110	111	111	1
	D1 D2 D3				

Excitation / output table

	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	111	101	1
111	100	110	111	111	1
	D1 D2 D3				

Excitation / output table

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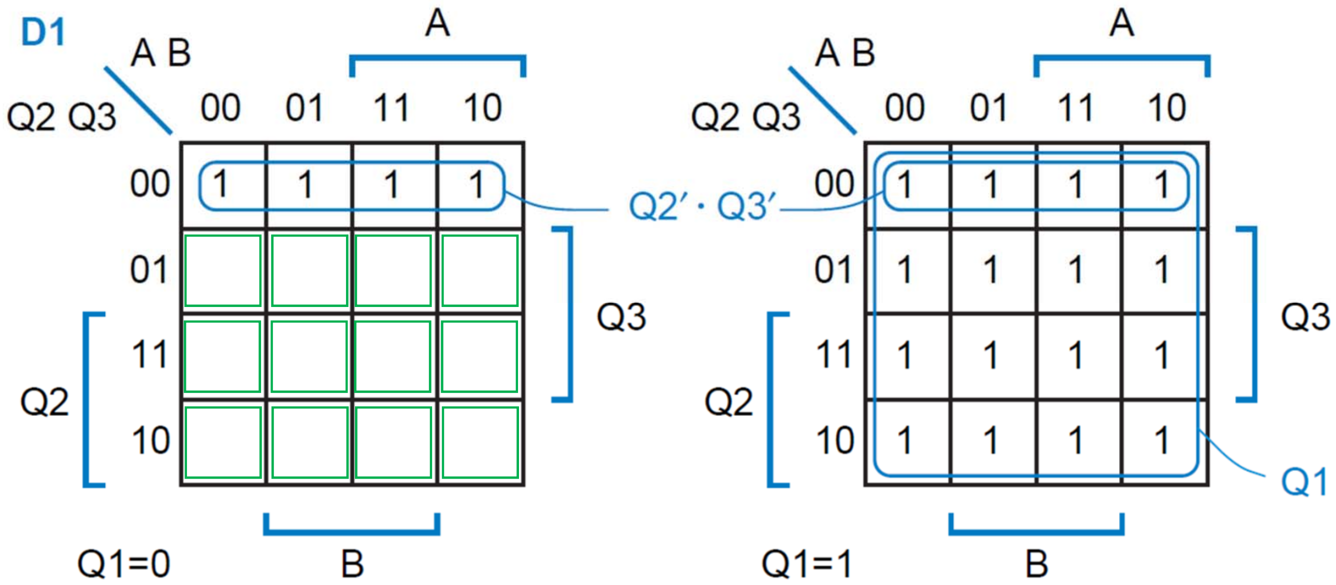

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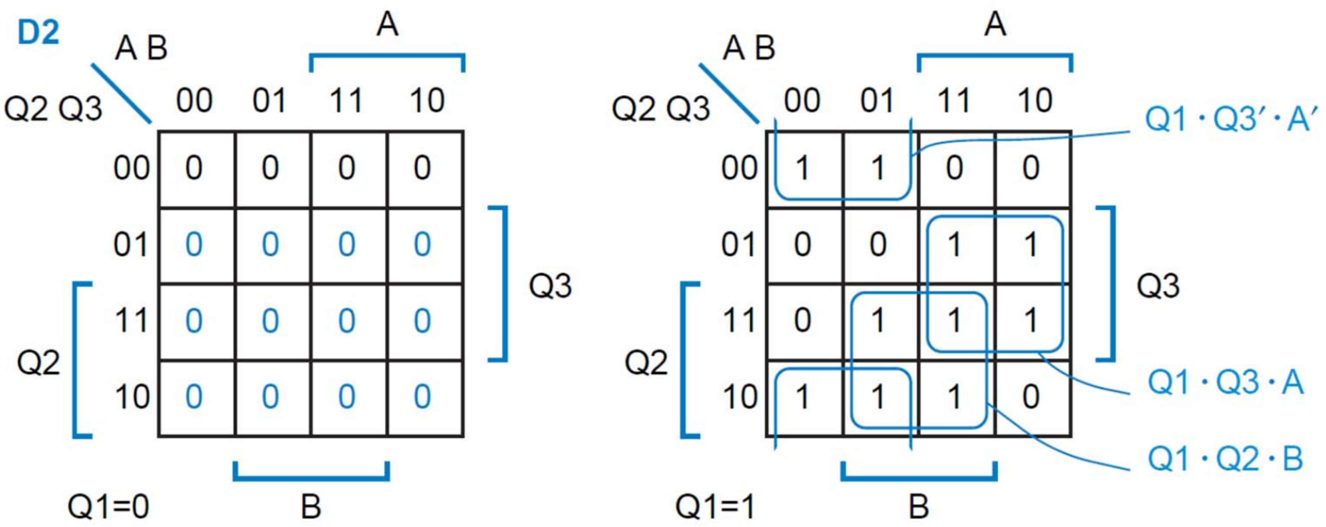
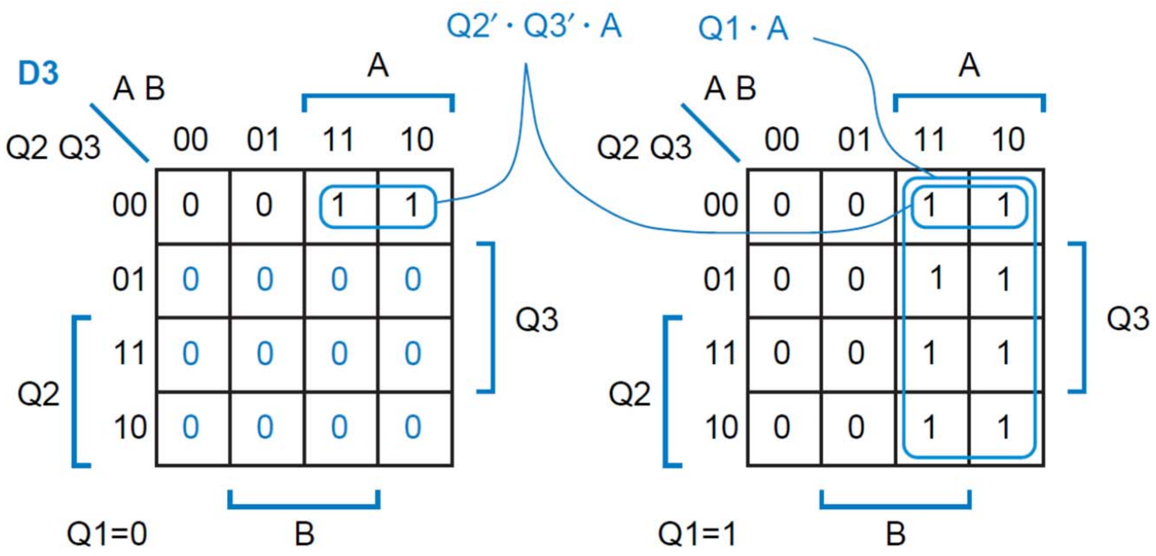
	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	111	101	1
111	100	110	111	111	1
	D1 D2 D3				

Excitation / output table



	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	111	101	1
111	100	110	111	111	1
	D1 D2 D3				

Excitation / output table



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In case “don’t-cares” are used in the unused states.

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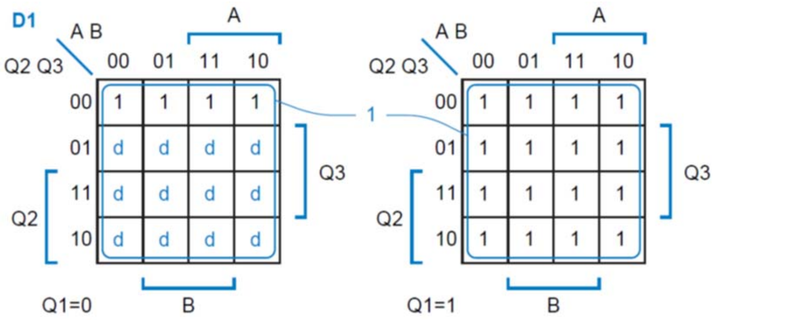

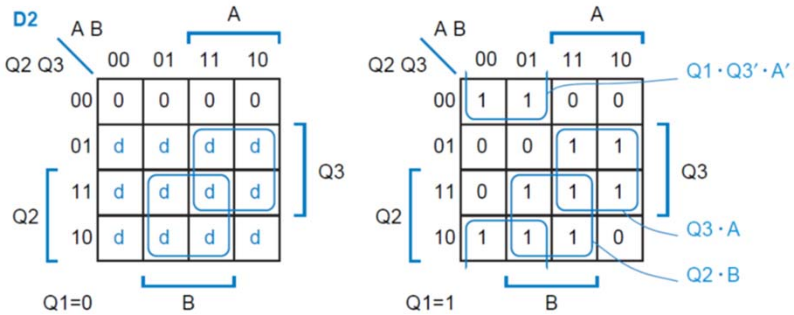

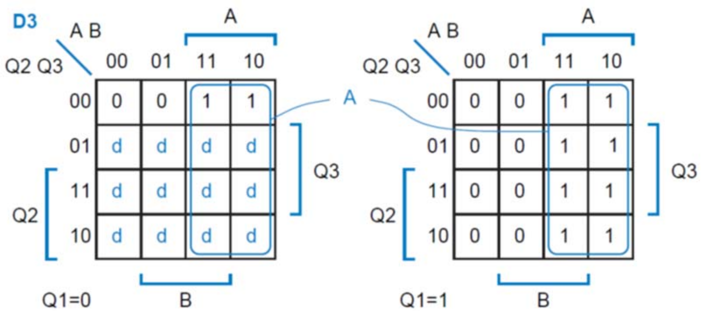

$D1 = 1$

$D2 = Q1 \cdot Q3' \cdot A + Q3 \cdot A + Q2 \cdot B$

$D3 = A$

$Z = Q1 \cdot Q2$

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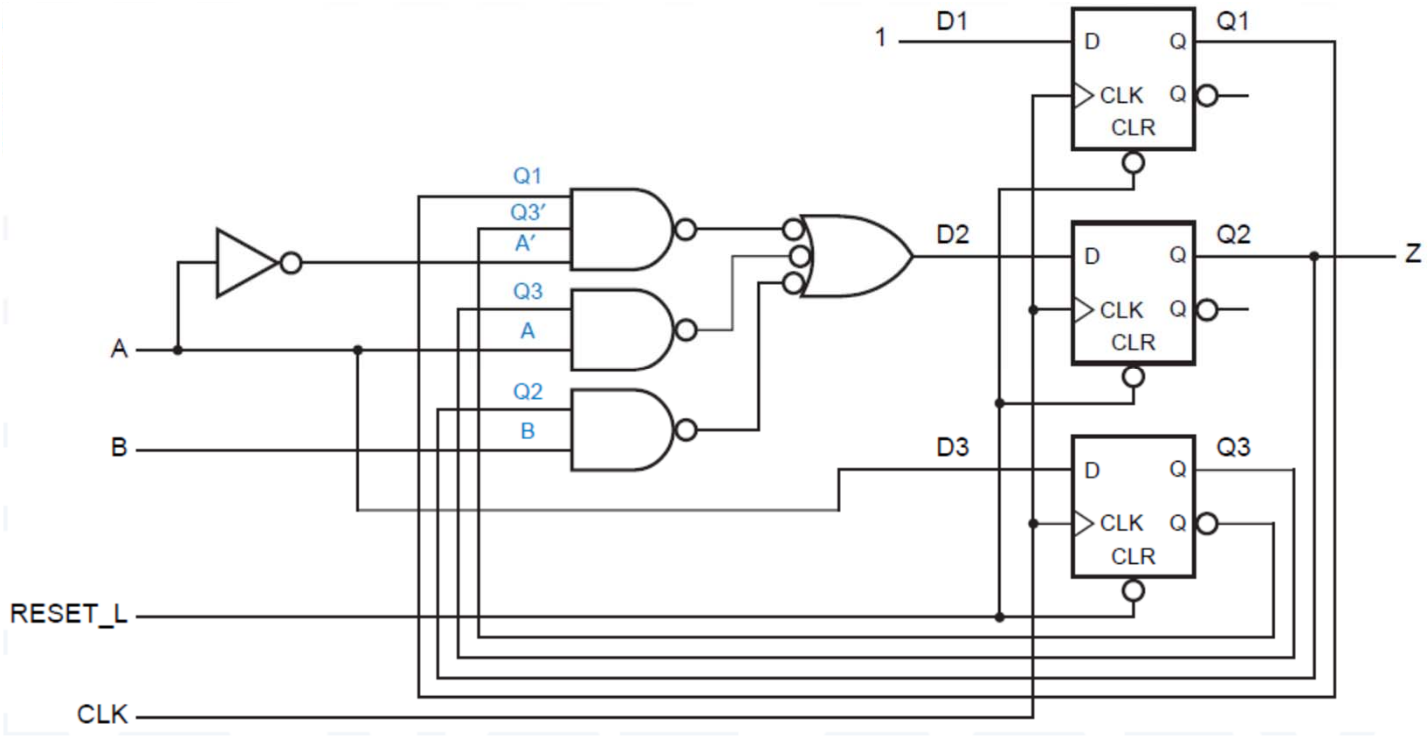

Synthesis Using J-K Flip-Flops

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Q	Q*	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	100	100	101	101	0
100	110	110	101	101	0
101	100	100	111	111	0
110	110	110	111	101	1
111	100	110	111	111	1
	Q1* Q2* Q3*				

Transition / output table
(possibly minimized)

	A B				
Q1 Q2 Q3	00	01	11	10	Z
000	1d , 0d , 0d	1d , 0d , 0d	1d , 0d , 1d	1d , 0d , 1d	0
100	d0 , 1d , 0d	d0 , 1d , 0d	d0 , 0d , 1d	d0 , 0d , 1d	0
101	d0 , 0d , d1	d0 , 0d , d1	d0 , 1d , d0	d0 , 1d , d0	0
110	d0 , d0 , 0d	d0 , d0 , 0d	d0 , d0 , 1d	d0 , d1 , 1d	1
111	d0 , d1 , d1	d0 , d0 , d1	d0 , d0 , d0	d0 , d0 , d0	1
	J1 K1 , J2 K2 , J3 K3				

Excitation / output table

Excitation maps for J1, K1
Assuming that unused states go to state 000

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J1

Q1=0

Q2 Q3 \ A B	00	01	11	10
00	1	1	1	1
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

$Q2 \cdot Q3'$

Q1=1

Q2 Q3 \ A B	00	01	11	10
00	d	d	d	d
01	d	d	d	d
11	d	d	d	d
10	d	d	d	d

K1

Q1=0

Q2 Q3 \ A B	00	01	11	10
00	d	d	d	d
01	d	d	d	d
11	d	d	d	d
10	d	d	d	d

Q1=1

Q2 Q3 \ A B	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

Excitation maps for J2, K2
Assuming that unused states go to state 000

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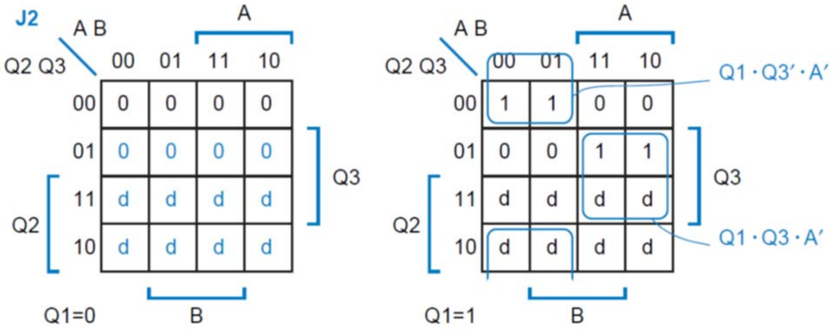

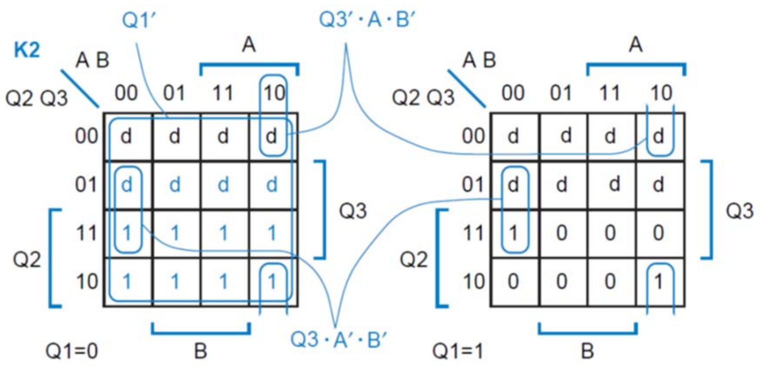

Excitation maps for J3, K3
Assuming that unused states go to state 000

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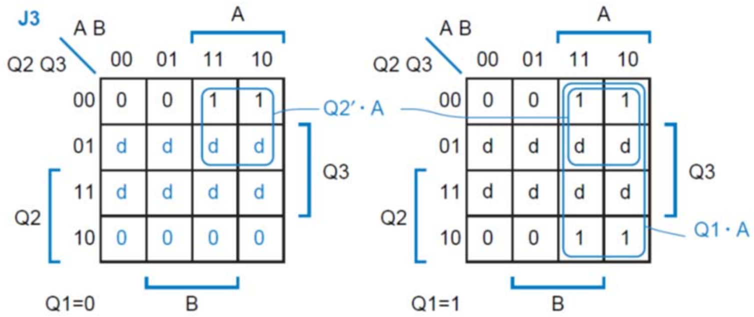

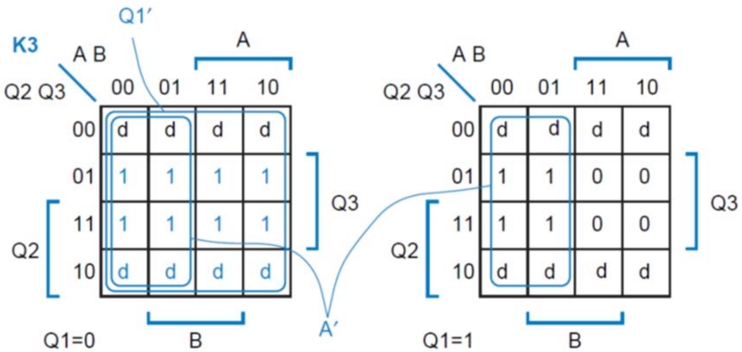

Excitation equations using J-K flip-flops

by putting d's in all of the unused state entries

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$J1 = 1$

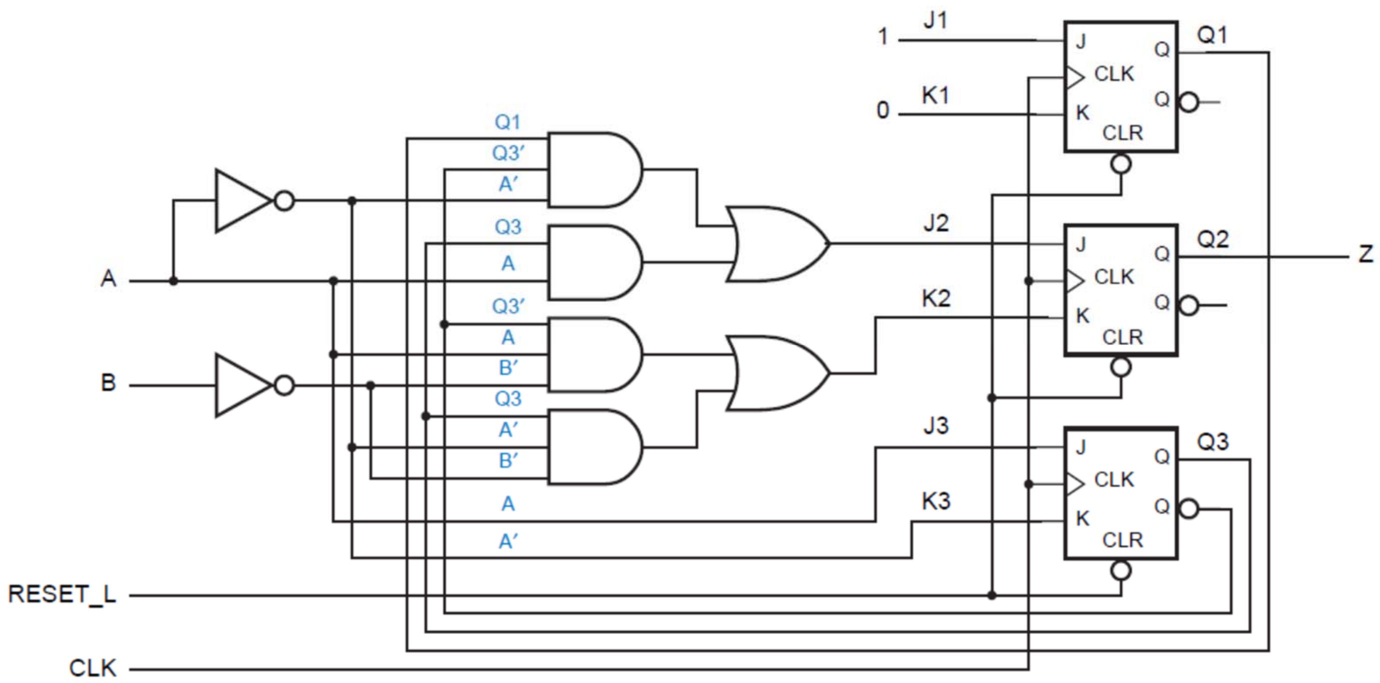
$J2 = Q1 \cdot Q3 \cdot A' + Q3 \cdot A$

$J3 = A$

$K1 = 0$

$K2 = Q3' \cdot A \cdot B' + Q3 \cdot A' \cdot B'$

$K3 = A'$



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Q & A