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Sequential Logic Design Principles

- Logic circuits are classified into two types

- Combinational \Rightarrow O/P ขึ้นกับ I/P only Ex. TV เพียงอย่างเดียว

- Sequential \Rightarrow O/P ขึ้นกับ I/P & Mem ก่อนหน้ามีอยู่ ^(State)



Combinational



Sequential

Sequential Logic Design Principles

- Logic circuits are classified into two types
 - Combinational
 - One whose O/P depend only on its current I/P
 - Sequential
 - One whose O/P depend not only on It's current I/P. but also on the past sequence of I/P. possibly arbitrarily far back in time
(state)

Design base on I/P

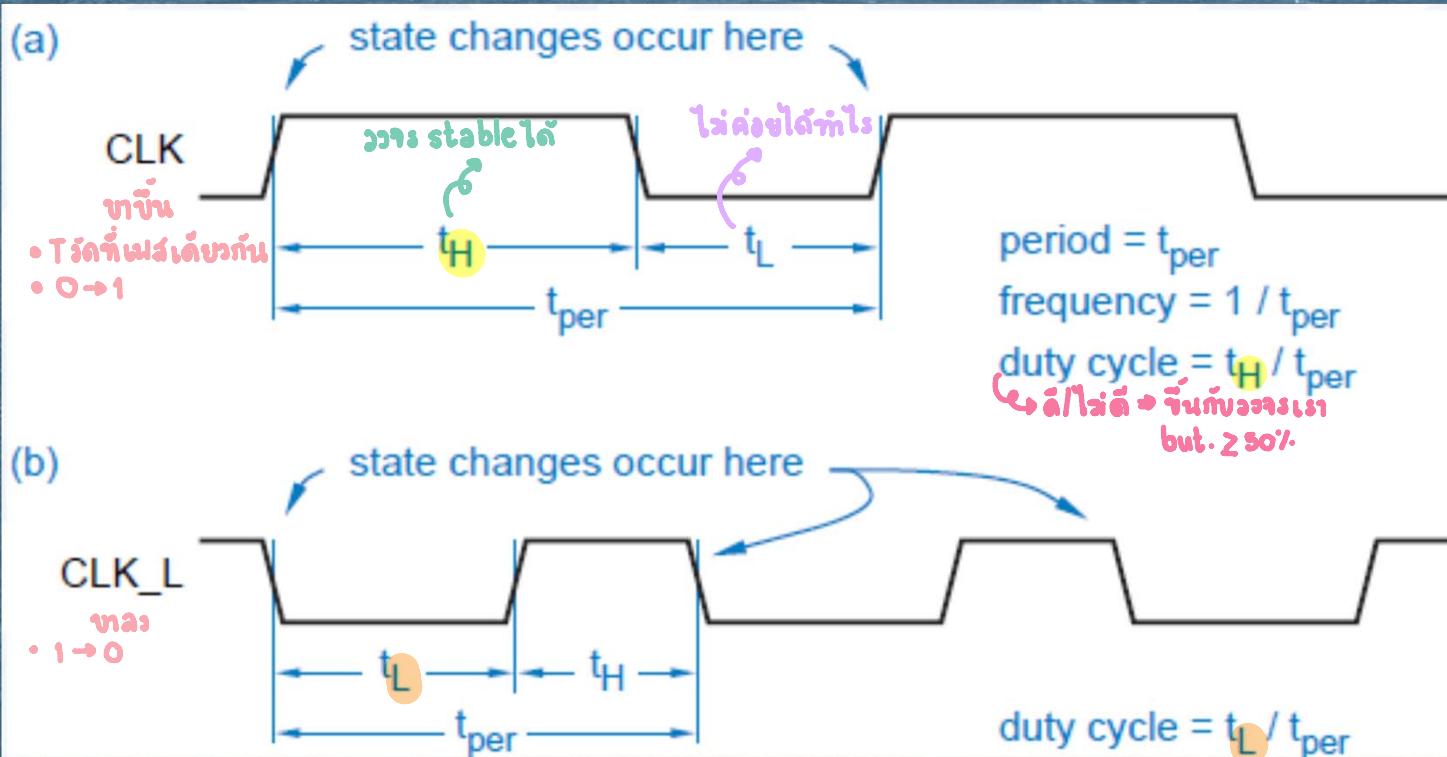
How to design

“The **State** of a sequential circuit is a collection of **State variables**
whose values at any one time contain all the information about the
past necessary to account for the circuit's future behavior.”

= Digital Computer System Principles, McGraw-Hill (1967) =

- ▶ In a digital logic circuit, state variables are **binary values**
ตัวดำเนินงาน ช่วง ที่ ถูกต้อง
corresponding to certain logic signals in the circuit.
- ▶ A circuit with n binary state variables has 2^n possible states.
จำนวน bit
ตัวบ่งไปได้
- ▶ 2^n is always finite, never infinite, so sequential circuits are
sometimes called **finite-state machines**
ต่อเนื่อง, เป็นไปตามลำดับ

HW. สั่นเทอม เขียน Com 1 หรือ 4 bit



เลือกใช้อะไร bec. อะไร ? (ได้ทั้ง 2 อย่าง bec.)
แนะนำอ่องปะภานน์ but. ไม่มีข้อบังคับ

Types of sequential circuits

► A **feedback sequential circuit**

ຮຽນຕາ

- Use ordinary gates and feedback loops to obtain memory in a logic circuit, thereby creating sequential-circuit building blocks such as **latches & Flip-flops** that are used in **higher-level designs**

ໄດ້ຮັບ

► A **clocked synchronous state machine**

ວຽກທີ່ຈໍາສັນ CLK ເປັນນັກ (ຄວບຖຸນກ.ທ່າງວານ) ໂດຍກ່າວໄປເປັນ **edge-trigger** (ກ.ພລືບນະສານະ ຈະເກີດຂຶ້ນທີ່ຂອບຂອງ signal)

- Use **edge-triggered D flip-flops** to create circuits whose inputs are examined and whose outputs change in accordance with a controlling clock signal.

ກໍາຕານາຍະເປົ້ານ state ?

ຕາມນັ່ງ

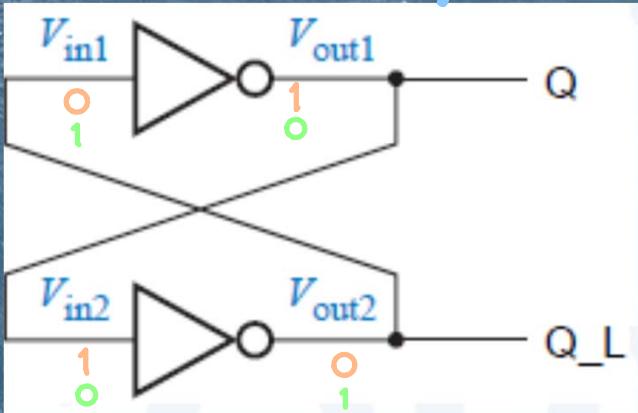
"feed output ຂາເປັນinput ໃນວິ"

ວຽກຮຽນຮູມຕາທີ່ສ່ວນໃນນີ້ signal feed ກັບໄປຈຳນວນລົງ ຈາກ output feed ໄດ້input ໃນວິ ເພື່ອໃນຄວາມຢູ່ໃນສະການໄດ້ສາມານ໌ໜັ້ງໄລ້ Ex. r-s, latch, FF, D,J-K

▷ សមតុលយោគ់វត្ថុ (digital binary)

Bistable Elements (រួចរាល់រាយការណ៍)

ផ្តល់ $Q = Q_{-L} = 1 \Rightarrow$ ដឹងថ្មីណា bec. $Q \neq Q_{-L}$



V _{in1}	Q	Q _{-L}
0	1	0
1	0	1

► The simplest sequential circuit

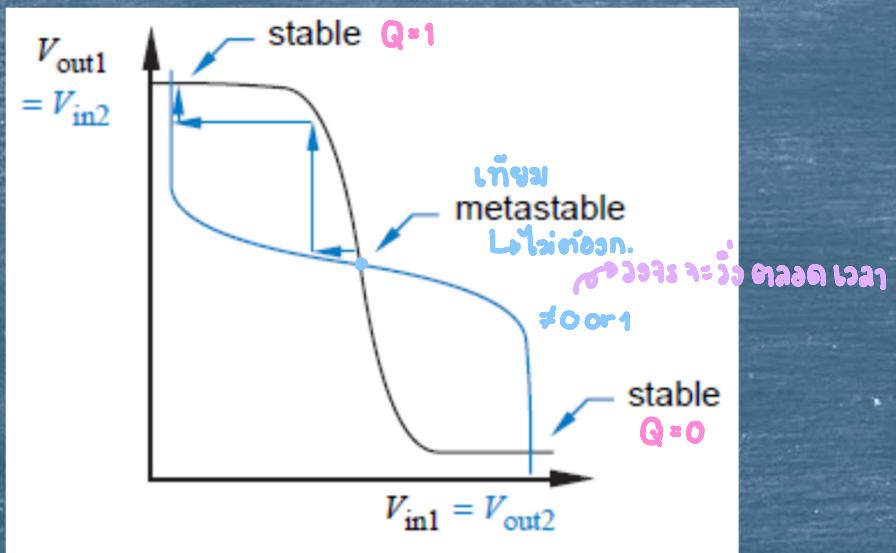
► No inputs and has two outputs,
Q and Q-L

► Describe the state of the circuit
using only Q; **Q = 0 or Q = 1**



Key: និងបង្កើរាយការណ៍ / រាយការណ៍

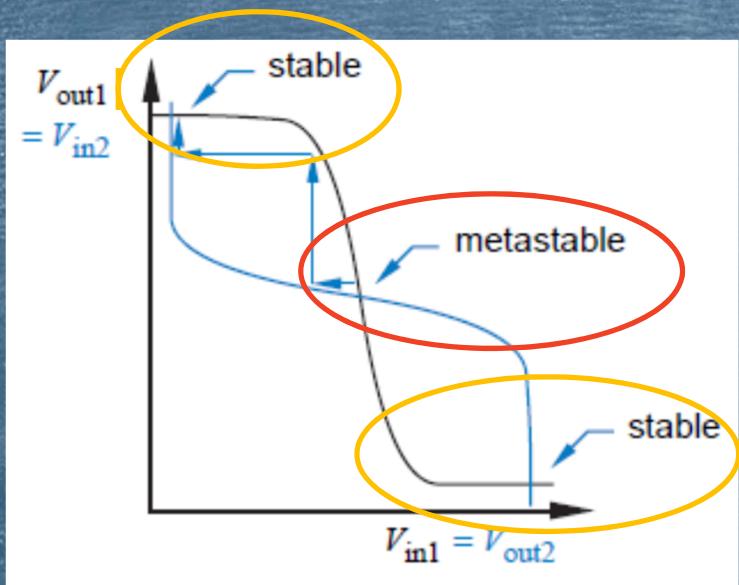
Bistable Elements (Analog Analysis)



$$\begin{aligned}V_{in1} &= V_{out2} \\&= T(V_{in2}) \text{ transfer f.} \\&= T(V_{out1}) \\&= T(T(V_{in1}))\end{aligned}$$

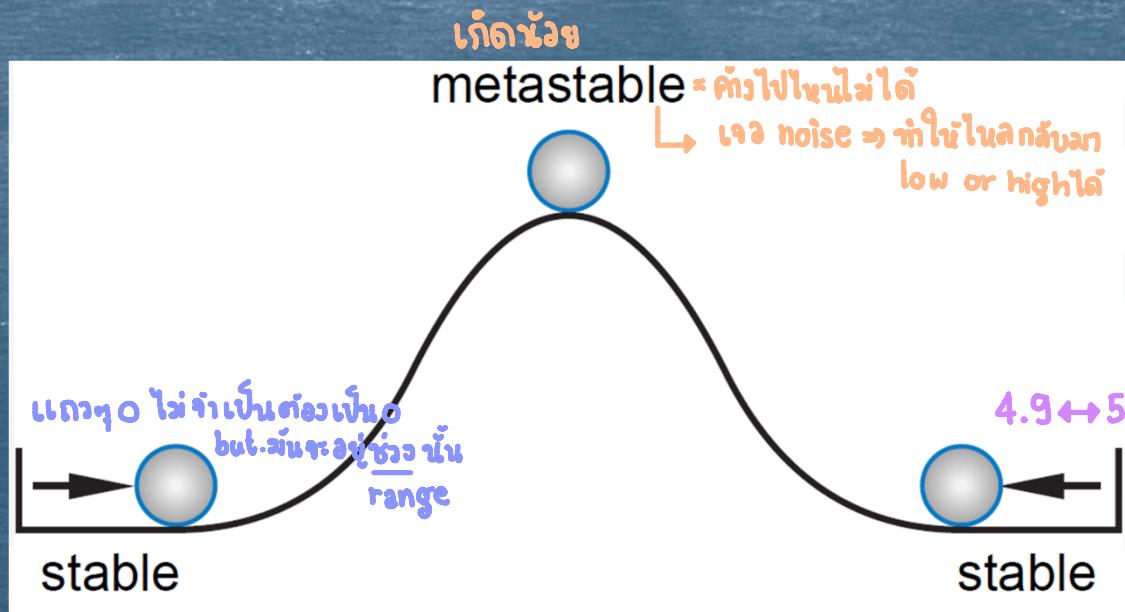
$$V_{in2} = T(T(V_{in2}))$$

Bistable Elements (Analog Analysis)



- ▶ Three equilibrium points
 - ▶ Two **stable** points
 - ▶ One **metastable**

Bistable Elements (Metastable Behavior)

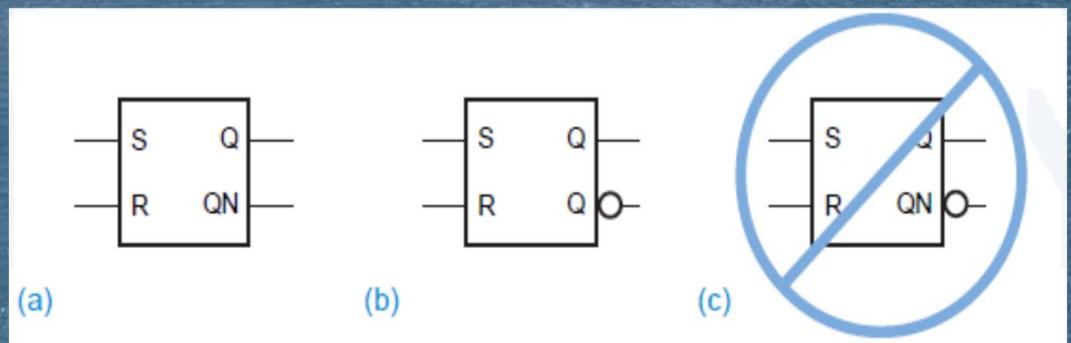
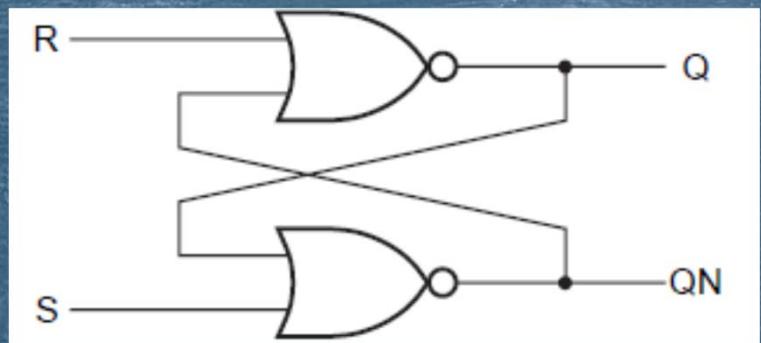


Flip-Flops and Latches

- ▶ **flip-flop** ⇒ មីត្រ clock ការណន៍ទំនួលភាពការងារ
- ▶ A sequential device that normally samples its inputs and changes its outputs only at times determined by **a clocking signal**
- ▶ **Latch** ⇒ មីត្រ clock
- ▶ A sequential device that watches all of its inputs continuously and changes its output at any time, **independent of a clocking signal**
⇒ គឺជា Computer ឬវឌ្ឍន៍ analog

ກຳນົດເປັນ 1 ກຳນົດເປັນ 0

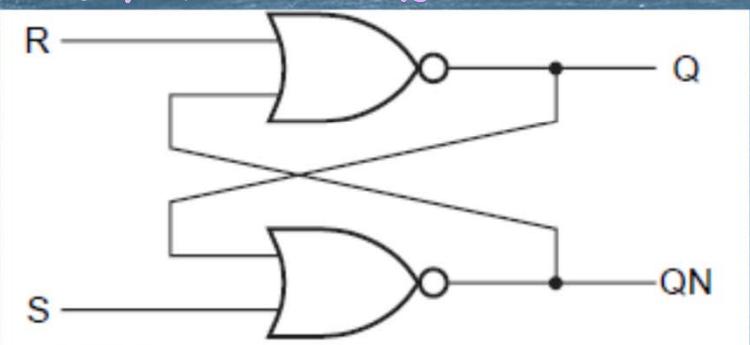
S-R (set – reset) Latch



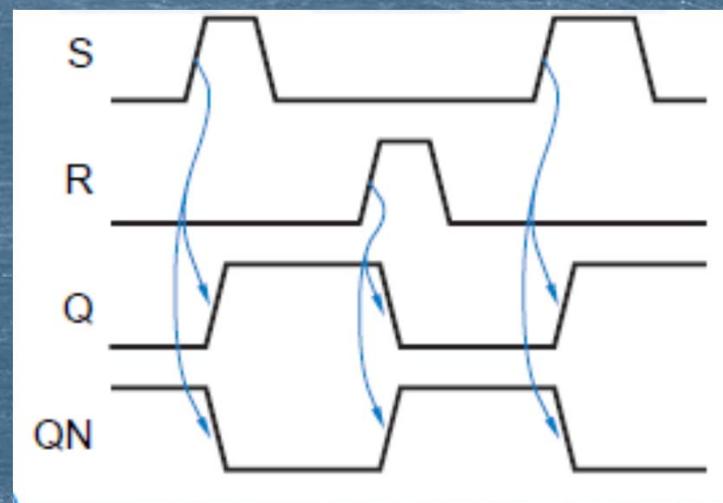
Circuit design using
NOR gates

Symbols for an SR latch

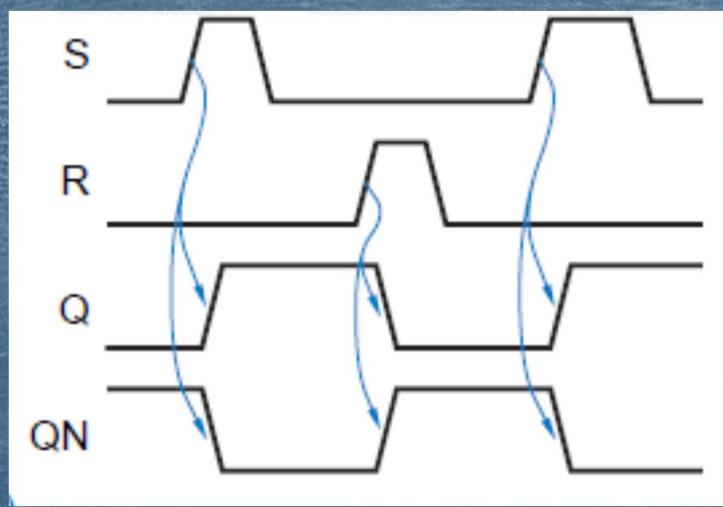
$\text{if } S = R = 1 \Rightarrow \text{Indeterminate}$



Circuit design using
NOR gates



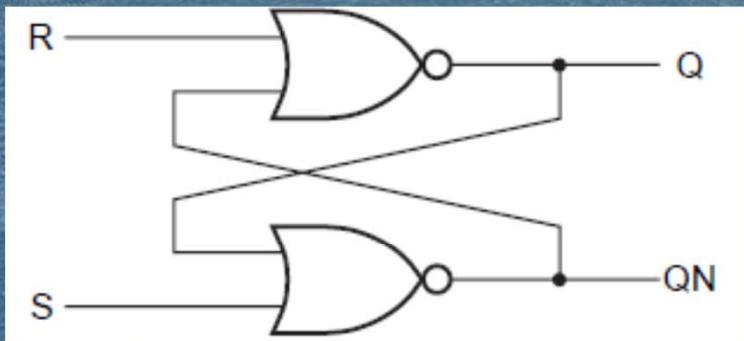
Typical operation of
an SR latch with
normal inputs



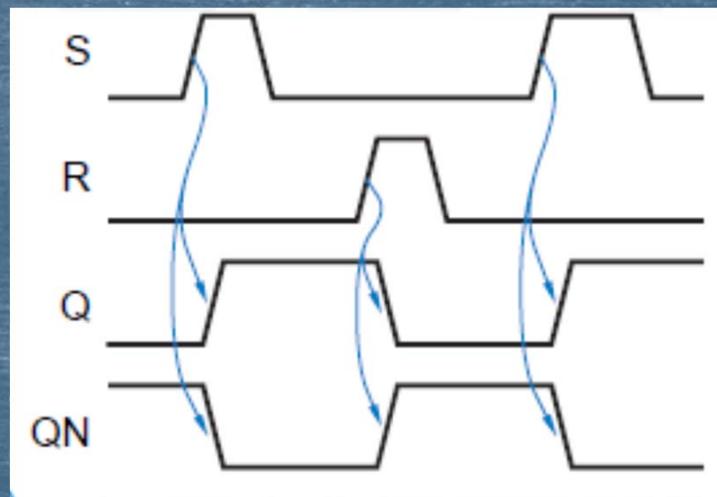
Typical operation of
an SR latch with
normal inputs

S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

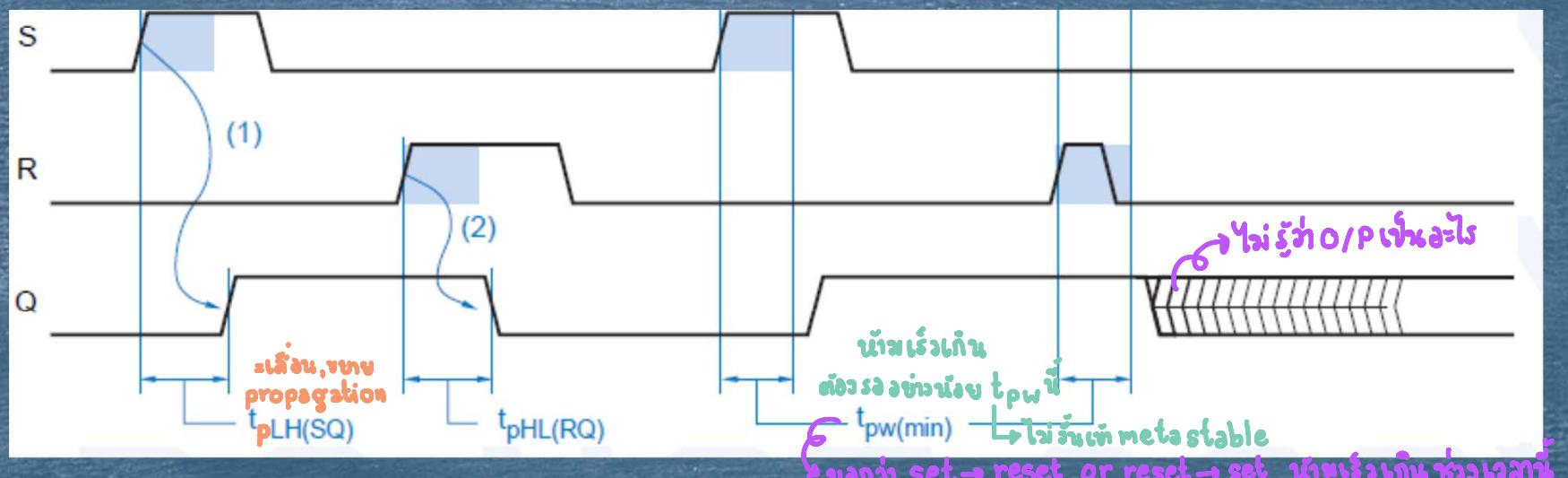
Function table



Circuit design using
NOR gates



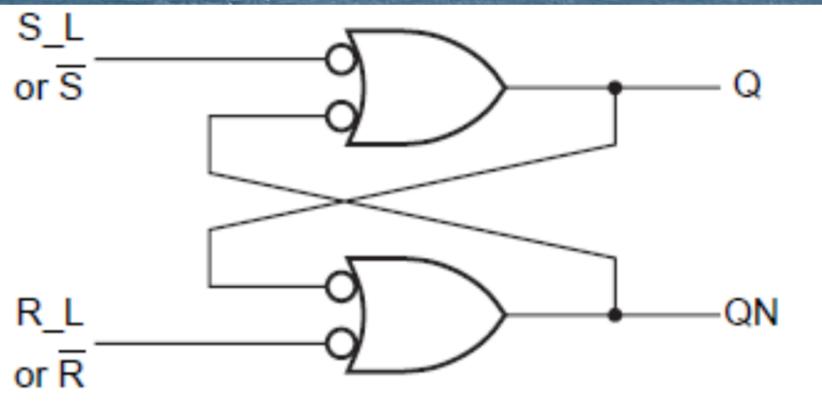
Typical operation of
an SR latch with
normal inputs



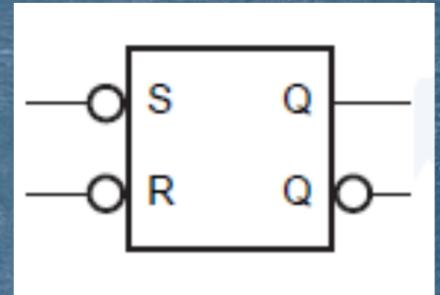
Timing parameters for an SR latch

t_p : propagation delay

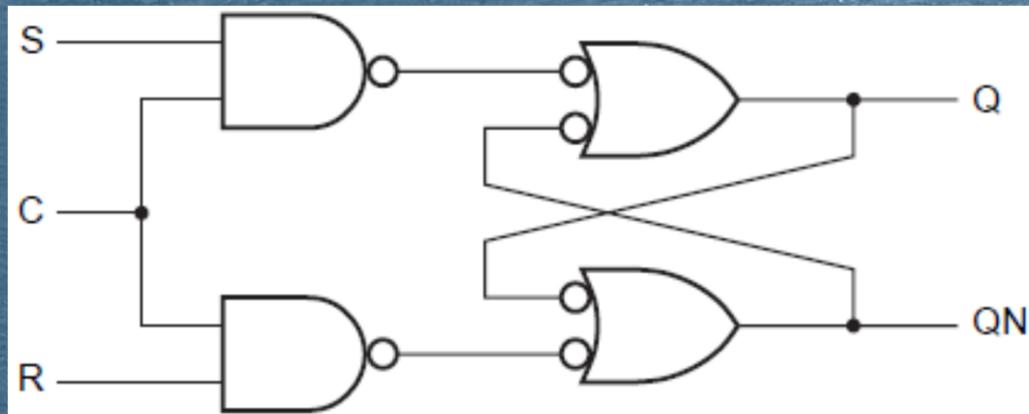
$\bar{S}\bar{R}$ (S-bar-R-bar) Latch



S_L	R_L	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	lastQ	lastQN

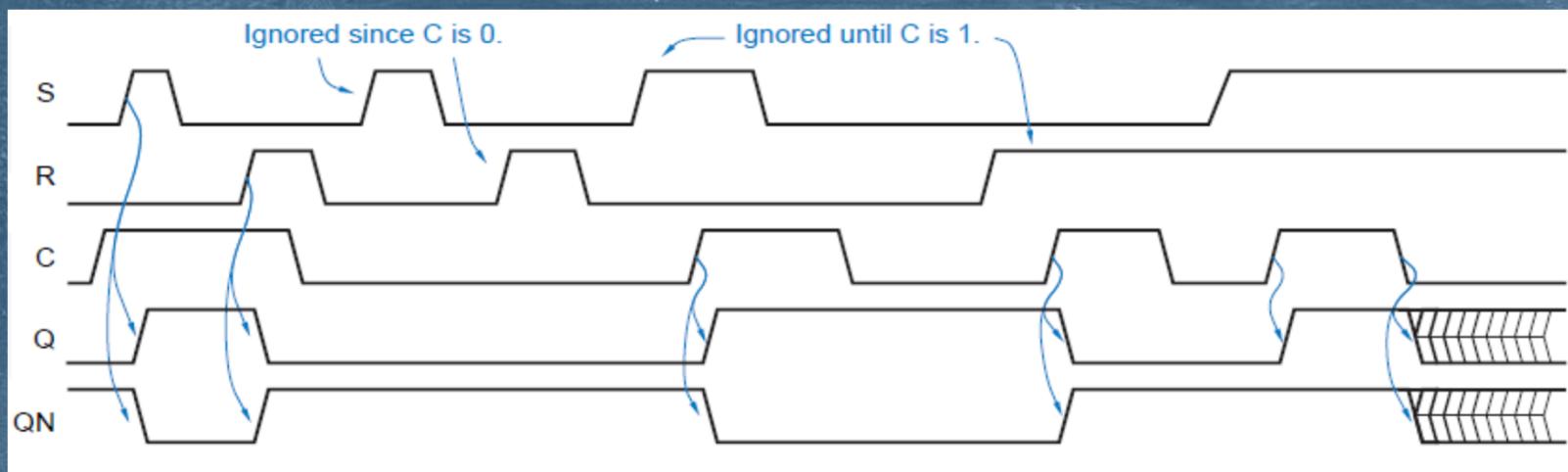
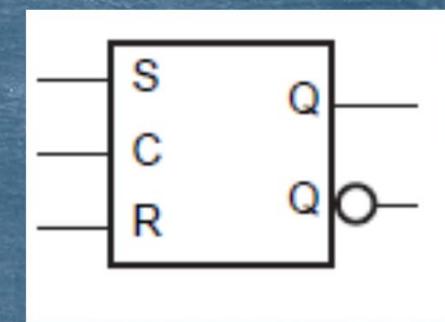


S-R Latch with Enable

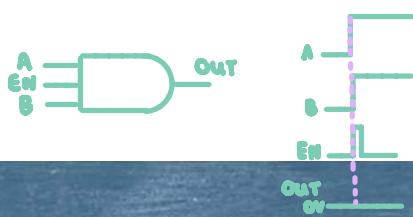


Control = EN (Enable)

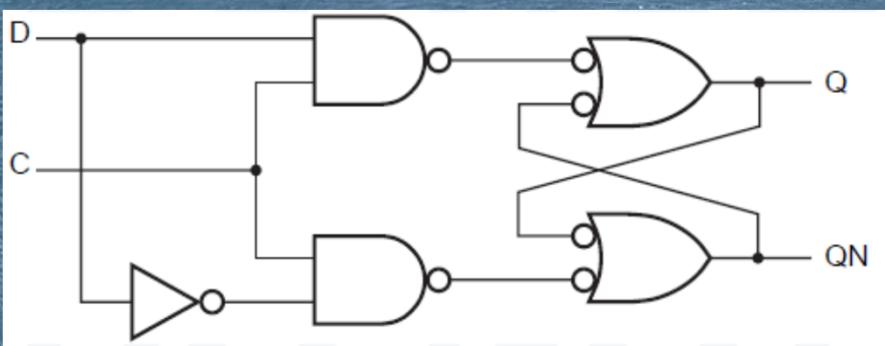
S	R	C	Q	QN
0	0	1	lastQ	lastQN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	lastQ	lastQN



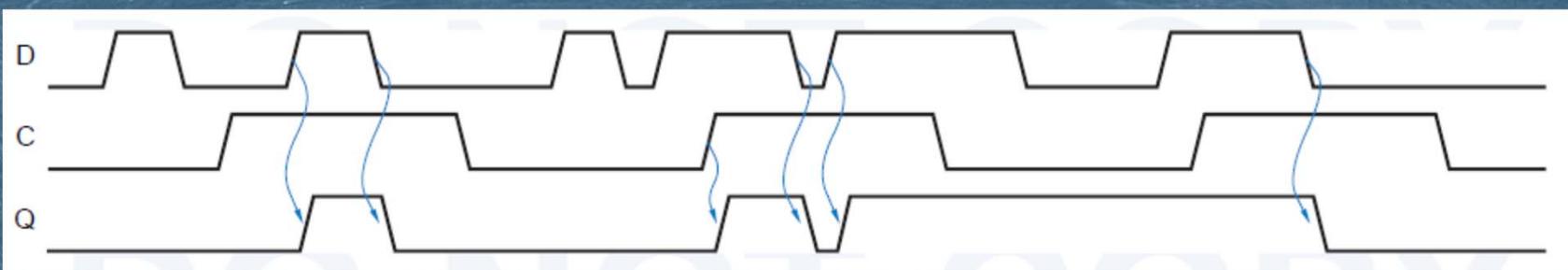
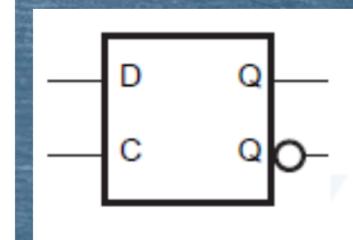
timing diagram օօնլիւ (S-R latch / J-K)



D Latch \Rightarrow เก็บข้อมูล
Ex. แบบ register ของ com

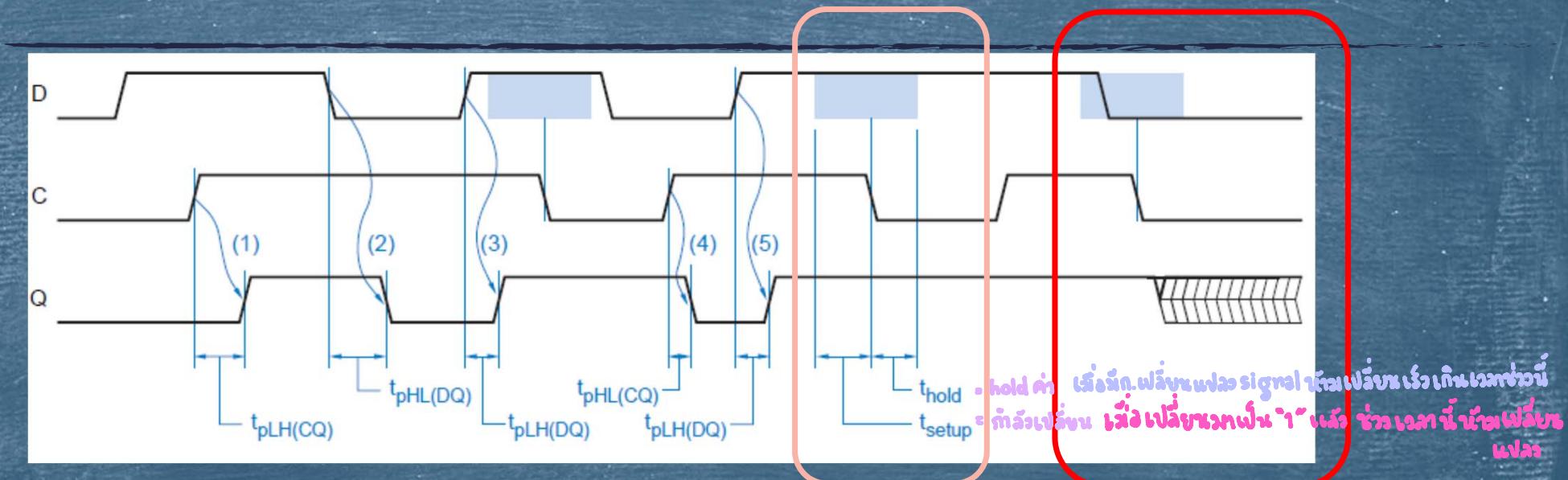


C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	lastQ	lastQN



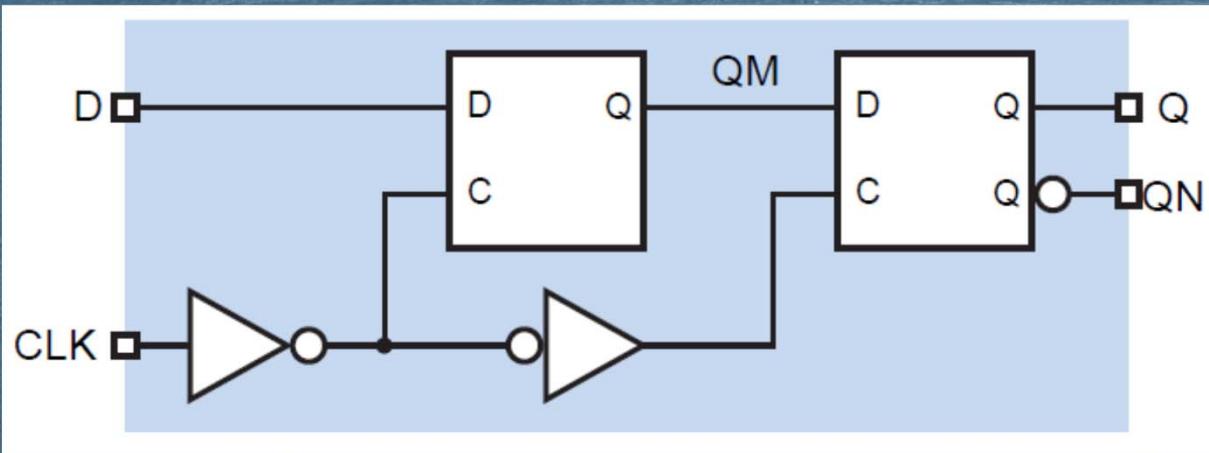
C : sometimes named ENABLE, CLK, G,
and is active "low" in some D-latch designs

D Latch (Timing parameters)

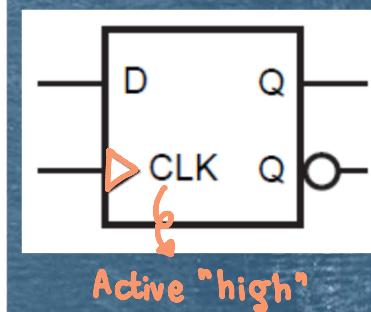


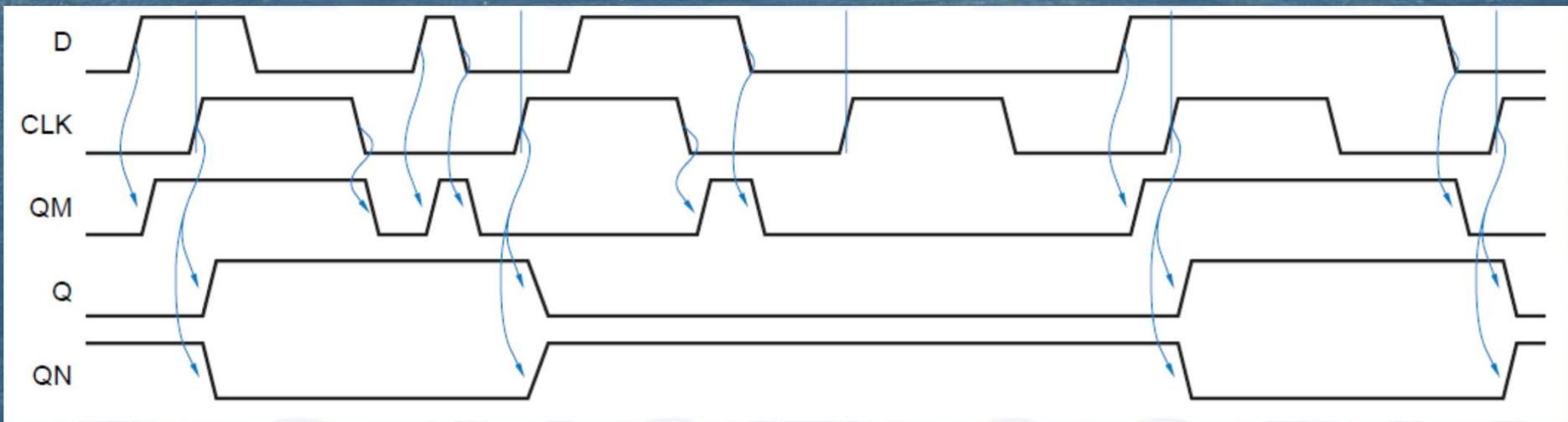
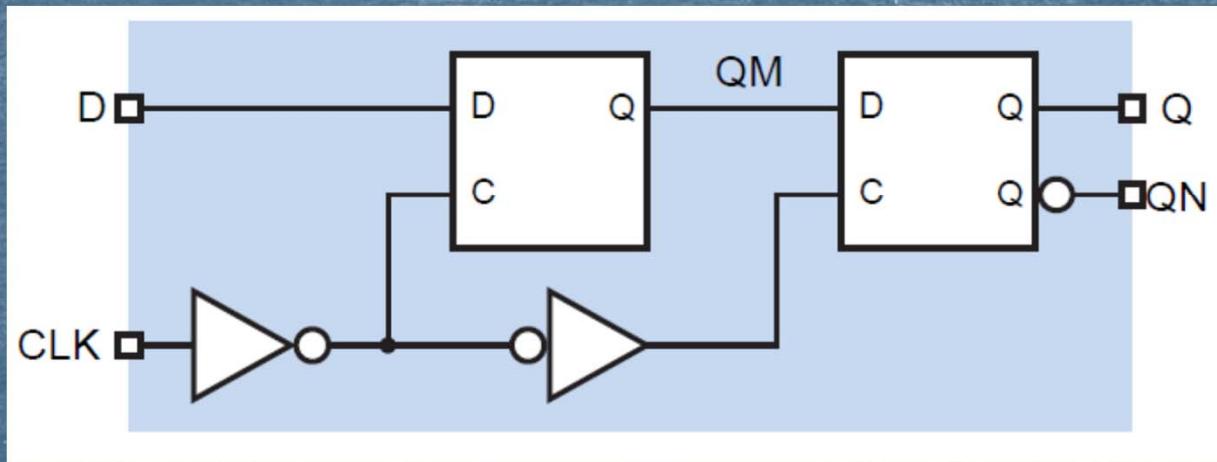
- D latch eliminates the **$S=R=1$ problem** of the S-R latch.
- D latch does **NOT** eliminate the **metastability problem**.
- The input must not change during the t_{setup} (setup time) and t_{hold} (hold time); otherwise, the output of the latch is unpredictable and may become metastable.

Edge-triggered D Flip-Flop



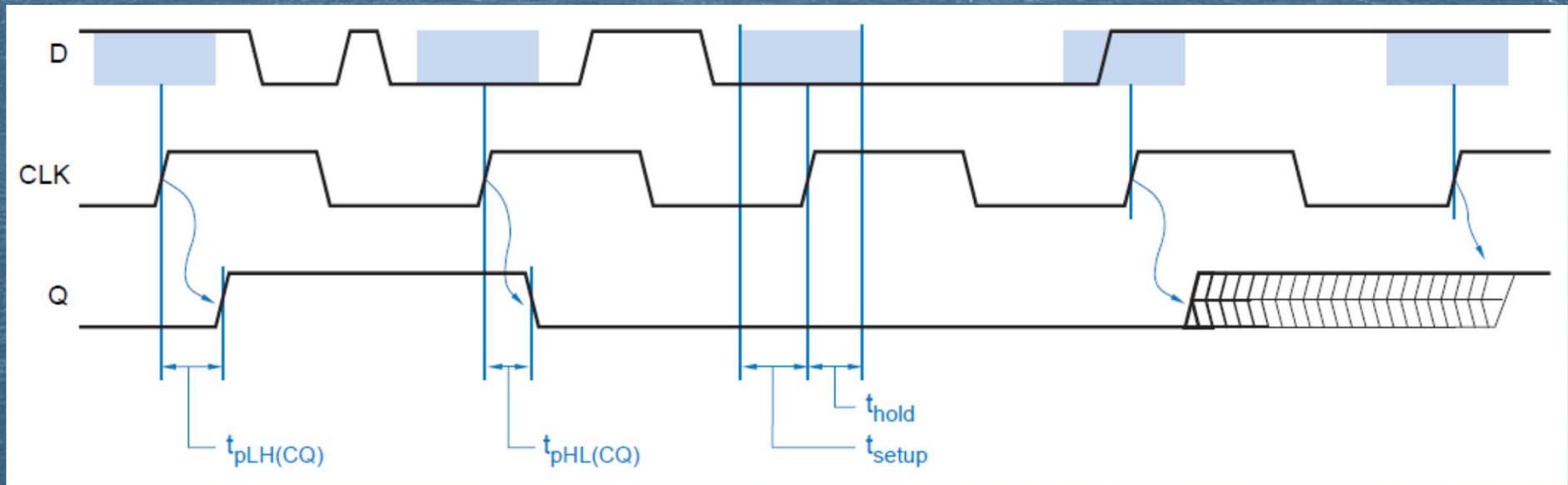
D	CLK	Q	QN
0	0	0	1
1	1	1	0
x	0	last Q	last Q N
x	1	last Q	last Q N



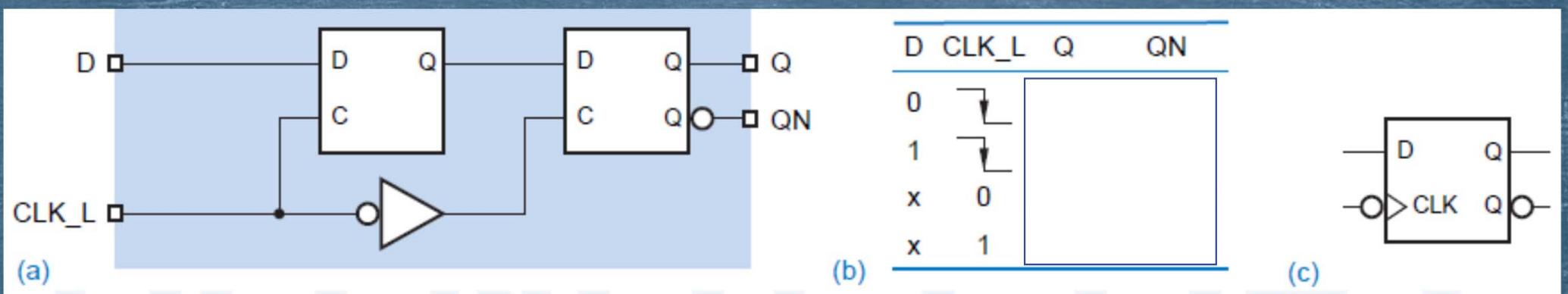


มี delay มาเก็บข้อมูล

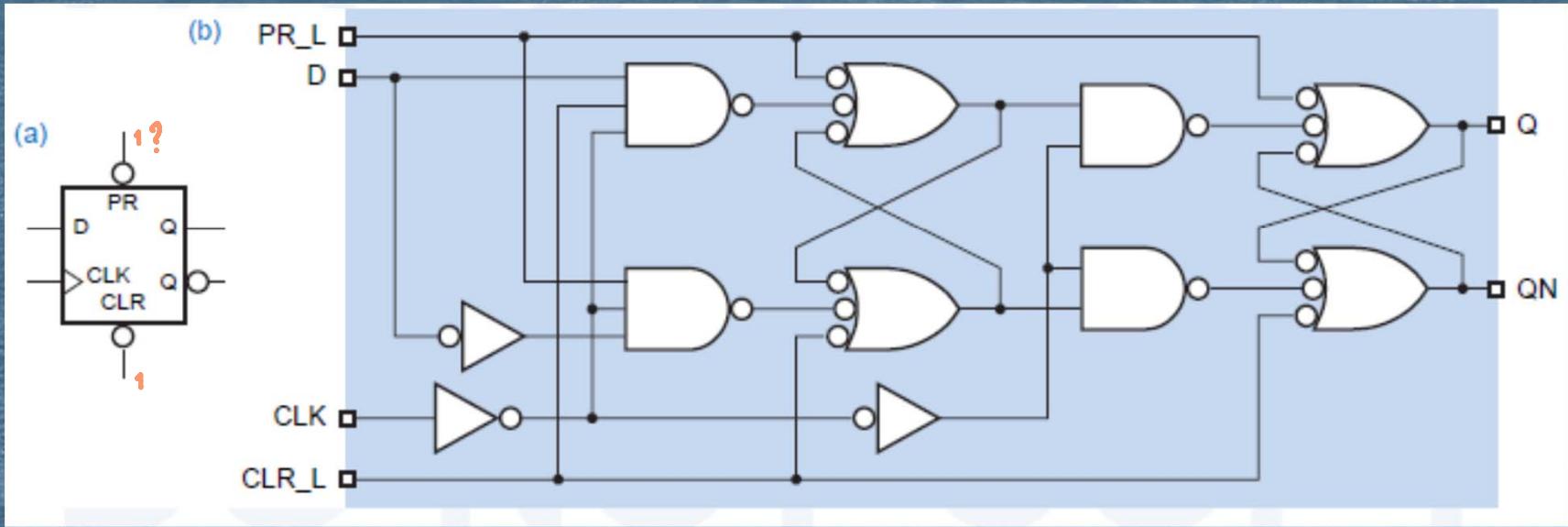
timing diagram
⇒ មួយໄក់តែងមែន delay



Timing behavior of a positive-edge-triggered D flip-flop

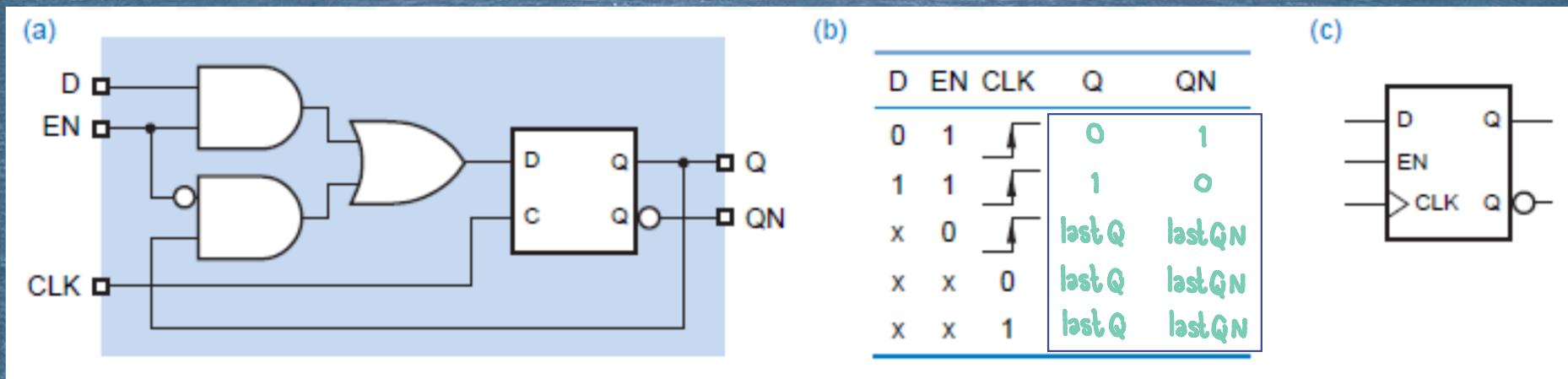


Timing behavior of a negative-edge-triggered D flip-flop



- Some D flip-flops have **bi-directional I/P** **asynchronous I/P** that may be used to force the flip-flop to a particular state independent of the CLK and D inputs.
- PR (preset) & CLR (clear)** behave like the **set & reset** inputs on an SR latch.

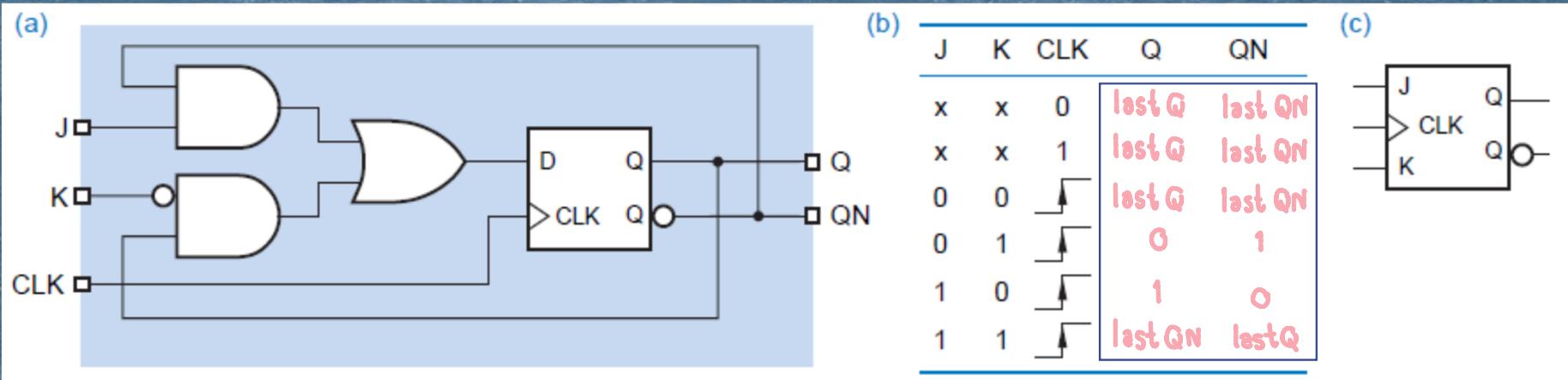
Edge-triggered D Flip-Flop with Enable



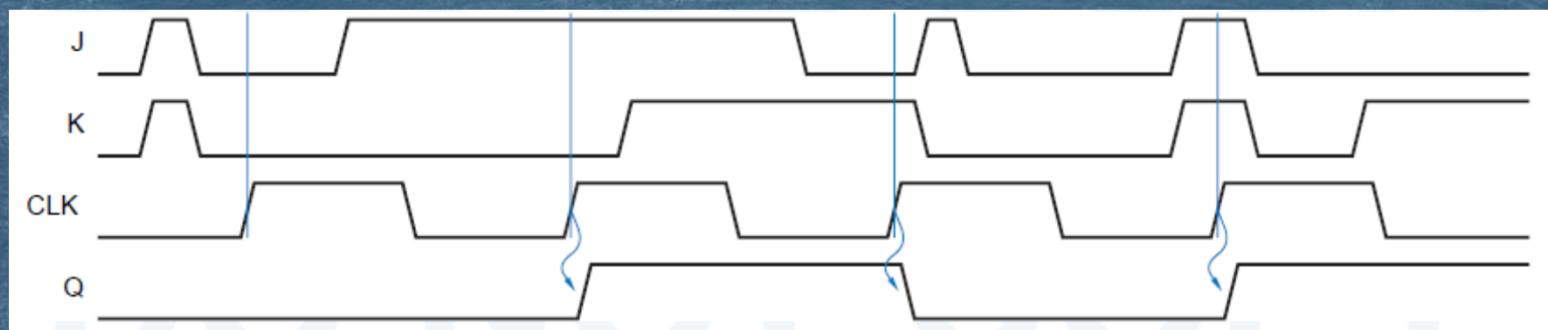
Positive-edge-triggered D flip-flop with enable:
(a) circuit design; (b) function table; (c) logic symbol

EN (enable input) or CE (clock enable)

Edge-triggered J-K Flip-Flop



Edge-triggered J-K flip-flop:
(a) equivalent function using an edge-triggered D flip-flop; (b) function table; (c) logic symbol

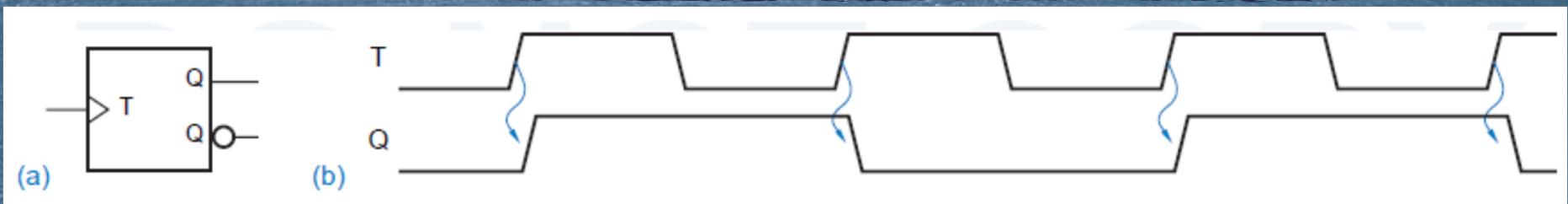


Functional behavior of a positive-edge-triggered J-K flip-flop

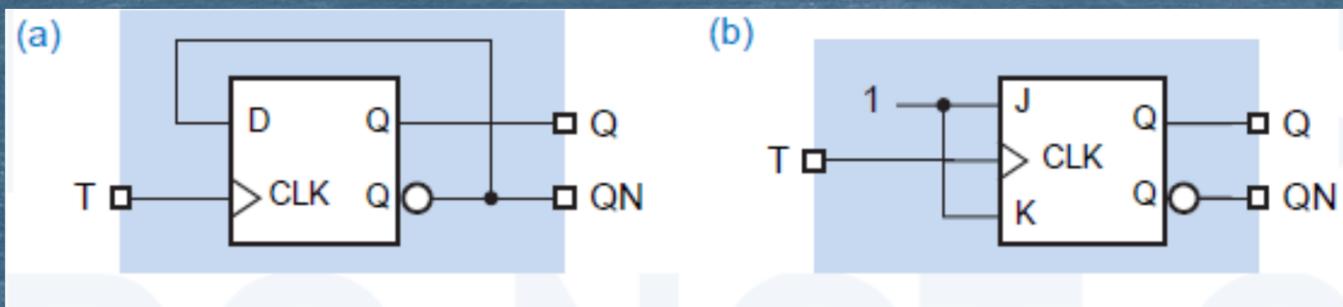
ກລັນຫວາງ

T (toggle) Flip-Flop

↳ ຕໍ່ມານ divider

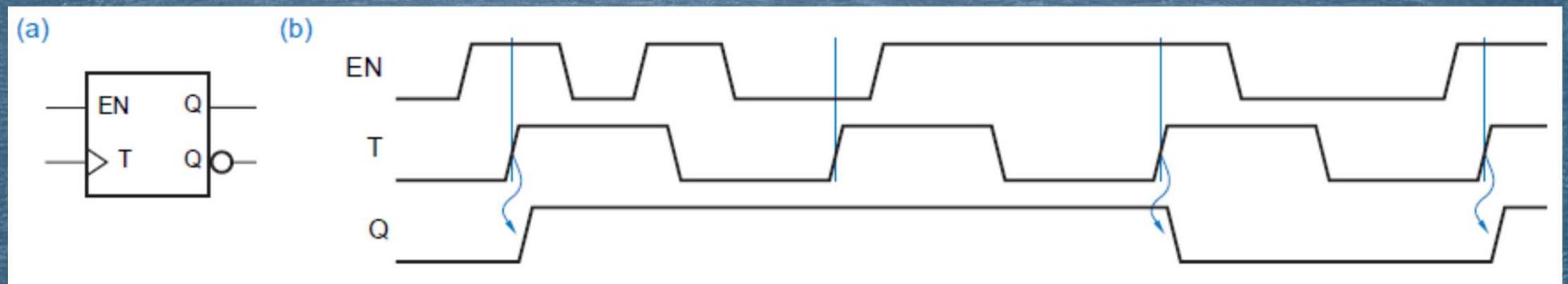


Positive-edge-triggered T flip-flop: (a) logic symbol; (b) function behavior



Possible circuit designs for a T flip-flop : (a) using a D flip-flop; (b) using a J-K flip-flop

T Flip-Flop with Enable



Positive-edge-triggered T flip-flop with enable:
(a) logic symbol; (b) functional behavior

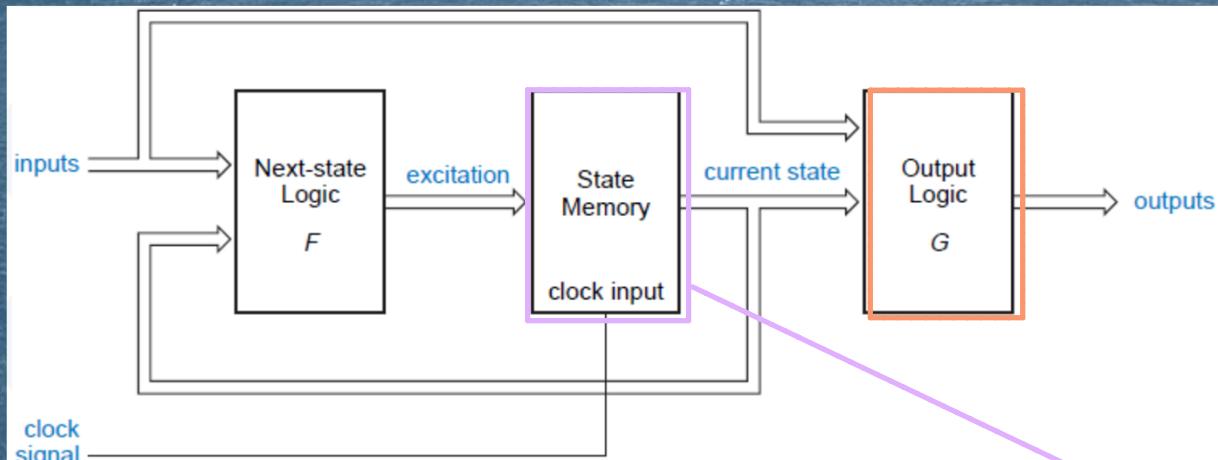
Clocked Synchronous State-Machine Analysis

State machine : a generic name given to these sequential circuit

Synchronous : all flip-flops use the
Same clock signal

Clocked : refers to the fact that
their storage elements employ a
clock I/P

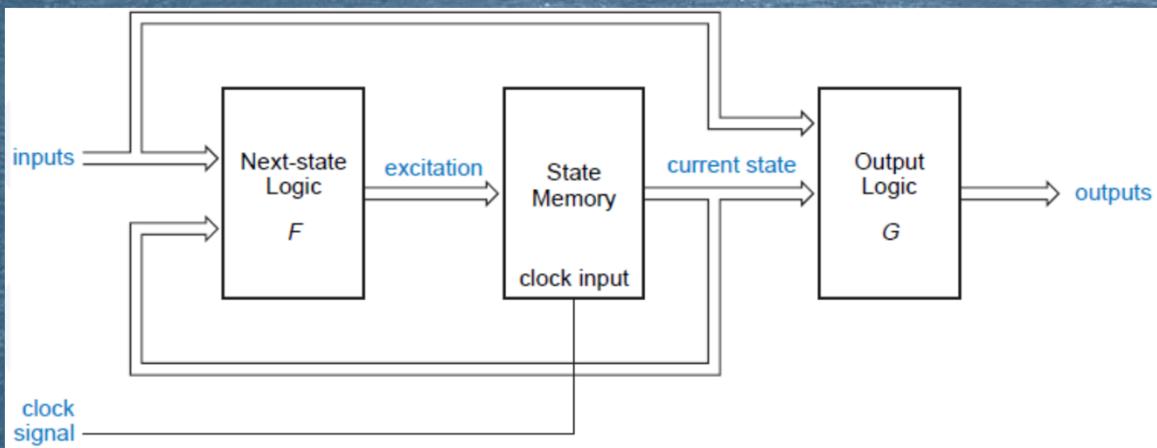
State-Machine Structure



Clocked synchronous state-machine structure

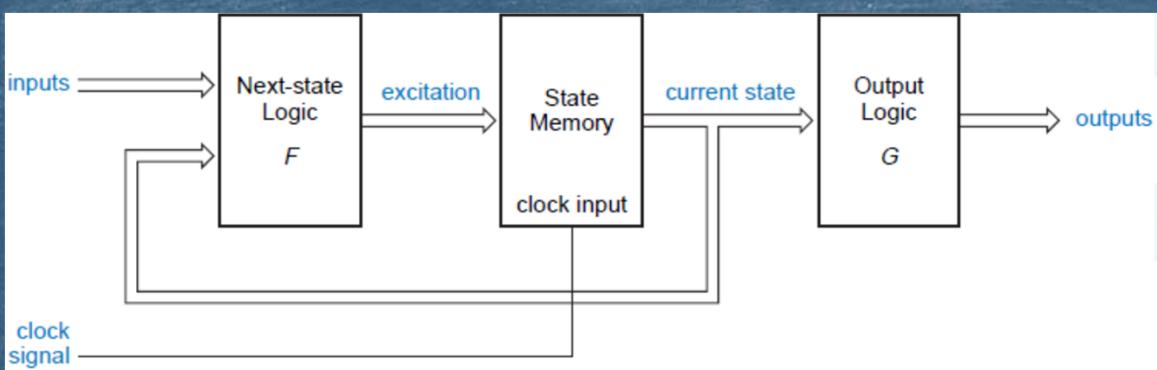
A set of n flip flop that store the current state of the machine and has 2^n distinct state

Output Logic



รูปนี้ก็คือ

Mealy machine :
O/P depends on both state and input



Moore machine :

O/P depends on state done
(state วิ่ง.)

Q & A