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01076244 Advanced Digital System Design

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State-Machine Structure

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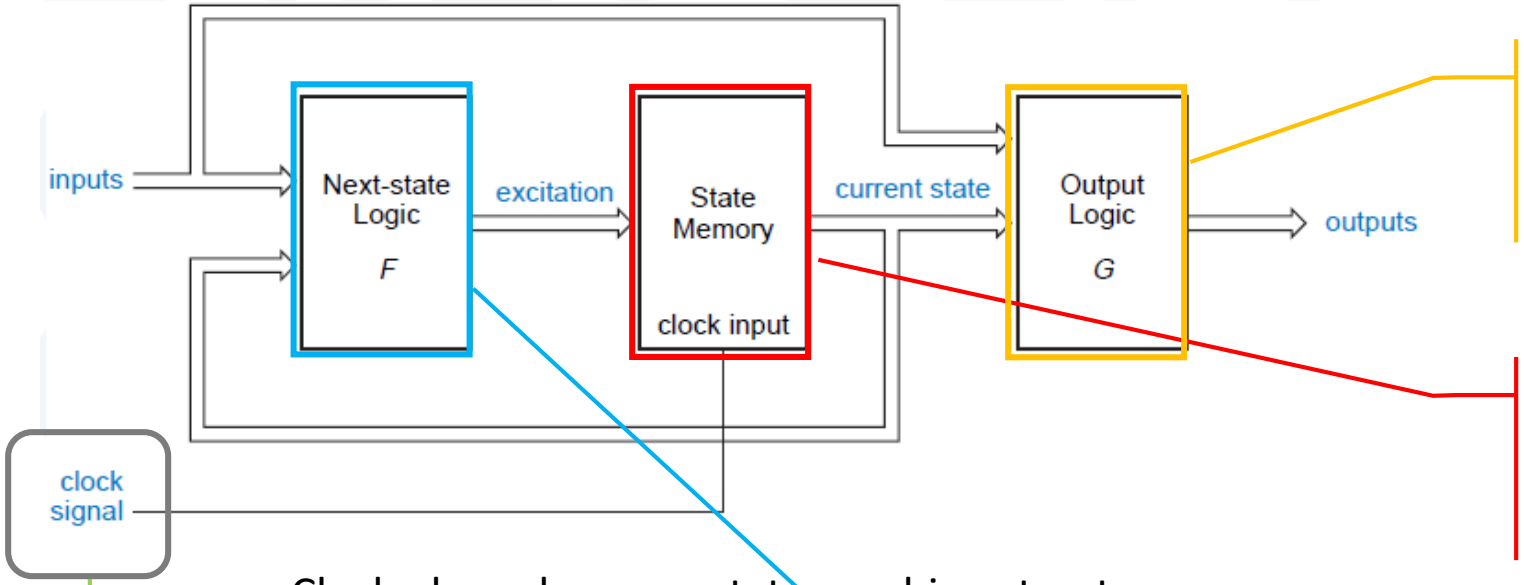

Clocked synchronous state-machine structure

The output logic G determines the output as a function of the current state and input

A set of *n* flip-flops that store the current state of the machine and has 2^n distinct states

A common clock signal that causes the flip-flops to change state at each *tick* of the clock

A function of the current state and input

F and *G* are strictly combinational logic circuits.

Next state = *F (current state, input)*
Output = *G (current state, input)*

Output Logic

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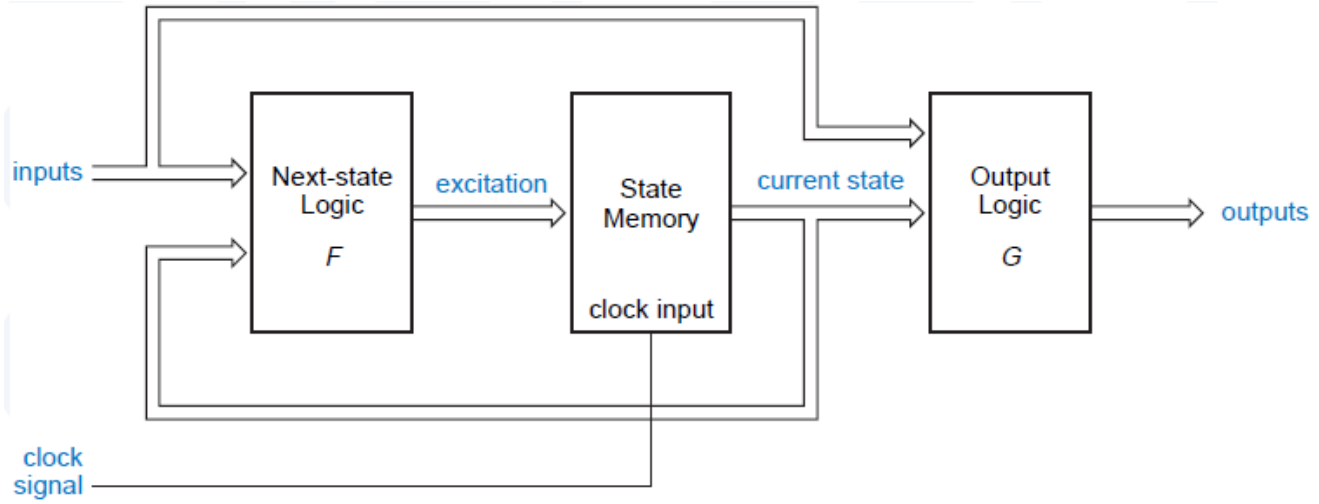
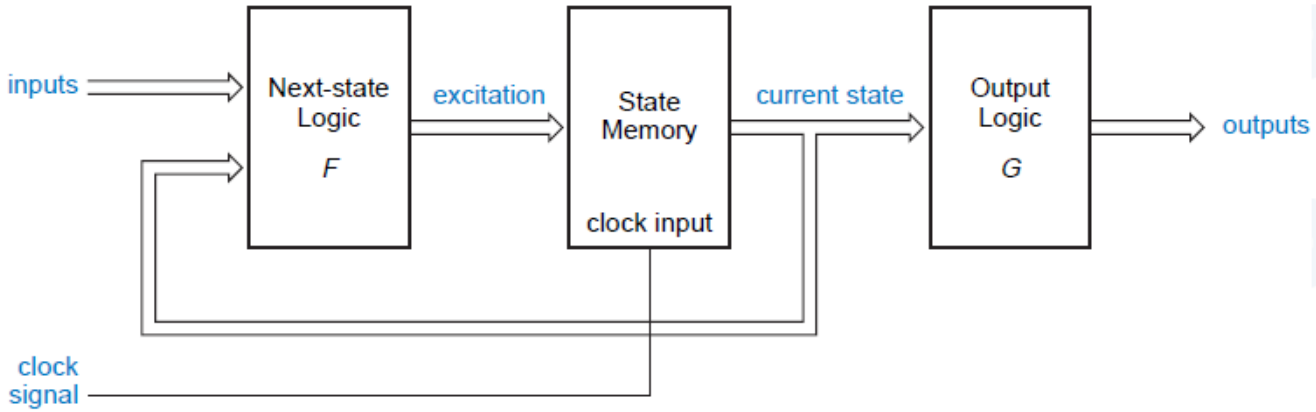


Mealy machine : output depends on both state and input



Moore machine : the output depends on state alone

Characteristic Equations

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- A _____ is a formally description of a _____
- The _____ suffix means the "_____"
- Note: the characteristic equation does not describe detailed timing behavior of the device (latching vs. edge-triggered, etc.), only _____

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Device Type	Characteristic Equation
S-R latch	$Q^* = S + R' \cdot Q$
D latch	$Q^* = D$
Edge-triggered D flip-flop	$Q^* = D$
D flip-flop with enable	$Q^* = EN \cdot D + EN' \cdot Q$
Edge-triggered J-K flip-flop	$Q^* = J \cdot Q' + K' \cdot Q$
T flip-flop	$Q^* = Q'$
T flip-flop with enable	$Q^* = EN \cdot Q' + EN' \cdot Q$

Analysis of State Machines with D Flip-Flops

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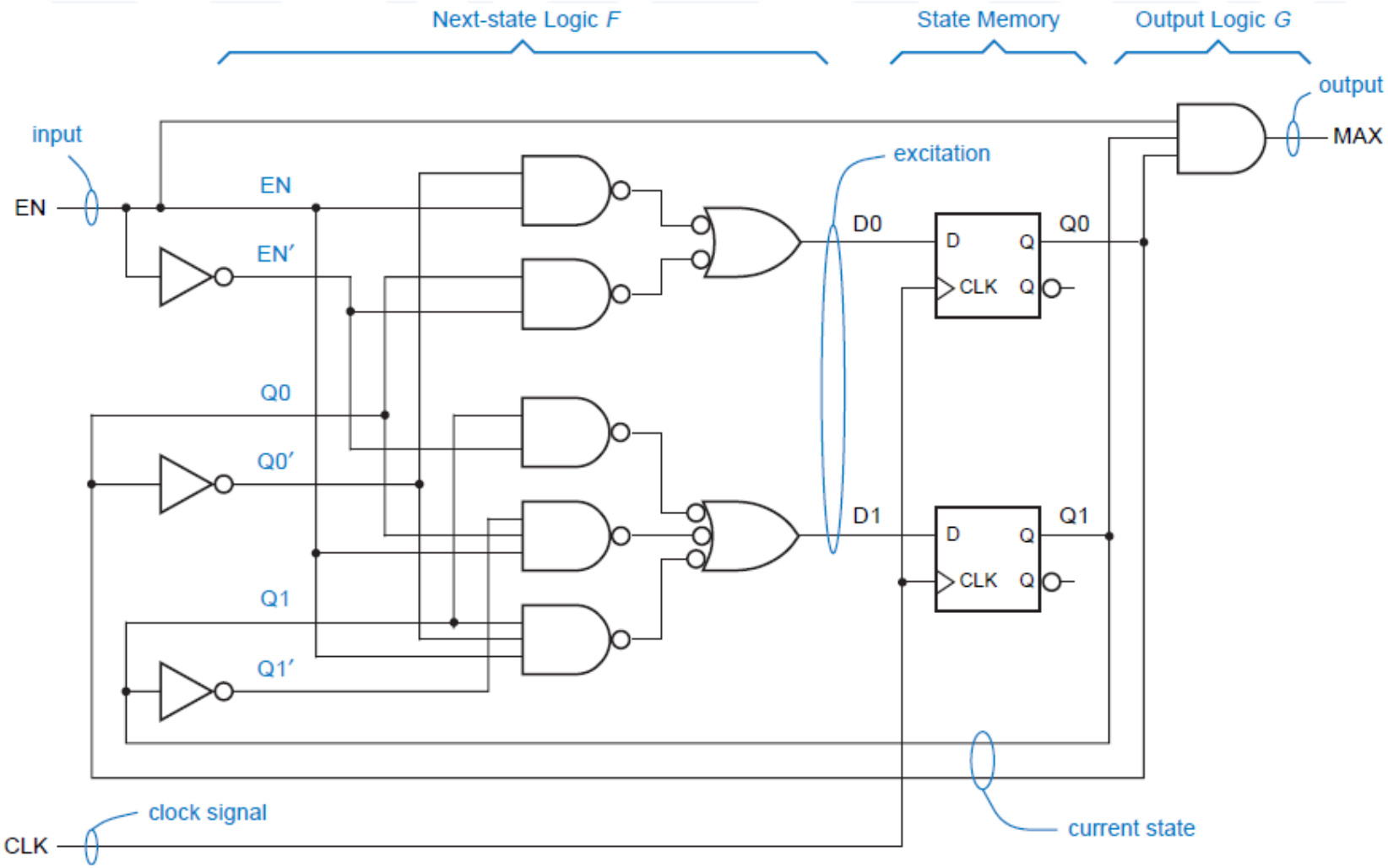
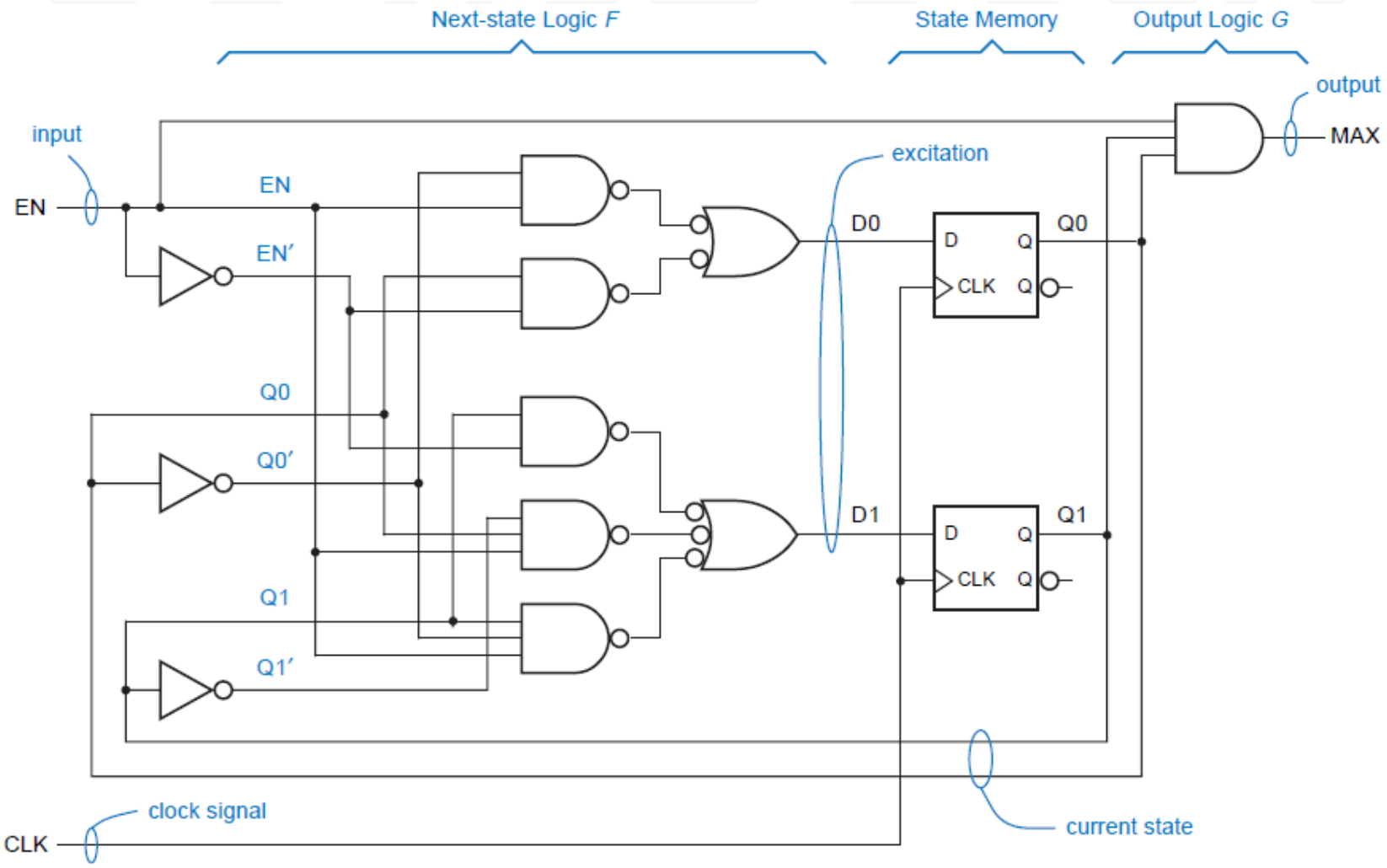
1. Determine the _____ and _____ *F* and *G*.
2. Use *F* and *G* to construct a _____ that completely specifies the _____and _____ of the circuit for every possible combination of current state and input.
3. (Optional) Draw a _____ that presents the information from the previous step in graphical form.



D0 =

D1 =

Clocked synchronous state machine using positive-edge-triggered D flip-flops

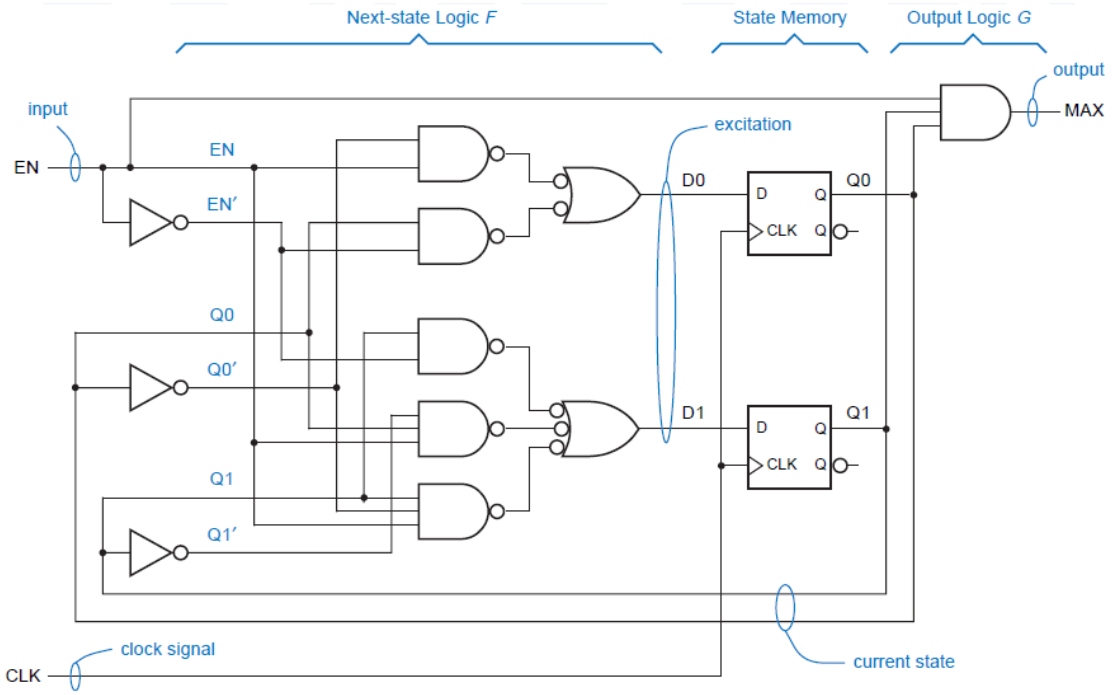


Clocked synchronous state machine using positive-edge-triggered D flip-flops

The _____ _____after a clock tick is denoted by _____ _____ to the state-variable name.

Q0* =
Q1* =

Q0* =
Q1* =



Clocked synchronous state machine using positive-edge-triggered D flip-flops

Q1 Q0	EN	
	0	1
0 0		
0 1		
1 0		
1 1		
	Q1* Q0*	

Transition table

S	EN	
	0	1
A		
B		
C		
D		
	S* , MAX	

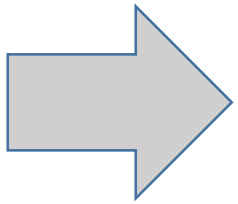
State/output table

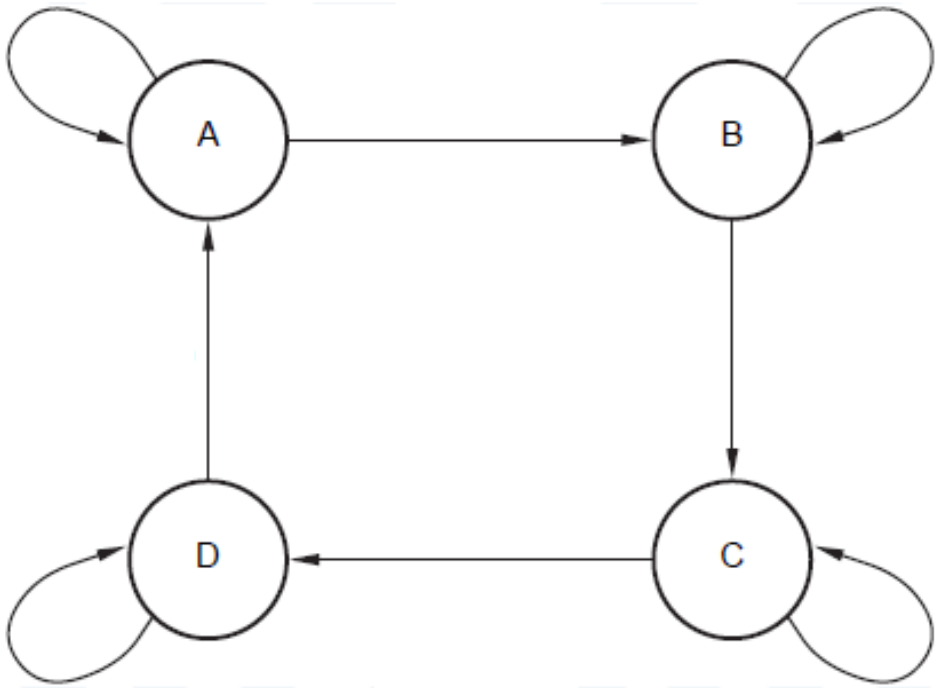
S	EN	
	0	1
A		
B		
C		
D		
	S*	

State table

S	EN	
	0	1
A	A , 0	B , 0
B	B , 0	C , 0
C	C , 0	D , 0
D	D , 0	A , 1
	S* , MAX	

State/output table





State diagram

- A __ presents the information from the in a graphical format.
- A circle (or) for each state.
- An arrow (or) for each transition.

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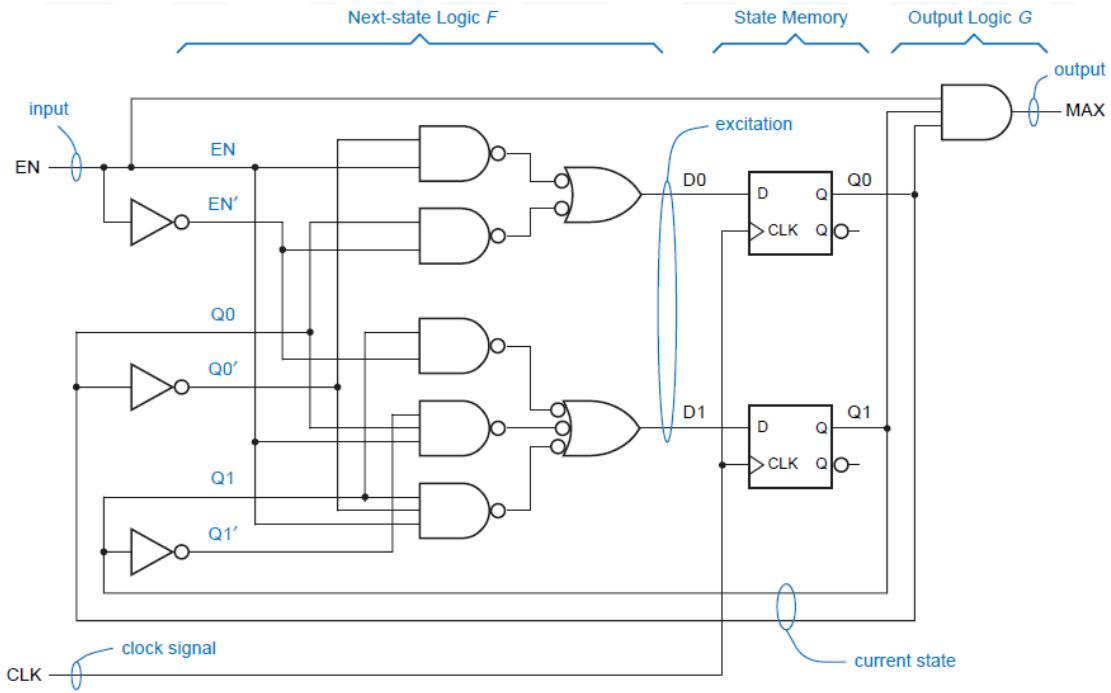
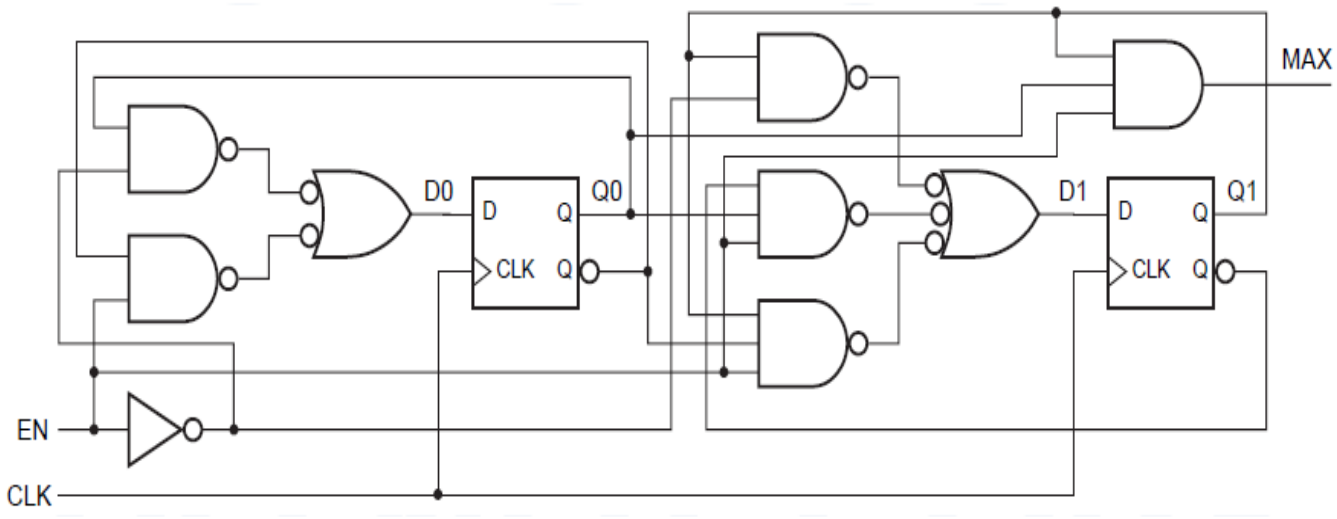
Redrawn



Clocked synchronous state machine using positive-edge-triggered D flip-flops



Redrawn logic diagram for a clocked synchronous state machine

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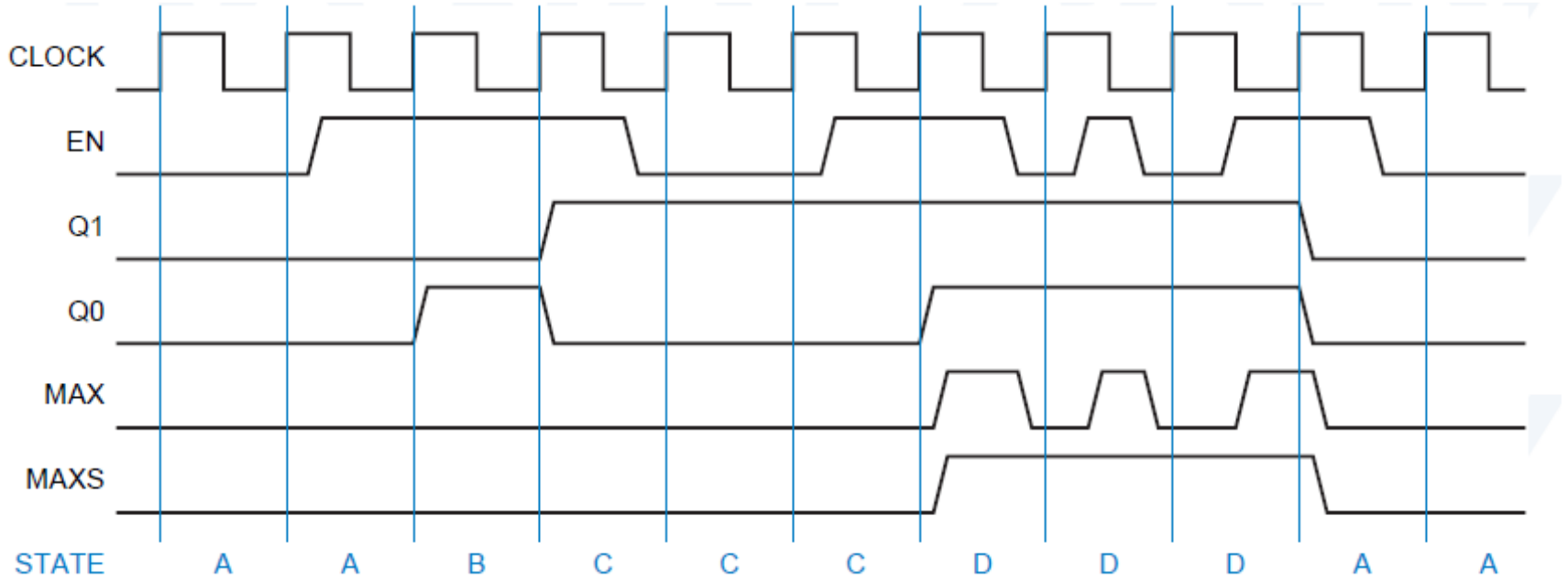
S	EN	
	0	1
A	A , 0	B , 0
B	B , 0	C , 0
C	C , 0	D , 0
D	D , 0	A , 1
	S* , MAX	



MAX = Q1·Q0·EN

Timing diagram for example state machine

Summarizing detailed steps for analyzing a clocked synchronous state machine

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1. Determine _____for the flip-flop control inputs.
2. _____ the excitation equations into the flip-flop characteristic equations to obtain transition equations.
3. Use the _____to construct a transition table.
4. Determine the _____.
5. Add _____to the transition table for each state (Moore) or _____ _____(Mealy) to create a transition/output table.
6. _____and _____ for state-variable combinations in the transition/output table to obtain a state/output table.
7. (Optional) Draw a state diagram corresponding to the state/output table.

Another example

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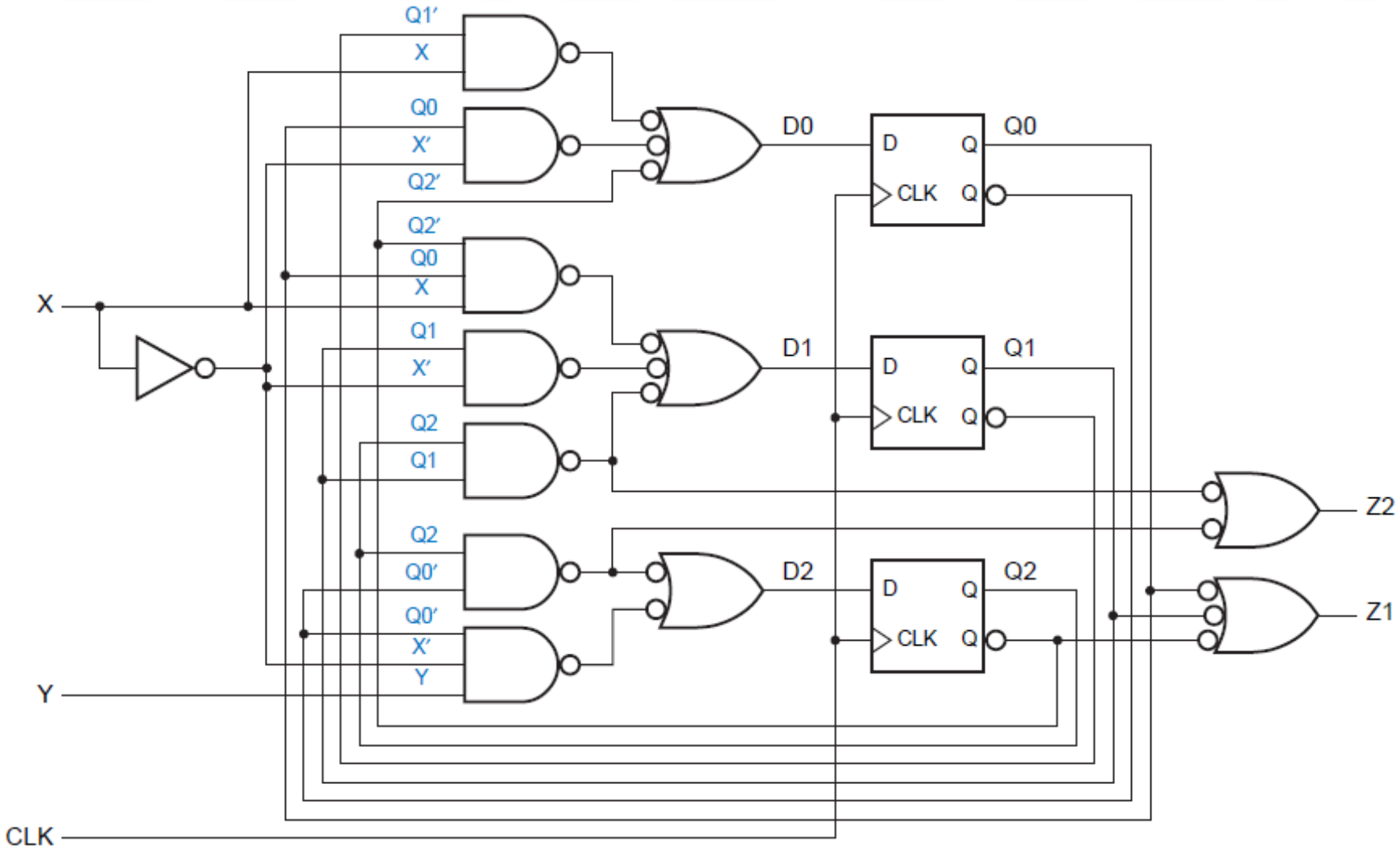

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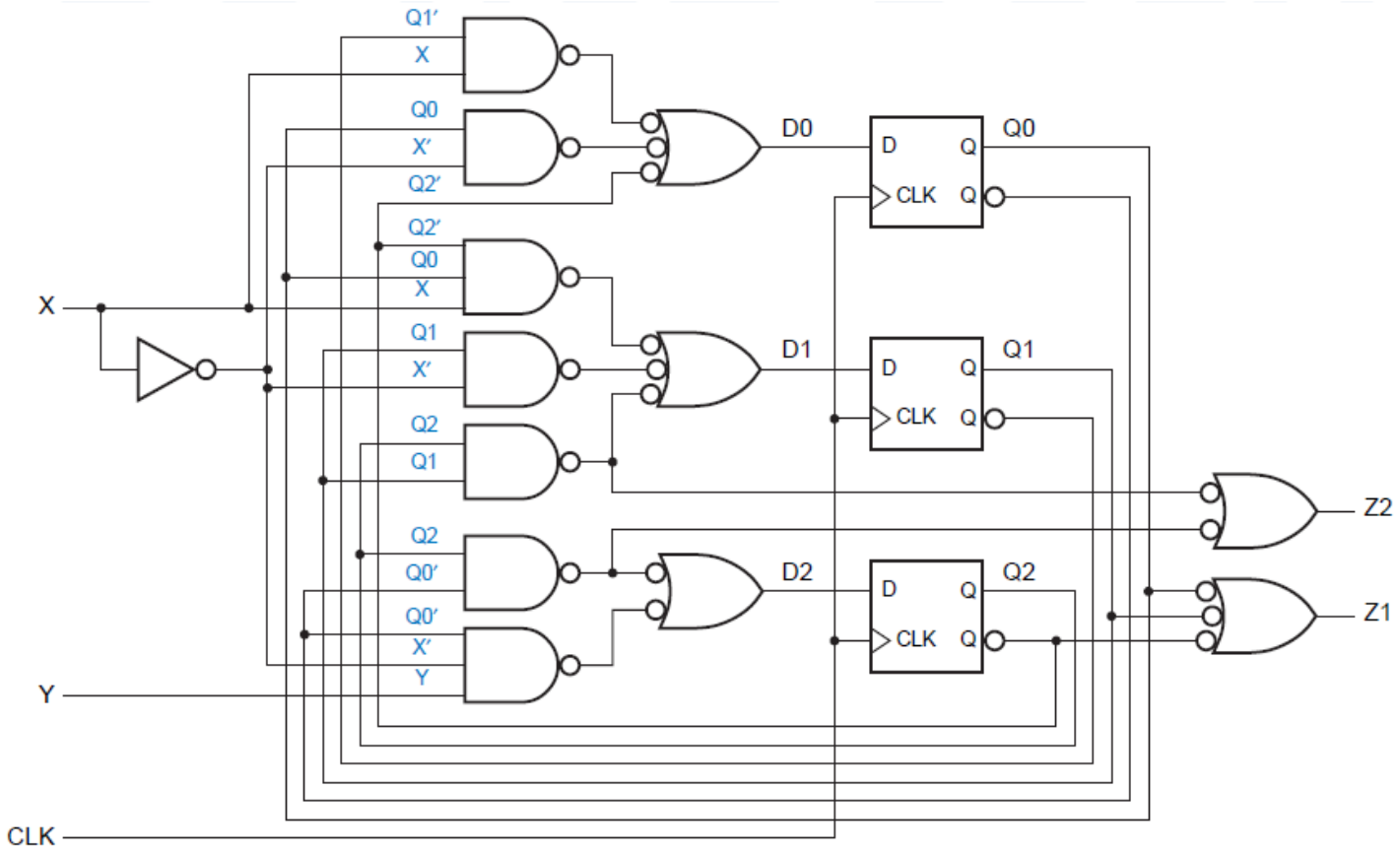

The excitation equations are :

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$$Q0^* = Q1'\cdot X + Q0\cdot X' + Q2$$
$$Q1^* = Q2'\cdot Q0\cdot X + Q1\cdot X' + Q2\cdot Q1$$
$$Q2^* = Q2\cdot Q0' + Q0'\cdot X'\cdot Y$$

Transition equation

$$Z1 = Q2 + Q1' + Q0'$$
$$Z2 = Q2\cdot Q1 + Q2\cdot Q0'$$

Two output equation

	X Y				
Q2 Q1 Q0	00	01	10	11	Z1 Z2
000	000	100	001	001	10
001	001	001	011	011	10
010	010	110	000	000	10
011	011	011	010	010	00
100	101	101	101	101	11
101	001	001	001	001	10
110	111	111	111	111	11
111	011	011	011	011	11
	Q2* Q1* Q0*				

Transition/output table

	X Y				
S	00	01	10	11	Z1 Z2
A	A	E	B	B	10
B	B	B	D	D	10
C	C	G	A	A	10
D	D	D	C	C	00
E	F	F	F	F	11
F	B	B	B	B	10
G	H	H	H	H	11
H	D	D	D	D	11
	S*				

State/output table

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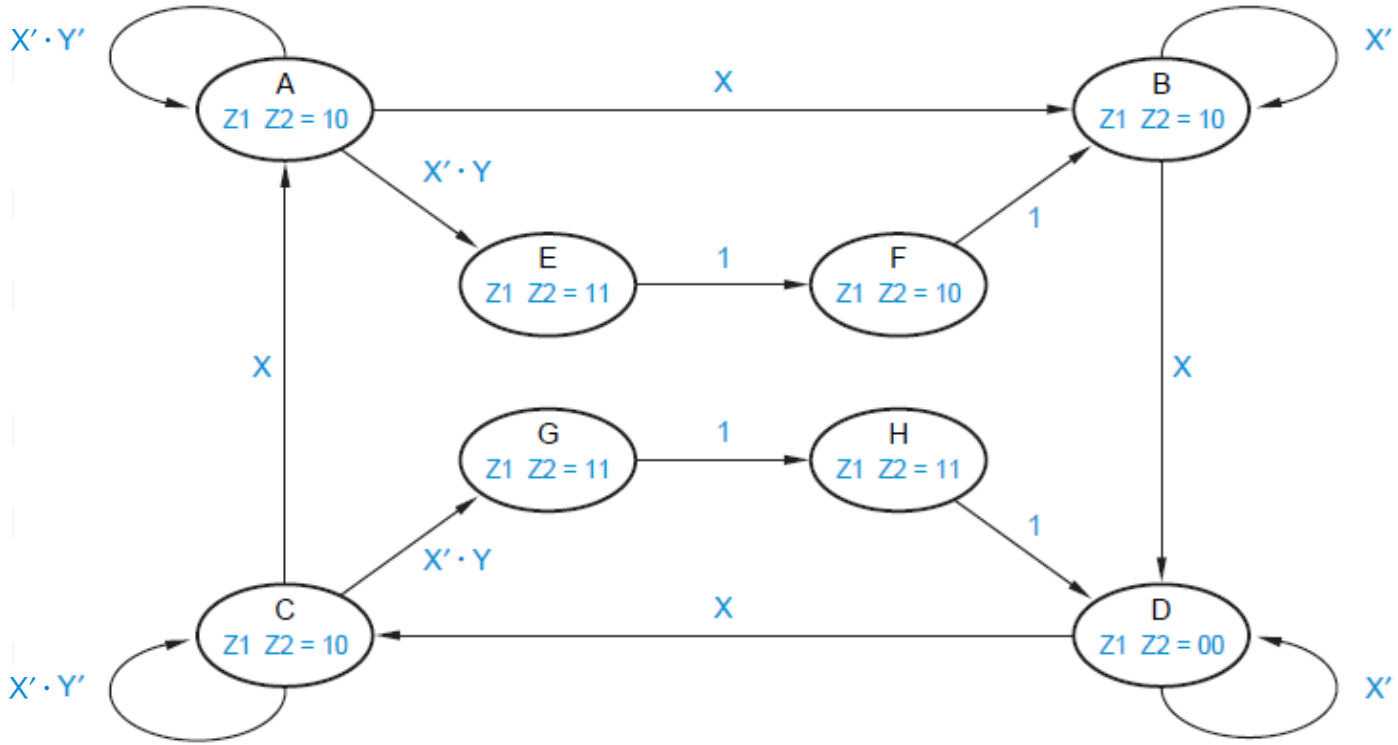
$$Z1 = Q2 + Q1' + Q0'$$
$$Z2 = Q2 \cdot Q1 + Q2 \cdot Q0'$$

Two output equation

	X Y				
S	00	01	10	11	Z1 Z2
A	A	E	B	B	10
B	B	B	D	D	10
C	C	G	A	A	10
D	D	D	C	C	00
E	F	F	F	F	11
F	B	B	B	B	10
G	H	H	H	H	11
H	D	D	D	D	11
	S*				

State/output table



State diagram

Transition expression constraints

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- _____can equal 1 for the same input combination since a machine cannot have _____for one input combination.
- For every possible _____, some _____must equal 1, so that all next states are defined.

"The transition expressions on arcs leaving a particular state must be _____and _____."