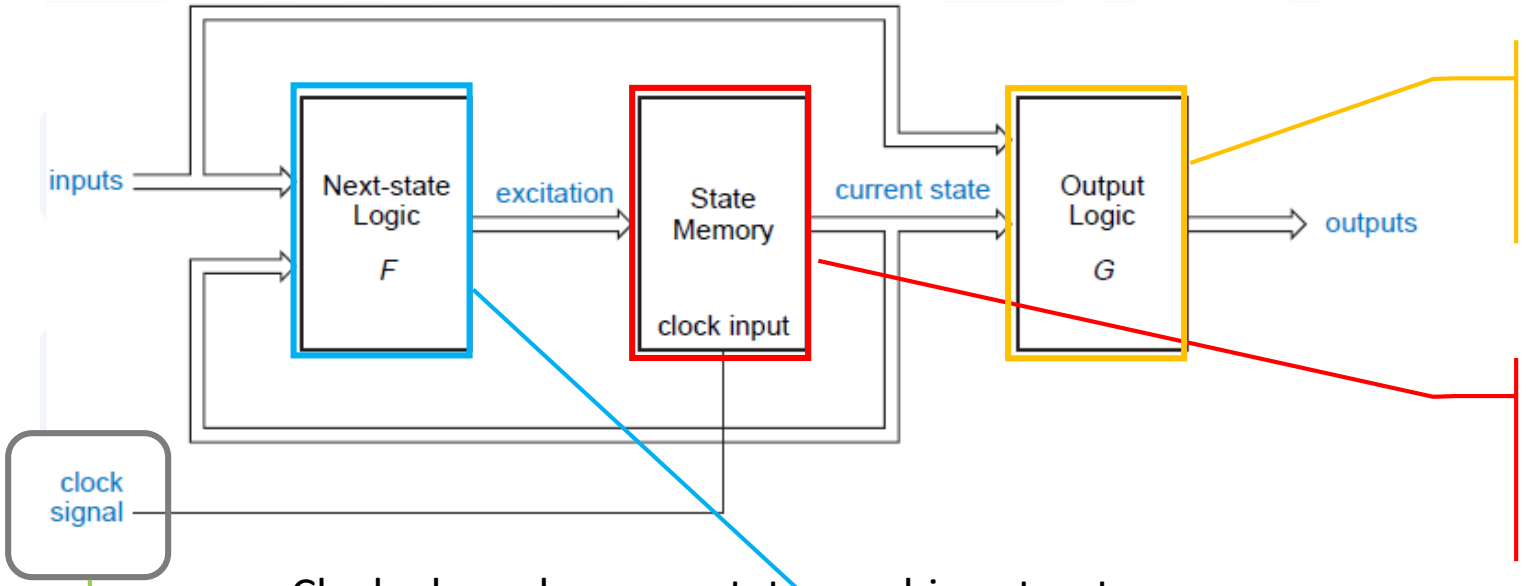
Pakorn Watanachaturaporn
pakorn.wa@KMITL.ac.th

01076244 Advanced Digital System Design

Bachelor Program in Computer Engineering (B.Eng.)
Faculty of Engineering
King Mongkut's Institute of Technology Ladkrabang

State-Machine Structure

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th



Clocked synchronous state-machine structure

The output logic G determines the output as a function of the current state and input

A set of *n* flip-flops that store the current state of the machine and has 2^n distinct states

A common clock signal that causes the flip-flops to change state at each *tick* of the clock

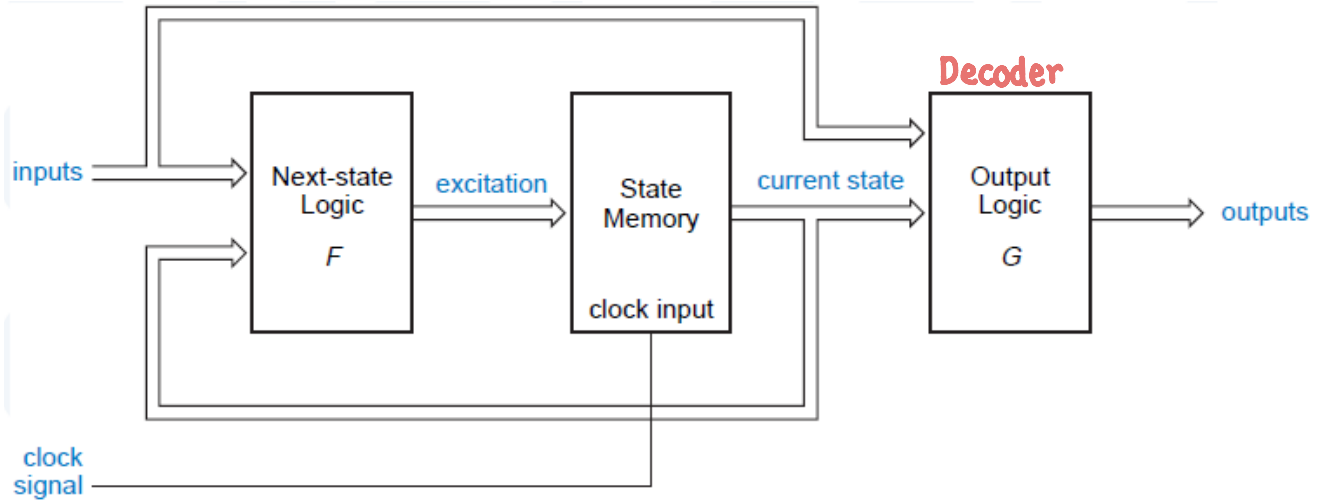
A function of the current state and input

F and *G* are strictly combinational logic circuits.

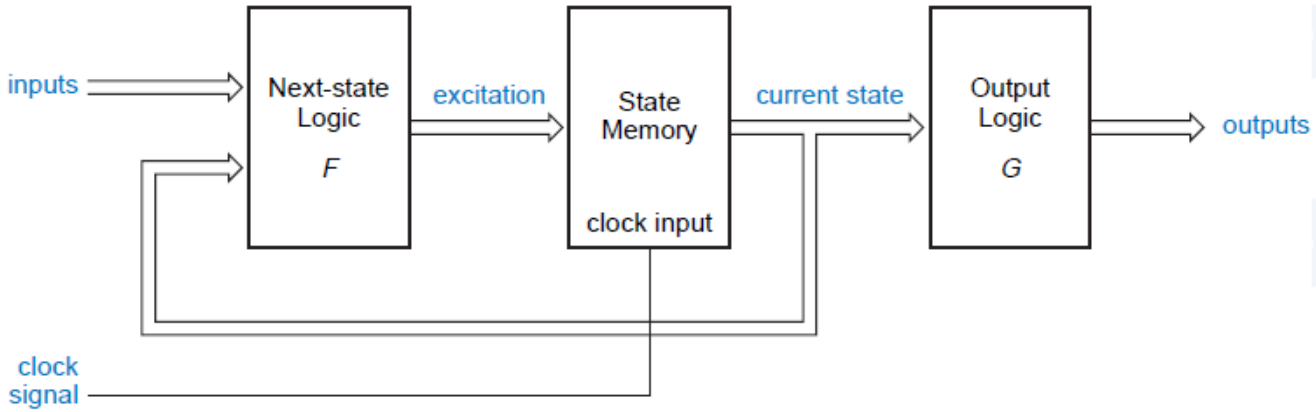
Next state = *F (current state, input)*
Output = *G (current state, input)*

Output Logic

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th



Mealy machine : output depends on both state and input



Moore machine : the output depends on state alone

Characteristic Equations

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

ที่ให้ logic เป็น สมการ ทางคณิตศาสตร์ ที่ระบุว่าหน้าที่เป็นไง

- A Characteristic equation is a formally description of a fn behavior
- The * suffix means the "next value"
- Note: the characteristic equation does not describe detailed timing behavior of the device (latching vs. edge-triggered, etc.), only the fn response to the control input

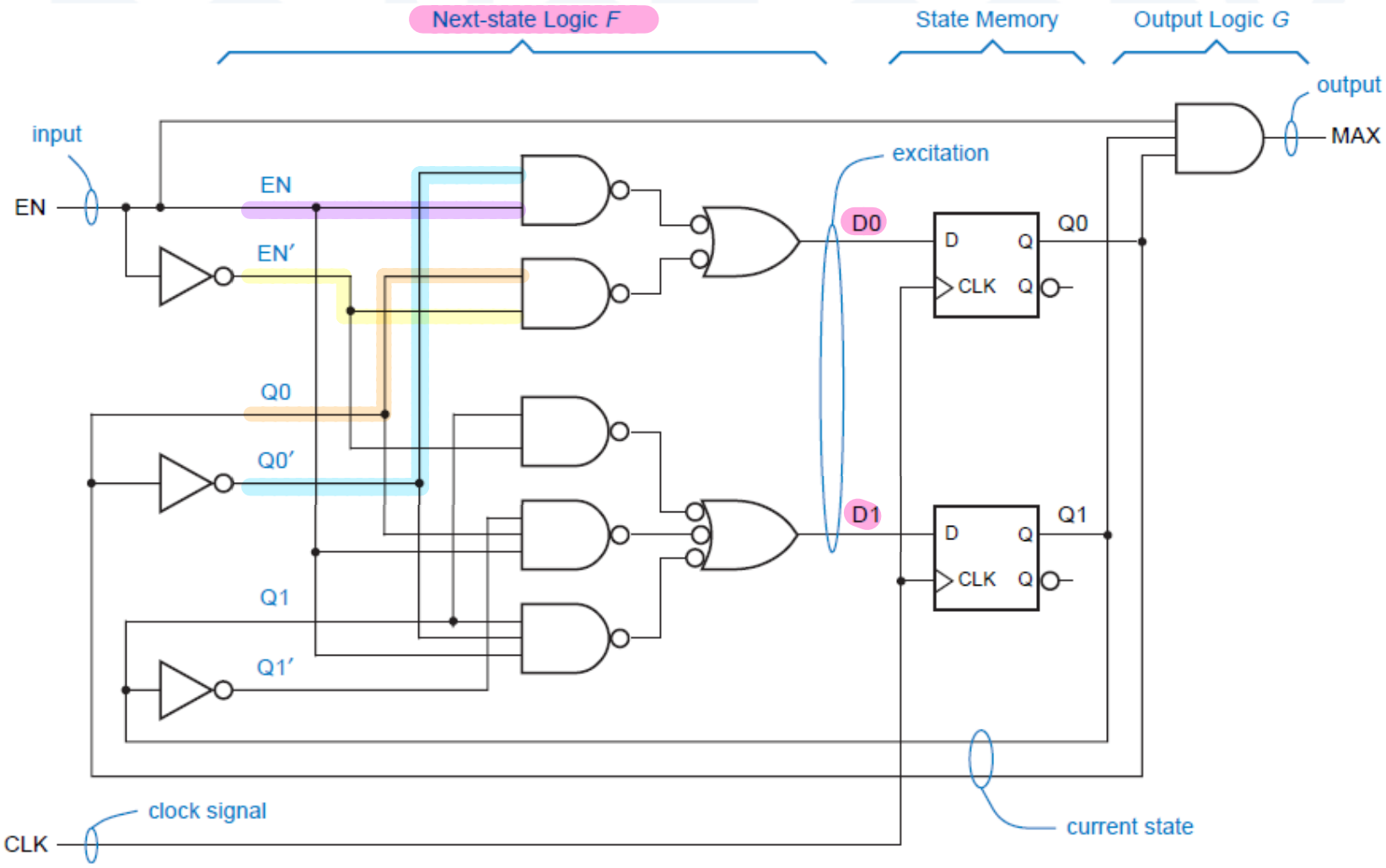
KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

Device Type	Characteristic Equation
S-R latch	$Q^* = S + R' \cdot Q$
D latch	$Q^* = D$
Edge-triggered D flip-flop	$Q^* = D$
D flip-flop with enable	$Q^* = EN \cdot D + EN' \cdot Q$
Edge-triggered J-K flip-flop	$Q^* = J \cdot Q' + K' \cdot Q$
T flip-flop	$Q^* = Q'$
T flip-flop with enable	$Q^* = EN \cdot Q' + EN' \cdot Q$

Analysis of State Machines with D Flip-Flops

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

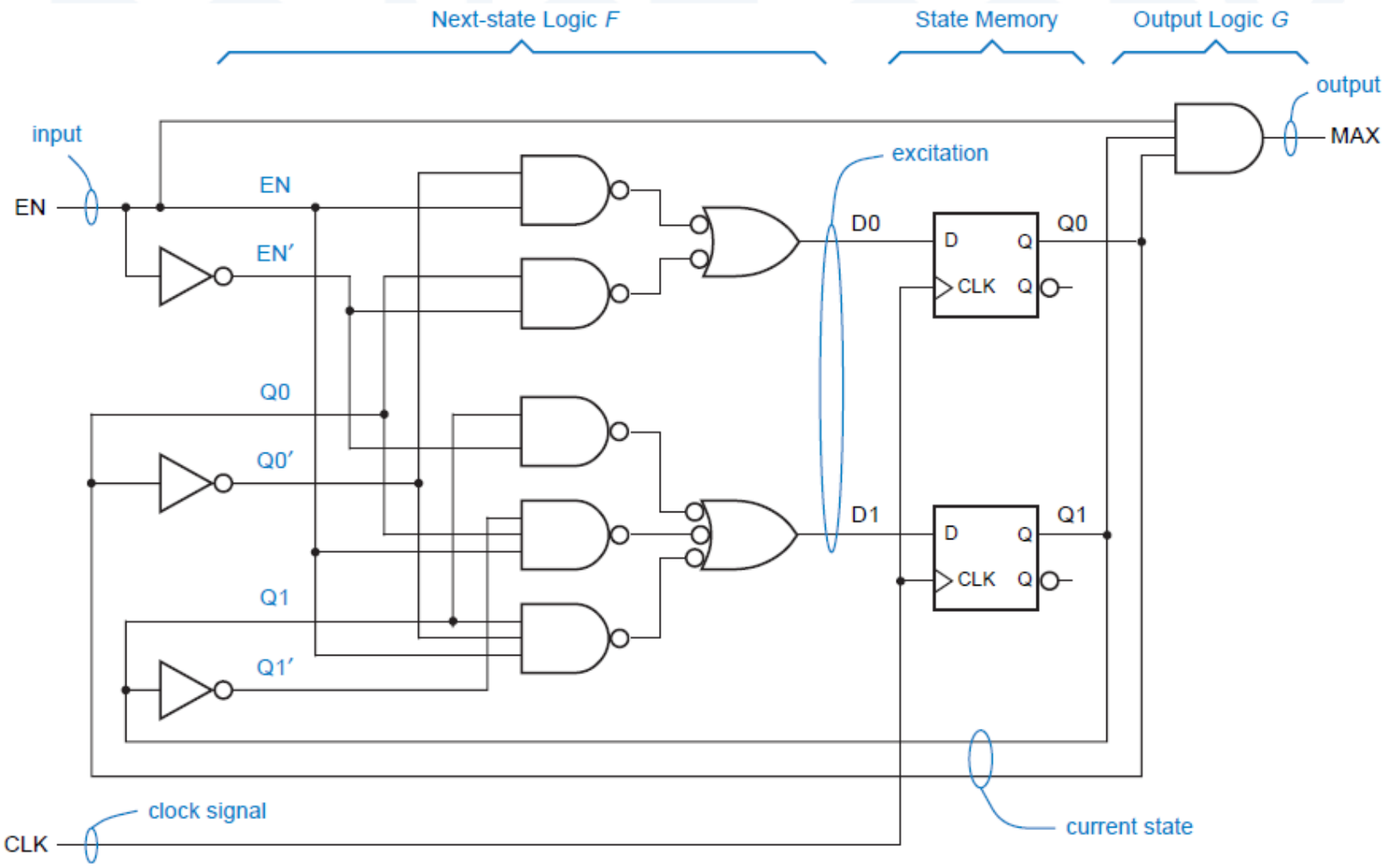
1. Determine the next state and output functions F and G.
2. Use F and G to construct a state / output table that completely specifies the next state and Output of the circuit for every possible combination of current state and input.
3. (Optional) Draw a State diagram that presents the information from the previous step in graphical form.



Clocked synchronous state machine using positive-edge-triggered D flip-flops

$$D0 = Q0 \cdot EN' + Q0' \cdot EN$$

$$D1 = Q1 \cdot EN' + Q1' \cdot Q0 \cdot E0 + Q1 \cdot Q0' QN$$

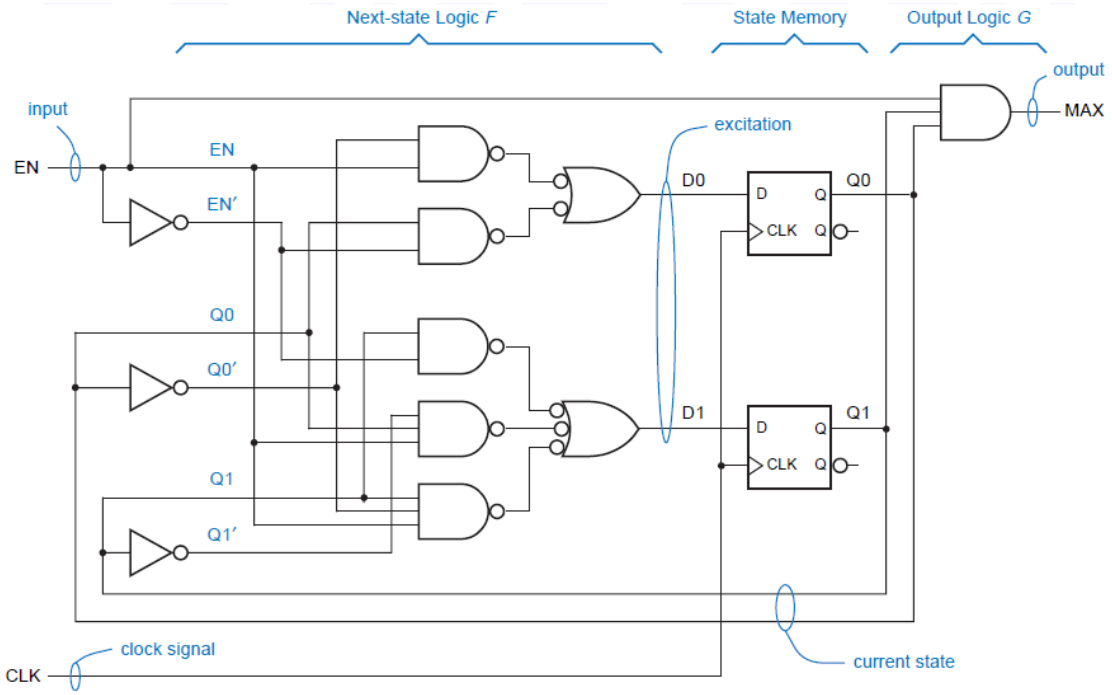


Clocked synchronous state machine using positive-edge-triggered D flip-flops

The next value of a state variable after a clock tick is denoted by appending a star to the state-variable name.

Q0* = D0
Q1* = D1

Q0* = Q0·EN′ + Q0′EN
Q1* = Q1·EN′ + Q1′·Q0·EN + Q1·Q0′·QN



Clocked synchronous state machine using positive-edge-triggered D flip-flops

K-map

Q1 Q0	EN = 0	EN = 1
0 0	00	01
0 1	01	10
1 0	10	11
1 1	11	00
	Q1* Q0*	

Transition table

S	EN = 0	EN = 1
A	A	B
B	B	C
C	C	D
D	D	A
	S*	

State table

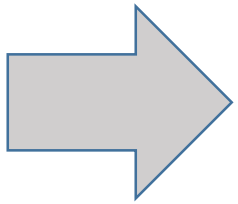
S	EN = 0	EN = 1
A	A,0	B,0
B	B,0	C,0
C	C,0	D,0
D	D,0	A,1
	S* , MAX	

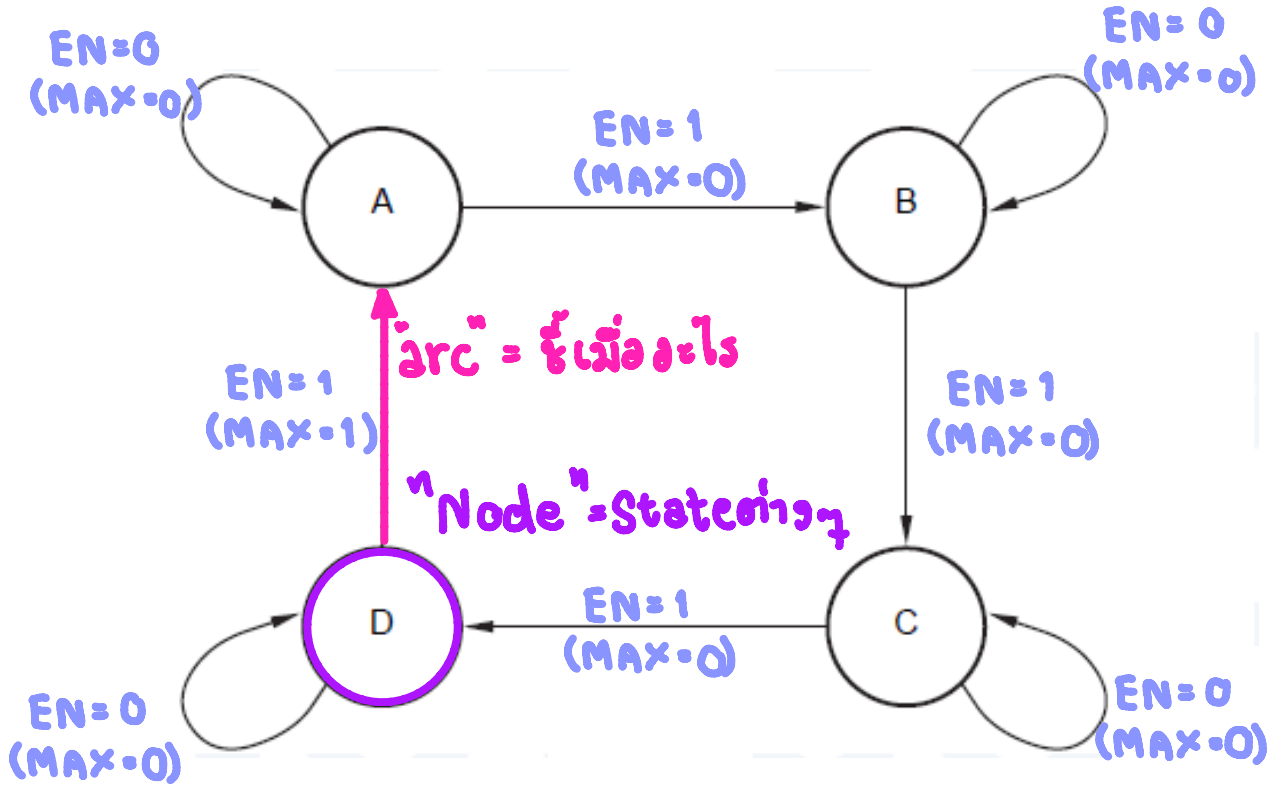
State/output table

MAX = Q1 · Q0 · EN

S	EN	
	0	1
A	A , 0	B , 0
B	B , 0	C , 0
C	C , 0	D , 0
D	D , 0	A , 1
	S* , MAX	

State/output table



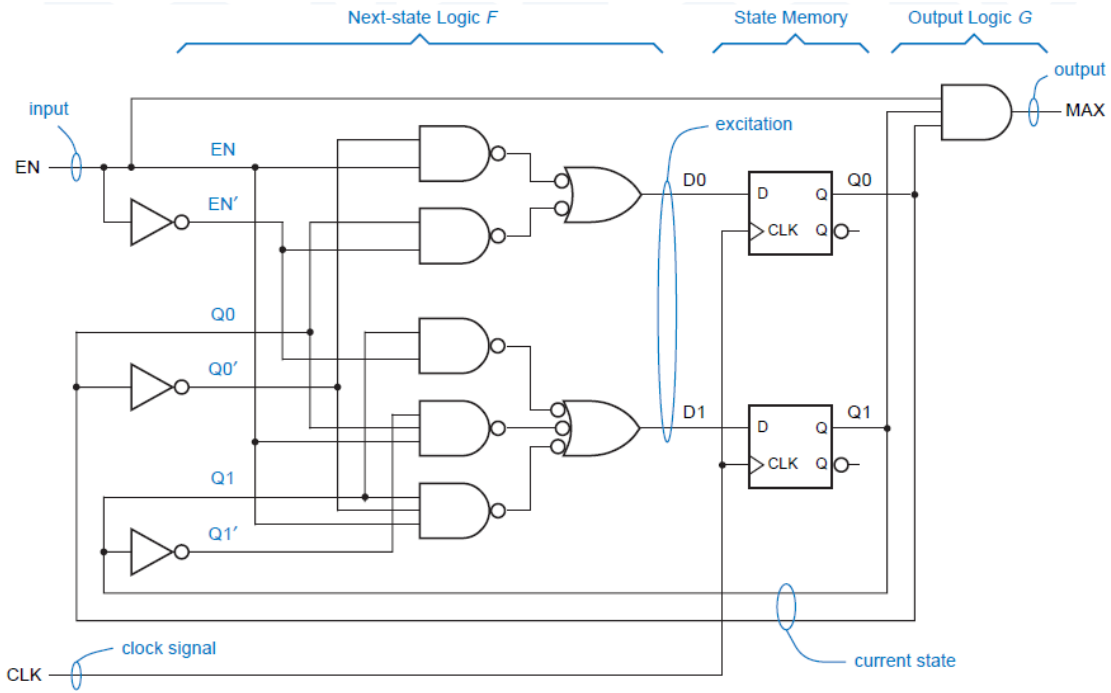


State diagram

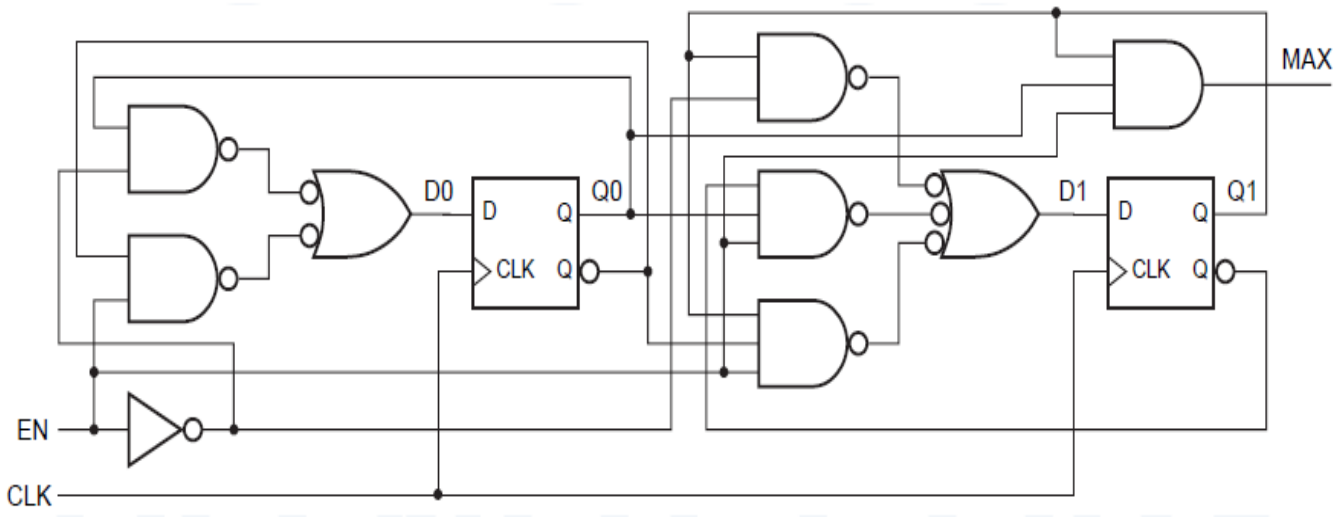
- A State diagram presents the information from the state / output table in a graphical format.
- A circle (or node) for each state.
- An arrow (or directed arc) for each transition.

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

Redrawn



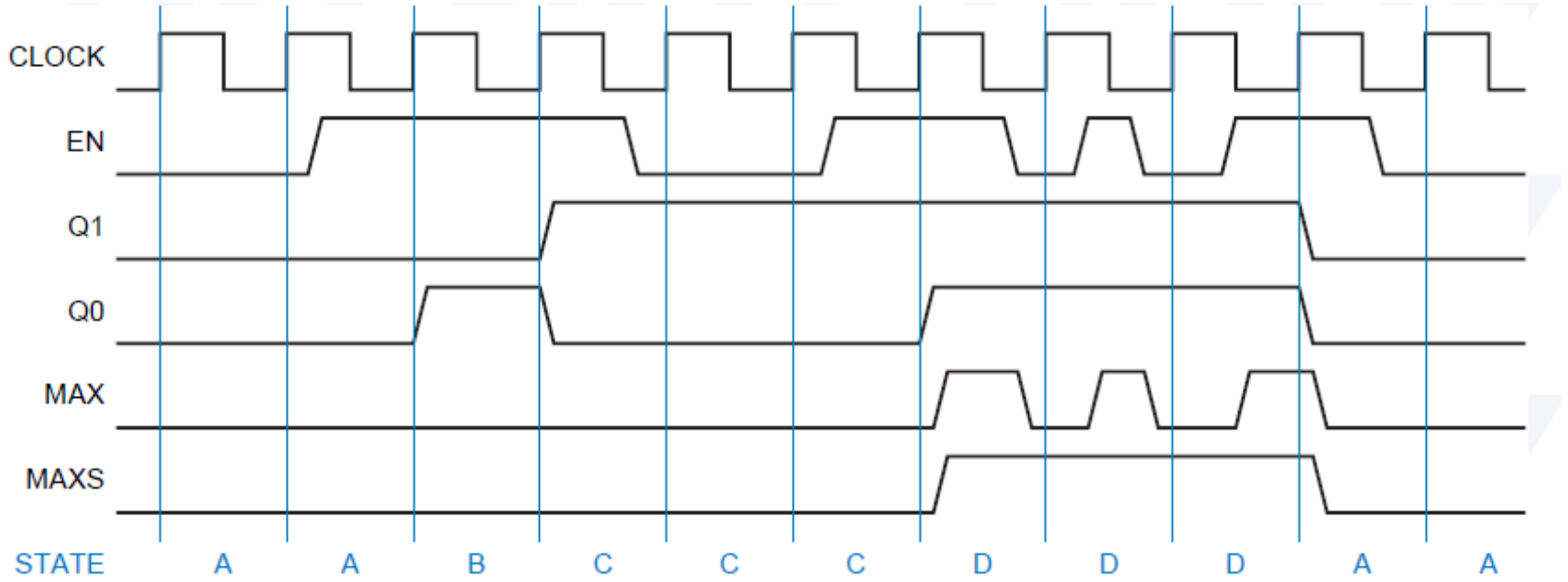
Clocked synchronous state machine using positive-edge-triggered D flip-flops



Redrawn logic diagram for a clocked synchronous state machine

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

S	EN	
	0	1
A	A , 0	B , 0
B	B , 0	C , 0
C	C , 0	D , 0
D	D , 0	A , 1
	S* , MAX	



MAX = Q1·Q0·EN

Timing diagram for example state machine

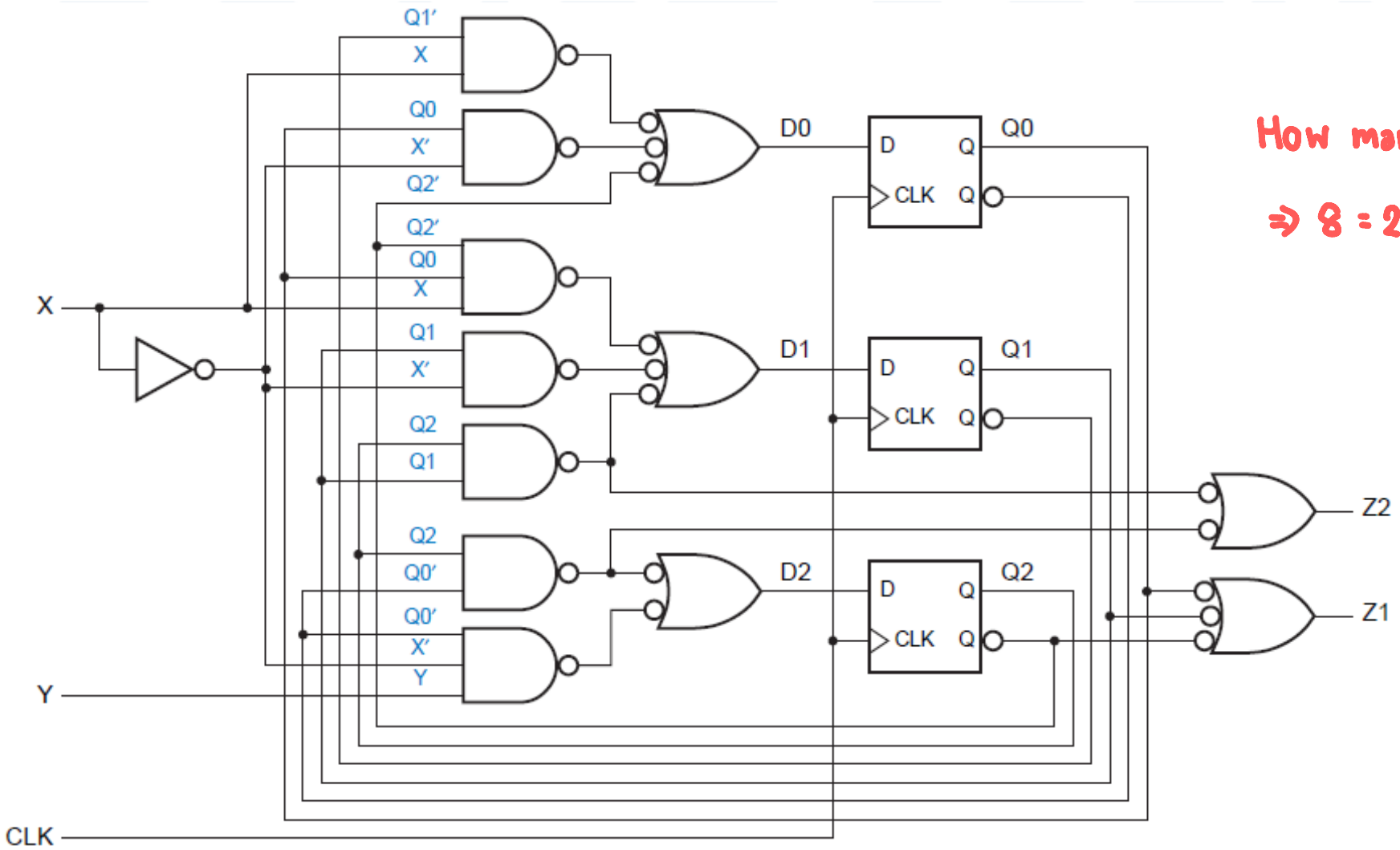
Summarizing detailed steps for analyzing a clocked synchronous state machine

KMITL พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

1. Determine the excitation equations (ที่ทำให้เปลี่ยนสถานะได้) for the flip-flop control inputs.
2. Substitute (แทนที่) the excitation equations into the flip-flop characteristic equations to obtain transition equations.
3. Use the transition equations to construct a transition table.
4. Determine the output equations.
5. Add output value to the transition table for each state (Moore) or state / input combination (Mealy) to create a transition/output table.
6. Name the states and substitute state names for state-variable combinations in the transition/output table to obtain a state/output table.
7. (Optional) Draw a state diagram corresponding to the state/output table.

Another example

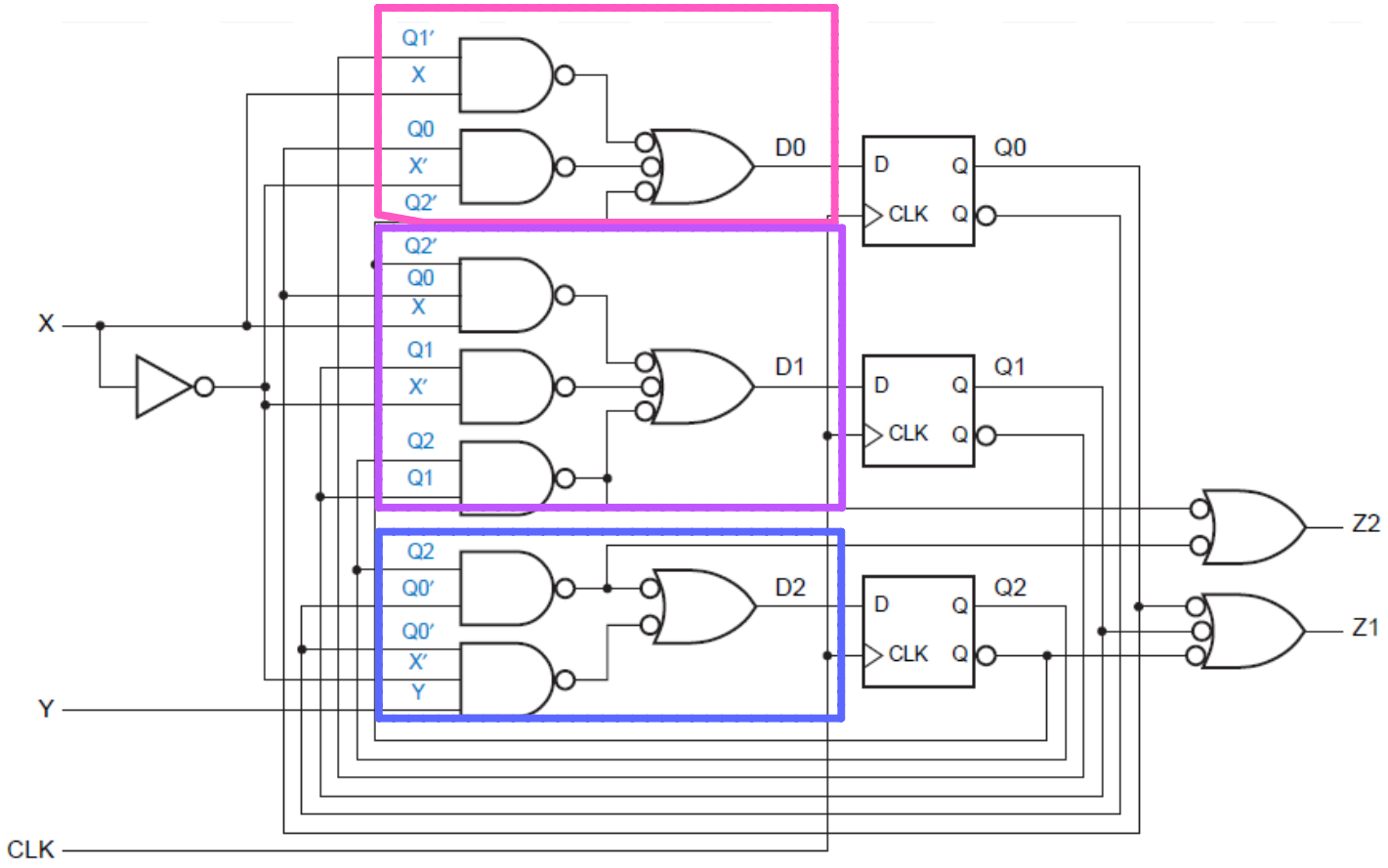
KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th



How many state this logic diagram

$\Rightarrow 8 = 2^3$

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th



The excitation equations are :

$D0 = Q1' \cdot X + Q0 \cdot X' + Q2$

$D1 = Q2 \cdot Q0 \cdot X + Q1 \cdot X' + Q2 \cdot Q1$

$D2 = Q\ \ Q0' + Q0' \cdot X' \cdot Y$

Substituting into the characteristic equation for D flip-flops

$Q0^{+} = Q1' \cdot X + Q0 \cdot X' + Q2$

$Q1^{+} = Q2' \cdot Q0 \cdot X + Q1 \cdot X' + Q2 \cdot Q1$

$Q2^{+} = Q2 \cdot Q0' + Q0' \cdot X' \cdot Y$

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

$$Q0^* = Q1'\cdot X + Q0\cdot X' + Q2$$
$$Q1^* = Q2'\cdot Q0\cdot X + Q1\cdot X' + Q2\cdot Q1$$
$$Q2^* = Q2\cdot Q0' + Q0'\cdot X'\cdot Y$$

Transition equation

$$Z1 = Q2 + Q1' + Q0'$$
$$Z2 = Q2\cdot Q1 + Q2\cdot Q0'$$

Two output equation

	X Y				
Q2 Q1 Q0	00	01	10	11	Z1 Z2
000	000	100	001	001	10
001	001	001	011	011	10
010	010	110	000	000	10
011	011	011	010	010	00
100	101	101	101	101	11
101	001	001	001	001	10
110	111	111	111	111	11
111	011	011	011	011	11
	Q2* Q1* Q0*				

Transition/output table

	X Y				
S	00	01	10	11	Z1 Z2
A	A	E	B	B	10
B	B	B	D	D	10
C	C	G	A	A	10
D	D	D	C	C	00
E	F	F	F	F	11
F	B	B	B	B	10
G	H	H	H	H	11
H	D	D	D	D	11
	S*				

State/output table

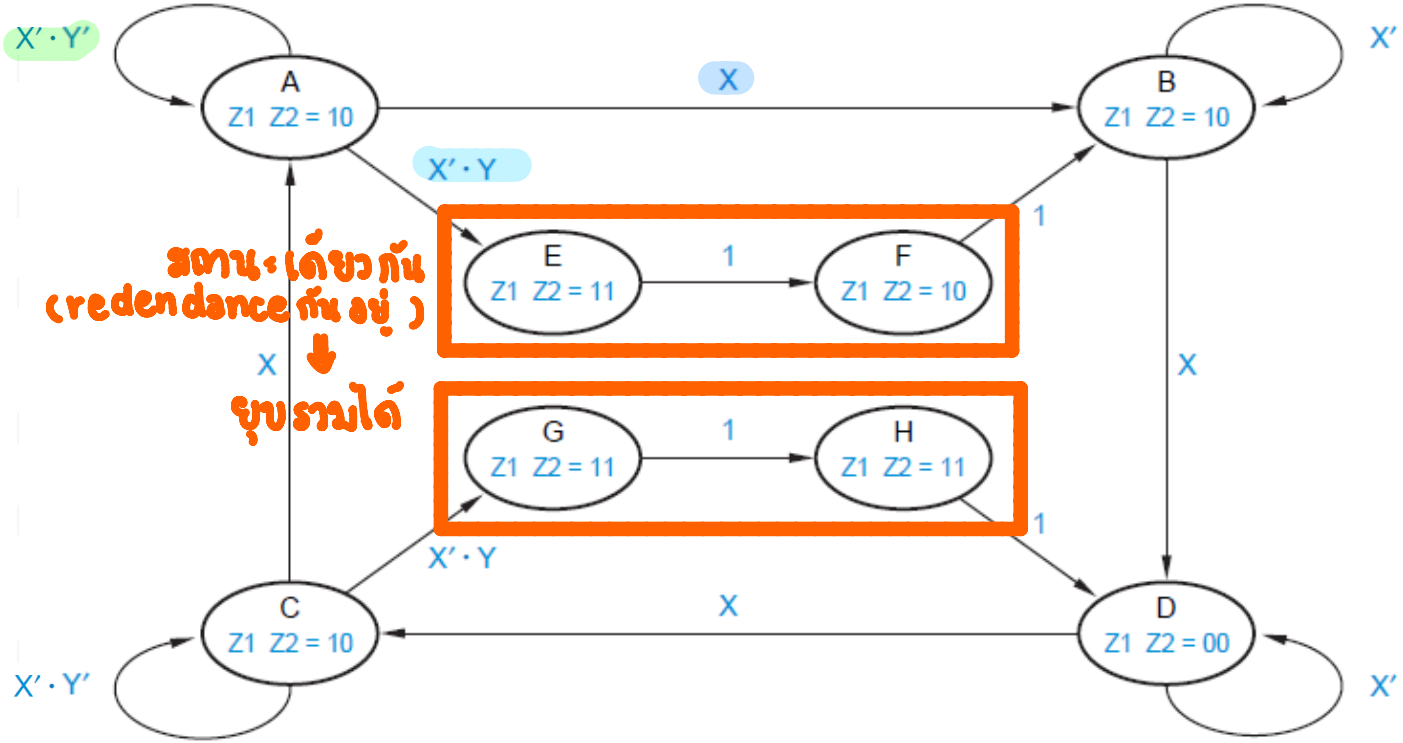
KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

$$Z1 = Q2 + Q1' + Q0'$$
$$Z2 = Q2 \cdot Q1 + Q2 \cdot Q0'$$

Two output equation

	X Y				
S	00	01	10	11	Z1 Z2
A	A	E	B	B	10
B	B	B	D	D	10
C	C	G	A	A	10
D	D	D	C	C	00
E	F	F	F	F	11
F	B	B	B	B	10
G	H	H	H	H	11
H	D	D	D	D	11
	S*				

State/output table



State diagram

Transition expression constraints

KMITL
พระจอมเกล้าลาดกระบัง
pakorn.wa@kmitl.ac.th

- No Two transition can equal 1 for the same input combination since a machine cannot have two next state for one input combination.

  Mutual exclusion

- For every possible input combination, some transition expression must equal 1, so that all next states are defined.

  All inclusion

"The transition expressions on arcs leaving a particular state must be mutually exclusive and all inclusive."