Text : Digital Systems : Principles and Applications; Ronald J. Tocci, Neal S. Widmel; Prentice Hall; 10 th Edition.

Lecture 1 : Introductory Concepts and Number Systems (Ch 1 & 2)

1-1 Numerical Representation

1-2 Digital and Analog Systems

1-3 Digital Number Systems

1-4 Representing Binary Quantities

1-5 Digital Circuits/Logic Circuits

1-6 Parallel and Serial Transmission

1-7 Memory

1-8 Digital Computers

2-1 Binary-to-Decimal Conversions

2-2 Decimal-to-Binary Conversions

2-3 Hexadecimal Number System

2-4 BCD Code

2-5 The Gray Code

2-6 Putting it All Together

2-7 The Byte, Nibble, and Word

2-8 Alphanumeric Codes

2-9 Parity Method for Error Detection

2-10 Applications

Lecture 2 : Logic Circuits (Ch 3)

Boolean Constants and Variables

3-2 Truth Tables

3-3 OR Operation with OR Gates

3-4 AND Operation with AND Gates

3-5 NOT Operation

3-6 Describing Logic Circuits Algebraically

3-7 Evaluating Logic-Circuit Outputs

3-8 Implementing Circuits from Boolean Expressions

3-9 NOR Gates and NAND Gates

3-10 Boolean Theorems

3-11 DeMorgan7s Theorems

3-12 Universality of NAND Gates and NOR Gates

3-13 Alternate Logic-Gate Representations

3-14 Which Gate Representation to Use

3-1 5 IEEE/ANSI Standard Logic Symbols

3-16 Summary of Methods to Describe Logic Circuits

3-17 Description Languages Versus Programming Languages

3-18 Implementing Logic Circuits with PLDs

3-19 HDL Format and Syntax

3-20 Intermediate Signals

Lecture 3 : Combinational Logic Circuits (Ch 4)

4-1 Sum-of-Products Form

4-2 Simplifying Logic Circuits

4-3 Algebraic Simplification

4-4 Designing Combinational Logic Circuits

4-5 Karnaugh Map Method

4-6 Exclusive-OR and Exclusive-NOR Circuits

4-7 Parity Generator and Checker

4-8 Enable/Disable Circuits

4-9 Basic Characteristics of Digital ICs

4-10 Troubleshooting Digital Systems

4-11 Internal Digital IC Faults

4-12 External Faults

4-13 Troubleshooting Case Study

4-14 Programmable Logic Devices

4-1 5 Representing Data in HDL

4-16 Truth Tables Using HDL

4-17 Decision Control Structures in HDL

*** Quine–McCluskey

Lecture 4: Flip-Flops and Related Devices (Ch 5)

5-1 NAND Gate Latch

5-2 NOR Gate Latch

5-3 Troubleshooting Case Study

5-4 Digital Pulses

5-5 Clock Signals and Clocked Flip-Flops

5-6 Clocked S-R Flip-Flop

5-7 Clocked J-K Flip-Flop

5-8 Clocked D Flip-Flop

5-9 D Latch (Transparent Latch)

5-10 Asynchronous Inputs

5-11 IEEE/ANSI Symbols

5-12 Flip-Flop Timing Considerations

5-13 Potential Timing Problem in FF Circuits

5-14 Flip-Flop Applications

5-15 Flip-Flop Synchronization

5-16 Detecting an Input Sequence

5-17 Data Storage and Transfer

5-18 Serial Data Transfer: Shift Registers

5-19 Frequency Division and Counting

5-20 Microcomputer Application

5-21 Schmitt-Trigger Devices

5-22 One-Shot (Monostable Multivibrator)

5-23 Clock Generator Circuits

5-24 Troubleshooting Flip-Flop Circuits

5-25 Sequential Circuits Using HDL

5-26 Edge-Triggered Devices

5-27 HDL Circuits with Multiple Components

Lecture 5 : Digital Arithmetic, Operations and Circuits (Ch 6)

6-1 Binary Addition

6-2 Representing Signed Numbers

6-3 Addition in the 2's-Complement System

6-4 Subtraction in the 2's-Complement System

6-5 Multiplication of Binary Numbers

6-6 Binary Division

6-7 BCD Addition

6-8 Hexadecimal Arithmetic

6-9 Arithmetic Circuits

6-10 Parallel Binary Adder

6-11 Design of a Full Adder

6-12 Complete Parallel Adder with Registers

6-13 Carry Propagation

6-14 Integrated-Circuit Parallel Adder

6-15 2's-Complement System

6-16 ALU Integrated Circuits

6-17 Troubleshooting Case Study

6-18 Using TTL Library Functions with Altera

6-19 Logical Operations on Bit Arrays

6-20 HDL Adders

6-2 1 Expanding the Bit Capacity of a Circuit

Lecture 6 : Counters and Registers Part 1 (Ch 7)

7-1 Asynchronous (Ripple) Counters

7-2 Propagation Delay in Ripple Counters

7-3 Synchronous (Parallel) Counters

7-4 Counters with MOD Numbers < 2^N

7-5 Synchronous Down and Up/Down Counters

7-6 Presettable Counters

7-7 IC Synchronous Counters

7-8 Decoding a Counter

7-9 Analyzing Synchronous Counters

7-10 Synchronous Counter Design

7-11 Basic Counters Using HDLs

7-12 Full-Featured Counters in HDL

7-13 Writing HDL Modules Together

7-14 State Machines

Lecture 7 : Counters and Registers Part 2 (Ch 7)

7-15 Integrated Circuit Registers

7-16 Parallel In/Parallel Out-The 74ALS174/74HC174

7-17 Serial In/Serial Out-The 74ALS166/74HC166

7-18 Parallel In/Serial Out-The 74ALS165/74HC165

7-19 Serial In/Parallel Out-The 74ALS164/74HC164

7-20 Shift-Register Counters

7-21 Troubleshooting

7-22 HDL Registers

7-23 HDL Ring Counters

7-24 HDL One-Shots

Lecture 8 : Integrated-Circuit Logic Families (Ch 8)

8-1 Digital IC Terminology

8-2 The TTL Logic Family

8-3 TTL Data Sheets

8-4 TTL Series Characteristics

8-5 Other TTL Characteristics

8-7 MOS Technology

8-8 Complementary MOS Logic

8-9 CMOS Series Characteristics

8-10 Low-Voltage Technology

8-11 Open-Collector/Open-Drain Outputs

8-12 Tristate (Three-State) Logic Outputs

8-13 High-speed Bus Interface Logic

8-14 The ECL Digital IC Family

8-15 CMOS Transmission Gate (Bilateral Switch)

8-16 IC Interfacing

8-17 Mixed-Voltage Interfacing

8-18 Analog Voltage Comparators

8-19 Troubleshooting

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9-1 Decoders

9-2 BCD-to-7-Segment Decoder/Drivers

9-3 Liquid-Crystal Displays

9-4 Encoders

9-5 Troubleshooting

9-6 Multiplexers (Data Selectors)

9-7 Multiplexer Applications

9-8 Demultiplexers (Data Distributors)

9-9 More Troubleshooting

9-10 Magnitude Comparator

9-11 Code Converters

9-12 Data Busing

9-13 The 74ALS173/HC173 Tristate Register

9-14 Data Bus Operation

9-15 Decoders Using HDL

9-16 The HDL 7-Segment Decoder/Driver

9-17 Encoders Using HDL

9-18 HDL Multiplexers and Demultiplexers

9-19 HDL Magnitude Comparators

9-20 HDL Code Converters

Lecture 10 : Interfacing with the Analog World (Ch 11)

11-1 Review of Digital Versus Analog

11-2 Digital-to-Analog Conversion

11-3 D/A-Converter Circuitry

11-4 DAC Specifications

11-5 An Integrated-Circuit DAC

11-6 DAC Applications

11-7 Troubleshooting DACs

11-8 Analog-to-Digital Conversion

11-9 Digital-Ramp ADC

11-10 Data Acquisition

11-11 Successive-Approximation ADC

11-12 Flash ADCs

11-13 Other A/D Conversion Methods

11-14 Sample-and-Hold Circuits

11-15 Multiplexing

11-16 Digital Storage Oscilloscope

11-17 Digital Signal Processing (DSP)

Lecture 11 : Memory Devices (Ch 12)

12-1 Memory Terminology

12-2 General Memory Operation

12-3 CPU-Memory Connections

12-4 Read-only Memories

12-5 ROM Architecture

12-6 ROM Timing

12-7 Types of ROMs

12-8 Flash Memory

12-9 ROM Applications

12-10 Semiconductor RAM

12-11 RAM Architecture

12-12 Static RAM (SRAM)

12-13 Dynamic RAM (DRAM)

12-14 Dynamic RAM Structure and Operation

12-15 DRAM Read/Write Cycles

12-16 DRAM Refreshing

12-17 DRAM Technology

12-18 Expanding Word Size and Capacity

12-19 Special Memory Functions

12-20 Troubleshooting RAM Systems

12-21 Testing ROM

Lecture 12 : Programmable Logic Device Architectures (Ch 13)

13-1 Digital Systems Family Tree

13-2 Fundamentals of PLD Circuitry

13-3 PLD Architectures

13-4 The GAL 16V8 (Generic Array Logic)

** Introduction to Xilinx CPLD, FPGA

** State machine, Moore and mealy model