Department of Electrical and Computer Engineering

University of Victoria
ENGR 446 – A01 – Fall

ENGR 446 Final Report

Design and Analysis of a Data Acquisition System

Brett Dionello V01026046
Email: bdionello@uvic.ca
Program: Computer Engineering

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In partial fulfillment of the requirements of the B.Eng. Degree

Letter of Transmittal

University of Victoria Nov 28, 2024

Faculty of Engineering

Re: ENGR 446 Report

Dear Sana Shuja,

Please accept the attached technical report “Design and Analysis of a Data Acquisition System” as partial fulfillment of the ENGR 446 course requirements.

This report has been completed entirely by me, Brett Dionello, a 4th year Engineering student at the University of Victoria in the computer engineering program, as a requirement of the ENGR 446 course. During a previous Co-op work term with ViVitro Labs inc. I had an opportunity to work with a ViVitro designed data acquisition unit

Regards,

Brett Dionello , 4th Yr. Engineering Student

ENGR 446-A01, Fall 2024 Term

bdionello@uvic.ca

Contents

Executive Summary

Glossary

Term	Definition
Analog-to-Digital Converter (ADC)	An electronic circuit or device that converts analog signals into digital signals.
Digital Acquisition System (DAQ / DAS)	An electronic system designed to convert physical conditions into electronic (analog or digital) signals
Successive Approximation (SAR)	An iterative method implementation of an ADC
Programmable Gain Amplifier (PGA)	A type of amplifier that can modify its gain factor with an external component or other control mechanism
Resistance Temperature Detector (RTD)	A resistance-based temperature detecting transducer
Direct Current (DC)	Electrical current that flows in one direction only
Instrumentation Amplifier (InAmp)	A type of differential amplifier with input buffers. Ideal for test equipment
Multiplexer (MUX)	A device that chooses between multiple input signals and switches it to a single output line

Introduction

Data Acquisition System

Data acquisition is the process of capturing physical conditions in the real-world as continuous analog signals and converting them into discrete digital numeric values that can be processed by a computer program. The systems used to perform this task are known as Data Acquisition systems (DAQs or DAS) and are comprised mainly of sensors, signal conditioning circuitry, Analog-to-digital converters (ADCs) and software components. [2] *Sensors/Transducers* are the first item in the signal path, and they convert physical parameters to electrical signals, some examples are temperature, pressure, vibration, light intensity and radiation. *Signal conditioning*

modifies the signal from the sensor into a form that is ready for digital conversion for example the signal may need to be filtered, amplified and linearized etc. Additionally, the sensor may need to be energized by some additional circuitry such as a constant current source or voltage across a Wheatstone bridge in the case of a resistive sensor. There are often multiplexing components as well to control the signal path of multiple sensors and possibly synchronization circuitry for real-time systems with strict control requirements. The *ADC* converts the continuous analog signal into digital "samples". Each of the above components introduce some amount of noise and error into the signal and so do the signal paths not mentioned above such as cables, connectors and circuit board traces.

Measurement concepts

Accuracy, precision and error are concepts that are used to describe how closely a measurement is to the true value. Accuracy describes how close a measurement is to the true value; precision is independent of accuracy and relates to repeatability or how close a set of measurements are to each other. Error is a term that refers to all factors that cause a measurement to differ from the true value and includes systematic errors and random errors. Systematic errors are repeatable and can be calibrated or compensated for, random errors are not repeatable and known as noise, a concept that will be discussed shortly.

DAQ Accuracy

Steps to determine accuracy in a DAQ system as presented by national instruments [3]

1. Determine your accuracy effecting variables and environmental parameters:

   Identify the components connected to the system and the values of pertinent variables such as operating mode, temperature, and input ranges. These are used to identify the correct error values from the data sheets

2. Calculate *Absolute Accuracy* for each system component based off data sheet error values and operating conditions from step 1. Note: some variations to this equation are made depending on the error parameters of the specified component such as the inclusion of a temperature drift factor.

$$Absolute\ Accuracy = \pm[(VoltageReading \times GainError) + (VoltageRange \times OffsetError) + SystemNoise] \quad (1)$$

   Note in equation (1) the voltage range is a device setting and can be neglected in the following analysis.

3. Use the *Absolute Accuracy* values to calculate the system Accuracy and *System Accuracy Relative to Input (RTI)*

$$System\ Accuracy = \sqrt{AbsoluteAccuracy_1{}^2 + AbsoluteAccuracy_2{}^2 + \cdots + AbsoluteAccuracy_n{}^2} \quad (2)$$

$$System\ Accuracy\ RTI = \pm \frac{System\ Accuracy}{Input\ Voltage} \quad (3)$$

Noise

Noise is the voltage and current fluctuations caused by the random motion of charged particles and exists in all electronic systems. Circuit elements and environmental factors can add noise which can obscure and mask small signals adding uncertainty to the measurement. [4]

Spectral density is a common noise parameter and is represented as a noise voltage or noise current per root hertz V/$\sqrt{Hz}$ or A/$\sqrt{Hz}$. The characteristic equations that identify noise sources are integrated over frequency, that is why spectral densities are a natural representation for noise sources.

Types of Noise

In op-amp circuits such as those that are commonly used to form the instrumentation amplifier and filter components of a DAQ system, there are 3 common types of noise that are relevant for analysis. *Shot Noise* which is associated with current flow and results from charges crossing a barrier such as in a pn-junction. *Thermal Noise* which is caused by thermal excitation of charge carriers in a conductor and is present in all passive resistive elements. *Flicker Noise* also known as 1/f noise, is present in all active devices, has various origins and is proportional to DC current. Note that Shot Noise and Thermal Noise have uniform power density, meaning a constant value when plotted vs frequency, while flicker noise has an inverse relationship 1/f. Other types of noise not relevant to op-amp circuits are *Burst Noise* and *Avalanche Noise*. [5]

Adding Noise Sources

If the noise sources are independent, which is typically true, then the sum of each independent noise source is the sum of the individual average mean square values [5]

Please see appendix B for a full review of noise analysis in electronic devices.

$$Total\ Noise = \sqrt{NoiseSource_1{}^2 + NoiseSource_2{}^2 + \cdots + NoiseSource_n{}^2} \quad (4)$$

Approaches

Traditional DAQ system includes transducer, amplifier, filter, channel-multiplexor, programmable gain amplifier (PGA), track/hold component, an ADC with accurate voltage reference and transducer excitation circuitry. The amplifier is typically an instrumentation amplifier, which is a specific type of differential input amplifier that offers differential gain and high common-mode rejection, as well as high input impedance and low output impedance. The input can be connected in differential mode (across a sense voltage) or single ended (from a voltage point to ground). The filter is included to reduce aliasing errors and noise. The PGA may be included if the transducer is selectable by the user, meaning the required system gain is not known at the time of manufacturing. The most used ADC types are SAR (power efficiency), Sigma-Delta (high resolution and noise reduction) and integrating type (high accuracy, slow response). A simple DAQ system diagram is shown in Figure 1, note, the track and hold

components are required if a successive-approximation (SAR) ADC is used and are typically built into the IC package in modern ADCs.

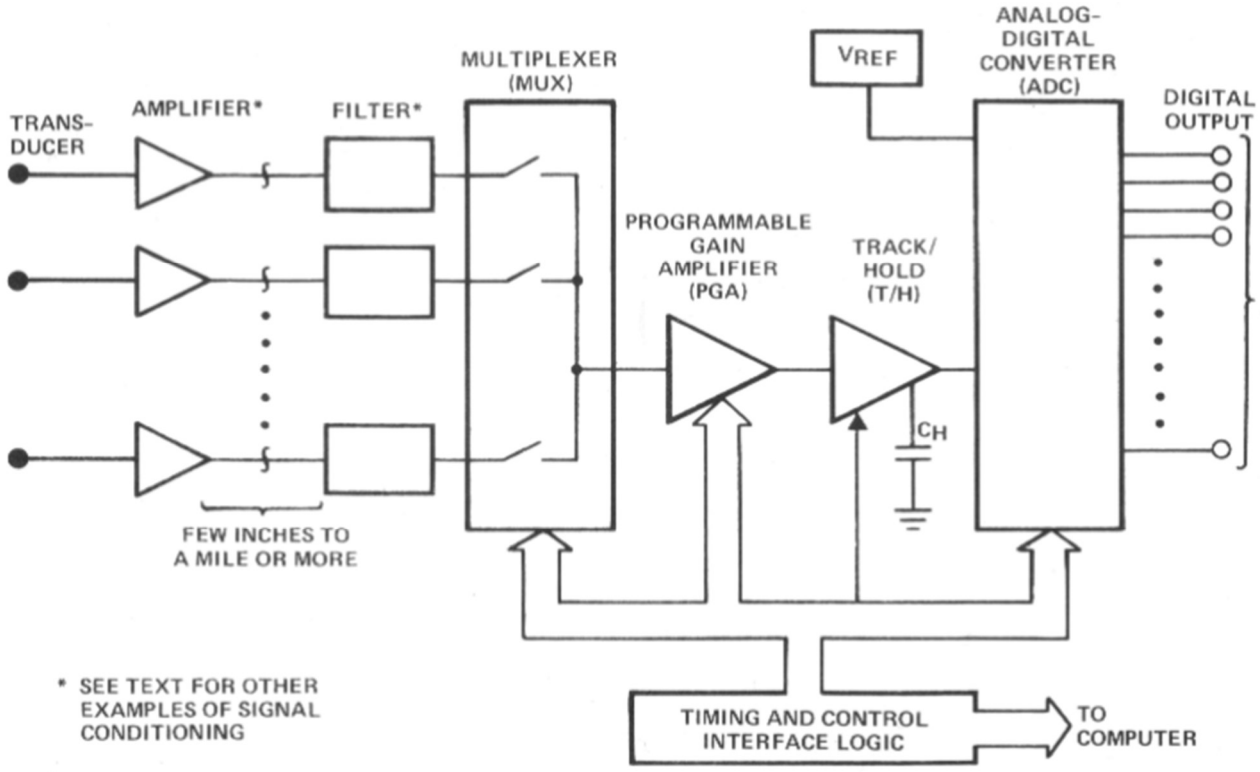

Figure 1: Typical DAQ system [2]

Objective

The problem

Noise and component errors effect the accuracy of a measurement device and the uncertainty of the measurement signal. It is important to know the level of uncertainty in a measurement device so the signal data can be analysed correctly, and the correct decisions can be made. For example, in a control system the error of the signal will affect the feedback signal, and in the analysis of scientific data the margin of error must be correctly identified in all subsequent analysis and processing. Noise and Accuracy analysis will be the topic of this report, specifically as they relate to the design of a practical high-accuracy low-noise DAQ.

Purpose

To explore and communicate the process noise and accuracy analysis and how it is performed during the design of an electronic measurement system, as well as to discover and develop methods that can be used in subsequent designs such as excel spreadsheets and LTspice modeling techniques.

Aims

- Discover the sources for noise and systematic errors in developing a DAQ system.
- Develop methods for analysing and quantifying accuracy of the system.
- Design a practical DAQ system and apply the analysis techniques described above.

Limitations

The physical circuit will not be developed due to time constraints on the project. Hand calculations and simulations can provide a good approximation of the real device but will not be the exact response of the system. Many simplifications will be made to the design and analysis to provide as much detail as possible without exceeded the constraints of the maximum report length. The design will focus on direct current (DC) analysis and will be limited to hardware design.

Initial Assessment

There are a few different approaches to implementing a DAQ system, such as the traditional approach detailed in the background section, or FPGA based and scalable/modular. These latter approaches that may implement a "card rack" format are commonly used in scientific research and nuclear applications [6]. For the simplest design that allows a component-based focus, the traditional DAQ system is preferred. The design variables will be in deciding the following system components, transducer types, input protection, input filtering, multiplexer, PGA, anti-aliasing filter and ADC.

Initial Design choices

The design approach will be to make as many design simplifications as possible while achieving a practical implementation that can be later modified for further development with respect to functionality and performance. The design will be a fixed design with no configurable parameters or components, it will be designed for the selected transducers.

Transducers

The simplest type of transducers is a linear resistive type such as a resistance temperature detector (RTD) or strain gauge, both of which are commonly used in industrial and commercial applications. Both can be used with the same excitation and measurement circuitry.

Transducer Excitation

The RTD and strain gauge can be implemented using a Wheatstone Bridge or a constant current source. A constant current source is selected due to simplicity in calculating the transducer resistance, note that the measurement signal is still differential and does not affect the DAQ design.

Input filtering and protection

These will be omitted from the initial design to simplify the process and are not expected to be the primary cause of loss of accuracy.

Multiplexer

A multiplexed DAQ system can reduce the total system cost by reusing the same circuitry for multiple channels, however significant errors can be introduced due to settling time and synchronization with the ADC sample rate.

Amplifier

An instrumentation amplifier (InAmp) is a special type of differential amplifier that includes input buffering and is ideal for test equipment. The gain will be fixed to a value that is ideal for the RTD and strain gauge that are selected.

Anti-alias filtering

A low-pass anti-alias filter will be included before the ADC to limit the high frequency noise in the ADC measurement.

ADC

The SAR ADC is recommended for instrumentation and data acquisition applications and offer good speed-to-resolution ratios

Design Methodology

With the above design decisions in place the selection of components will be the next step. The process for selecting the specific components will be based on further research into DAQ design principles and precision low noise systems.

Discussion

Proposed Solution

Select transducers, then follow the component selection process to maintain an error budget that does not degrade the quality of signal from the transducer.

The solution will include:

- Analog multiplexer (MUX)
- Instrumentation amplifier (Inamp)
- Antialiasing filtering and analog to digital converter (ADC)

The excitation circuitry will be assumed to be a current source with 1% error. There will be no consideration of the design of any power sources or reference voltages for any components in this analysis.

Problem domain

A DAQ should be able to be implemented in various applications and with different transducers, however the more versatile a DAQ is the more complicated it becomes since the signal types can vary greatly between transducers in terms of signal level, frequency and input type (differential vs single ended). For an initial design, a common problem domain that can be solved with a limited variety of transducer types is proposed.

Hypothetical Problem domain: Boiler system or pressure vessel

A boiler system consists of fluid contained within pressurized vessels, which are heated and used in many different applications such as heating systems and industrial processes. The temperature, pressure, and vessel integrity need to be monitored with transducers such as thermos-couples, RTDs and strain gauges. Since these transducer types are compatible with a differential input, the design changes between each type can be minimized and including in a later design.

Engineering Analysis

The following analysis will cover component selection and calculations to determine the system error, noise, and timing constraints. The analysis will be simplified to the factors that contribute significant error detecting DC signals such as those proposed in this example situation, therefore the analysis of capacitor errors, op-amp distortion, phase distortion, and total harmonic distortion (THD) will be omitted.

The main sources of error to be analysed are the system settling time requirements for accurate ADC sampling within a multiplexed system, input offset and gain errors of the amplifier, and component errors.

Selection of transducers

To determine the transducers a brief survey of Digikey available parts can provide a good idea of what products are on the market, leading manufacturers, the specification ranges, availability and a somewhat arbitrary assessment of what is considered a typical or common component for this application.

Strain gauge

The strain gauge manufacturers distributing through Digikey leave only a few options, based on this Micro-Measurements (Vishay Precision Group) is the clear choice for availability. The ranges for some critical specifications are listed below in Table 1

Table 1 Strain gauge supplier specification ranges

Component:	Strain gauge
Supplier:	Micro-Measurements
Family/Series:	C5K

	min	max
Resistance (ohms)	120	350
Resistance tolerance (%)	0.2	0.5
Strain range (%)	1.5	5
Active length (mm)	0.76	6.35

From the products offered by Micro-Measurements the cheapest option is selected, which has the following specifications shown in Appendix A: Table 4, which includes the highest tolerance available.

Strain Gauge parameters

In a linear strain gauge the resistance changes linearly with deflections in length, and this part is specified to a maximum of 1.5% deflection. The gauge factor (GF) is the ratio between the relative change in resistance for a relative change in length, nominal gauge factors are values are 2-3, with the exact value being determined by calibration and attached to the device when shipped by the manufacturer.

RTD

Following the same procedure above, the search results included more manufacturer variability for an RTD. The part selection was based on the high tolerance specification, price, and availability.

Table 2 RTD Manufacturer specification ranges

Component:	RTD
Supplier:	TE Connectivity
Family/Series:	PTF

	min	max
Resistance (ohms)	100	1000
Tolerance (%)	0.12	0.14

Table 3 RTD Co-efficients

RTD Co-efficients	
a	0.0039083
b	-5.78E-07
c	-4.18E-12

RTD Resistance

The RTD resistance is calculated using the following equations and co-efficient from Table 3

For: $T \geq 0°C$: $$R_T = R_{(0)} * (1 + a * T + b * T^2)$$

For: $T \leq 0°C$: $$R_T = R_{(0)} * [1 + a * T + b * T^2 + c * (t - 100°C) * T^3]$$

Transducer Analysis

With the transducers selected the measurement signal resolution is needed to determine the error budget and noise floor requirements. Both transducers can be energized by a constant current source, however only the RTD provides a measurement current value of 1.4 mA, this current will be assumed to be the same for both, however it could be made to be configurable in a later design.

Using the datasheet information the resistance curves can be plotted for both the transducers. The uncertainty of the transducer signal is the error present in the voltage across smallest resistance on the curve.

Strain Gauge Error

From the plotted resistance curve in Figure 2 Figure 2 Strain Gauge Resistance vs Lengththe lowest voltage for the strain gauge occurs at a minimum theoretical resistance of 339.5 Ω and is equal to 475 mV with a 1.4mA source, and with a resistance tolerance of 0.2% and a current tolerance of 1%.

Strain gauge voltage resolution: $\Delta V_{SG} = 0.475 * 0.012 = 0.0057 = \pm 5.7mV$

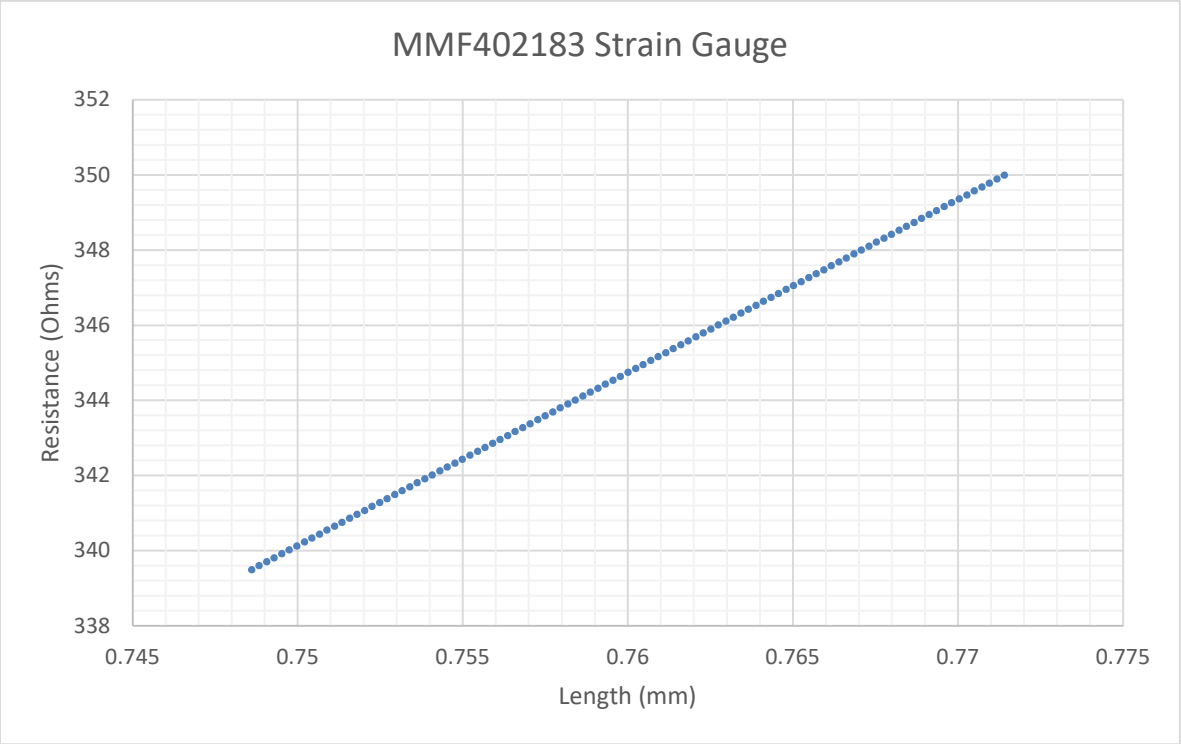

Figure 2 Strain Gauge Resistance vs Length

RTD Error

From the plotted resistance curve in Figure 3 the lowest voltage for the RTD occurs at a minimum theoretical resistance of 80.31 Ω and is equal to 113mV with a 1.4mA source, and with a resistance tolerance of 0.12% and a current tolerance of 1%

RTD voltage resolution: $\Delta V_{RTD} = 0.113 * 0.0112 = 0.00129 = \pm 1.29mV$

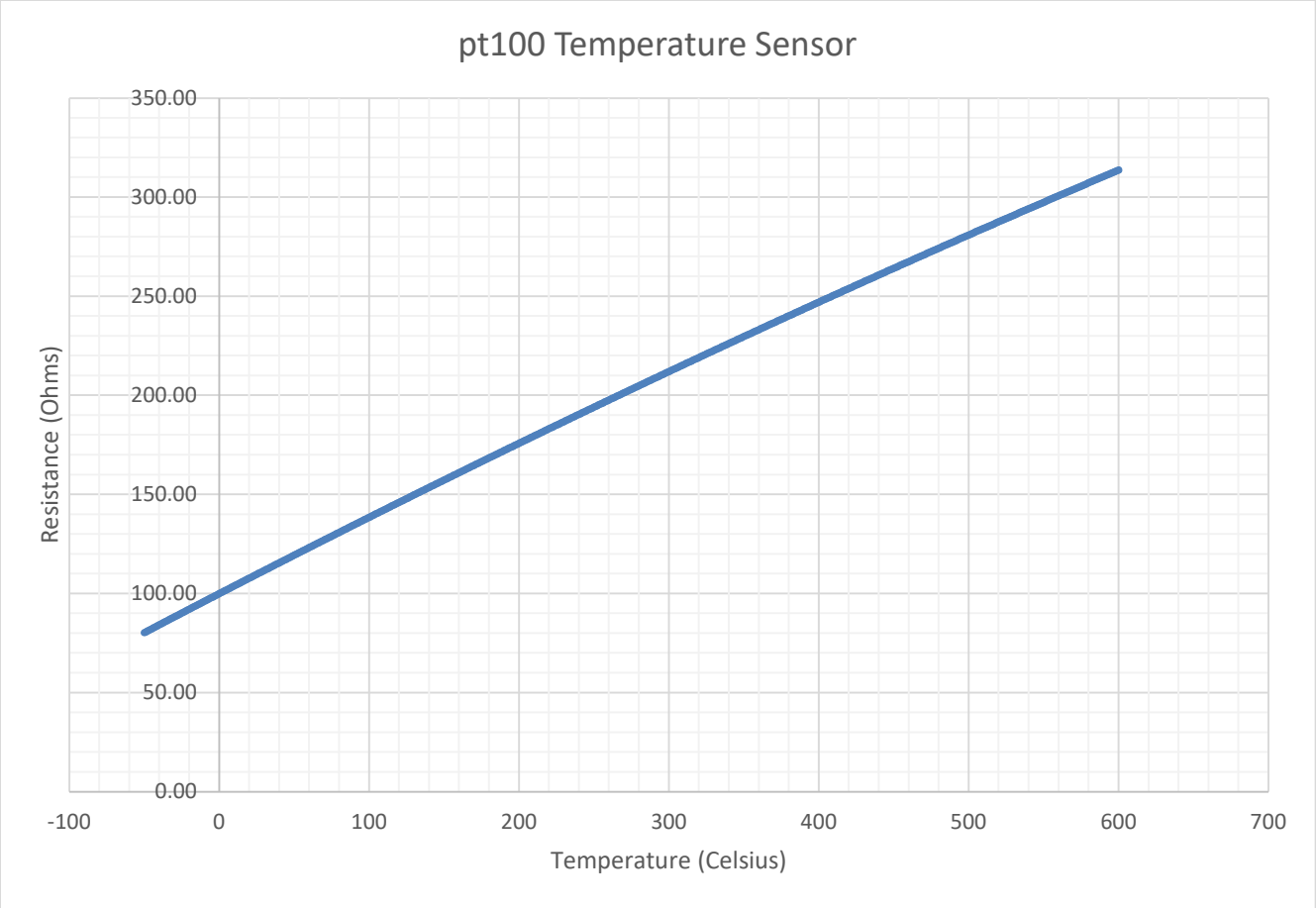

Figure 3 RTD Resistance vs Temperature

Multiplexer – 2-Channel Precision Analog Differential MUX

Based on the design notes in the design reference by Texas Instruments for a multiplexed DAQ system, the MUX36D04 is used and considered a good choice for an analog front-end multiplexer due to its differential input, low on-resistance and fast switching time [1]. The specifications are summarized in Appendix A: Table 6.

The on-resistance and switch capacitance are important factors in considering a multiplexer since it will contribute to the source resistance noise, and the settling time. It is important that the settling time of all the components in the signal path are fast enough to maintain the ADC sample rate without errors.

See Appendix C: Multiplexer Considerations for more details on timing considerations in a multiplexed DAQ system.

Settling time

The settling time of a multiplexer t_{s_mux} is the combination of the transition time and the RC time constant of the MUX output using the R_{on}, C_D and $t_{transition}$ from the data sheet. The resistance is scaled by an error factor based on the least significant bit of a 16-bit ADC. [1]

$$\%Error = \frac{1}{2^{16}} * 100 = 0.0016\%$$

$$t_{s_{mux}} = t_{s_{RC_{out}}} + t_{s_{transition}} = -\ln\left(\frac{\%Error}{100}\right) \times (R_{ON} \times C_D) + t_{transition} \quad (5)$$

$$= -\ln\left(\frac{1}{2^{16}}\right) \times (230 \times 7.7 \times 10^{-12}) + 151 \times 10^{-9} = 173\ ns$$

The multiplexer settling time is 173 ns, which can be used to verify the sampling rate of the DAQ in the following sections.

Noise

The multiplexer will contribute primarily Johnson noise due to its on-resistance, and this will be considered in a following section, with a maximum of 230Ω per channel and 460Ω total that contributes to the input resistance.

Error

The error due to the multiplexer will be the contribution of its on-resistance to the total input resistance which can add offset voltage equivalent to the resistance multiplied by the input bias current I_B of the amplifier.

Instrumentation Amplifier

The InAmp will need to settle to its output within the ADC sample time, and have low noise, offset voltage, and bias current. The LT1167 from Linear Technology was chosen due to its low noise, high bandwidth, low gain error and detailed data sheet with Spice models available. The specifications are summarized in Appendix A: Table 7.

Amplifier Gain

The Gain of the front end is determined by the constraint that the input to the ADC should be a reasonable level with respect to the ADC full scale (FS) voltage ($\frac{FS}{2} \leq V_{in} \leq FS$). With an ADC voltage reference of 5V, the transducer signal should be amplified to at least 2.5V but not more than 5V. Using min and max values for the expected voltages of the transducers as 100mV to 500mV approximately, a gain of 10 will scale the input range as 1V to 5V, which will utilize the full-scale range of the ADC.

$$G_{Required} = \frac{V_{ref}}{V_{in(max)}} \quad (6)$$

$$G_{Required} = \frac{5V}{0.5V} = 10$$

Gain calculation (Formula from datasheet of the LT1167):

Selecting a precision 5488Ω resistor for R_G with 0.05% tolerance

$$G = 1 + \frac{49400}{R_G} \tag{7}$$

$$G = 1 + \frac{49400}{5488} = 10.001457$$

Settling time

The Amplifier datasheet lists a maximum of 14µs as the settling time for a 10V step, extrapolating from the Settling Time Vs Step Size graph in the datasheet, the settling time for a step equal to the ADC full scale input of 5V is approximately 6µs.

Noise

The noise considerations for the amplifier come directly off the data sheet with the voltage and current noise spectral density as $12\ \frac{nV}{\sqrt{Hz}}$ and $124\ \frac{fA}{\sqrt{Hz}}$, respectively. These numbers will be used in a following section to calculate the total noise of the system.

Gain error

From the Datasheet for the LT1167:

Input offset voltage V_{OS} = 60µv; drift = 0.3µv/°C
Input bias current I_B = 350pA
Gain Error = 0.08%

The gain error is a combination of datasheet listed gain error of 0.08% as well as resistor component error of 0.05%

The Gain error due to resistor tolerance:

$$G_{min} = 1 + \frac{49400}{5490.744} = 9.996959$$

$$G_{max} = 1 + \frac{49400}{5485.256} = 10.00596071$$

$$Error\ _{component} = \frac{10.00596061 - 9.996959}{2} = 0.0045$$

$$Error_{Component}\% = \frac{0.0045}{10.001457} = 0.045\%$$

$$GainError\% = \pm(0.08 + 0.045)\% = \pm 0.125\%$$

Input error

The input error is a combination of the input offset voltage, and the additional input offset voltage due to the input bias current through the source resistance which is the total of the sensor and multiplexer on-resistance.

Considering a drift of 25°C to include error for a system operating temperature range of 0-50°C

$$V_{Drift} = DriftRate * Temp \tag{8}$$

$$V_{Drift} = 0.3\frac{\mu V}{°C} * 25°C = \pm 7.5\mu V$$

$$V_{OS_{Total}} = V_{OS} + I_B * R_S + V_{Drift} \tag{9}$$

$$V_{OS_{Total}} = 60\mu V + 350pA * (350\Omega + 460\Omega) + 7.5\mu V = \pm 67.784\mu V$$

ADC – 16 bit-SAR-S/H

The ADC is selected ADS8864 by Texas instruments, based on available design references, 16-bit resolution, high sample rate and fast settling time. The specifications are summarized in Appendix A: Table 8.

ADC Charge-Kickback Filter

The datasheet for the ADS8864 recommends an input filter to provide antialiasing as well as to reduce the effects of the internal sampling capacitor as it discharges between samples.

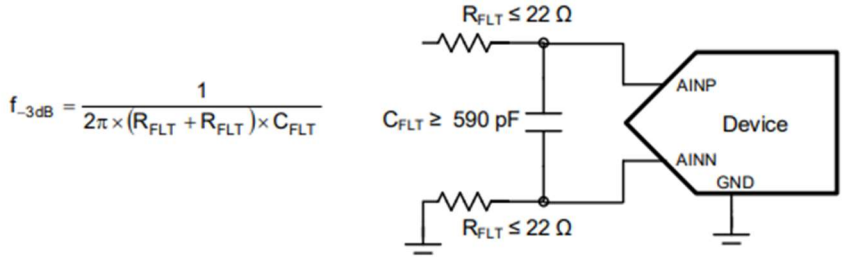

Figure 4 Recommended FilterADS8864 Datasheet

Following the above recommendations and selecting R_{FLT} = 22 Ω, C_{FLT} = 1nF. The bandwidth and settling time of the filter are found as follows. 1nF is selected based on the max load capacitance listed in the previous stage gain amplifiers datasheet.

$$BW = \frac{1}{2\pi(R_{\mathrm{FLT}}+R_{\mathrm{FLT}})C_{\mathrm{FLT}}} \tag{10}$$

$$BW = \frac{1}{2\pi * 44 * 1 \times 10^{-9}} = 3.62\ \mathrm{MHz}$$

$$t_{s_{alias}} = -\ln\left(\frac{1}{2^{16}}\right) \times (R_{\mathrm{FLT}} + R_{\mathrm{FLT}} \times C_{\mathrm{FLT}}) \tag{11}$$

$$t_{s\_alias} = -\ln\left(\frac{1}{2^{16}}\right) \times (44 \times 1 \times 10^{-9}) = 0.48\,\mu s$$

Note:

The cut off frequency of the anti-aliasing filter does not meet the Nyquist-Shannon criterion of at least half the sample rate, however the InAmp is stable for a maximum of 1nF output capacitance.

Settling Time

The stages leading up to the ADC input must settle to within the required resolution (16 bits) during the ADC acquisition window. The time for each sample acquisition in the ADC is 2.4 µs based on the data sheet. Therefore, the signal path must settle to within a 16-bit resolution in that time with a worst-case voltage step of +5V

The total settling time t_{s_total} can be found by taking the root sum square of each stages settling time. [1]

The settling time of the InAmp can be acquired off the graphs in the data sheet for 5V to be approximately 6 µs

$$t_{s\_total} = \sqrt{{t_{s_{mux}}}^2 + {t_{s_{inamp}}}^2 + {t_{s_{alias}}}^2} \tag{12}$$

$$t_{s\_total} = \sqrt{.173^2 + 6^2 + 0.48^2} = 6.02\,\mu s$$

Noise

The Data sheet for the ADS8864 states that the front-end noise must be below the value set by this formula to maintain the stability of the ADC

$$FrontEnd_{noise} = \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\frac{SNR}{20}} \tag{13}$$

$$FrontEnd_{noise} = \frac{1}{5} \times \frac{5V}{\sqrt{2}} \times 10^{-\frac{93dB}{20}} = 15.8\,\mu V_{rms}$$

Error

ADC Resolution is given by the full-scale output divided by the number of voltage levels, which gives the voltage level of the smallest step size, the “least significant bit” LSB.

$$LSB_{Resolution} = \frac{V_{ref}}{2^n} \tag{14}$$

$$LSB\_Resolution = \frac{5V}{2^{16}} = 76.29\ \mu V$$

The Quantization Error is given by half LSB resolution as $^{76.29}/_{2} = 38.14\ \mu V$

Final Analysis

Settling time

The total settling time of the front end is dominated by the InAmp and is approximately 6.02µs, the acquisition time of the ADC is 2.4µs, therefore, to achieve an accurate sample the ADC will need to be run at a slower sample rate.

Noise

The full spectrum noise of the front end is given by the following equation that is further explained in Appendix B. It is the gain multiplied by the root square sum of the primary sources of noise. Which are briefly the Johnson noise of the input resistance, the InAmps input voltage noise spectral density, and the input current noise spectral density through the input resistance.

$$V_n = G\sqrt{\left(4kTR_s + {e_n}^2 + {i_n}^2{R_s}^2\right)} \quad [V_{rms}] \tag{15}$$

G = Amplifier Gain, T = 298.15 Kelvin, k = Boltzmann constant = $1.3806*10^{-23}$

From the data sheet for LT1167: $e_n = 12*10^{-9}$, $i_n = 124*10^{-15}$

The maximum input resistance for this application is the combination of the highest input resistance possible, in this case the strain gauge plus the multiplexer on-resistance for 2 channels. And neglecting the gain error for now.

$$R_s = R_{SG} + R_{MUX} = (2 * 230) + 350 = 810$$

$$V_n = G\sqrt{4(1.3806 \times 10^{-23} \times 298.15 \times 810) + (12 \times 10^{-9})^2 + (124 \times 10^{-15})^2 \times (810)^2}$$

$$= G \times 12.54\ nV_{rms} \quad = 10.001457 \times 12.54 \times 10^{-9} = 130\ nV_{rms}$$

The front-end noise of $130\ nV_{rms}$ as calculated above is much smaller than the requirements of the ADC of $15.8\ \mu V_{rms}$

Error

Transducers

Recall that the strain gauge and RTD have a resolution or uncertainty of $5.7\ mV$, and $1.29\ mV$ respectively due to component tolerances.

System Front-End

The total error of the front-end is the combination of the error due to noise and the gain due to offsets, leakages and gain errors.

Front-end noise before gain:

$$V_n = 12.54\ nV_{rms}$$

$$V_{n\_peak} = 12.54\ nV_{rms} * 1.4142 = 17.74\ nV_{peak}$$

Input Errors before gain are $\pm 67.784 \mu V$, The total input error is then:

$$\pm(67.784 \mu V + 17.74\ nV) = \pm 67.8\ \mu V$$

Since this is significantly lower than the error due to the transducer tolerance the system will not degrade the measurement signal.

The system absolute accuracy and accuracy relative to input for the given transducers are then determined using equation (1) and equation (2) respectively, for a maximum transducer voltage of 490mV at 0°C to 25°C

$$Absolute\ Accuracy = \pm[(490mV * 0.00125) + 67.8\mu V]$$

$$= 680.3\mu V$$

$$System\ accuracy\ RTI = \pm \frac{Absolute\ Accuracy}{Input\ Voltage} = \frac{680.3\mu V}{490mV} = 0.1388\%$$

Simulation

Modeling the system transient behavior in LTspice as seen in Figure 5, using a simplified multiplexer model based on the specified resistances and capacitances, and using a generic ADC with sample period of 10µs, and a multiplexer switching period of 20µs. The first channel has a max input voltage corresponding to a transducer resistance of 350Ω, while the other channel a minimum voltage due to a minimum resistance of 100Ω, this will cause a maximum expected voltage step from 4.9V to 1.4V at the output of the InAmp.

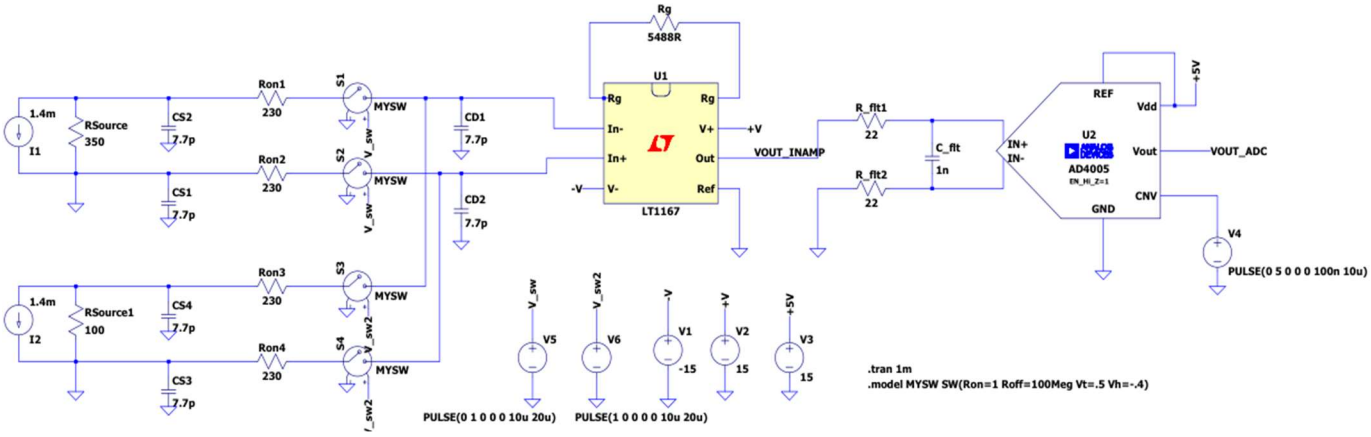

Figure 5 System Simulation

Simulation output

The signals:
Green: ADC output voltage
Blue: InAmp output voltage
Red: InAmp differential input voltage
Teal: Multiplexer switching signal

From the simulation output seen in Figure 5, the cursors indicate that the InAmp is able to setting within 6µs, and as the signal switches from channel 1 to channel 2, the ADC is able to correctly capture the voltage at the point where the signal has settled.

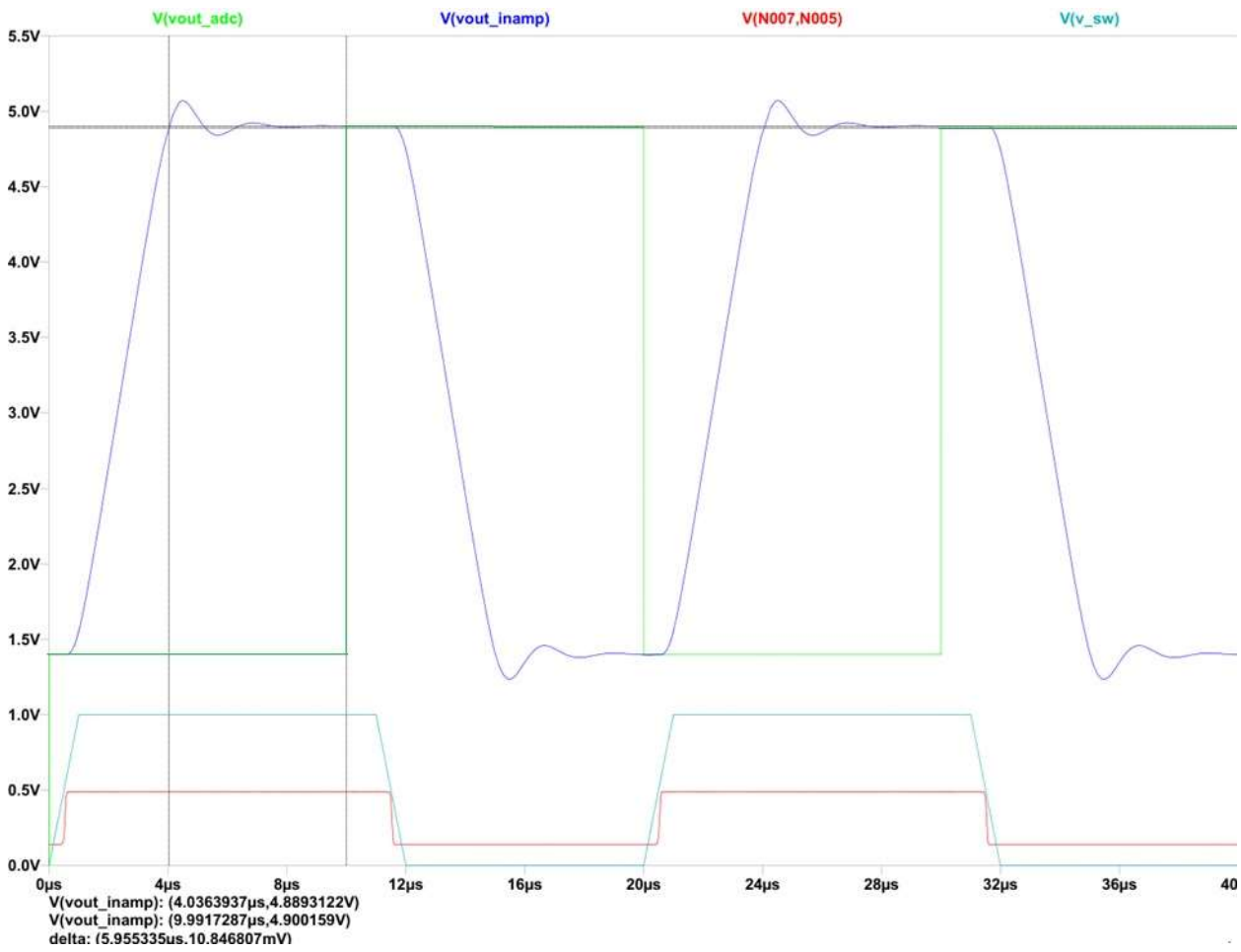

Figure 6 Circuit Simulation Traces

Results

The analysis above produced the following results that define the characteristics of the DAQ.

The DAQ system Accuracy and specifications for 0°C to 25°C:

Number of Differential Channels	2
Sample Rate/Channel	50 kHz
Gain Error %	0.125%
Offset Error	± 67.83µV
Absolute Accuracy RTI	±0.1388%
Input noise	12.54 nV_{rms}

Conclusion

The design process followed above has succeeded in proving that the front-end amplifier components and configuration generate low noise that is well within the resolution required for the proposed application.

Noise calculation

The ADC requires input noise less than 15.8 μV_{rms} to function correctly, while the front-end signal path was calculated to have 130 nV_{rms}. It should be noted that the formula used for the front-end noise is the full-spectrum noise and the anti-aliasing filter will further reduce this.

Settling Time

The settling time of the InAmp output is causing the front end to exceed acquisition time of the ADC; therefore, the ADC sample rate was reduced to allow for an accurate measurement.

Error

The total system accuracy of ±0.1388% was determined to be less than the error of the transducer itself, therefore the DAQ system as designed will not degrade the transducer signal and is accurate enough to detect the smallest reliable signals expected for the proposed application.

Recommendations

The design detailed above had many simplifications to provide a basic understanding of the concepts accuracy and noise as they relate to the design of a DAQ, the design should be developed further to handle the following omissions and issues found during the design. The input protection and filtering should be considered a top priority as ESD protection is a common requirement for commercial/industrial products. And input filtering can help improve the quality of the measurement if there are significant environmental noise factors. The main issues in the above design relate to the settling time of the InAmp, as a result the ADC sample rate must be slowed down. The InAmp also has a load capacitance limitation that effects the anti-aliasing filter cut off frequency to not meet the Nyquist-Shannon criterion. The recommended solution is to change the InAmp for one with similar noise and accuracy specifications but with faster settling time and the ability to drive higher capacitance loads.

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Appendix A: Component Specifications

Component Specification Summary

Table 4 Strain Gauge Specifications

Strain Gauge Part#:	MMF402183
Cost:	$ 44.57
Resistance (ohms)	350
Resistance Tolerance (%)	0.20%
Strain range (%)	1.50%
Length (mm)	0.76
max deflection (mm)	0.0114
ΔR (ohms)	10.5
GF	2

Table 5 Selected RTD specifications

RTD Part #:	NB-PTCO-002
Cost:	$ 4.61
Resistance @ 0°C	100
Tolerance (%)	0.12%
Operating Current (A)	0.0014

Table 6 Multiplexer Specifications

MUX36D04	max	
On-Resistance	230	ohm
Transition time	151	ns
Output Capacitance	7.7	pF

Table 7 InAmp Specifications

LT1167		
Input Offset Voltage @ G=10	60	uV
Input Bias Current	350	pA
PSRR @ G=1	105	dB
CMRR @ G=1	90	dB
Voltage Noise @1kHz	12	$nV/(Hz^{0.5})$
Current Noise	124	$fA/(Hz^{0.5})$
Setting time 10V step	14	uS
Slew Rate	1.2	V/us
Bandwidth G=1	1000	kHz

Bandwidth G=10	800	kHz
Bandwidth G=100	120	kHz

Table 8 ADC Specifications

ADS8864		
Resolution	16	bits
Sample rate	400	kHz
SNR	93	dB
Acquisition time	1200	ns
Conversion Time	1300	ns
Sample time	2500	ns

Appendix B: Precision and low noise circuits

This section is a literature review on precision and low noise circuits from the Art of Electronics 15th Edition. Chapters 1, 5 and 8. [7]

Chapter 1.3 - Signals

Noise: A term that applies to random variations in signal, typically of a thermal origin. Noise voltages are specified by their frequency spectrum (power per hertz) or amplitude distribution.

Band-limited white Gaussian noise is one of the most common kinds of noise. It is a signal with equal power per hertz in some band of frequencies (Flat frequency response), but many instantaneous samples of the amplitude have a Gaussian (bell-shape) distribution. When this kind of noise is generated by a resistor it is known as Johnson or Nyquist noise.

Chapter 5 – Precision Circuits

Precision vs Dynamic range

A 5-digit multimeter is high precision, accurate to 0.01% or better voltage measurements. And has a high Dynamic range: can measure millivolts and volts on the same scale. Input offsets can create disproportionate errors near zero since an offset error has greater effect on measurements of a smaller magnitude.

Error budget

Represents the result of the design

Error Terminology:

- Zero-Error – Measuring a reading when it should measure zero

- Input offset voltage V_{OS} – The voltage that must be applied to the inputs to obtain zero volts at the output (related to zero-error)
- Input bias current I_B: Contributes to V_{OS} by creating a voltage across the source impedance
- Full-scale accuracy (scale accuracy) – The error is the same anywhere in the measurement scale ex +/- 1% of scale will have a 1% of FS error whether the input is near zero or near FS

(a) first, you've got to identify and quantify the sources of error within a circuit to create an error budget; and

(b) strict worst-case design requires that all components (passive and active) be operated

within their datasheet specifications, and that the effects of their guaranteed worst-case errors be added (as unsigned magnitudes) to determine the overall circuit's performance.

Design of a precision amplifier with null offset Example

Front end begins with an InAmp, with high common-mode rejection, gain selection with a single resistor. When selecting an op-amp look for, low input current, offset drift and noise.

Sources for errors in op-amp circuit:

(a) Errors in the external network components
(b) Op-amps and amplifier errors with associated input circuitry
(c) Op-amp and amplifier errors with associated output circuitry

Notes:

- Look at resistor tolerances, input offset voltage, errors due to finite slew rates (distortion).

Error budget items:

(a) Data sheet parameters (Knowns)
(b) Estimates of poorly specified/unspecified parameters (Known unknowns)
(c) Parameters that are overlooked (Unknowns)

Examples
1. ×100 Difference amplifier (U1: LT1167A) at 25 C

Offset voltage: 40 μV.
Noise voltage (0.1–10 Hz): 0.28 μVpp (Typically no "max" spec).
Temperature: 0.3 μV/◦C.
Power supply: 28 nV/100 mV change.
Input offset current ×Rs: 0.11 μV/350 Ω of Rs

Passive Component Errors:

Initial accuracy, changes in value with time (stability) and temperature, nonlinearity ("voltage coefficient"). Capacitor leakage current and dielectric absorption, the tendency of a capacitor to return to a previous state of charge.

Amplifier Input errors:

Finite input impedance, input current, voltage offset, common-mode rejection ratio, power-supply rejection ratio, and their drifts with time and temperature.

Finite input impedance: Forms a voltage divider with the input source impedance and lowers the gain., the input impedance is boot-strapped by feedback, raising its value from differential mode to common-mode levels.

Input Bias Current: Nanoamps at the input can produce microvolts for source impedances as small as 1kOhm. FET op-amps have greater input impedance and lower bias current, but greater voltage offsets. FET op-amps suffer greater input bias current drift with temperature.

Variation with common-mode input voltage: Find a datasheet that specified input current vs input voltage plotted over the full input range.

Voltage offset: Precision op-amps should be in the 10s of uV. A trimmed offset has larger drift with temperature.

Common-mode rejection (CMRR): Common mode error introduces a voltage offset as a function of the dc level across both input terminals. It is the ratio of how much a differential signal is amplified to how much a common mode signal is amplified.

$$CMRR = \left(\frac{A_d}{|A_{cm}|}\right) = 10\log_{10}\left(\frac{A_d}{|A_{cm}|}\right)^2 dB = 20\log_{10}\left(\frac{A_d}{|A_{cm}|}\right) dB$$

A_d – Differential gain
A_{cm} – Common mode gain

Power-Supply rejection (PSRR): Like CMRR but related the power supply voltage to a signal at the input, for example a 126dB PSRR at DC means a 1 volt change in one of the power supply voltages causes a change at the output equivalent to a change in the differential input signal of 0.5uV. PSRR is gain dependent. 20log(1v/0.5uv) = 126dB.

$$PSRR = 20\log_{10}\frac{\Delta V_{Supply}}{\Delta V_{in}} = 20\log_{10}\frac{1V}{0.5\mu V} = 126dB$$

Amplifier Output errors:

Limited slew rate, output crossover distortion, and finite open-loop output impedance, settling-time, gain error, gain nonlinearity.

Choosing a precision Op-amp

Voltage noise

The in-band variation of op-amp input offset voltage that is indistinguishable from the signal is called the "voltage noise-spectral density" is a function of frequency and represents the rms noise voltage in a 1Hz bandwidth of the signal and is in units of volts per square root of frequency. Data sheet values typically ranging from $0.85\left[\frac{nV}{\sqrt{Hz}}\right]$ to $325\left[\frac{nV}{\sqrt{Hz}}\right]$

Voltage Noise-spectral density: $e_n(f) \quad \left[\frac{nV}{\sqrt{Hz}}\right]$

In the flat (White noise) region of e_n above the 1/f corner the voltage noise is simply

Total Integrated Voltage Noise: $V_n = e_n\sqrt{BW} \quad [V_{rms}]$

1/f noise

1/f noise is the phenomenon that there are increasingly higher levels of noise closer to DC, however when integrating e_n the lower frequency bandwidths (starting from DC) are multiplied by a smaller frequency span so for higher bandwidths the higher frequency contributes more to the total noise. The total noise voltage depends on the noise density and the circuits bandwidth.

The mean square noise voltage is the integral of e_n^2 over the bandpass.

$$v_n^2 = \int_{fa}^{fb} e_n^2(f)df$$

$e_n(f)$ is the noise spectral density, often found in data sheets, and the bandpass is from fa to fb. The rms noise voltage is given by $\sqrt{v_n^2}$. More bandwidth = more noise, and the curves rise as $\sqrt{f}$ at the high end.

The $V_{n(pp)}$ parameter is your primary clue about an op-amp's long-term drift performance.

Bias Current

Ranging from femto-amps to microamps. The bias current of JFET and CMOS op-amps is a leakage current and increases exponentially with temperature.

Current Noise

Current noise is due to any fluctuations in bias current caused by many sources. The input current noise density i_n flows through the source impedance and contributes to the noise voltage density by i_nZ_s but is often negligible compared to the amplifier's voltage noise density due to input offset voltage error e_n. An op-amps noise-impedance $Z_n=e_n/i_n$, so the current noise can be safely ignored if $Z_s<<Z_n$.

At high frequencies the current noise may be mostly shot noise, then the lower bound on noise current noise is calculated simply buy the following:

Current noise spectral density: $i_n = \sqrt{2qI_B} \quad \left[\frac{nA}{\sqrt{Hz}}\right]$

CMRR and PSRR

CMRR tells how much the input offset voltage V_{OS} varies with common-mode input voltage. The issue is that a change in V_{OS} appears as a change in the input signal voltage. Degradation of CMRR at high frequencies is a problem, look for the plots I the datasheets. CMRR often applies to only a limited common-mode range. An inverting configuration can avoid CMRR troubles entirely. The PSRR tells how much V_{OS} varies with the power supply voltage, areas of concert are 100-120 Hz and harmonics for power-supply ripple, and high frequencies for crosstalk from other circuitry. The analog plane should be separated from the digital plane.

GBW, f_T, Slew rate and "m", and settling time

Gain-bandwidth product: The Gain Bandwidth Product (GBWP) of an amplifier is the product of the amplifier open-loop gain times the frequency at any point in the frequency range where the amplifier's response is attenuating at a rate of -20 dB per decade of frequency.

Higher GBW means higher loop gain, and higher loop gain means lower error in gain, phase and distortion.

Higher GBW means faster slew rate, and greater full-power bandwidth FPBW

Distortion

Most precision analog-design is concerned with low frequency and DC signals; however, audio, video, communications and scientific measurement require high accuracy and high speeds.

A harmonic distortion curve provides an indication of errors at higher frequencies, since at higher frequencies op-amp open loop gain decreases, and input errors increase, output impedance is rising, and slew-rate and capacitances becomes a concern.

Chapter 8 -Low noise Techniques

The random noise that is of significance is characterized by its density (rms noise amplitude in 1 Hz band of frequency) voltage noise density e_n, In units $\frac{nV}{\sqrt{Hz}}$

White noise is a noise source that is uniform over frequency, the rms noise voltage contained within a bandwidth B is.

$$V_n = e_n\sqrt{B}$$

Simple noise calculations in op-amps: find e_n and i_n Z_s to find the noise at the input and multiply by the amplifiers gain to find the output noise. To find the total noise in a circuit with multiple independent noise sources, take the sum of the squares of each noise density, multiply by the bandwidth and take the square root.

- Resistors generate Johnson Noise
- Discrete charges in flow create shot noise

Types of noise

Johnson noise: Random-noise voltage created by thermal fluctuations in a resistor, the open-circuit noise voltage generated by a resistance R, at temperature T, and filtered by a perfect bandpass filter with bandwidth B is the noise voltage.

$$v_{noise}(rms) = v_n = \sqrt{4kTRB} \quad [V_{rms}]$$

R – Resistance
T - Temperature in Kelvin
K – Boltzmann
B – Bandwidth

A resistor shorted with itself produces a current:

$$i_{noise}(rms) = \frac{v_n}{R} = \sqrt{\frac{4kTB}{R}}$$

It is convenient to express noise as a density, rms value per square root bandwidth.

$$e_n = \sqrt{4kTR} \quad \left[\frac{V}{\sqrt{Hz}}\right]$$

$$i_n = \frac{v_n}{R} = \sqrt{\frac{4kT}{R}} \quad \left[\frac{A}{\sqrt{Hz}}\right]$$

And for flat (white) noise spectrum such as Johnson noise, the rms noise voltage in some limited bandwidth B is simply:

$$V_n = e_n\sqrt{B}$$

Johnson noise sets a lower limit on the noise voltage of any detector, signal source or amplifier having resistance.

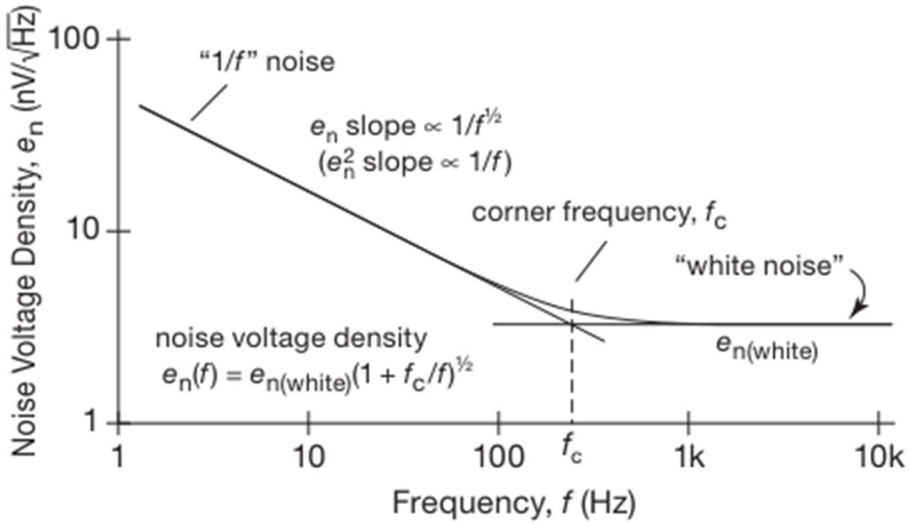
Shot noise: Random statistical fluctuations in a flowing current caused by the discrete nature of electrical charge.

$$i_n = \sqrt{2qI_{dc}} \quad \left[\frac{A}{\sqrt{Hz}}\right]$$

Is white gaussian noise, and its amplitude taken over a measurement bandwidth B is:

$$i_{noise}(rms) = \sqrt{2qI_{dc}B} \quad [A_{rms}]$$

Flicker noise: Additional random noise, rising typically as 1/f in power at low frequencies, with a multitude of causes. Such as fluctuating resistance, base-current noise and transistors and cathode current noise. Also called “excess noise” and is in addition to shot noise and Johnson noise. The noise has approximately a 1/f power spectrum which means equal power per decade of frequency, sometimes called “pink noise”, when plotted as voltage or current amplitude it falls $\frac{1}{\sqrt{f}}$



At some point the flicker noise drops to the same level as the underlying white noise, this is the corner frequency f_c, then the combination of white noise and excess noise is

$$e_n(f) = e_{n(white)}\sqrt{1 + {f_c}/{f}}$$

Band-limited noise and Equivalent Noise Bandwidth

The rms noise amplitude contained within bandwidth B was said to be

$$V_n = e_n\sqrt{B}$$

But this is only true for a "brick wall" bandpass filter of bandwidth B, for any real filter such as a first order RC filter that is not true, some power is still transferred past the cutoff frequency as it is not fully attenuated. The previous equations assume a perfect "brick wall" filter, so an equivalent noise bandwidth is used to adjust the width of the perfect filter to have the same level of noise as the actual filter. In other words, the cut off frequency is moved to make the ideal filter bandwidth larger.

For a first order RC low pass,

$$B = \frac{\pi}{2} f_{3dB} = 1.57 f_{3dB} = \frac{1}{4RC} \quad [Hz]$$

For a second order Butterworth lowpass,

$$B = 1.11 f_{3d}$$

For very low frequency or DC signals averaging can work instead of filtering (integrating ADC) in that case equivalent noise bandwidth is B=1/2T where T is the duration of the uniform averaging of the input signal.

If the noise spectrum is not just white noise, such as being 1/f noise and white noise, the noise density must be integrated over the bandpass, for the ideal "brick wall bandpass" that is

$$v_n^2 = \int e_n^2(f)df$$

From the lower cutoff frequency to the upper cutoff frequency

For a real filter with arbitrary noise spectrum, you need to multiply the noise density by the filters spectral response H(f), since that will provide the actual filter gain at each frequency including the attenuation near the fc.

$$v_n^2 = \int |e_n(f)H(f)|^2 df$$

In the case of 1/f noise and white noise the integrals can be expressed analytically and are available in tabulated form for various filter noise and filter types.

Interference

An interfering signal or stray pickup is a form of noise. This noise spectrum and amplitude characteristics depends on the interfering signal such as 60hz powerline pickup which has a sharp spectrum and almost constant amplitude. Other sources such as radio and television stations, electrical equipment, motors, elevators, switching regulators and cellphones.

Signal-to-noise (SNR) ratio and noise figure (NF)

SNR

Is the ratio of the signal voltage to the noise voltage, where the voltages are rms values at some bandwidth and center frequency.

$$SNR = 10\log_{10}\left({v_s^2}/{v_n^2}\right) = 20\log_{10}({v_s}/{v_n}) \quad [dB]$$

Noise figure

For an amplifier the NF is simply the ratio in dB of the output of the amplifier compared to the output of a perfect (noiseless) amplifier of the same gain, with a resistor of value Rs connected across the input terminals, in other words, it's the ratio of the amplifiers output response to *just* the Johnson noise of the source resistance compared to the perfect noiseless amplifier

$$NF = 10\log_{10}\left(1 + \frac{v_n^2}{4kTR_s}\right) \quad [dB]$$

v_n^2 is the mean squared noise voltage per hertz contributed by the amplifier with a noiseless (cold) resistor R_s connected across its input.

NF varies with frequency and source impedance.

Converting from NF to SNR at a source voltage V_s(rms) and impedance R_s

$$SNR = 10\log_{10}\left(\frac{v_s^2}{4kTR_s}\right) - NF \quad [dB]$$

Where the NF is calculated at Rs and in decibels.

Noise temperature

The noise temperature is an equivalent of NF and is used to express the noise performance of an amplifier. The NF and noise temperature convey the excess noise contributed by the amplifier when driven by a source impedance R_s. The noise temperature is the temperature in Kevlin that when applied to a source resistance Rs will contribute Johnson noise equivalent to the noise of the amplifier. In other words, a real and noisy amplifier with a noiseless input with resistance Rs (at absolute zero) has amplifier output noise equivalent to a perfect noiseless amplifier with a real noisy source Rs at temperature T_n.

$$T_n = T\left(10^{\frac{NF}{10}} - 1\right) \quad [K]$$

$$NF = \log_{10} 10\left(\frac{T_n}{T} + 1\right)$$

Putting it all together

Combining Johnson noise, input voltage noise, input current noise (relating to Rs), the Effective input Noise Density is of an op-amp plus source resistance is a combination of the op-amp's input voltage noise, the op-amp's current noise flowing through the signal's source impedance, and Johnson noise in the source impedance. Which are uncorrelated therefore to find the total noise-voltage density add their squares and take the square root

$$V_n = \sqrt{\left(4kTR_s + {e_n}^2 + {i_n}^2{R_s}^2\right)} \quad [V_{rms}]$$

Noise Integrals

Table of Integrated squared noise voltages ${V_n}^2$ for lower and upper frequencies of bandwidth $B = f_2 - f_1$, the term ${e_n}^2(f_2)$ is abbreviated as ${e_{n2}}^2$. For noise current substitute i_n in place of e_n

	Noise Spectral Shape		
	white	pink	red
Filter Type	$(e_n = \text{const})$	$(e_n \sim 1/\sqrt{f})$	$(e_n \sim 1/f)$
brickwall	$e_n^2\ (f_2 - f_1)$	$e_{n2}^2\ f_2 \log_e \frac{f_2}{f_1}$	$e_{n2}^2 \frac{f_2}{f_1}(f_2 - f_1)$
1-pole (*RC*)	$e_n^2 \frac{\pi}{2} \frac{f_2^2}{f_1 + f_2}$	$e_{n2}^2 \frac{f_2^3}{f_2^2 - f_1^2} \log_e \frac{f_2}{f_1}$	$e_{n2}^2 \frac{\pi}{2} \frac{f_2^3}{f_1(f_1 + f_2)}$
2-pole Butterworth	$e_n^2 \frac{\pi}{2\sqrt{2}} \frac{f_2^4}{(f_1 + f_2)(f_1^2 + f_2^2)}$	$e_{n2}^2 \frac{f_2^5}{f_2^4 - f_1^4} \log_e \frac{f_2}{f_1}$	$e_{n2}^2 \frac{\pi}{2\sqrt{2}} \frac{f_2^5}{f_1(f_1 + f_2)(f_1^2 + f_2^2)}$
m-pole Butterworth	$e_n^2 \frac{\pi/2m}{\sin(\pi/2m)} \frac{f_2 - f_1}{1 - (f_1/f_2)^{2m}}$	$e_{n2}^2 \frac{f_2}{1 - (f_1/f_2)^{2m}} \log_e \frac{f_2}{f_1}$	$e_{n2}^2 \frac{\pi/2m}{\sin(\pi/2m)} \frac{f_2 - f_1}{1 - (f_1/f_2)^{2m}}$

Figure 7: Noise Integrals [7] p.564

Noise resistance R_n

$$R_n = {}^{e_n}/_{i_n} \quad [ohms]$$

Gives the source resistance that corresponds to the minimum possible amplifier noise, is useful in finding the maximum feedback resistor value, Rs should be 5x to 30x smaller than Rn to keep En as the dominant noise source.

Appendix C: DAQ Design review

This section contains a review of various DAQ Design documents

Linear Desing Seminar – Data Acquisition Fundamentals [8]

Multiplexing

Specifications:

- Switching time
- On resistance
- On-resistance modulation
- Off-channel isolation (crosstalk)
- Grounding of un-used inputs

Filtering

- Prevents aliasing
- Reduces noise by limiting bandwidth
- In multiplexed systems, filter placed in each channel input and before the ADC
- Filter at the input of each channel is used to prevent aliasing of signals outside the Nyquist bandwidth
- The filter after the PGA must have a cut off frequency that does not distort a full scale switching from the MUX

Renesas Design considerations for a Data Acquisition system (DAS) [2]

Differential signal is beneficial for low level signals since common-mode voltages from interference noise can be removed using an instrumentation or differential amplifier.

Low level signals

Sub 100mV signals, the main issues being noise and offset voltage,

- A shielded differential signal path with twisted pair is essential to maintain noise level below 50uVrms
- Most transducers are low level and low bandwidth.
- Transmission cable must present a balanced line to sources of noise interference, meaning an equal series impedance of each conductor, and equally distributed impedance for each conductor to ground. This will provide equal and opposite signal on each cable, in phase noise, and the ability to reject the CM signal.
- Noise in transmission line is directly proportional to the source impedance driving the line.

- Transmission line may be terminated by an isolation or in-amp buffering the signal before the MUX

Filters

Passive anti-aliasing filters at the input, active band limiting filter before the ADC, 2nd order Butterworth

PGA

Unless the ratio of highest to lowest signal across any channel is <=2 the PGA is needed.

- The PGA makes sure the MSB of the ADC are utilized by maintaining FS/2 <= Vin <= FS
    - ADC resolution is FS/2^n
- PGA provides
    - Buffering: Prevents a loading effect due to the mux ON resistance
    - Differential to single ended conversion – required for SHA ADCS
    - Common mode rejection ratio

Sampling rate

Throughput rate for a DAQ may be defined as the max # of digital samples / second without exceeding an accuracy limit.

$$\text{System Sample Rate} = (\text{Highest Channel Rate}) \times (\text{Number of Channels})$$

A high sample rate is required to preserve the high frequency content of voltage transient (switching)

- A multi-channel DAQ with modest bandwidth on each channel

Multiplexer Considerations

A review of “Demystifying High-Performance Multiplexed Data-Acquisition Systems” by Maithil Pachchigar [9] and “Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design” by Texas instruments [1].

Timing

Challenges in a multiplexed DAQ system require wideband amplifiers that settle quickly while driving the ADC’s full-scale (FS) input range. The switching and sequential sampling of the MUX channels must be synchronized with the ADC conversion cycle. An issue commonly referred to as crosstalk occurs when switching between MUX channels and sampling before the

signal has settled to the correct value, this error is maximized when one channel is at the maximum positive input value while the next is at the maximum negative input value which causes a full-scale step output when switching between channels. The multiplexer should have a large bandwidth and fast switching time to minimize these errors, the on-resistance of the internal switch must be low to reduce the next stage amplifier gain errors as well. [9]

The diagram in Figure 8 shows how the input settling time and ADC must be aligned, During the ADC acquire mode, the ADC samples the input voltage on an internal sampling capacitor. And in conversion mode, the ADC disconnects the input and converts the sampled voltage to a digital value. The CONVST line indicates the conversion start control logic for the example in the reference design [1]. The minimum conversion and acquire times for an ADC are specified in the datasheet. All the components in the signal path must have a combined settling time that provides an input value to within a desired accuracy by the time the ADC is ready for the next channel conversion. The settling time of the system should be designed to be faster than the conversion time of the ADC, otherwise the ADC sample rate will have to be reduced.

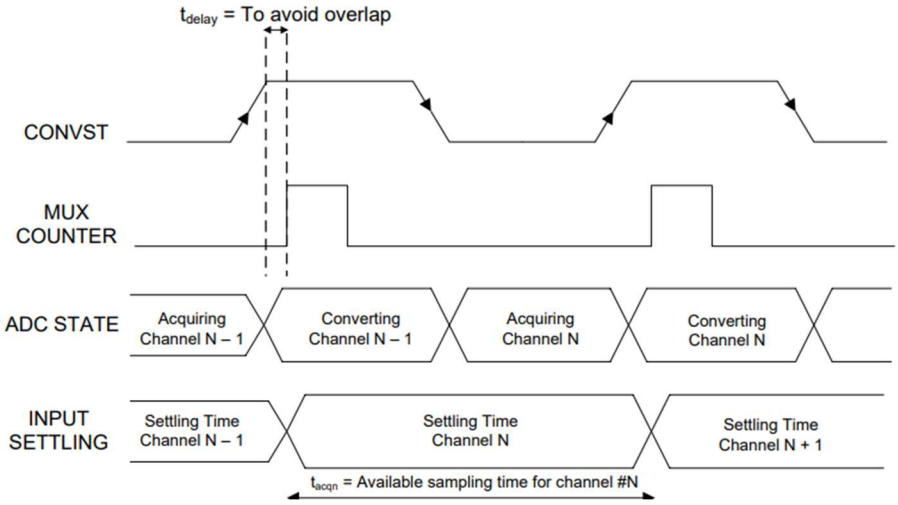


Figure 8 Multiplexed DAQ Timing diagram [1]

Appendix D: Simulation Circuit LTspice

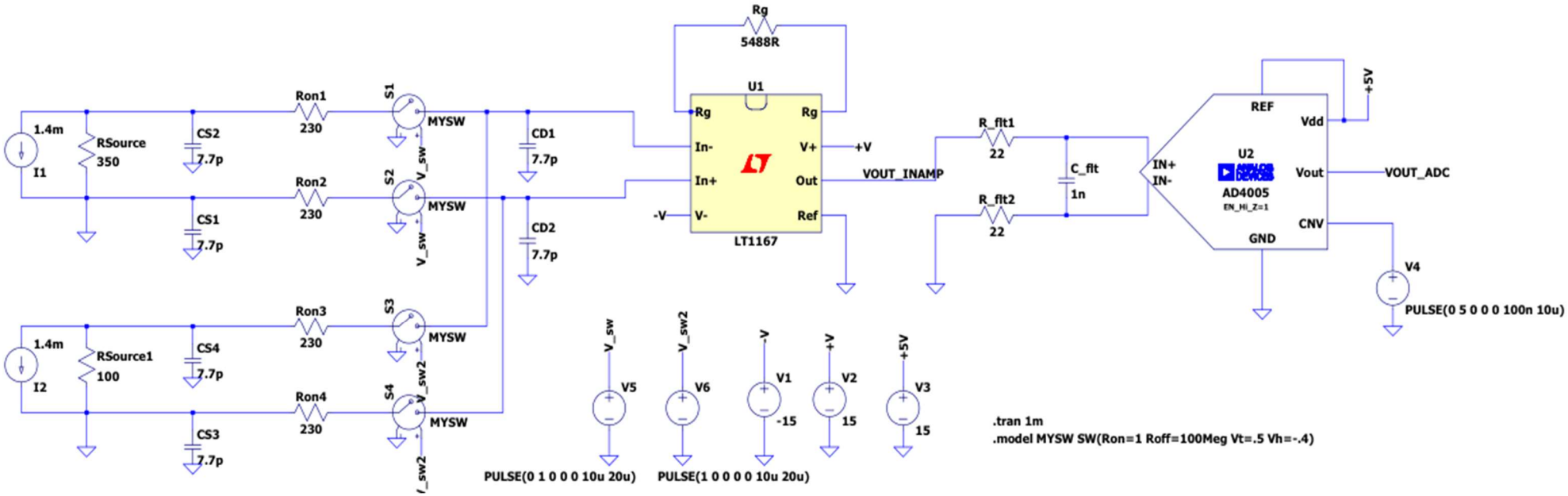


Figure 9: LTSpice full page