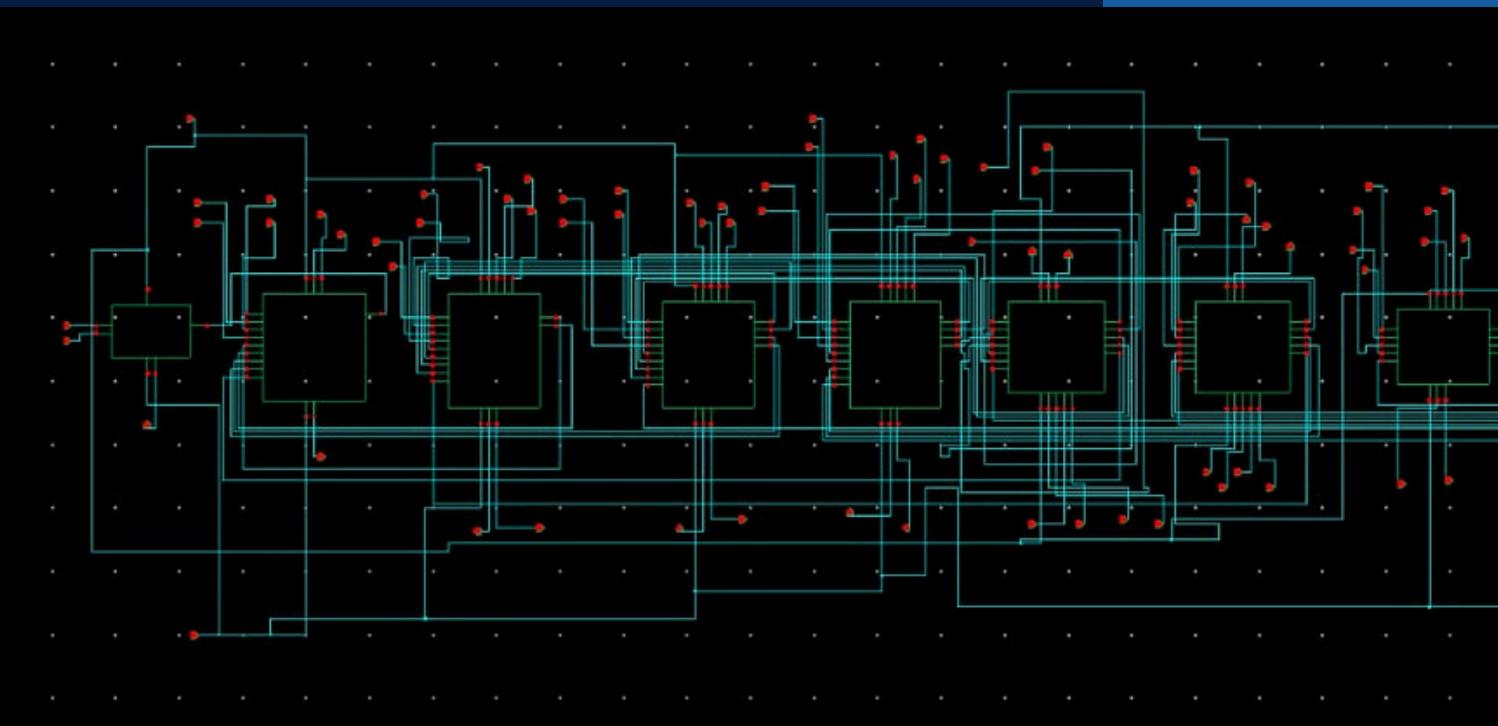
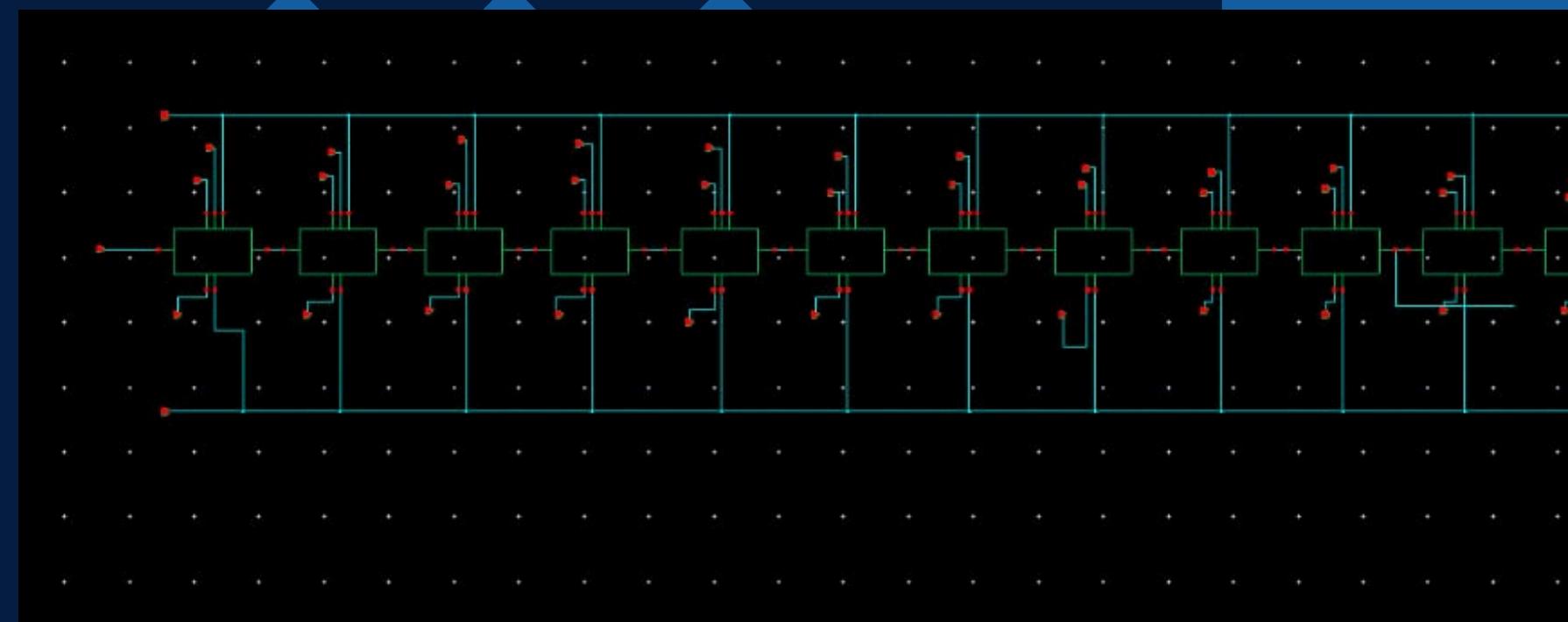
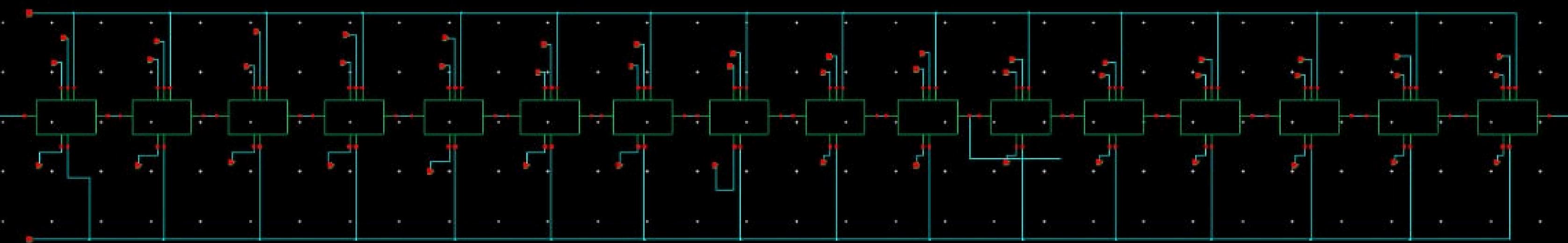


REVIEW 2

Implementing RCA and
Weinberger Adder



RIPPLE CARRY ADDER SCHEMATIC



TRUTH TABLE VERIFICATION:

0000	0000	0000	0001
0000	0000	0000	0001
0000	0000	0000	①
0000	0000	0000	0010

0000	0000	0000	1111
0000	0000	0000	00001
0000	0000	00001	DDDD

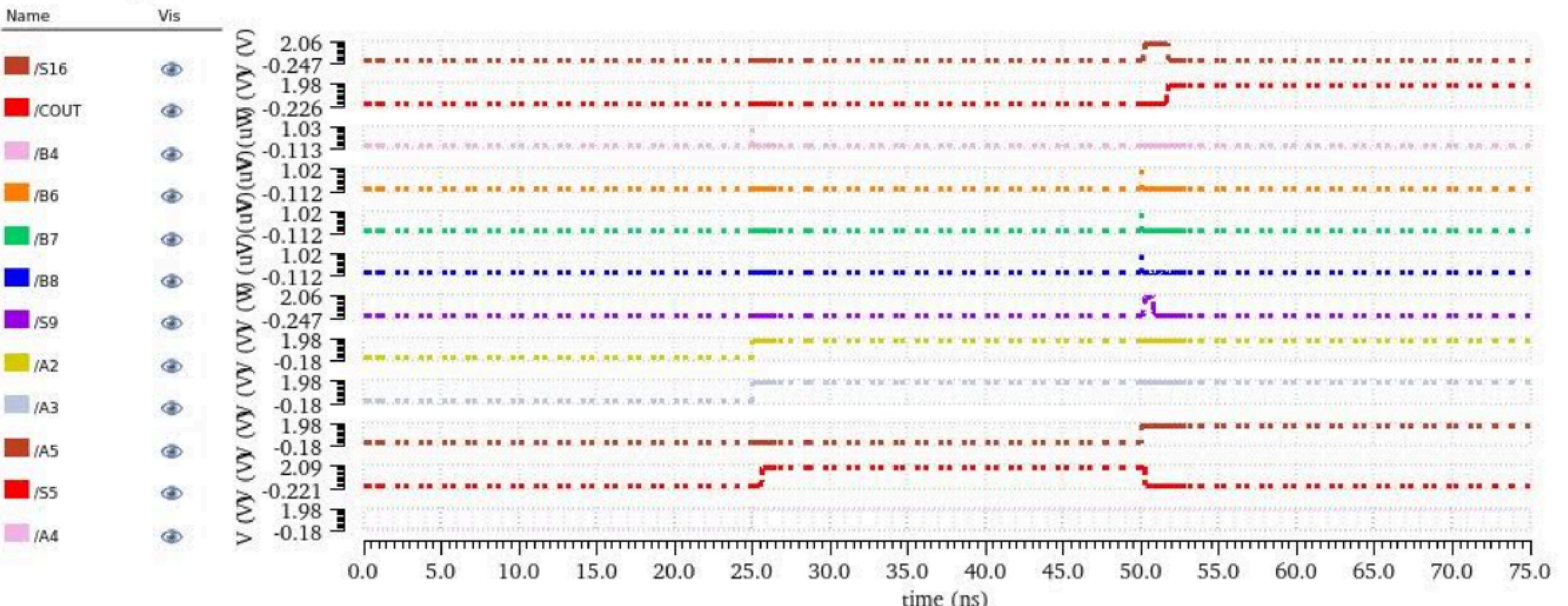
1111	1111	1111	1111
00000	00000	00000	00001
①0 000	0 000	0 000	DDDD

↓
Cout.

OUTPUT WAVEFORM

Transient Response

Wed Mar 26 09:56:59 2025 1



Transient Response

Wed Mar 26 09:56:59 2025

Transient Response

Wed Mar 26 09:56:59 2025 1

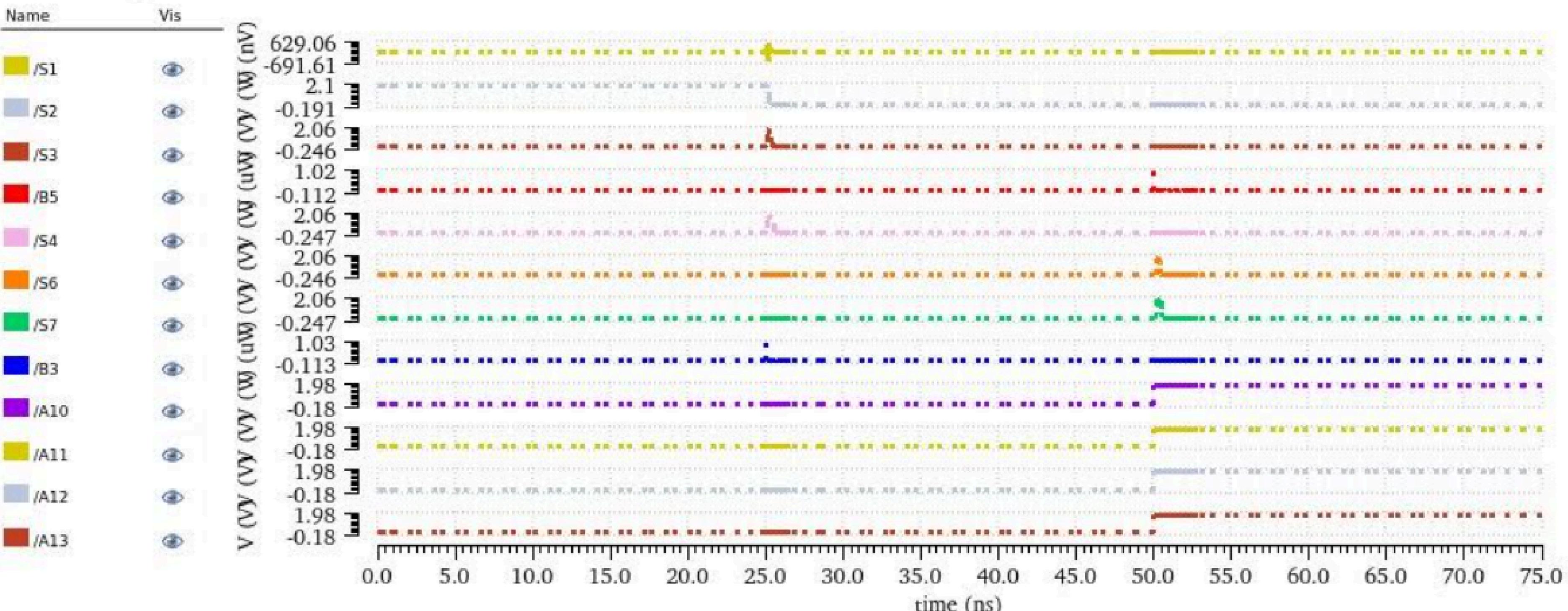
The figure displays a timing diagram with 15 horizontal traces representing different nodes. The y-axis is labeled $V (\mu V)$ and ranges from -0.18 to 1.98. The x-axis is labeled "time (ns)" and ranges from 0.0 to 75.0. Each trace shows a sequence of logic levels (high or low) over time. A legend on the left maps colors to node names:

- /A11 (Yellow)
- /A12 (Light Blue)
- /A13 (Dark Red)
- /A14 (Red)
- /A15 (Pink)
- /A16 (Orange)
- /S8 (Green)
- /B2 (Dark Blue)
- /B10 (Purple)
- /B11 (Yellow)
- /B12 (Light Blue)
- /B13 (Dark Red)

Nodes /A11, /A12, /A13, /A14, /A15, /A16, and /S8 are high (around 1.98-2.06 μV) for most of the time. Nodes /B2, /B10, and /B11 are low (around -0.112 μV). Node /B12 is high for the first 25 ns and then goes low. Node /B13 is low for the first 50 ns and then goes high.

Transient Response

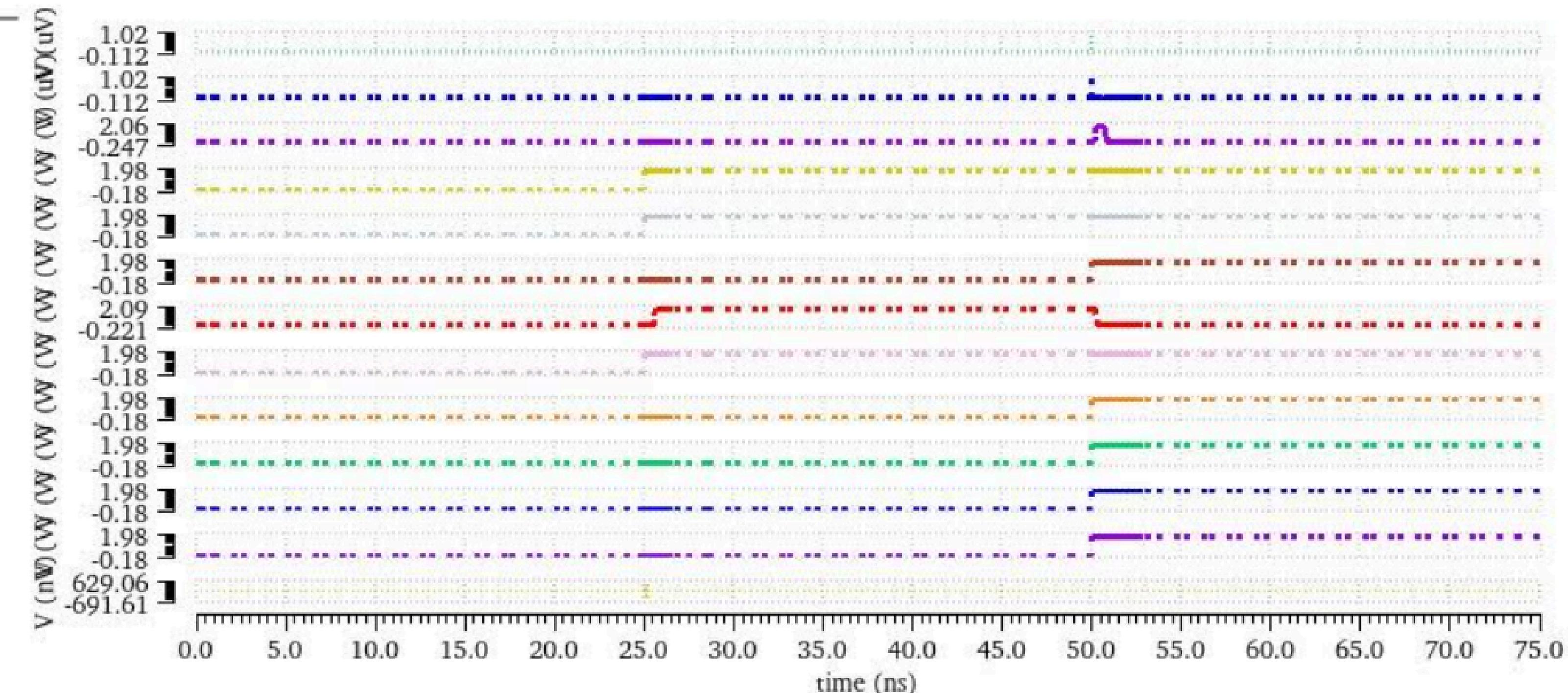
Wed Mar 26 09:56:59 2025



Transient Response

Wed Mar 26 09:56:59 2025 1

Name	Vis
 /B7	
 /B8	
 /S9	
 /A2	
 /A3	
 /A5	
 /S5	
 /A4	
 /A6	
 /A7	
 /AB	
 /A9	
 /S1	



WEINBERGER ADDER ARCHITECTURE

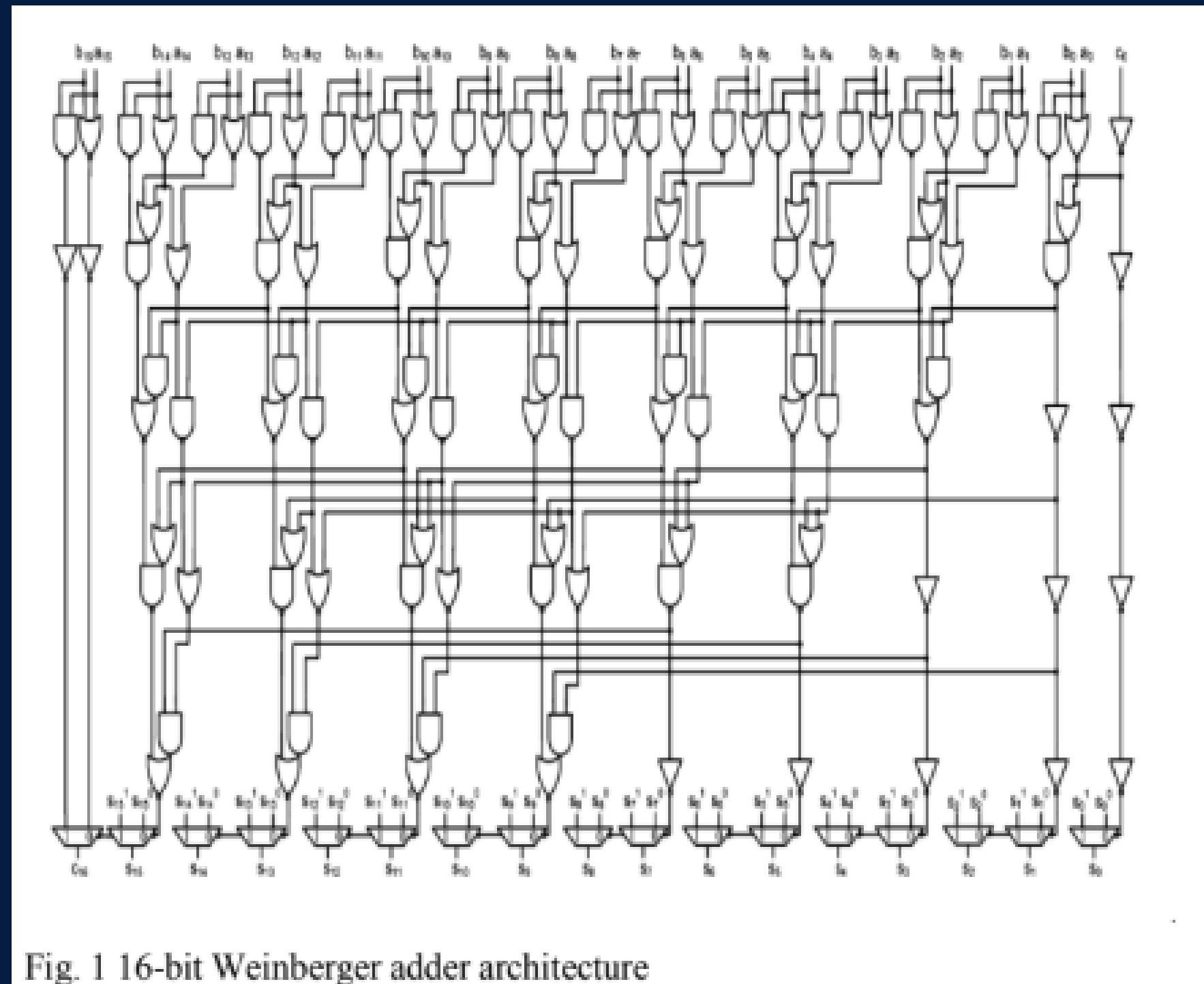
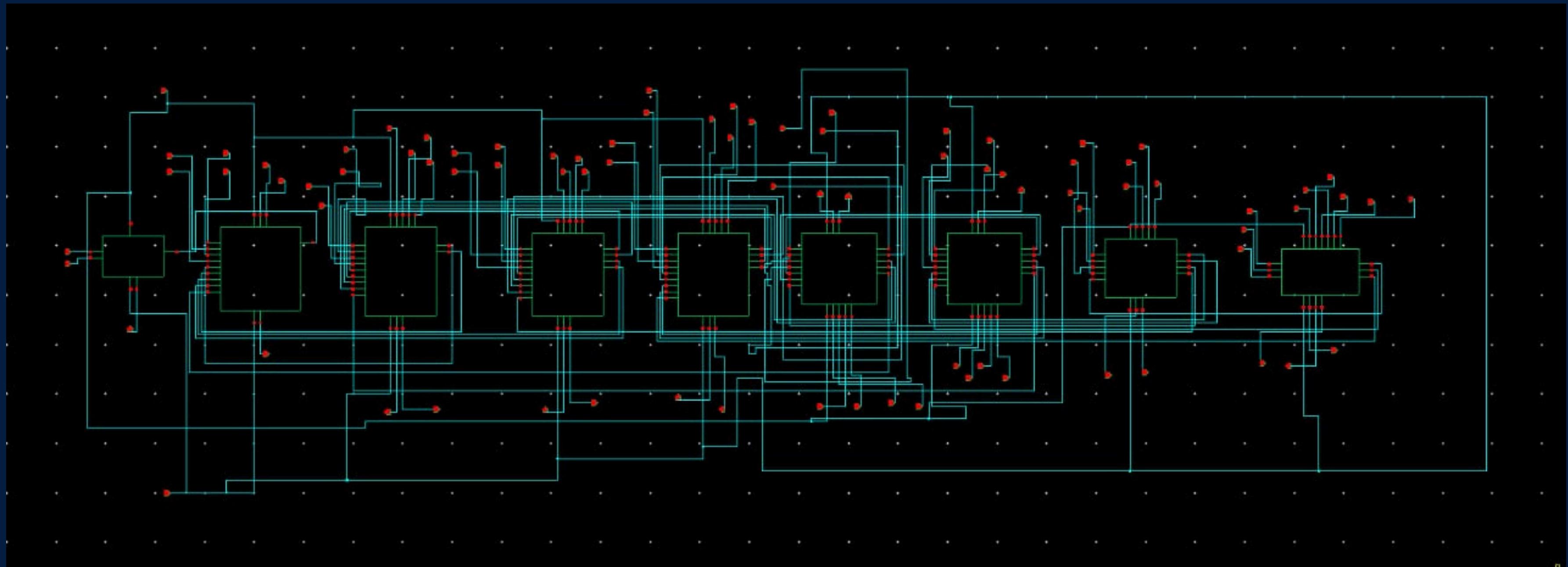
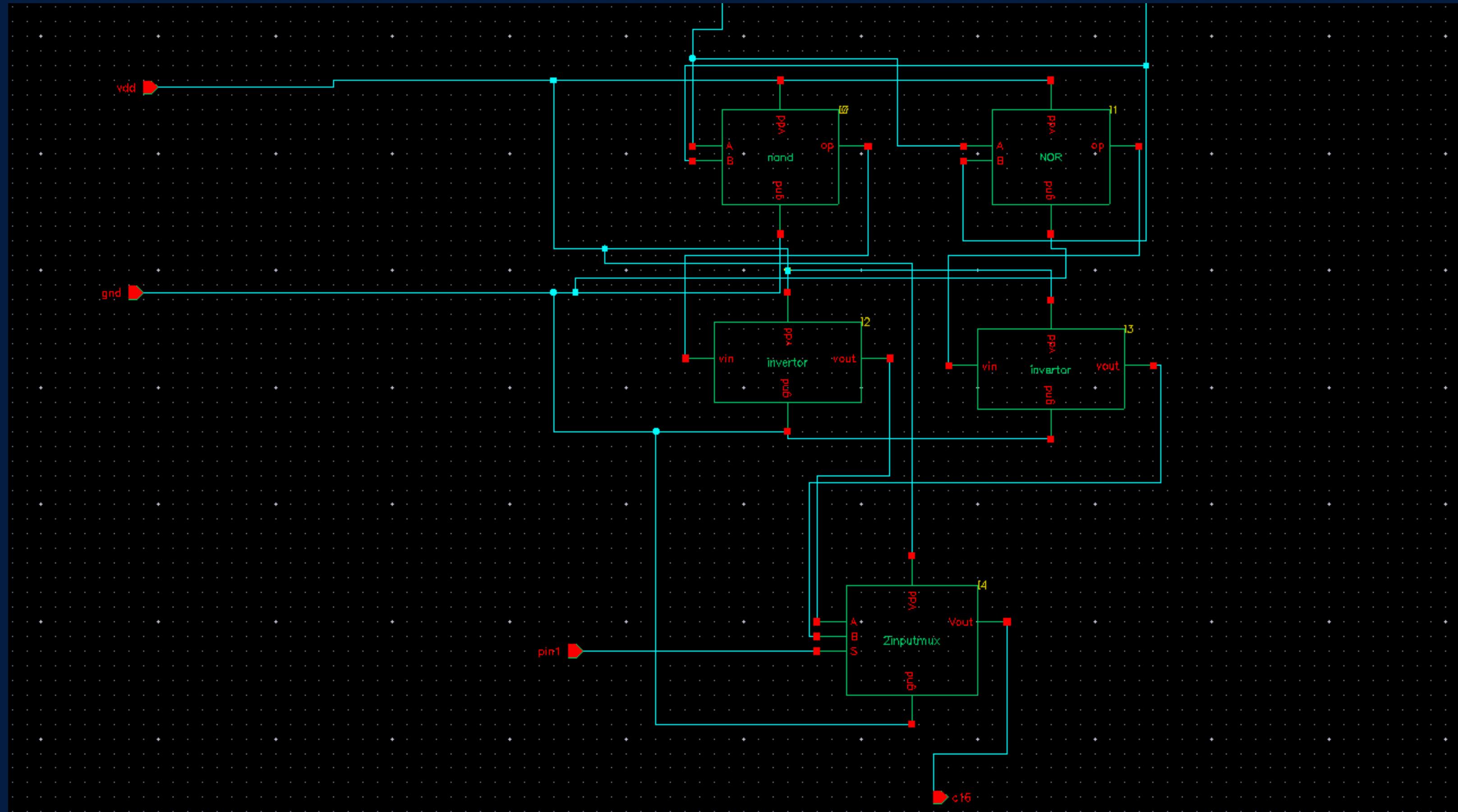


Fig. 1 16-bit Weinberger adder architecture

WEINBERGER ADDER SCHEMATIC



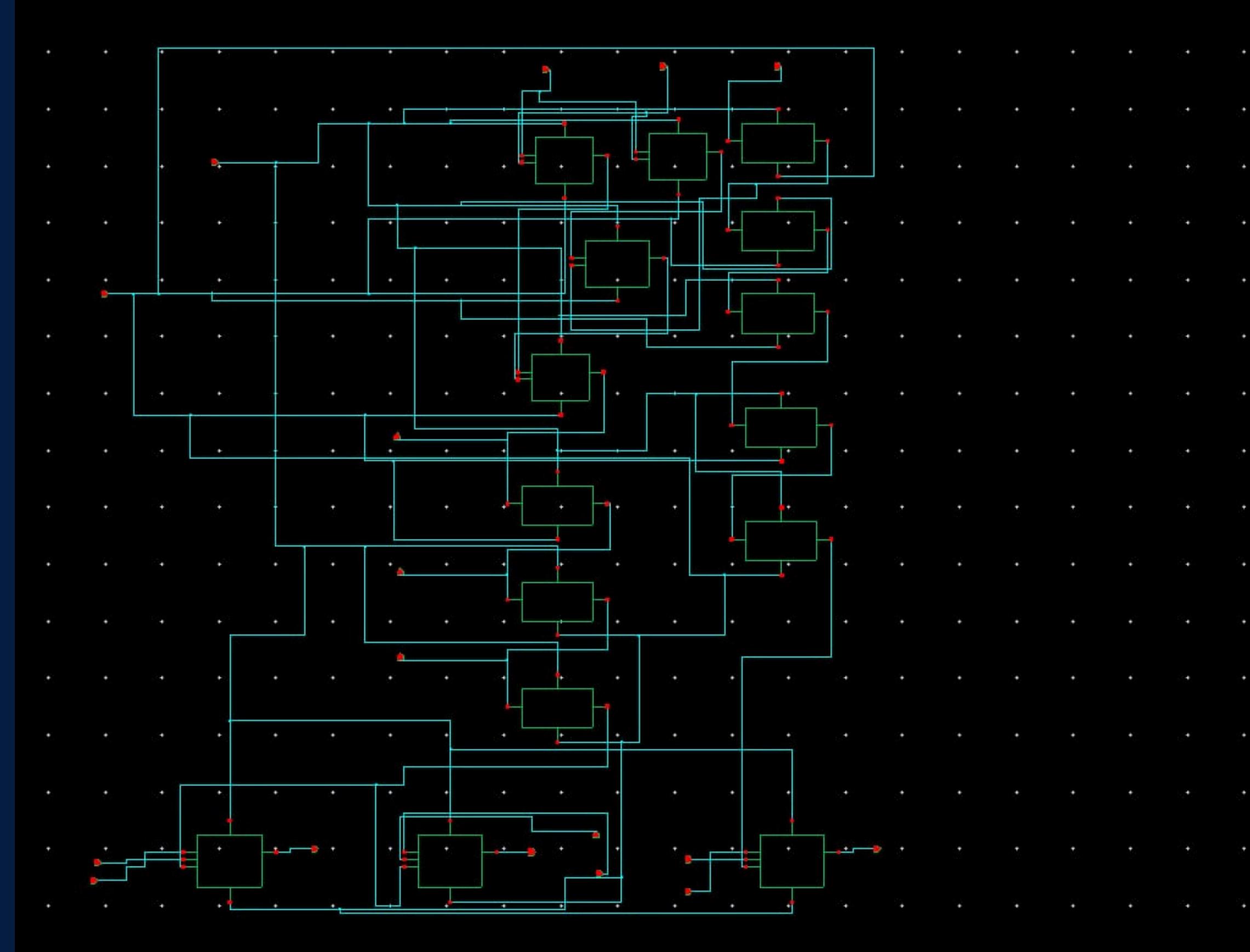
Schematic a15b15



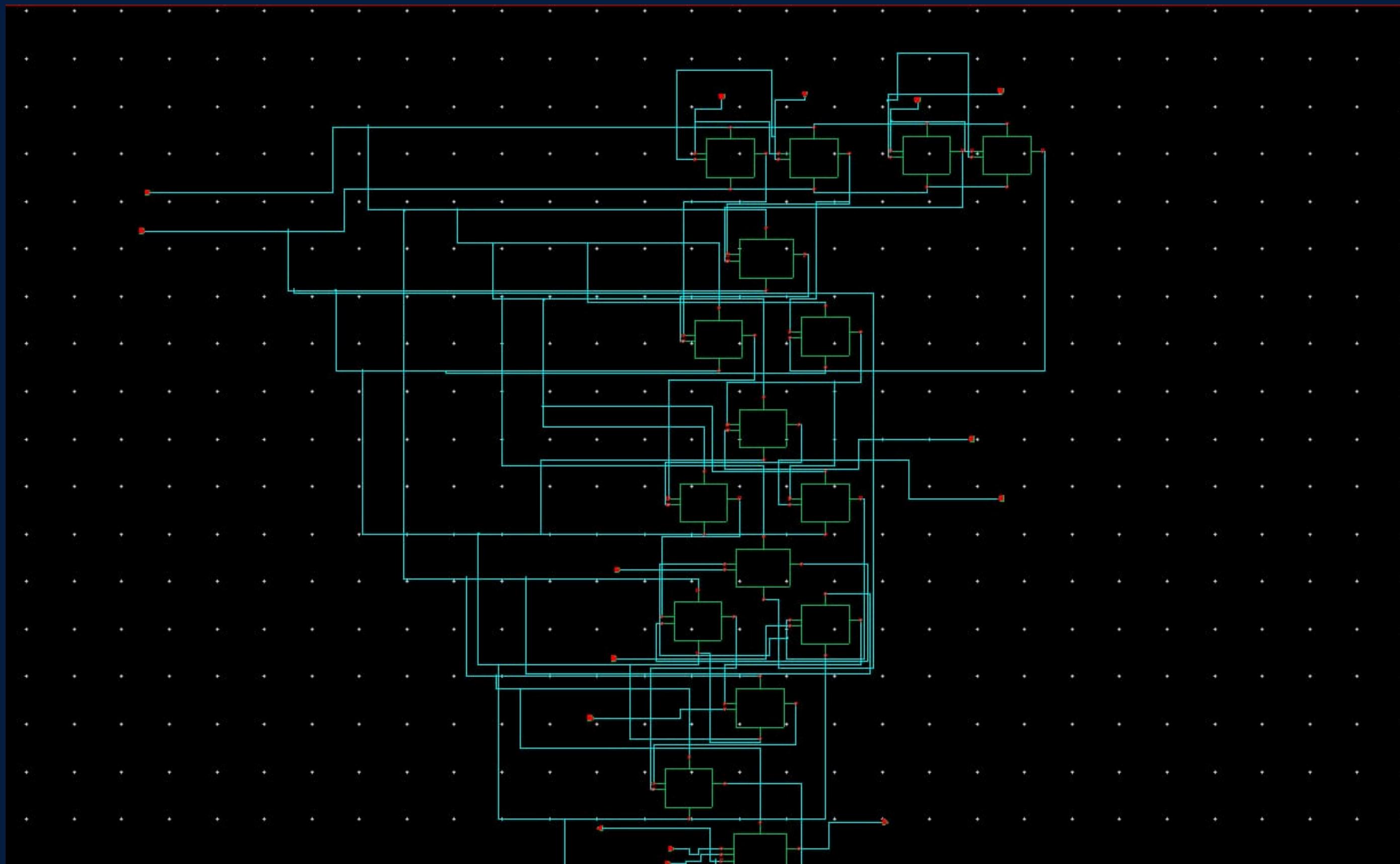
Schematic a14b14-a13b13



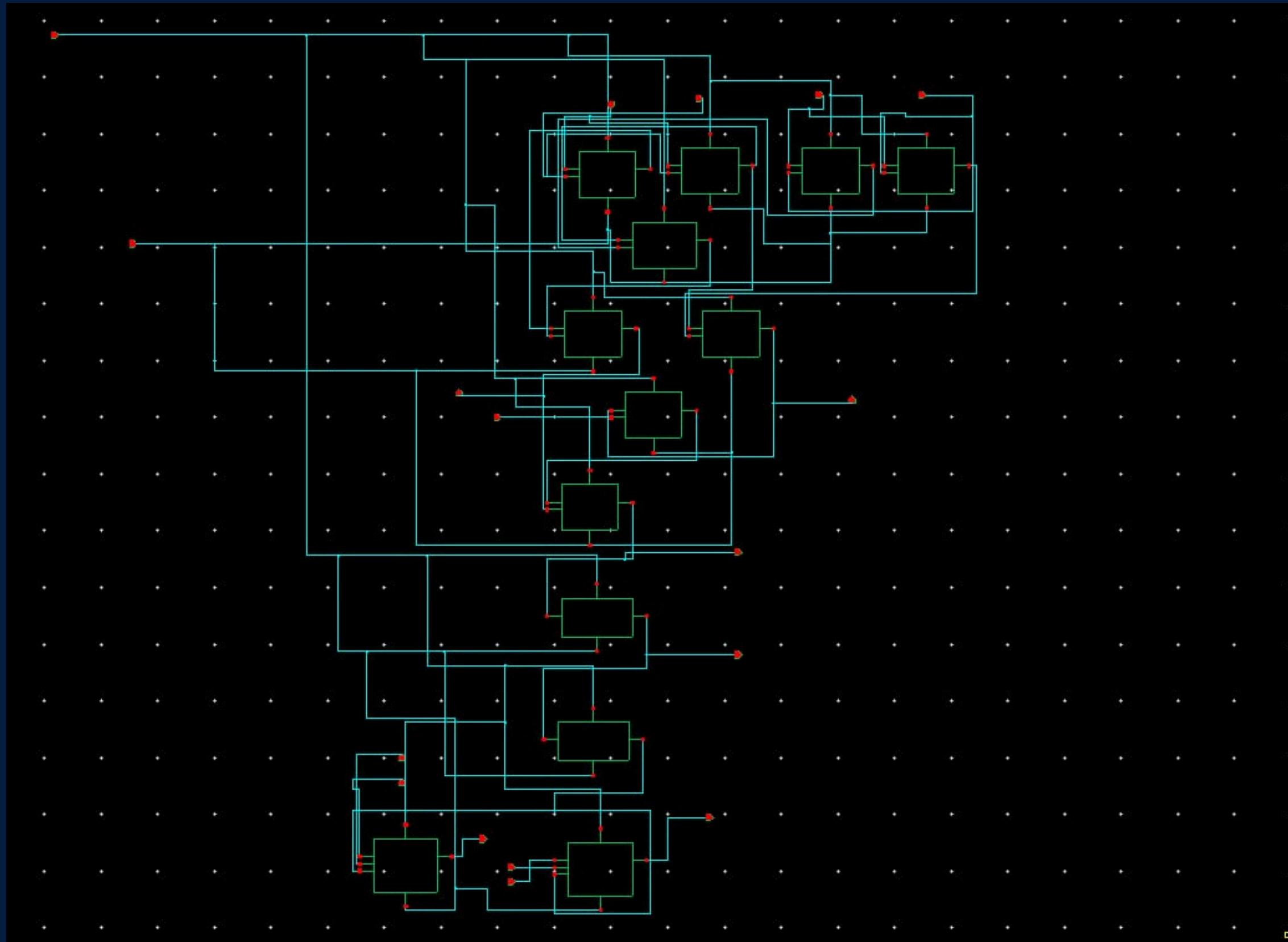
Schematic a12b12-a11b11



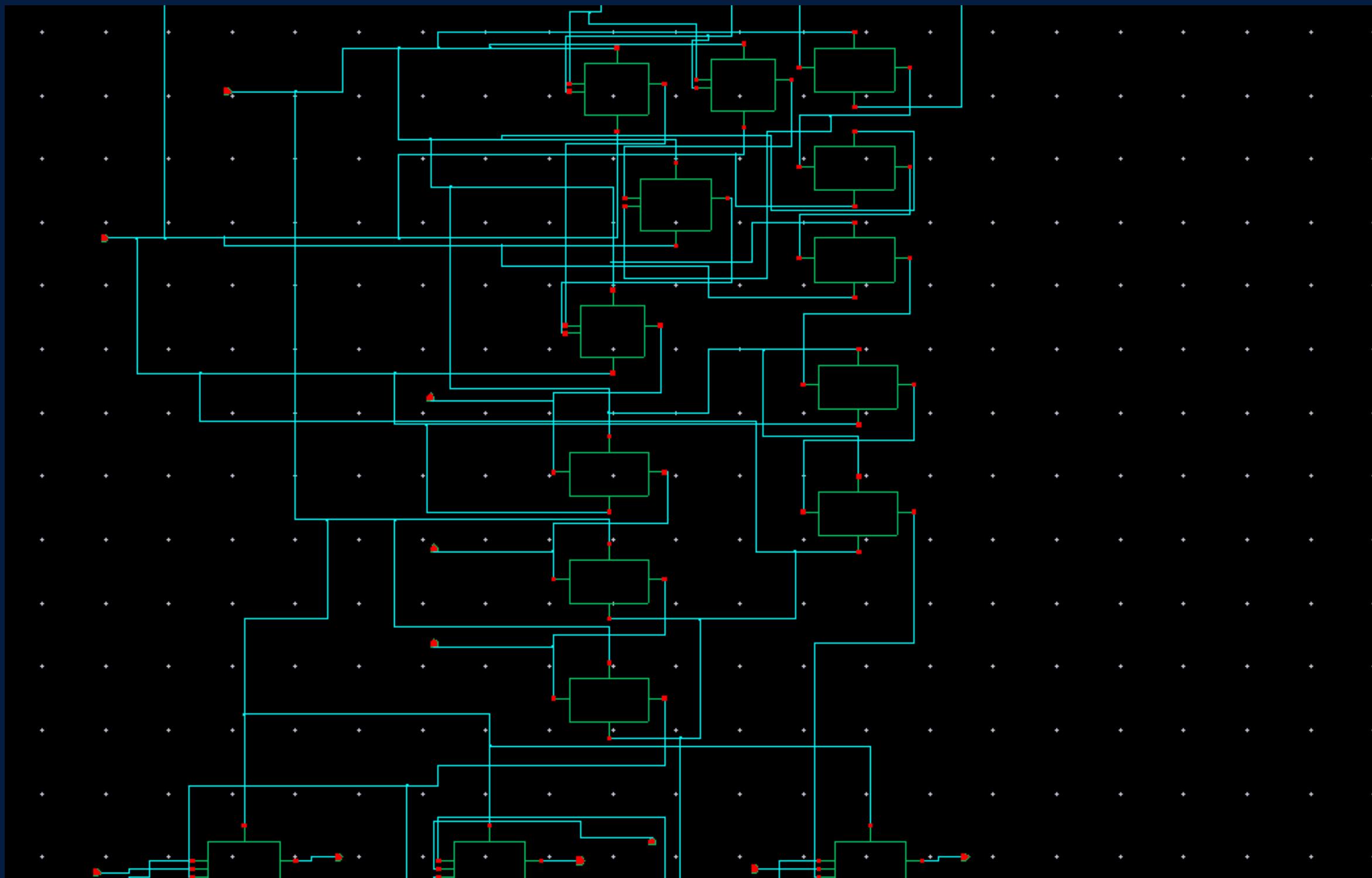
Schematic a4b4-a3b3



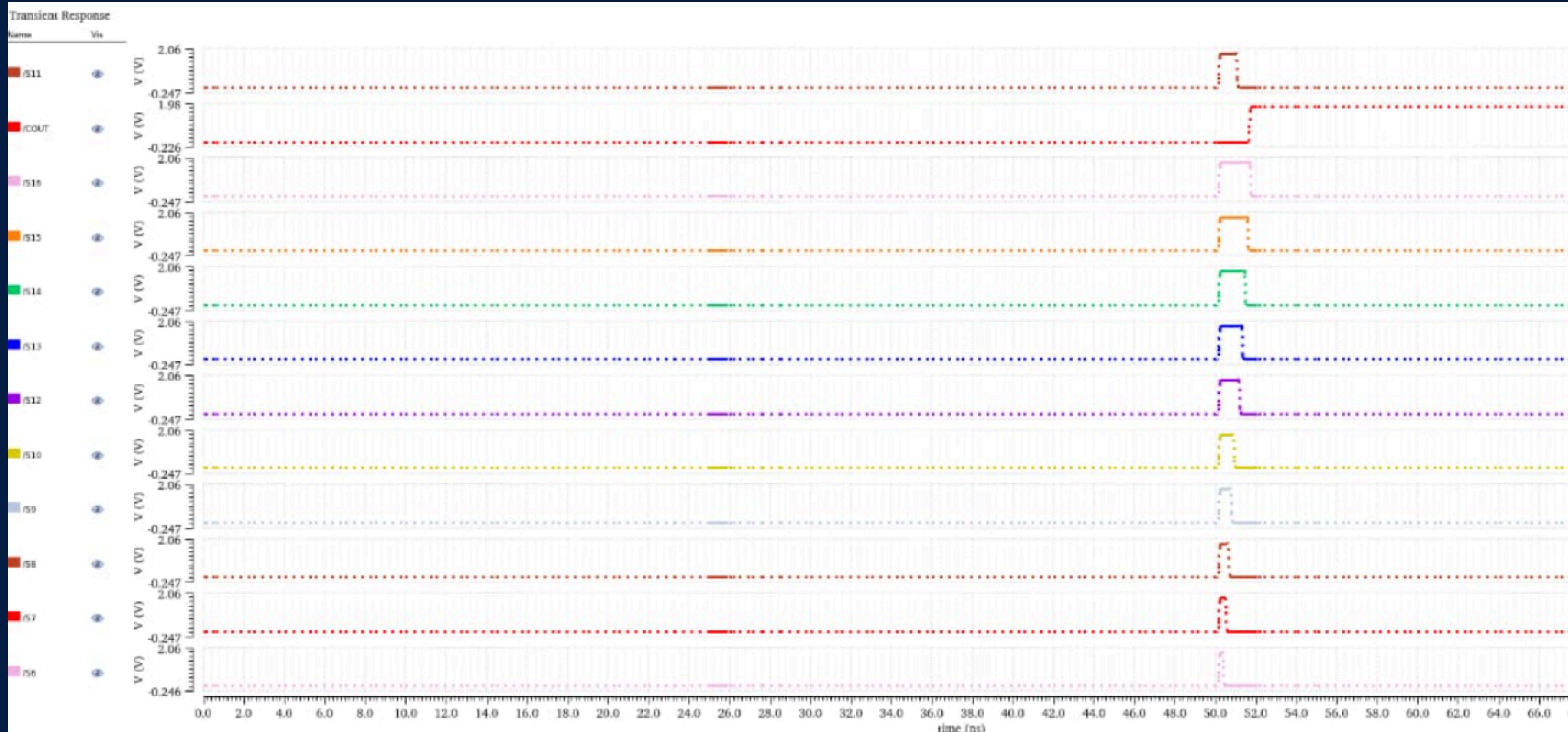
Schematic a2b2-a1b1



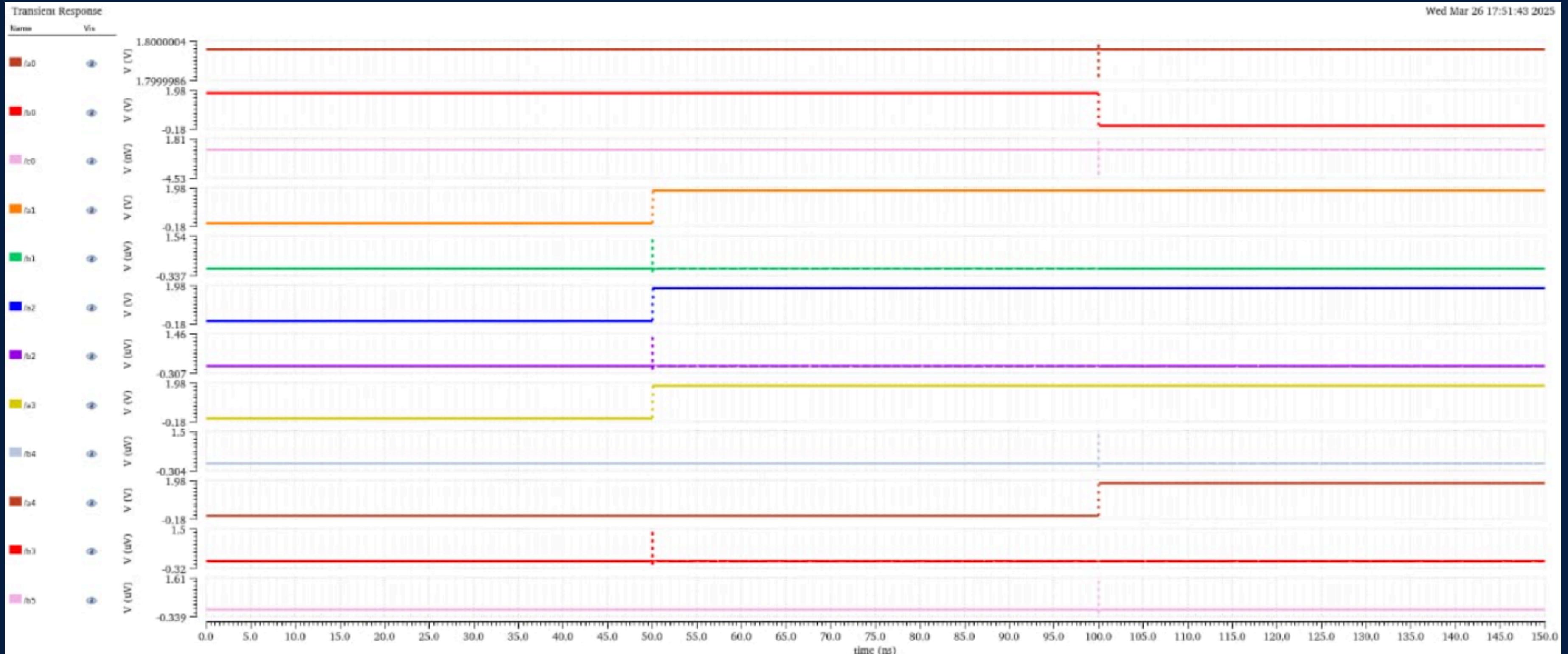
Schematic a0b0-c0

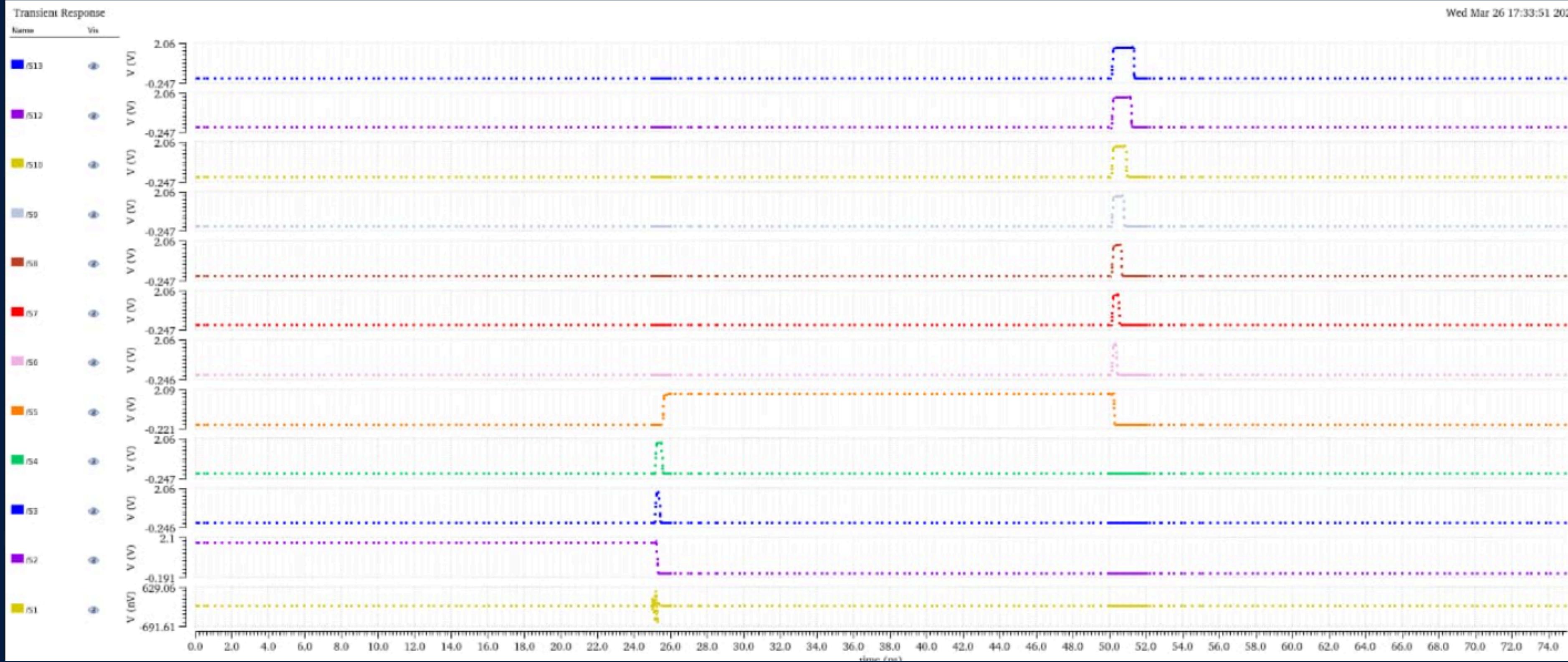


OUTPUT WAVEFORM



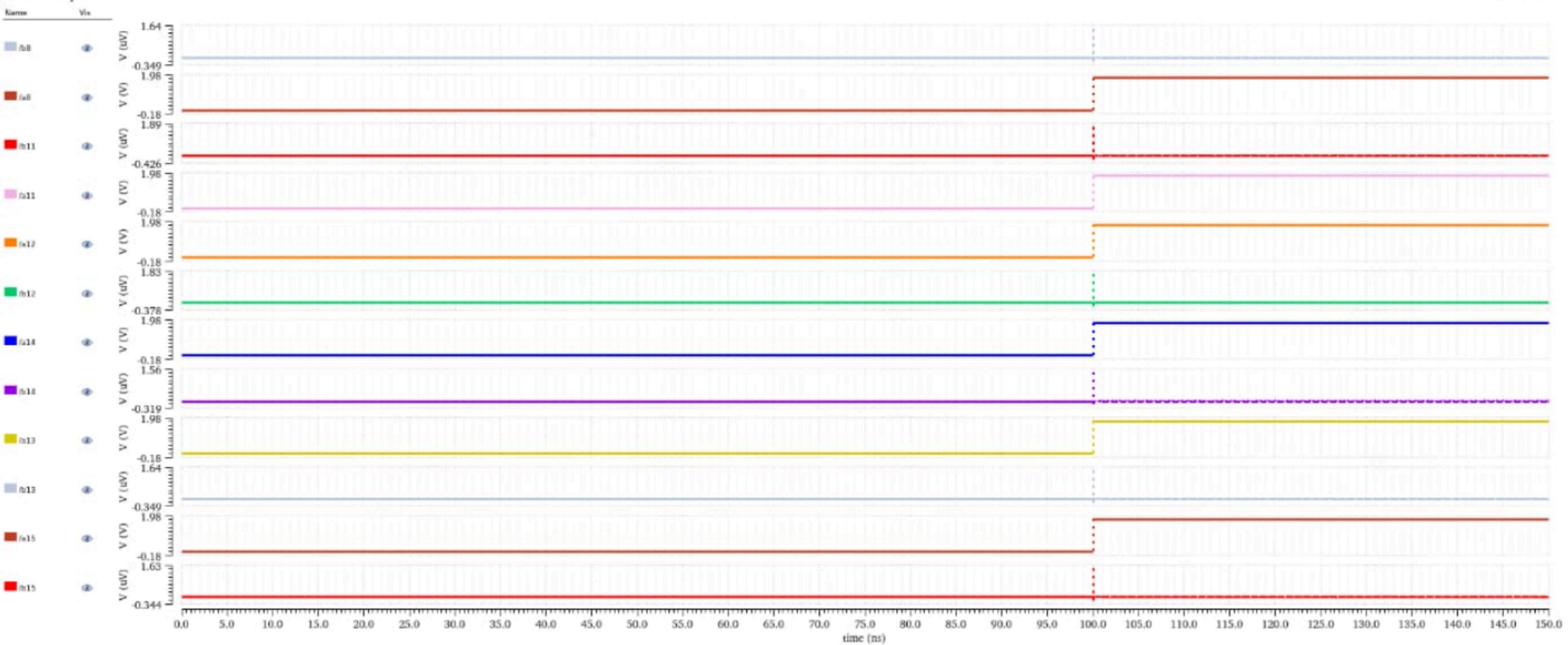
Wed Mar 26 17:51:43 2025





Transient Response

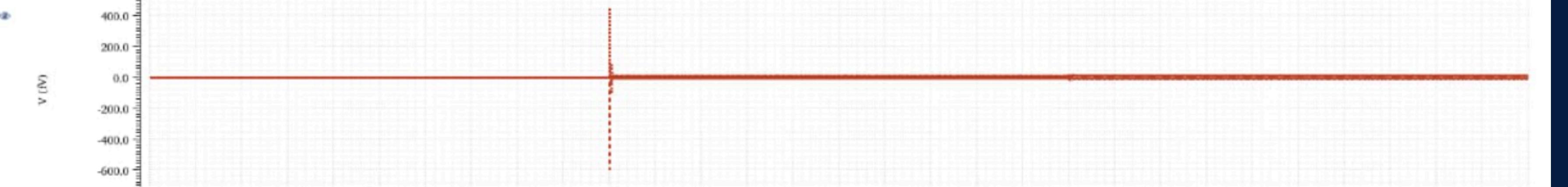
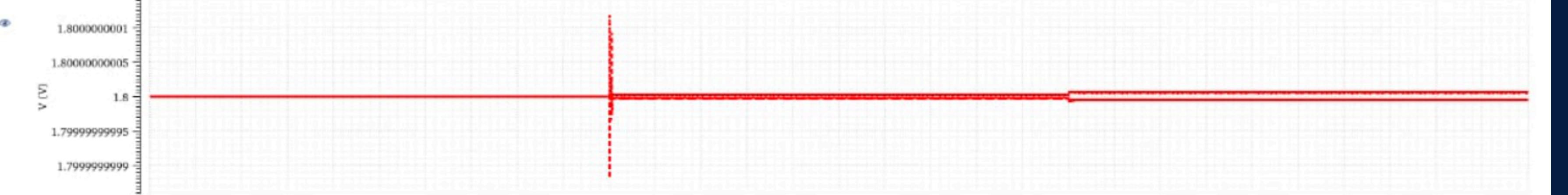
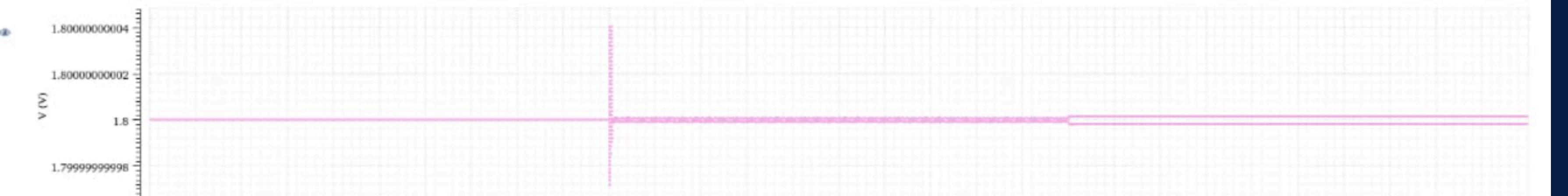
Wed Mar 26 17:51:43 2025



Transient Response

Wed Mar 26 18:08:48 2025

Name Vis

f₀f₀₀f₀₀

time (ns)

