

No.4794B

LC3564S, SS, SM, ST-70/85/10

64K (8192words×8 bits)SRAM

Overview

The LC3564S, LC3564SM, and LC3564ST are asynchronous silicon gate CMOS static RAMs with an 8192-word X 8-bit organization. These SRAMs are full CMOS type SRAMs with a six-transistor memory cell and feature high-speed access, a low operating current, and an ultra-low standby current. Control signal inputs include an OE input for high-speed memory access and two chip enable inputs, CE1 and CE2, for power-down and device selection. Thus these products are optimal for systems that require low power and/or battery backup and they support easy expansion of memory capacities. The ultra-low standby mode current drain allows capacitors to be used for backup and 3V operation makes these devices an excellent choice for use in battery operated portable equipment.

Features

 Supply voltage : 2.7 to 5.5V 5V operation : $5.0V \pm 10\%$ 3V operation $: 3.0V \pm 10\%$

• Address access time (tAA)

5V operation

LC3564S, SS, SM, ST-70 : 70ns (max.) LC3564S, SS, SM, ST-85 : 85ns (max.) LC3564S, SS, SM, ST-10 : 100ns (max.)

3V operation

LC3564S, SS, SM, SS-70 : 200ns (max.) LC3564S, SS, SM, SS-85 : 250ns (max.) LC3564S, SS, SM, SS-10 : 500ns (max.)

• Ultra-low standby current

5V operation : $1.0\mu A$ (Ta $\leq 70^{\circ}C$) 3.0µA (Ta≦85°C)

3V operation : 0.8μA (Ta≦70°C)

 $2.5\mu A (Ta \leq 85^{\circ}C)$

• Operating temperature

3V operation : -40°C to +85°C 5V operation : -40° C to $+85^{\circ}$ C • Data retention voltage : 2.0 to 5.5V

• All I/O levels

5V operation : TTL compatible 3V operation : $V_{CC} - 0.2V/0.2V$

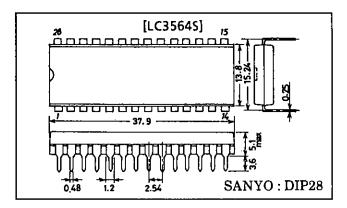
- Three control inputs (OE, CE1, CE2)
- Common input/output pins, three-state outputs
- No clock or timing signals required

• Package:

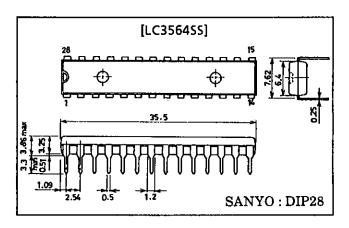
28-pin DIP (600mil)plastic package: LC3564S 28-pin DIP (300mil)plastic package: LC3564SS 28-pin SOP (450mil)plastic package: LC3564SM 28-pin TSOP (8×13.4mm)plastic package: LC3564ST

Package Dimensions

unit: mm 3012A-DIP28

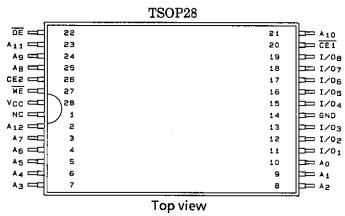


unit: mm 3133-DIP28



Pin Assignments

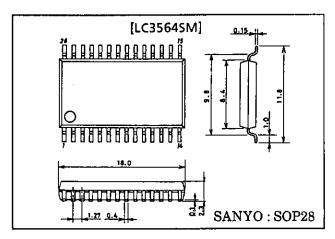
DIP28, SOP28 NC 1 28 VCC 27 WE A12 2 A7 3 SE CES 25 AB A6 4 24 49 A5 5 23 A11 25 <u>0E</u> 21 A10 20 CE 1 A0 10 19 1/08 18 1/07 1/01 11 17 1/06 1/02 12 16 1/05 1/03 13 GND 14 15 1/04 Top view



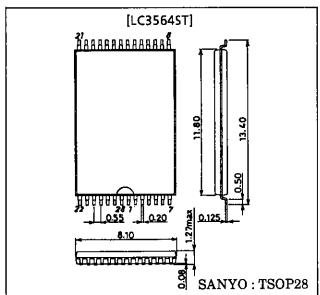
A0 to A12	Address input
WE	Write enable
ŌĒ	Output enable
CE1, CE2	Chip enable
I/O ₁ to I/O ₈	Data input/output
V _{CC} , GND	Power, ground

Package Dimensions

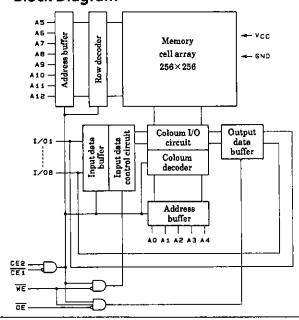
unit: mm 3187-SOP28



unit: mm **3221-TSOP28**



Block Diagram



Pin Functions

Mode	CE1	CE2	ŌĒ	WE	I/O	Current
Read Cycle	L	H	L	Н	Data output	I _{CCA}
Write Cycle	L	Н	×	L	Data input	I _{CCA}
Output Disable	L	Н	Н	Н	High impedance	I _{CCA}
TT 1 4 1	Н	×	×	×	High impedance	I_{CCS}
Unselected	×	L	×	×	High impedance	I _{CCS}

 $[\]times$: Arbitrary H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Max supply voltage	V _{CC} max		7.0	V
Inputvoltage	V _{IN}		-0.3* to V _{CC} + 0.3	V
1/O voltage	V _{I/O}		-0.3 to V _{CC} + 0.3	V
Operating temperature range	Topr		-40 to +85	°C
Storage temperature range	Tstg		-55 to + 125	°C

^{*)} The inputs may undershoot to -3.0V (min.) for periods less than 30ns.

I/O Capacitance at Ta = 25°C, f = 1MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	C _{I/O}	V _{I/O} = 0V		6	10	рF
Input capacitance	C	V _{IN} = 0V		6	10	рF

(Note) This parameter is sampled and not 100% tested.

5V Operation

DC Recommended Operating Ranges at $Ta = -40 \text{ to } +85 ^{\circ}\text{C}$, $V_{CC} = 4.5 \text{ to } 5.5 \text{V}$

Parameter	Symbol	min	typ	max	Unit
Supplyvoltage	V _{CC}	4.5	5.0	5.5	>
Input voltage	V _{IH}	2.2		V _{CC} + 0.3	V
	V _{IL}	-0.3*		+ 0.8	٧

^{*)} The inputs may undershoot to $-3.0\mathrm{V}$ (min.) for periods less than 30ns.

DC Electrical Characteristics at Ta = -40 to +85 °C, $V_{CC} = 4.5$ to 5.5 V

Para	ameter	Symbol	Cond	ditions			min	typ*	max	Unit
Input leaka	ge current	I _{LI}	$V_{IN} = 0$ to V_{CC}				-1.0		+ 1.0	μΑ
I/O leakage	current	I _{LO}	$V_{\overline{CE1}} = V_{IH} \text{ or } V_{CE2} = V_{\overline{OE}} = V_{IH} \text{ or } V_{\overline{WE}} = V_{I/O} = 0 \text{ to } V_{CC}$				-1.0		+ 1.0	μΑ
Output high	n level voltage	V _{OH}	I _{OH} = -1.0mA	•			2.4			٧
Output low	level voltage	V _{OL}	I _{OL} = 2.0mA						0.4	V
Operating current	V _{CC} = 0.2V/ 0.2V input	I _{CCA1}	V _{CE1} ≦0.2V, V _{CE2} ≧V _{CC} −0.2V,		Ta≦70°C		0.01	1.0		
			$V_{IN} \leq 0.2V$ or $V_{IN} \leq V_{CC} = 0.2V$	O = 0mA, IN≦0.2V or IN≧V _{CC} −0.2V		Ta≦85°C			3.0	μΑ
		I _{CCA4}	$V_{\overline{CE1}} \leq 0.2V$, $V_{CE2} \geq V_{CC} = 0.2V$,	min cycle		35645, SS, I, ST-70			35	
			I _{I/O} = 0mA, DUTY 100%		LC3564S, SS SM, ST-85				35	mA
						3564S, SS, I, ST-10			30	
				1μs cy	/cle			4		mA
	TTL input	I _{CCA2}	$V_{\overline{CE1}} = V_{ L}, V_{CE2} = V_{ L}$ $I_{ /O} = 0 \text{ mA}, V_{ N} = V_{ L}$						7	mA
		ICCA3	$V_{\overline{CE1}} = V_{IL},$ $V_{CE2} = V_{IH},$	min cycle	LC3564S, SS, SM, SS-70				40	
			I _{I/O} = 0mA, DUTY 100%			3564S, SS, I, SS-85			40	mA
						3564S, SS, I, SS-10			35	
		i		1μs cy	/cle			7		mA
Standby	V _{CC} -0.2V/	I _{CCS1}	V _{CE2} ≦0.2V	2V		Ta≦70°C		0.01	1.0	μΑ
current	0.2V input		or VCE2 VCC -0	$\begin{array}{c} V_{\text{CE2}} \leq 0.2 \text{V} & \text{Ta} \leq 70^{\circ}\text{C} \\ \text{or} & V_{\text{CE1}} \geq V_{\text{CC}} - 0.2 \text{V} \\ V_{\text{CE2}} \geq V_{\text{CC}} - 0.2 \text{V} & \text{Ta} \leq 85^{\circ}\text{C} \end{array}$		Ta≦85°C			3.0	μΛ
	TTL input	I _{CCS2}	$V_{CE2} = V_{IL} \text{ or } V_{\overline{CE1}} = V_{IN} = 0 \text{ to } V_{CC}$	V ^{IH}					2.0	mA

^{*)} Reference value at $V_{CC} = 5V$, Ta = 25°C

AC Electrical Characteristics at $Ta = -40 \text{ to } +85 ^{\circ}\text{C}$, $V_{CC} = 4.5 \text{ to } 5.5 \text{V}$

AC test conditions

Input pulse levels

 $: V_{IH} = 2.4V, V_{IL} = 0.6V$

Input rise and fall time

: 5ns : 1.5V

Input and output timing reference levels Output load

LC3564S, SS, SM, ST-70

: 30pF + 1TTL gate

(including jig capacitance)

LC3564S, SS, SM, ST-85/10 : 100pF+1TTL gate

(including jig capacitance)

Read Cycle

			LC	3564S,	SS, SM,	ST		
Parameter	Symbol		70	-	-85		-10	
		min	max	min	max	min	max	
Read cycle time	t _{RC}	70		85		100		ns
Address access time	t _{AA}		70		85		100	ns
CE1 access time	t _{CA1}		70		85		100	ns
CE2 access time	t _{CA2}		70		85		100	ns
OE access time	toA		35		45		50	ns
Output hold time	t _{OH}	10		10		10		ns
CE1 — output enable time	t _{COE1}	10		10		10		ns
CE2—output enable time	t _{COE2}	10		10		10		ns
OE – output enable time	t _{OOE}	5		5		5		ns
CE1 — output disable time	t _{COD1}		30		35		35	ns
CE2 — output disable time	t _{COD2}		30		35		35	ns
OE – output disable time	tood		25		25		25	ns

Write Cycle

			LC	35645,	SS, SM,	ST		
Parameter	Symbol	_	70	-85		_	10	Unit
		min	max	min	max	min	max	
Write cycle time	t _{WC}	70		85		100		ns
Address setup time	t _{AS}	0		0		0		ns
Write pulse width	t _{WP}	50		55		55		ns
CE1 setup time	t _{CW1}	60		65		65		ns
CE2 setup time	t _{CW2}	60		65		65		ns
Write recovery time	t _{WR}	0		0		0		ns
CE1 write recovery time	t _{WR1}	0		0		0		ns
CE2 write recovery time	t _{WR2}	0		0		0		ns
Data setup time	t _{DS}	35		40		40		ns
Data hold time	t _{DH}	0		0		0	,	ns
CE1 data hold time	t _{DH1}	0		0		0		ns
CE2 data hold time	t _{DH2}	0		0		0		ns
WE — output enable time	t _{WOE}	5		5		5		ns
WE – output disable time	t _{WOD}		30		35		35	ns

3V Operation

DC Recommended Operating Ranges at Ta = -40 to +85 °C, $V_{CC} = 2.7$ to 3.3V

Parameter	Symbol	min	typ	max	Unit
Supplyvoltage	Vcc	2.7	3.0	3.3	V
Input voltage	V _{IH}	V _{CC} 0.2		Vcc	>
	V _{IL}	0		0.2	V

DC Electrical Characteristics at Ta = -40 to +85 °C, $V_{CC} = 2.7 \text{ to } 3.3 \text{ V}$

Para	meter	Symbol	Co	ndition	S		min	typ*	max	Unit
Inputleakag	ge current	lu	$V_{IN} = 0 \text{ to } V_{CC}$				-1.0		+ 1.0	μΑ
I/O leakage	current	I _{LO}	$V_{\overline{CE1}} = V_{IH} \text{ or } V_{CE2} = V_{IL} \text{ or}$ $V_{\overline{OE}} = V_{IH} \text{ or } V_{\overline{WE}} = V_{IL}$, $V_{I/O} = 0 \text{ to } V_{CC}$			-1.0		+ 1.0	μΑ	
Output high	level voltage	V _{OH}	I _{OH} = - 0.5mA				V _{CC} - 0.2V			٧
Output low	level voltage	V _{OL}	I _{OL} = 1.0mA						0,2	V
Operating	V _{CC} -0.2V/	I _{CCA1}	$V_{\overline{CE1}} \leq V_{IL}, V_{CE2} \geq V_{IH},$ $I_{I/O} = 0 \text{mA}, V_{IN} \leq V_{IL},$ $V_{IN} \geq V_{IH}$ $Ta \leq 70 ^{\circ}\text{C}$ $Ta \leq 85 ^{\circ}\text{C}$				0.01	0.8		
current	0,2V input		IIIO = OITA, VIN⊒ VIN≧VIH	· VIL,		Ta≦85°C			2.5	μΑ
		I _{CCA4}	V CE1 ≦V _{IL} , V _{CE2} ≧V _{IH} ,	min cycle		564S, SS, , ST-70			20	
			l _{I/O} = 0mA, DUTY = 100%			564S, SS, , ST-85			20	mΑ
						564S, SS, , ST-10			10	l
				1μs cy	cle			3		mA
Standby	V _{CC} -0.2V/	I _{CCS1}	V _{CE2} ≦V _{IL}			Ta≦70°C		0.01	8.0	μΑ
current	0.2V input		or VCE1 \SVIH			Ta≦85°C			2.5	μΑ.

^{*)} Reference value at $V_{CC}\!=\!3V,\,Ta\!=\!25^{\circ}C$

AC Electrical Characteristics at $\mathrm{Ta} = -40~\mathrm{to}~+85^{\circ}\mathrm{C}, \, V_{CC} = 2.7~\mathrm{to}~3.3\mathrm{V}$

AC test conditions

Input pulse levels $: V_{IH} = V_{CC} - 0.2V, V_{IL} = 0.2V$

Input rise and fall time : 10ns
Input and output timing reference levels : 1.5V

Output load LC3564S, SS, SM, ST-70 : 30pF (including scope and jig) LC3564S, SS, SM, ST-85/10 : 100pF (including scope and jig)

Read Cycle

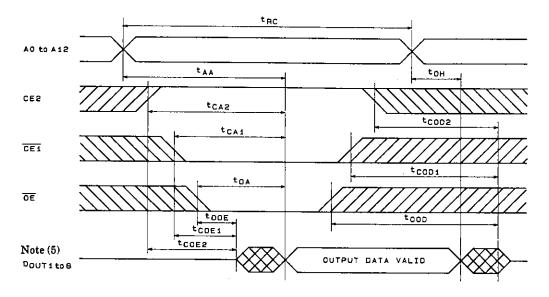
			LC	3564S,	SS, SM,	ST		
Parameter	Symbol	-70		-85		-10		Unit
		min	max	min	max	min	max	
Read cycle time	t _{RC}	200		250		500		ns
Address access time	t _{AA}		200		250		500	ns
CE1 access time	t _{CA1}		200		250		500	ns
CE2 access time	t _{CA2}		200		250		500	ns
OE access time	toA		100		130		250	ns
Output hold time	t _{OH}	20		20		20		ns
CE1 — output enable time	t _{COE1}	20		20		20		ns
CE2 — output enable time	t _{COE2}	20		20		20		ns
OE – output enable time	tooe	10		10		10		ns
CE1 – output disable time	t _{COD1}		60		80		120	ns
CE2 – output disable time	t _{COD2}		60		80		120	ns
OE – output disable time	toop		50		70		100	ns

Write Cycle

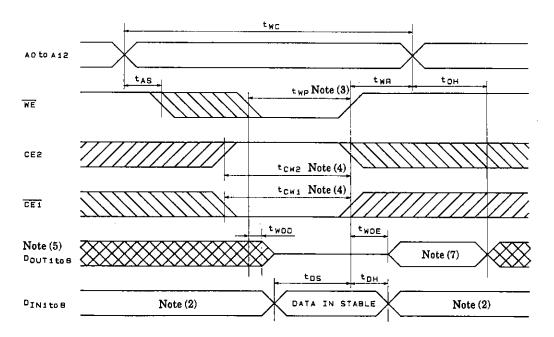
			LC	3564S,	SS, SM,	ST		
Parameter	Symbol		70	85		-10		Unit
		min	max	min	max	min	max	
Write cycle time	t _{WC}	200		250		500		ns
Address setup time	t _{AS}	0		0		0		ns
Write pulse width	t _{WP}	140		160		200		ns
CE1 setup time	t _{CW1}	150		180		250		ns
CE2 setup time	t _{CW2}	150		180		250		ns
Write recovery time	t _{WR}	0		0		0		ns
CE1 write recovery time	t _{WR1}	0		0		0		ns
CE2 write recovery time	t _{WR2}	0		0		0		ns
Data setup time	t _{DS}	130		150		180		ns
Data hold time	t _{DH}	0		0		0		ns
CE1 data hold time	t _{DH1}	0		0		0		ns
CE2 data hold time	t _{DH2}	0		0		0		ns
WE — output enable time	t _{WOE}	10		10		10		ns
WE — output disable time	t _{WOD}		60		80		120	ns

Timing Waveform

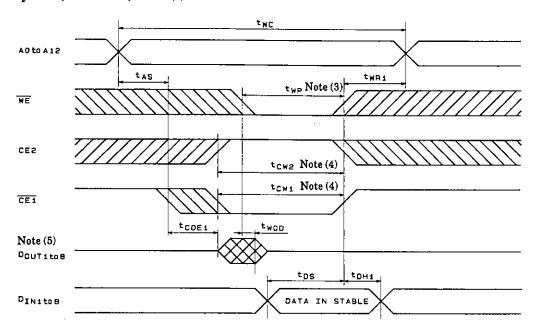
Read Cycle Note (1)



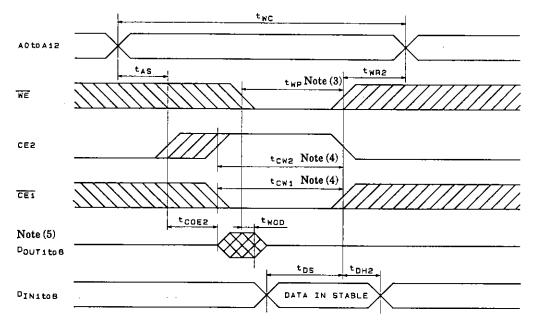
Write Cycle 1 (WE Write) Note (6)



Write Cycle 2 (CE1 Write) Note (6)



Write Cycle 3 (CE2 Write) Note (6)



Notes: (1) In Read Cycle, WE should be high.

- (2) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- (3) A write occurs during the overlap of a low \(\overlap{CE1}\), a high CE2 and a low \(\overlap{WE}\).
 A write begins at the latest transition among \(\overlap{CE1}\) going low, CE2 going high and \(\overlap{WE}\) going low.

A write ends at the earliest transition among $\overline{CE1}$ going high, CE2 going low and \overline{WE} going high.

 t_{WP} is measured from the beginning of write to the end of write.

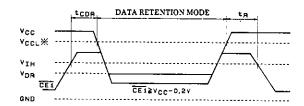
- (4) t_{CW1} , t_{CW2} are measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.
- (5) If one of these conditions (\overline{OE} is high, $\overline{CE1}$ is high, CE2 is low, \overline{WE} is low) at least is satisfied, D_{OUT} goes to high impedance state.
- (6) In Write Cycle, $\overline{OE} = V_{IH}$ or V_{IL} .
- (7) D_{OUT} is in the same phase of written data of this cycle.

Data Retention Characteristics at Ta = -40 to +85 °C

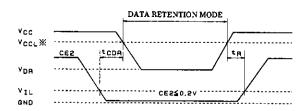
Parameter	Symbol Conditions			min	typ	max	Unit
Date retention supply voltage	V _{DR}	$V_{CE2} \le 0.2V$, $V_{\overline{CE1}} \ge V_{CC} - 0.2V$ or $V_{CE2} \ge V_{CC} - 0.2V$		2.0		5.5	v
Data retention current	I _{CCDR}	$V_{CC} = 3V,$ $V_{CE2} \le 0.2V,$ or $V_{\overline{CE1}} \ge V_{CC} - 0.2V$ $V_{CE2} \ge V_{CC} - 0.2V$	Ta≦70°C			8.0	μА
			Ta≦85°C			2.5	
Chip enable setup time	t _{CDR}			0			ns
Chip enable hold time	t _R			t _{RC} *			ns

^{*)} t_{RC} = Read Cycle Time

Data Retention Waveform (1) (CE1 CONTROL)



Data Retention Waveform (2) (CE2 CONTROL)



*)V_{CCL} - 5V operation: 4.5V 3V operation: 2.7V

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