EECS 151/251A Homework 1

Due Friday, Feb 4th, 2022

Problem 1: Dennard Scaling

Assuming ideal Dennard scaling, you have previously designed a microprocessor that runs at 5GHz but dissipates 55W. In the next technology node, with features that are scaled by 0.6x, what will be the power and performance of your microprocessor?

Power $55\,W \cdot 0.6^2 = 19.8\,W$

Performance $\frac{5}{0.6} = 8.33\,W$

Problem 2: Power/energy

(a) If you have a biomedical sensor interface to monitor a signal long term with on-chip processing where the chip is in contact with human skin and powered by a battery, what could be a primary concern for

a. Power consumption

Having a system small & discreet enough to be worn on human skin may have problems dissipating heat if it consumes enough power

b. Energy consumption

Having a wearable system that is constantly running may have problems having a large enough battery to power the system

(b) If the sensor dissipates 200mW and you expect it to have 6 hours of battery life, how much energy in Joules must the battery hold at full charge?

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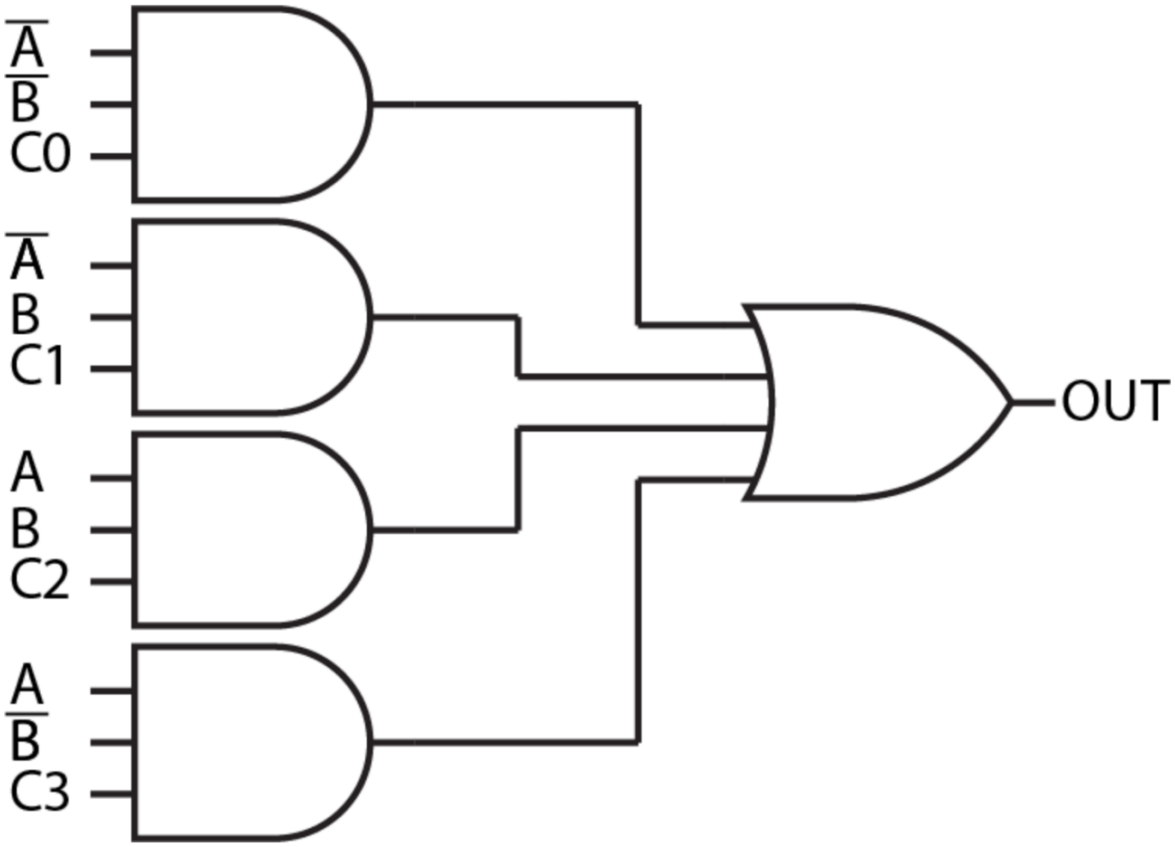
(c) The user removes the sensor to charge it while they sleep. It can take 8 hours to recharge, how much power should the charger be able to supply to make this possible?

150 mW

Problem 3: Boolean Algebra

Consider the given circuit. All inputs (A, B, C0, C1, C2, C3) must be either 0 or 1. What must C0, C1, C2, and C3 be such that the circuit computes the function XNOR (A, B)?



C0: 1

C1: 0

C2: 1

C3: 0

Problem 4: Avoid unintentional latch synthesis

For each of the following Verilog modules, which variables will generate latches? If none, write none.

(a)

```
1   input [1:0] a;
2   input b, c;
3   reg x, y;
4   always @(*) begin
5       y = b;
6       case (a)
7           2'b00 : x=b;
8           2'b01 : x=c;
9           2'b11 : y=b & c;
10          2'b10 : y=b | c;
11      endcase
12  end
```

x

(b)

```
input a;
output reg [1:0] y;
always@ (*)
    if (a)
        y = 2'b01;
    else begin
        y[0] = 1;
        y[1] = 0;
    end
end
```

none

(c)

```
input x, y;
reg [1:0] d, c;
always @(*) begin
    d = 2'b00;
    if (x && y) begin
        d = 2'b01;
        c = 2'b00;
    end
    else if (x)
        d = 2'b11;
end
```

C

Problem 5: Find the Verilog error

Find the line which has the Verilog error and rewrite it correctly

```
1   module mux_4to1 (
2       input a,b,c,d,
3       input [1:0] sel,
4       output out
5       );
6       always @(sel) begin
7           case (sel)
8               2'b00 : out = a;
9               2'b01 : out = b;
10              2'b10 : out = c;
11              2'b11 : out = d;
12          endcase
13      end
14  endmodule
```

`always @(sel) begin` ⟹ `always @(a b c d sel) begin`