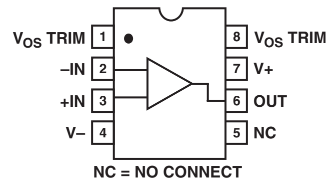
Ultraprecision Operational Amplifier

OP177

FEATURES
- **Ultralow Offset Voltage:**
  T_A = 25°C: 25 μV Max
- **Outstanding Offset Voltage Drift: 0.1 μV/°C Max**
- **Excellent Open-Loop Gain and Gain Linearity:**
  12 V/μV Typ
- **CMRR: 130 dB Min**
- **PSRR: 115 dB Min**
- **Low Supply Current: 2.0 mA Max**
- **Fits Industry Standard Precision Op Amp Sockets**
  (OP07/OP77)

PIN CONNECTIONS

Epoxy Mini-DIP
(P Suffix)
8-Pin SO
(S-Suffix)



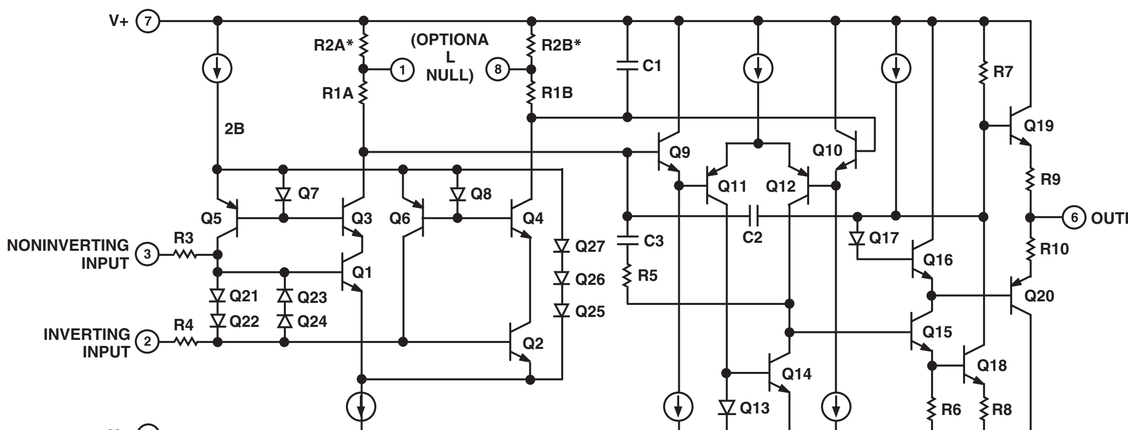
GENERAL DESCRIPTION

The OP177 features the highest precision performance of any op amp currently available. Offset voltage of the OP177 is only 25 μV max at room temperature. The ultralow V_{OS} of the OP177 combines with its exceptional offset voltage drift (TCV_{OS}) of 0.1 μV/°C max to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The OP177's open-loop gain of 12 V/μV is maintained over the full ±10 V output range. CMRR of 130 dB min, PSRR of 120 dB min, and maximum supply current of 2 mA are just a few examples of the excellent performance of this operational amplifier. The OP177's combination of outstanding specifications ensures accurate performance in high closed-loop gain applications.

This low noise bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

The OP177 is offered in the –40°C to +85°C extended industrial temperature ranges. This product is available in 8-pin epoxy DIPs, as well as the space saving 8-pin Small-Outline (SO).



*NOTE:
R2A AND R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY.

Figure 1. Simplified Schematic

REV. C

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ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP177F Min	OP177F Typ	OP177F Max	OP177G Min	OP177G Typ	OP177G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			10	25		20	60	µV
LONG-TERM INPUT OFFSET Voltage Stability	ΔV_{OS}/Time			0.3			0.4		µV/Mo
INPUT OFFSET[1] CURRENT	I_{OS}			0.3	1.5		0.3	2.8	nA
INPUT BIAS CURRENT	I_B		–0.2	1.2	2	–0.2	1.2	2.8	nA
INPUT NOISE VOLTAGE	e_n	f_o = 1 Hz to 100 Hz[2]		118	150		118	150	nV rms
INPUT NOISE CURRENT	i_n	f_o = 1 Hz to 100 Hz[2]		3	8		3	8	pA rms
INPUT RESISTANCE Differential-Mode[3]	R_{IN}		26	45		18.5	45		MΩ
INPUT RESISTANCE COMMON-MODE	R_{INCM}			200			200		GΩ
INPUT VOLTAGE RANGE[4]	IVR		±13	±14		±13	±14		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V	130	140		115	140		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±3 V to ±18 V		115	125		110	120	dB
LARGE SIGNAL VOLTAGE GAIN	A_{VO}	$R_L \geq$ 2 kΩ, V_O = 610 V[5]	5000	12000		2000	6000		V/mV
OUTPUT VOLTAGE SWING	V_O	$R_L \geq$ 10 kΩ	±13.5	±14.0		±13.5	±14.0		V
		$R_L \geq$ 2 kΩ	±12.5	±13.0		±12.5	±13.0		V
		$R_L \geq$ 1 kΩ	±12.0	±12.5		±12.0	±12.5		V
SLEW RATE[2]	SR	$R_L \geq$ 2 kΩ	0.1	0.3		0.1	0.3		V/µs
CLOSED-LOOP BANDWIDTH[2]	BW	A_{VCL} = 1	0.4	0.6		0.4	0.6		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O			60			60		Ω

POWER CONSUMPTION	P_D	$V_S = \pm 15$ V, No Load		50	60		50	60	mW
		$V_S = \pm 3$ V, No Load		3.5	4.5		3.5	4.5	mW
SUPPLY CURRENT	I_{SY}	$V_S = \pm 15$ V, No Load		1.6	2		1.6	2	mA
OFFSET ADJUSTMENT RANGE		$R_P = 20$ kΩ		±3			±3		mV

NOTES

[1]Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0 μV.

[2]Sample tested.

[3]Guaranteed by design.

[4]Guaranteed by CMRR test condition.

[5]To ensure high open-loop gain throughout the ±10 V output range, A_{VO} is tested at $-10\text{ V} \le V_O \le 0\text{ V}$, $0\text{ V} \le V_O \le +10\text{ V}$, and $-10\text{ V} \le V_O \le +10\text{ V}$.

Specifications subject to change without notice.

OP177–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP177F Min	OP177F Typ	OP177F Max	OP177G Min	OP177G Typ	OP177G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}			15	40		20	100	µV
AVERAGE INPUT OFFSET VOLTAGE DRIFT[1]	TCV_{OS}			0.1	0.3		0.7	1.2	µV/°C
INPUT OFFSET CURRENT	I_{OS}			0.5	2.2		0.5	4.5	nA
AVERAGE INPUT OFFSET CURRENT DRIFT[2]	TCI_{OS}			1.5	40		1.5	85	pA/°C
INPUT BIAS CURRENT	I_B		–0.2	2.4	4		2.4	±6	nA
AVERAGE INPUT BIAS CURRENT DRIFT[2]	TCI_B			8	40		15	60	pA/°C
INPUT VOLTAGE RANGE[3]	IVR		±13	±13.5		±13	±13.5		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±13 V	120	140		110	140		dB
POWER SUPPLY REJECTION RATIO	PSSR	V_S = ±3 V to ±18 V	110	120		106	115		dB
LARGE-SIGNAL VOLTAGE GAIN[4]	A_{VO}	R_L ≥ 2 kΩ, V_O = 10 V	2000	6000		1000	4000		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2/kΩ	±12	±13		±12	±13		V
POWER CONSUMPTION	P_D	V_S = ±15 V, No Load		60	75		60	75	mW
SUPPLY CURRENT	I_{SY}	V_S = ±15 V, No Load		20	2.5		2	2.5	mA

NOTES

[1] OP177TCV$_{OS}$ is sample tested.

[2] Guaranteed by endpoint limits.

[3] Guaranteed by CMRR test condition.

[4] To ensure high open-loop gain throughout the ±10 V output range, A_{VO} is tested at –10 V ≤ V_O ≤ 0 V, 0 V ≤ V_O ≤ +10 V, and –10 V ≤ V_O ≤ +10 V.

Specifications subject to change without notice.

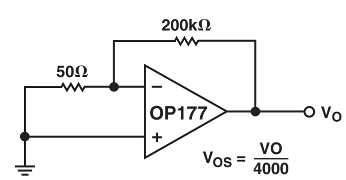

Figure 2. Typical Offset Voltage Test Circuit

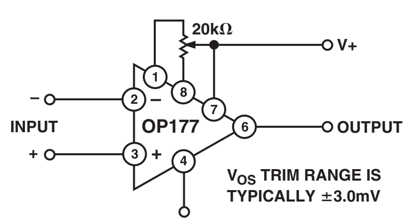

Figure 3. Optional Offset Nulling Circuit

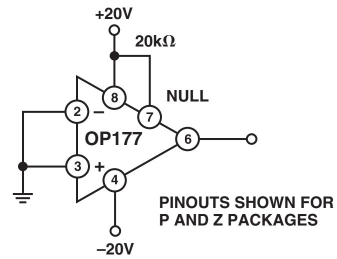

Figure 4. Burn-In Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . ±22 V
Internal Power Dissipation[1] . . . . 500 mW
Differential Input Voltage . . . . ±30 V
Input Voltage . . . . ±22 V
Output Short-Circuit Duration . . . . Indefinite
Storage Temperature Range
S, P Package . . . . –65°C to +125°C
Operating Temperature Range
OP177F, OP177G . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) . . . . 300°C
DICE Junction Temperature (T_J) . . . . –65°C to +150°C

Package Type	θ_{JA}[2]	θ_{JC}	Unit
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES
[1]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[2]θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP177FP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP177GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP177FS	–40°C to +85°C	8-Pin SO	SO-8
OP177GS	–40°C to +85°C	8-Pin SO	SO-8

APPLICATION INFORMATION

Gain Linearity

The actual open-loop gain of most monolithic op amps varies at different output voltages. This nonlinearity causes errors in high closed-loop gain circuits.

It is important to know that the manufacturer's A_{VO} specification is only a part of the solution, since all automated testers use endpoint testing and, therefore, show only the average gain. For example, Figure 5 shows a typical precision op amp with a respectable open-loop gain of 650 V/mV. However, the gain is not constant through the output voltage range, causing nonlinear errors. An ideal op amp would show a horizontal scope trace.

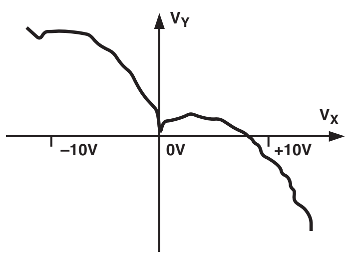

Figure 5. Typical Precision Op Amp

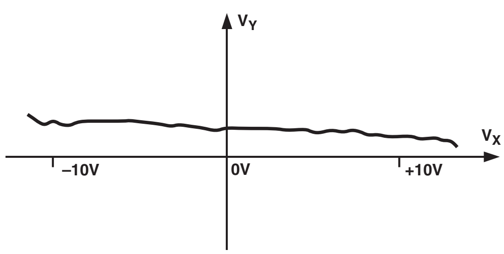

Figure 6. Output Gain Linearity Trace

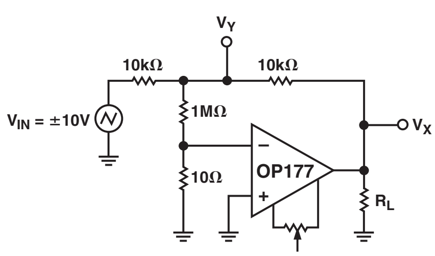

Figure 7. Open-Loop Gain Linearity Test Circuit

Figure 6 shows the OP177's output gain linearity trace with its truly impressive average A_{VO} of 12000 V/mV. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. ADI also performs additional testing to ensure consistent high open-loop gain at various output voltages.

Figure 7 is a simple open-loop gain test circuit for your own evaluation.

THERMOCOUPLE AMPLIFIER WITH COLD-JUNCTION COMPENSATION

An example of a precision circuit is a thermocouple amplifier that must amplify very low level signals accurately without introducing linearity and offset errors to the circuit. In this circuit, an S-type thermocouple, which has a Seebeck coefficient of 10.3 μV/°C, produces 10.3 mV of output voltage at a temperature of 1000°C. The amplifier gain is set at 973.16. Thus, it will produce an output voltage of 10.024 V. Extended temperature ranges to beyond 1500°C can be accomplished by reducing the amplifier gain. The circuit uses a low-cost diode to sense the temperature at the terminating junctions and, in turn, compensates for any ambient temperature change. The OP177, with its high open-loop gain, plus low offset voltage and drift combines to yield a very precision temperature sensing circuit. Circuit values for other thermocouple types are shown in Table I.

Table I.

Thermo-couple Type	Seebeck Coefficient	R1	R2	R7	R9
K	39.2 μV/°C	110 Ω	5.76 kΩ	102 kΩ	269 kΩ
J	50.2 μV/°C	100 Ω	4.02 kΩ	80.6 kΩ	200 kΩ
S	10.3 μV/°C	100 Ω	20.5 kΩ	392 kΩ	1.07 MΩ

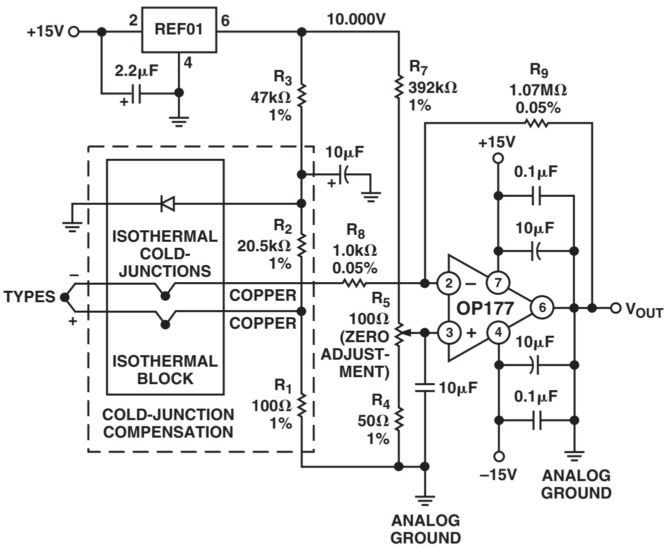

Figure 8. Thermocouple Amplifier with Cold Junction Compensation

PRECISION HIGH GAIN DIFFERENTIAL AMPLIFIER

The high gain, gain linearity, CMRR, and low TCV_{OS} of the OP177 make it possible to obtain performance not previously available in single stage, very high gain amplifier applications. See Figure 9.

For best CMR, $\frac{R1}{R2}$ must equal $\frac{R3}{R4}$. In this example, with a 10 mV differential signal, the maximum errors are as listed in Table II.

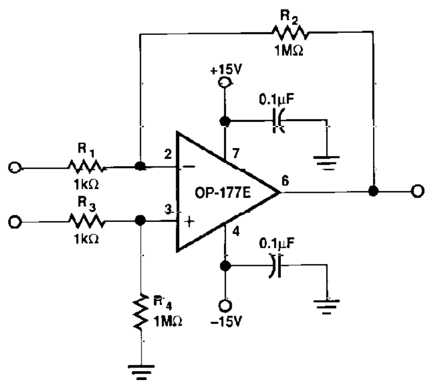

Figure 9. Precision High Gain Differential Amplifier

Table II. High Gain Differential Amp Performance

Type	Amount
Common-Mode Voltage	0.1%/V
Gain Linearity, Worst Case	0.02%
TCV_{OS}	0.0003%/°C
TCI_{OS}	0.008%/°C

ISOLATING LARGE CAPACITIVE LOADS

The circuit in Figure 10 reduces maximum slew rate but allows driving capacitive loads of any size without instability. Because the 100 Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP177.

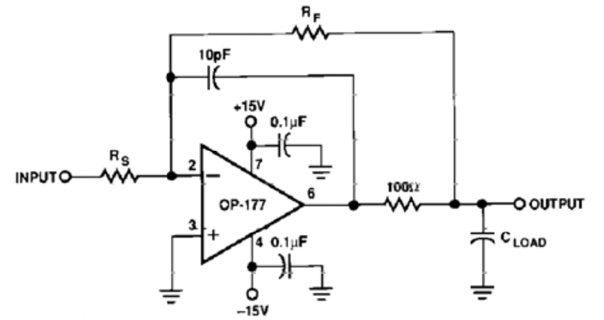

Figure 10. Isolating Capacitive Loads

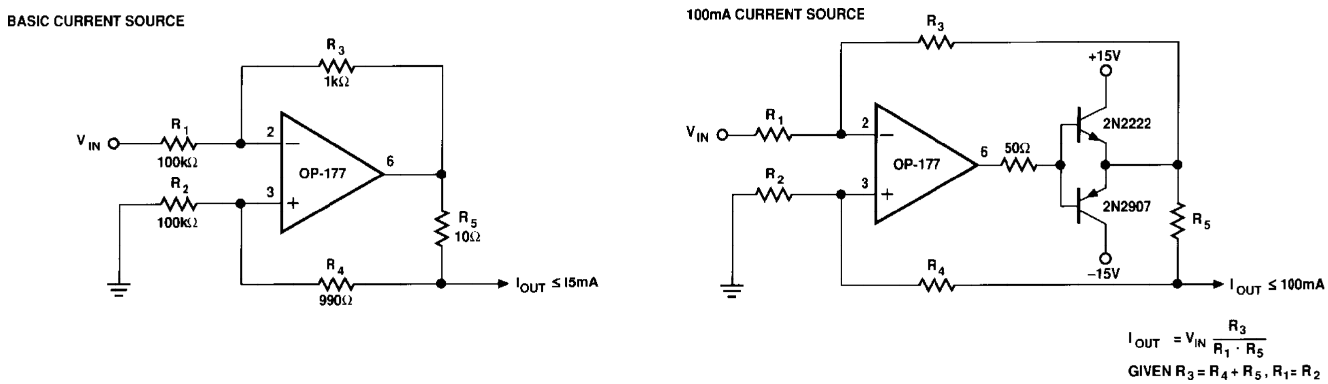

Figure 11. Bilateral Current Source

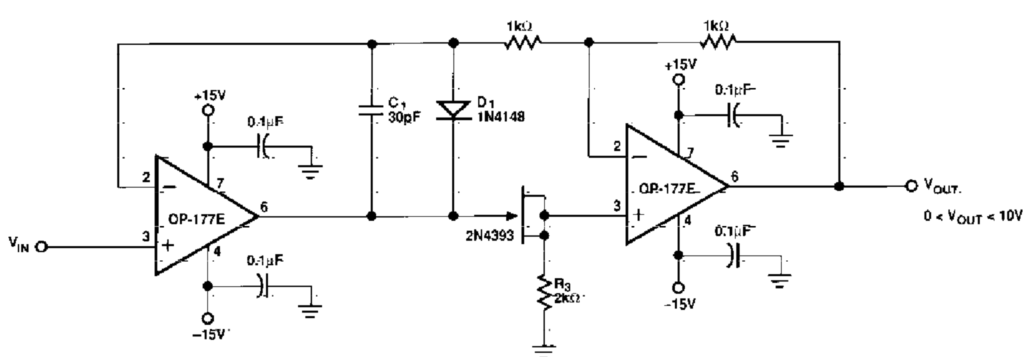

Figure 12. Precision Absolute Value Amplifier

BILATERAL CURRENT SOURCE

The current sources shown in Figure 11 will supply both positive and negative current into a grounded load.

Note that $Z_O = \dfrac{R5\left(\dfrac{R4}{R2}+1\right)}{\dfrac{R5+R4}{R2}-\dfrac{R3}{R1}}$

and that for Z_O to be infinite,

$$\frac{R5+R4}{R2} \text{ must} = \frac{R3}{R1}$$

PRECISION ABSOLUTE VALUE AMPLIFIER

The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. See Figure 12.

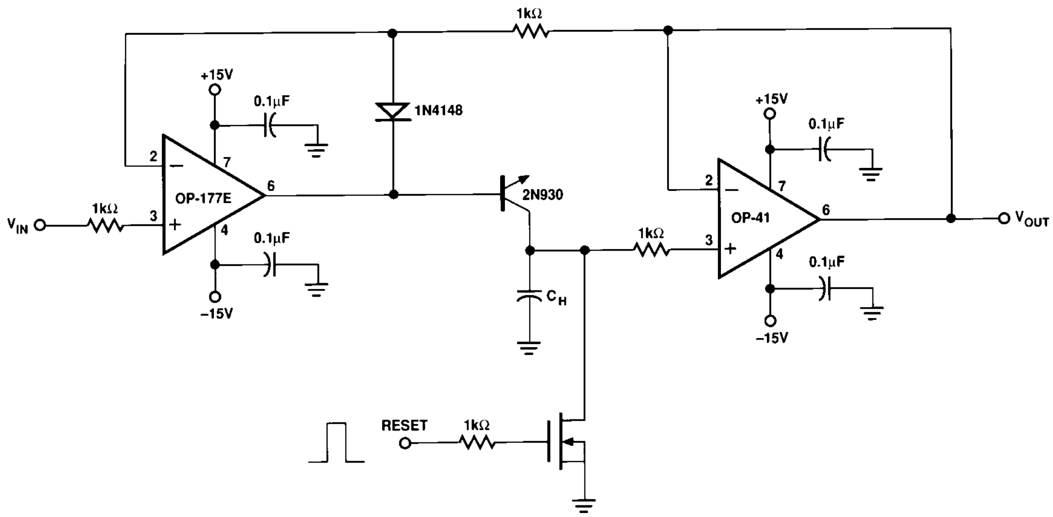

Figure 13. Precision Positive Peak Detector

PRECISION POSITIVE PEAK DETECTOR

In Figure 13, the C_H must be of polystyrene, Teflon,* or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the OP41.

PRECISION THRESHOLD DETECTOR/AMPLIFIER

In Figure 14, when $V_{IN} < V_{TH}$, amplifier output swings negative, reverse biasing diode D_1. $V_{OUT} = V_{TH}$ if $R_L = \infty$. When $V_{IN} \geq V_{TH}$, the loop closes,

$$V_{OUT} = V_{TH} + \left(V_{IN} - V_{TH}\right)\left(1+\frac{R_F}{R_S}\right)$$

C_C is selected to smooth the response of the loop.

*Teflon is a registered trademark of DuPont.

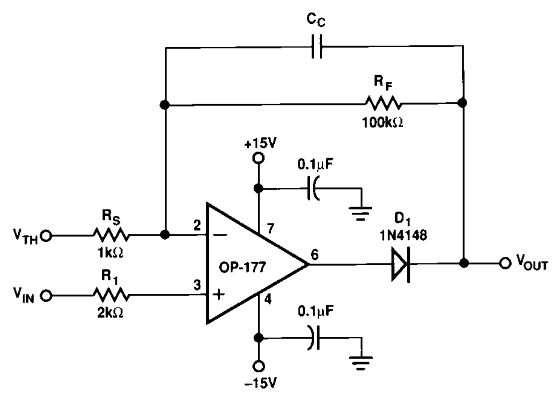

Figure 14. Precision Threshold Detector/Amplifier