Accessing the Dual-port SRAM Block from the FPGA Side of the FPSLIC®

1. Introduction

This application note provides designers with an understanding of how to access and achieve optimal performance from the Shared Dual-port SRAM block from the FPGA side of the FPSLIC.

2. Description

Atmel AT94K and AT94S FPSLIC devices contain up to 36 Kbytes of synchronous dual-port SRAM. Although a portion of the SRAM address space is dedicated to instruction code storage for the AVR® microcontroller core, the remaining SRAM space is intended for data storage that can be shared equally by the FPGA and AVR cores, see Figure 2-1.

Code space and data space are separated by a soft partition. The user has the choice of four partition locations, allowing for size customization of program and data space.

The AT94K40AL referenced in this application note will use the “10K word Program/16K byte Data” option. Please refer to the AT94K or AT94S datasheets for details on partition sizes and settings for the entire FPSLIC family of devices.

Programmable SLI

AT94K

AT94S

Application Note

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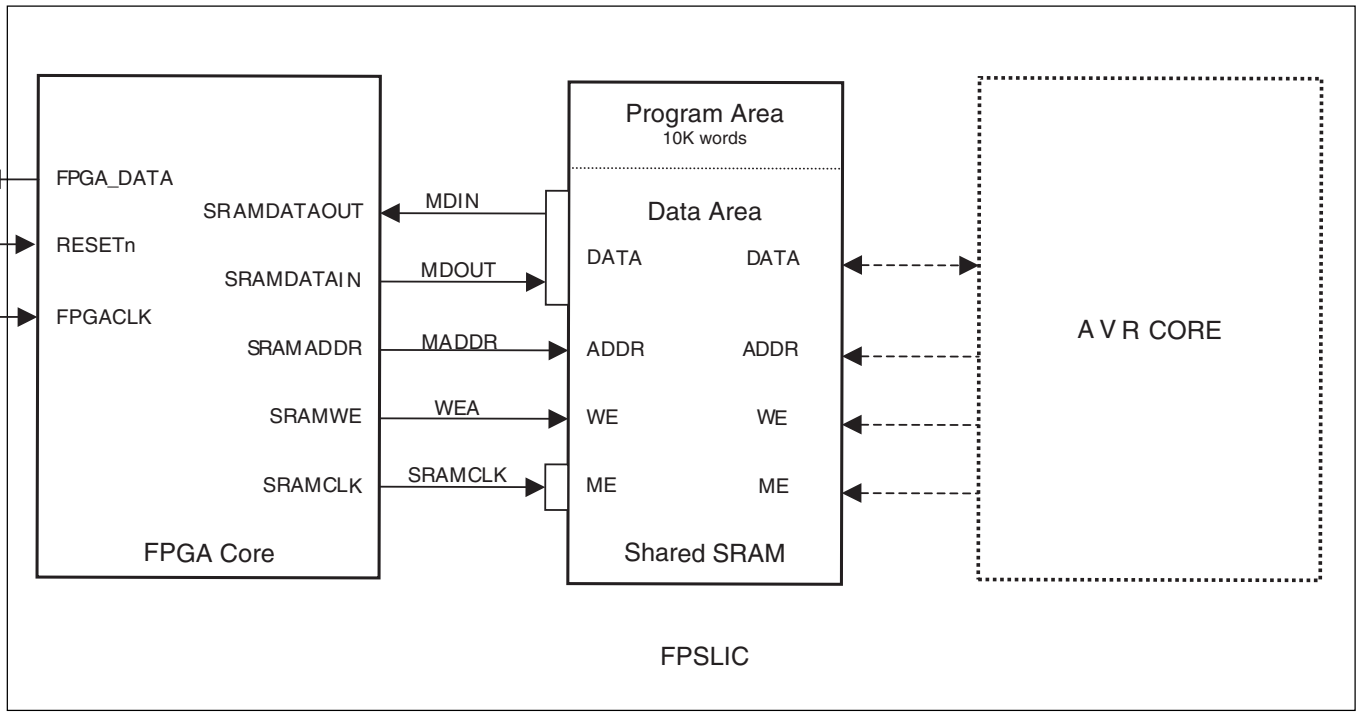
Figure 2-1. Block Diagram of FPGA Logic Interfacing to Shared SRAM

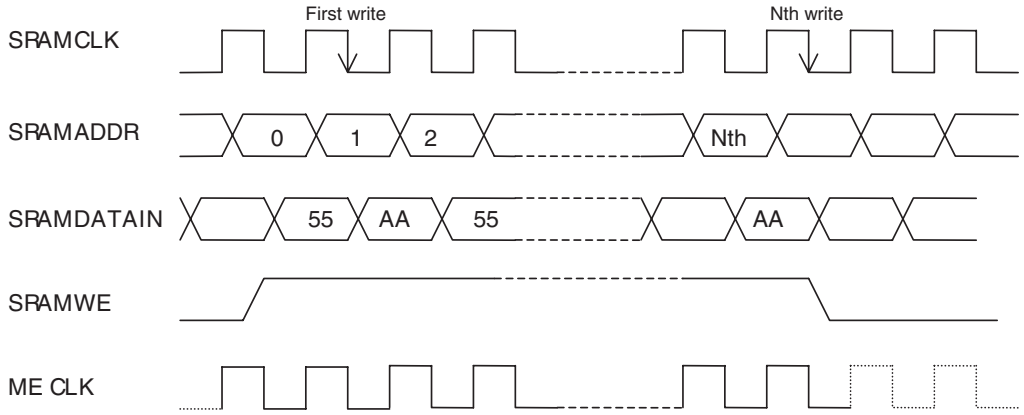


2.1 Interfacing the Data SRAM

When designing the FPGA logic that will access the shared SRAM block, it is important to note the proper clock edge and timing relationships between the address bus, data bus, write enable and clock signals being supplied to the SRAM interface ports. As indicated by the FPSLIC AT94K datasheet description of the Dual-port SRAM operation, addresses are registered on the rising edge of the internal ME clock, while data is latched on the falling edge of the ME clock. Additionally, write cycles begin by asserting a logic “1” on WE before the rising edge of the ME clock, while write cycles end on either the falling edge of the ME clock or falling edge of the WE, which ever comes first. Refer to the FPSLIC datasheet section covering the Dual-port SRAM timing characteristics. It is also important to choose the correct clock edge option in the System Designer software tool, refer to the AT94K device options.

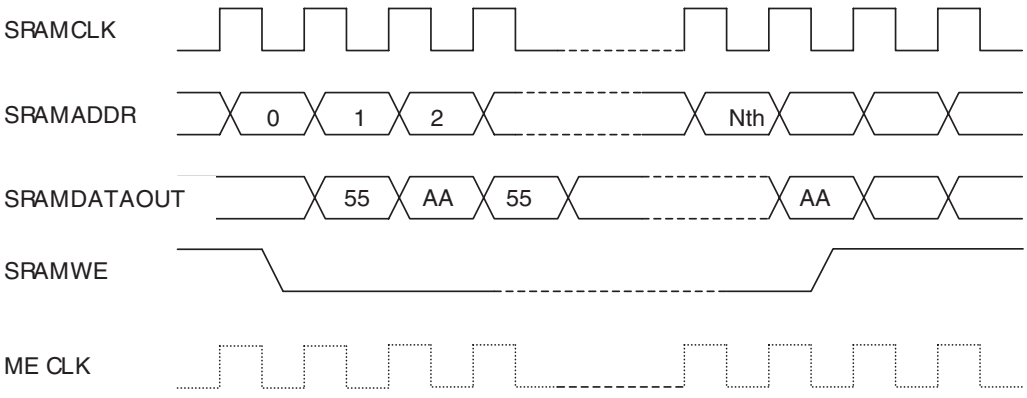
In the example provided herein, the “positive edge” clock option will be used. This will result in the SRAMCLK being passed directly to the ME clock port. Figure 2-2 shows the write cycle timing relationship of the FPGA logic. Notice that address updates are generated on the rising edge of the clock, while data and write strobe updates occur on the falling edge, half clock cycle later. This will result in the most optimal timing relationship at the SRAM interface.

Figure 2-2. SRAM Write Waveform Using “Positive Edge” Clock Option



To achieve the optimal timing relationship with the “negative edge” clock option (System Designer default setting), consider the ME clock will be inverted 180 degrees in phase from the SRAMCLK. Hence, address changes should occur with respect to the falling edge of SRAM-CLK, while updates to data and the write strobe should occur on the rising edge. In Figure 2-3, the Read cycle timing relationship of the FPGA logic is shown. Read cycles are started by asserting the SRAMWE signal Low and by supplying the address to be read on the SRAMADDR bus prior to the rising edge of the SRAMCLK. On the rising edge of the clock, the address will be latched and valid data will be driven onto the SRAMDATAOUT bus.

Figure 2-3. SRAM Read Waveform Using “Positive Clock Edge” Option



2.2 Interface Connections

Connections between the I/O ports referenced in the FPGA code and the SRAM interface ports are accomplished by way of the AVR-FPGA Interface flow within the System Designer software tool.

The ports MDIN, MDOUT, MADDR, WEA and SRAMCLK referenced in figure 1 can be found in AVR-FPGA Interface connection table.

2.3 Example Code

The Assembly code, the interconnect file (.ict), along with Verilog & VHDL versions of the example code are included in the software attachment. The example code causes the FPGA core logic to write the data pattern “55” at all even addresses and “AA” at all odd addresses, from address 60h to FFh. After reaching address FFh, the FPGA logic will begin to read the SRAM contents and output the data values on to the FPGA I/O pins.

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