Zedboard Hardware Peripheral Mapping

This document describes the default configuration for the ZedBoard when programmed with the ZynqConfiguration (this includes an FPGA bitstream and processor configuration). Each ZynqConfiguration is accompanied by a BSP with the necessary driver settings.

Version numbering:

Each BSP is numbered as follows: <Major>.<Minor>.<Revision>

<Major> is increased if address map is not backward compatible

<Minor> is increased if address map is backward compatible

<Revision> indicates a BSP software update without any hardware changes.

The following mapping is valid for ZynqConfiguration v3.2.1

# GPIOs:

The LEDs LD0 through LD6, switches SW0 through SW7 and push buttons are routed as GPIOs through Bank2 connecting to the GPIO peripheral of the processor (Refer to Zynq 7000 TRM - Chapter 14).

Table 1 LED, Swtich, Push button mapping

|  |  |  |
| --- | --- | --- |
| Bank | Pin | External Signal |
| 2 | 0 … 6 | LD0 … LD6 |
| 2 | 8 … 15 | SW0 … SW7 |
| 2 | 16 | BTNL |
| 2 | 17 | BTNC |
| 2 | 18 | BTND |
| 2 | 19 | BTNR |
| 2 | 20 | BTNU |

# PMOD-JA1 Header:

Out of the five available PMOD’s, JA is configured with GPIO interface and its mapping is described as below:

(The GPIO pins could be used for software PWM.)

Table PMOD-JA1 mapping

|  |  |  |
| --- | --- | --- |
| Bank | Pin | External Signal |
| 2 | 21 | JA1 |
| 2 | 22 | JA2 |
| 2 | 23 | JA3 |
| 2 | 24 | JA4 |
| 2 | 25 | JA7 |
| 2 | 26 | JA8 |
| 2 | 27 | JA9 |
| 2 | 28 | JA10 |

# Triple Timer Counter (TTC0 and TTC1)

The input clock frequency to the TTC Pre scalar is 111,111,115 Hz.

The Wave out pins of the TTC’s are mapped to the pins of the PMOD JD and one of the LED as described below:

(PWM with TTC implementation may need to use the following set of pins.)

|  |  |
| --- | --- |
| Signal Description | External Signal |
| TTC0\_WAVE0\_OUT | JB1 |
| TTC0\_WAVE1\_OUT | JB2 |
| TTC0\_WAVE2\_OUT | JB3 |
| TTC1\_WAVE0\_OUT | JB4 |
| TTC1\_WAVE1\_OUT | JB7 |
| TTC1\_WAVE2\_OUT | JB8 |

# UART:

UART1 is enabled and could be accessed from the USB port with/as a serial device.

UART0 is enabled and routed to the following PMOD pins:

|  |  |
| --- | --- |
| Signal Description | External Signal |
| TX | V7 |
| RX | W7 |

# I2C:

I2C1 is enabled and routed to the following PMOD pins:

|  |  |
| --- | --- |
| Signal Description | External Signal |
| SCL | AB6 |
| SDA | AB7 |

# ADAU1761:

The I2C of the CODEC is interfaced to the I2C\_0 port of the Zynq Processor.



Peripheral mapping of the AXI FIFO interface is as follows:

|  |  |
| --- | --- |
| Port Description | Port Address |
| FIFO\_BASEADDR | 0x43C00000 |
| FIFO\_HIGHADDR | 0x43C0FFFF |

|  |  |
| --- | --- |
| **Property** | **Value** |
| Cut Through | Enabled |
| FIFO Depth | 1024 |
| Programmable Full Threshold | 512 |
| Programmable Empty Threshold | 10 |

Peripheral mapping of the AXI I2S interface is as follows:

|  |  |
| --- | --- |
| Port Description | Port Address |
| I2S\_BASEADDR | 0x43C10000 |
| I2S\_HIGHADDR | 0x43C1FFFF |

FIFO Interrupt Source:

The interrupt port of the FIFO is connected to the IRQ0 port of the Zynq Processor.

|  |  |
| --- | --- |
| Interrupt Source | Interrupt ID# |
| IRQ0 | 91 |

OLED:

OLED is interfaced to the Zynq PS.

Please check the example program provided in the workspace for interfacing options.